

DON'T CARE CONDITIONS

→ In digital system some I/P Combinations

"JUST DON'T HAPPEN"

⇒ Example : BCD C(1010, 1011, 1100, 1101, 1110, 1111)

⇒ Enter 'x' or 'd' in K-map

Ans - AND

Example (any)

$$F(w, x, y, z) = \sum(1, 3, 7, 11, 15)$$

$$d(w, x, y, z) = \sum(0, 2, 5)$$

	$\bar{y}z$	$\bar{y}z$	yz	$y\bar{z}$
x	0	1	1	2
	4	5	1	6
w	7	13	15	14
	8	9	11	10

1	$\bar{w}xyz$
3	$\bar{w}xyz$
5	$\bar{w}xyz$
7	$\bar{w}xyz$
13	$\bar{w}xyz$
15	$\bar{w}xyz$
14	$\bar{w}xyz$
11	$\bar{w}xyz$
10	$\bar{w}xyz$

$$F(w, x, y, z) = yz + \bar{w}z$$

OVERLAPPING GROUPS

→ The same I. can be common to two or more groups.

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0	1	3	2
$\bar{A}B$	4	5	7	6
$A\bar{B}$	12	13	15	14
AB	1	1	1	1
$A\bar{B}$	8	9	11	10

	$\bar{B}\bar{A}$	$\bar{B}A$	$B\bar{A}$	BA
	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0	1	3	2
$\bar{A}B$	4	5	7	6
$A\bar{B}$	12	13	15	14
AB	1	1	1	1
$A\bar{B}$	8	9	11	10

(a) Overlapping

$$y = A + B\bar{C}\bar{D}$$

(b) Non-overlapping

$$y = A + \bar{A}B\bar{C}\bar{D}$$

ROLLING THE MAP

Simplify the following boolean functions using 3-variable maps.

a) $F(x,y,z) = \Sigma(0,1,5,7)$

b) $F(x,y,z) = \Sigma(1,2,3,6,7)$

a)

	$\bar{y}\bar{z}$	$\bar{y}z$	$y\bar{z}$	yz
\bar{x}	0	1	3	2
x	4	5	7	6

$$F = \bar{x}\bar{y} + xz$$

$$\begin{array}{l} \bar{x}\bar{y} \\ \times x \\ \hline 000 \\ 001 \\ \hline 1 - 111 \end{array}$$

b)

	$\bar{y}\bar{z}$	$\bar{y}z$	$y\bar{z}$	yz
\bar{x}	0	1	3	2
x	4	5	7	6

$$F = y + \bar{x}z$$

$$\begin{array}{l} xy \\ \times x \\ \hline 011 \\ 010 \\ \hline 1 - 111 \\ 011 \\ \hline 100 \\ 101 \\ \hline 111 \end{array}$$

	$\bar{B}D$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}B$	0	1	3	2
$\bar{A}B$	4	5	7	6
AB	18	13	15	14
$A\bar{B}$	8	9	11	10

Unrolled

	$\bar{C}D$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
$\bar{A}B$	0	1	3	2
$\bar{A}B$	4	5	7	6
AB	12	13	15	14
$A\bar{B}$	8	9	11	10

rolled groups

Eliminating Redundant Groups

→ Eliminating any group whose 1's core completely overlaped by other groups.

	$\bar{C}D$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
$\bar{A}B$	0	0	1	0
$\bar{A}B$	0	1	1	0
AB	0	1	1	1
$A\bar{B}$	0	1	0	0

	$\bar{C}D$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
$\bar{A}B$	0	0	1	0
$\bar{A}B$	0	1	1	0
AB	0	1	1	1
$A\bar{B}$	0	1	0	0

$$Y = BD + ABC + A\bar{C}D + \bar{A}B\bar{C} + \bar{A}CD$$

$$Y = \bar{A}B\bar{C} + A\bar{C}D + ABC + \bar{A}CD$$

UNIT-III

Combinational Logic Circuits

→ Logic circuits for digital systems are two types.

- i) Combinational
- ii) Sequential,

Combinational Logic Circuits

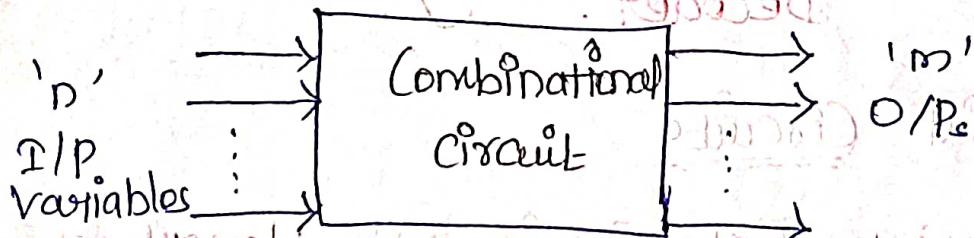
→ Logic circuits for digital Systems are 2 types.

Logic circuit
Combinational Sequential.

Combinational Circuit

→ Shows Combinational Circuits of logic gates. These Circuits Operate with binary values.

→ The O/P of Combinational Circuits depends on the combination of present i/p.



→ Combinational Circuits uses:

i) Input Variables

ii) Logic gates

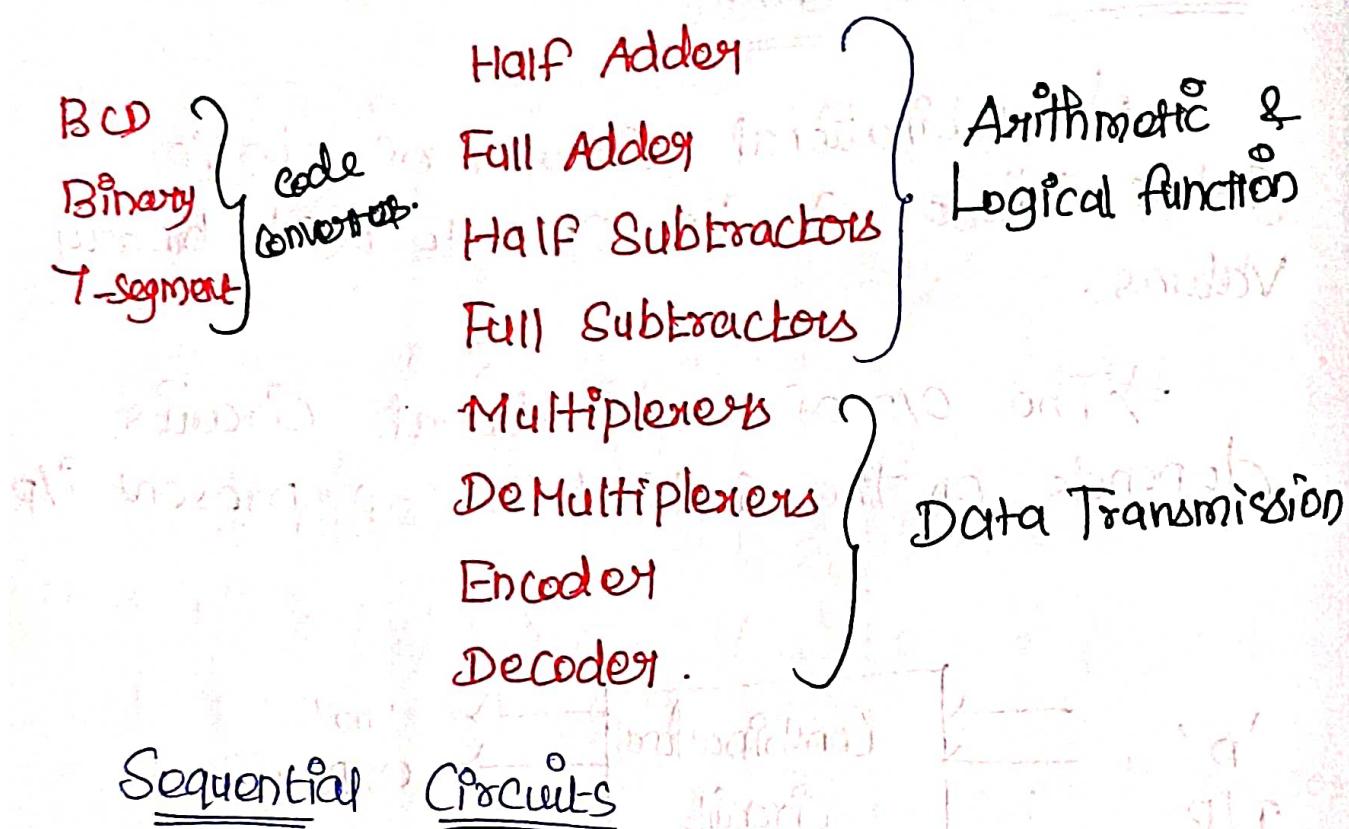
iii) Output Variables

→ A circuit in which different types of Logic gates are Combined is known as a Combinational Logic Circuit.

\Rightarrow This process transforms binary information from the given I/P data to the required O/P data.

\Rightarrow Both I/P and O/P data are represented by two possible values 1 and 0.

\Rightarrow Example of Combinational Circuits



\Rightarrow Sequential circuit has Memory so output can vary based on I/P.

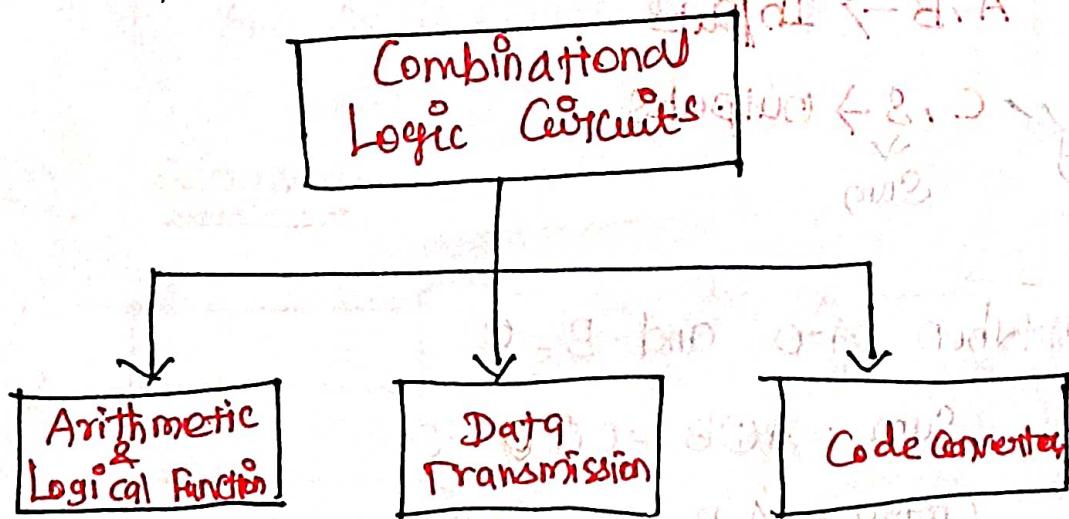
\Rightarrow Sequential circuits uses

- i) Previous I/P
- ii) O/P
- iii) Clock
- iv) Memory Element

Difference b/w Combinational & Sequential Circuit

Combinational Circuits	Sequential Circuits
□ O/P depends only on Present I/Ps.	□ O/P depends on both present I/P and Present State.
□ Feedback path is not present.	□ Feedback path is present.
□ Memory elements are not required.	□ Memory elements are required.
□ Clock signal is not required.	□ Clock signal is required.
□ Easy to design.	□ Difficult to design

⇒ Combinational Circuits are designed for three purpose.



Adders

→ There are many information - processing tasks performed by the digital computers.

→ A combinational circuit that performs the addition of 2 bits is called a half-adder.

→ The addition of three bits is called a full-adder.

The half-Adder

→ The half-adder is a logic circuit that performs the addition of two binary bits.

→ The half-adder is a basic building block having 2 i/p and 2 o/p.

→ The adder is used to perform OR operation of two single bit binary numbers.

→ The carry and sum are 2 DP states of half adder.

A, B → Inputs

Carry ← C, S → Outputs
↓
Sum

i) When A=0 and B=0

$$\begin{array}{|c|} \hline \text{Sum} = A \oplus B \\ \hline \end{array} \quad \begin{array}{|c|} \hline = 0 \oplus 0 = 0 \\ \hline \end{array}$$
$$\begin{array}{|c|} \hline \text{Carry} = A \cdot B \\ \hline \end{array} \quad \begin{array}{|c|} \hline = 0 \cdot 0 = 0 \\ \hline \end{array}$$

bit setting
of sum is 0

ii) When $A=0$ and $B=1$

$$\text{Sum} = 0 \oplus 1 = 1$$

$$\text{Carry} = 0 \cdot 1 = 0$$

iii) When $A=1$ and $B=0$

$$\text{Sum} = 1 \oplus 0 = 1$$

$$\text{Carry} = 1 \cdot 0 = 0$$

iv) When $A=1$ and $B=1$

$$\text{Sum} = 1 \oplus 1 = 0$$

$$\text{Carry} = 1 \cdot 1 = 1$$

Half-Adder Truth Table

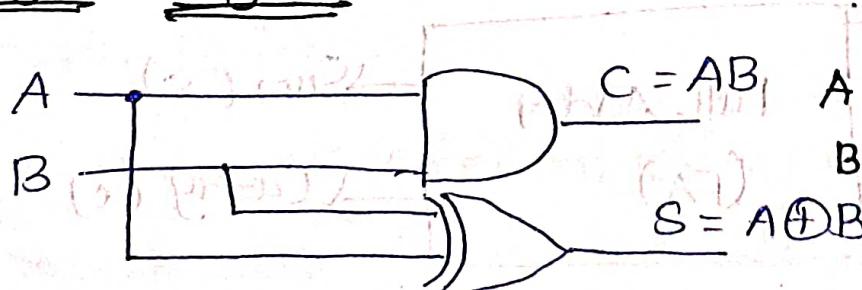
Input		Output	
A	B	s	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean Expressions.

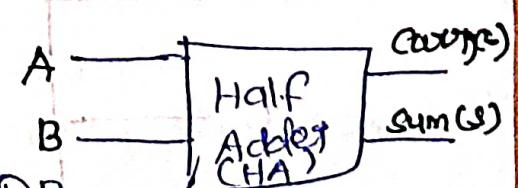
$$S = A \oplus B = \overline{A}B + A\overline{B}$$

$$C = AB$$

Logic diagram



Logic diagram



Block diagram.

The full - Adder

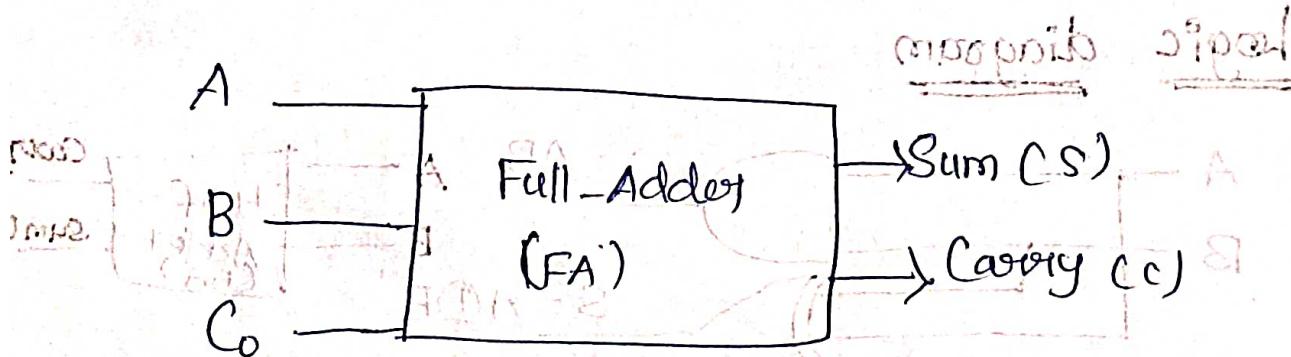
⇒ A full Adder is a Combinational Circuit that Forms the arithmetic Sum of 3 i/p bits.

→ The half Adder is used to only 2 numbers. To over come this Problem, the full adder was developed.

⇒ The full adder has 3 i/p States and 2 o/p States. i.e., Sum and Carry.

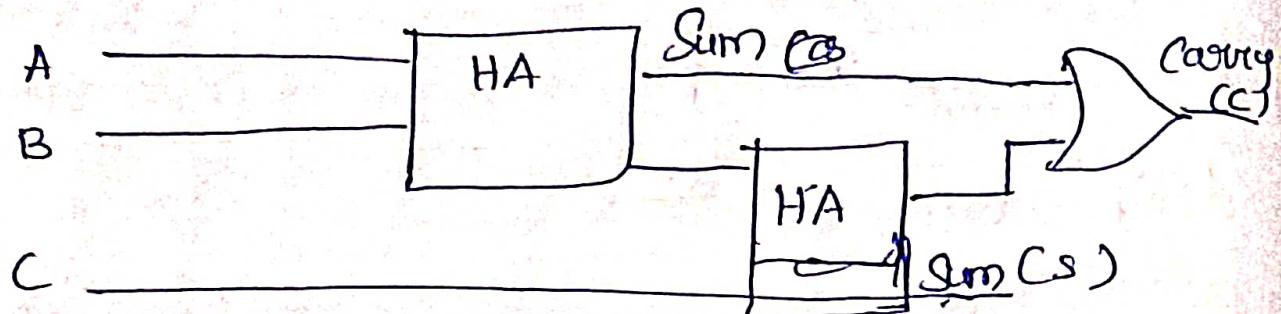
A	B	C_0	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table.



Block diagram.

A full-adder may be constructed by using 2 half-adders and one OR gate.



$$S = \overline{A}\overline{B}C_0 + \overline{A}B\overline{C}_0 + A\overline{B}\overline{C}_0 + ABC_0$$

$$= C_0(\overline{A}\overline{B} + AB) + \overline{C}_0(\overline{A}\overline{B} + A\overline{B})$$

$$= \overline{C}_0(A \oplus B) + C_0(\overline{A} \oplus B)$$

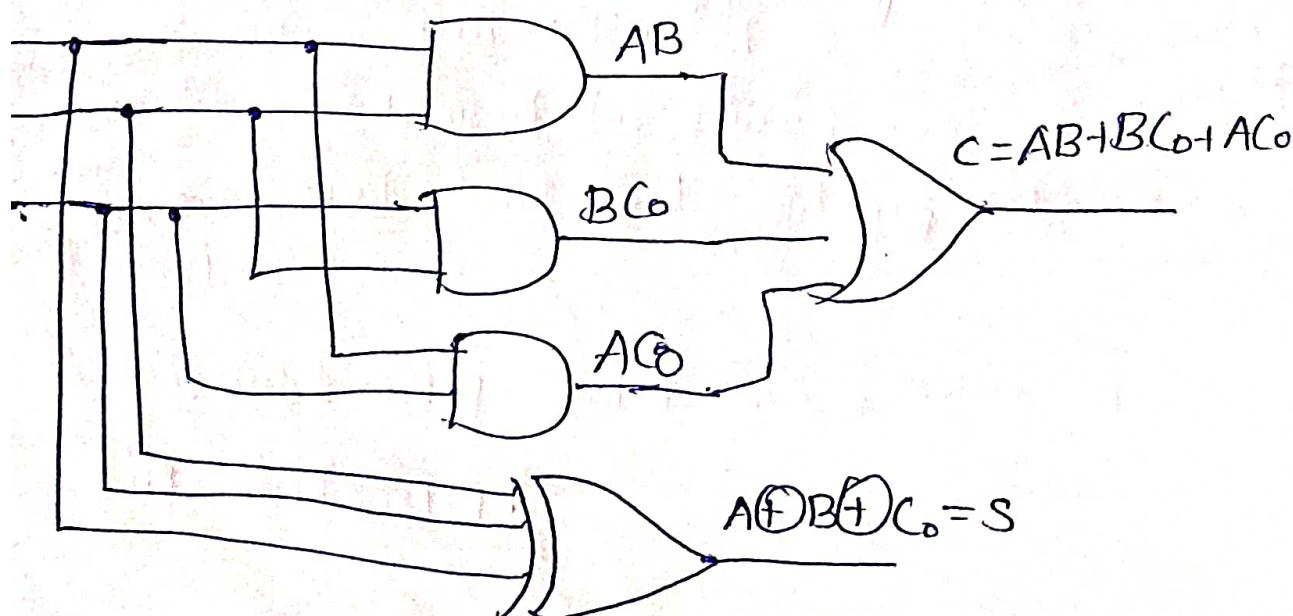
$S = A \oplus B \oplus C_0$

$$C = \overline{A}BC + A\overline{B}C + ABC + A\overline{B}\overline{C}$$

$$= ABC\overline{C} + BC(\overline{A} + A) + AC(\overline{B}C + \overline{B}\overline{C})$$

$$= AB + BC +$$

$$C = AB + BC_0 + AC_0$$



Sum

$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + AB\bar{C}$$

$$= A \oplus B \oplus C$$

	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
C_o	1	1	1	1	
\bar{C}_o	1		1		
C_o					

Carry

	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
C_o					
\bar{C}_o					
C_o					

$$C = AB + BG_o + AC_o$$

The binary parallel adder.

By making use of a number of full-adders, we can build binary adders of any length.



Method of summing binary numbers (block diagram)

(block diagram)

Sum

$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$$

$$= A \oplus B \oplus C$$

	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
C_0	1	1	1	1	
\bar{C}_0					1

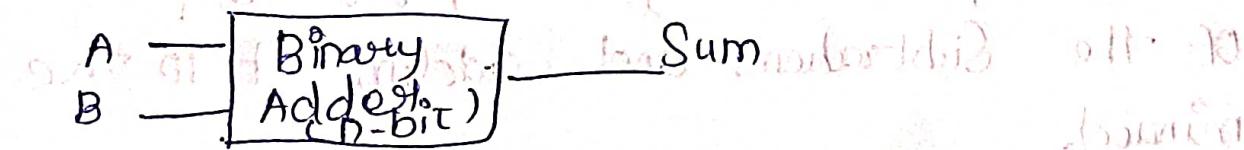
Carry

	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
C_0					
\bar{C}_0					

$$C = AB + BC_0 + AC_0$$

The binary parallel adder.

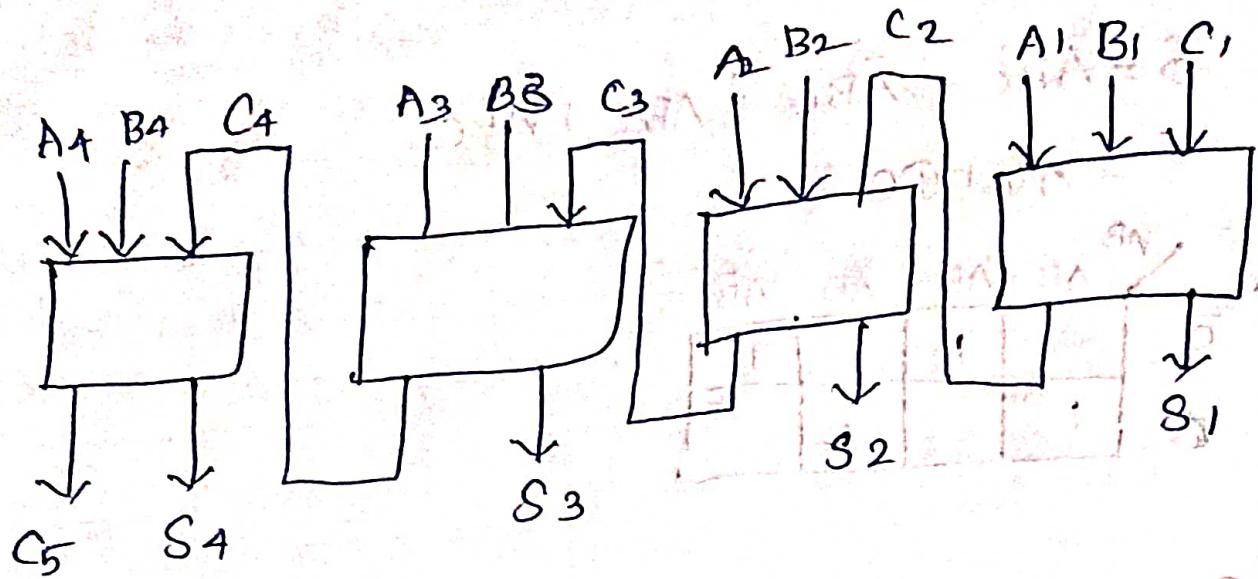
By making use of a number of full-adders, we can build binary adders of any length.



↓
Carry

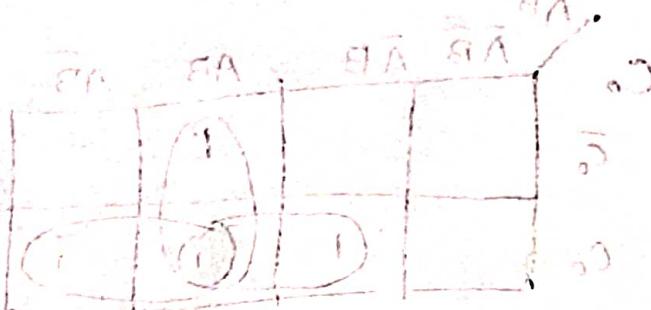
(Find a right-side bus placed directly below the sum bus)

(block diagram)



Example

$$\begin{array}{r}
 & C & 1 & 1 & 1 & 0 \\
 & 0 & 1 & 1 & 1 & \\
 & 0 & 1 & 0 & 1 & + \\
 \hline
 & 1 & 1 & 0 & 0
 \end{array}$$

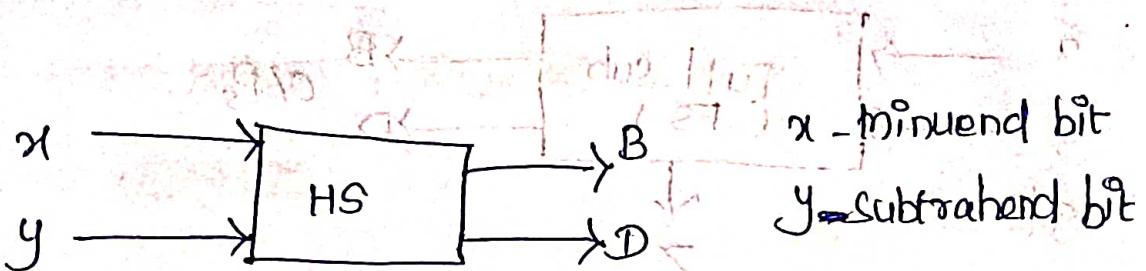


Subtractors

- The Subtractor is a Combinational Logic Circuit.
- The Subtraction of 2 binary numbers can be performed by taking the complement of the Subtrahend and adding it to the minuend.
- Subtractor could be either a half or full subtractor.

The half Subtractor

⇒ The half-subtractor is a combinational circuit that subtracts 2 bits & produces their difference.



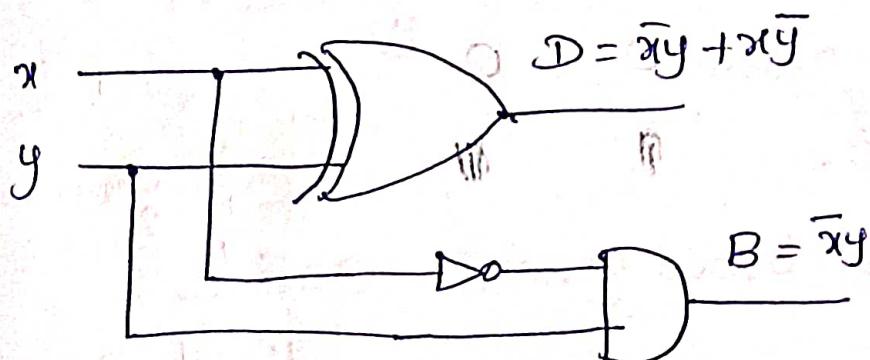
input		output	
x	y	B	D
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

x - minuend bit
y - subtrahend bit

B - Borrow
d - Difference.

$$\begin{aligned} D &= \bar{x}y + x\bar{y} \\ &= x \oplus y \end{aligned}$$

$$B = \bar{x}y$$



$$0 - 0 = 0$$

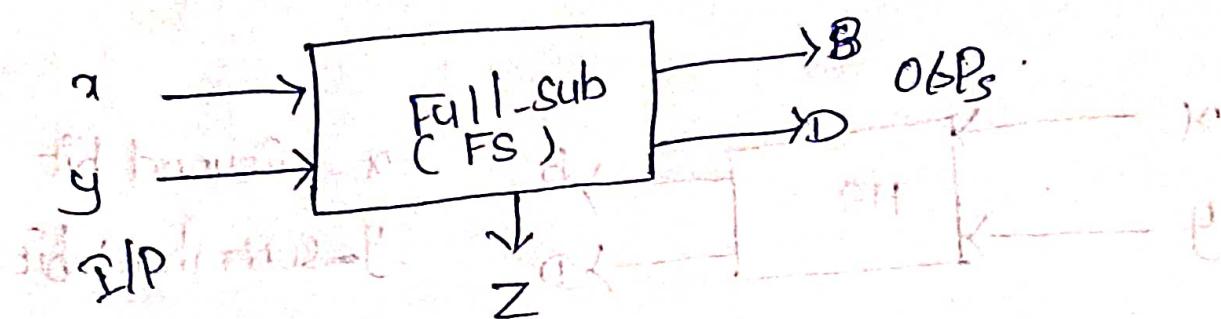
$$0 - 1 = 1$$

$$1 - 0 = 0$$

$$1 - 1 = 0$$

The full Subtractor

The full Subtractor is a Combinational circuit which has 3 i/Ps and 2 O/Ps.



x	y	z	c	B	D	e	①	②	③
0	0	0	0	0	0	0	0	0	0
0	0	1	0	10	0	0	0	0	0
0	1	0	1	0	0	1	1	1	1
10	1	0	0	0	10	1	1	1	1
10	1	1	1	0	0	1	1	1	1
10	2	0	0	0	10	1	1	1	1
10	2	1	0	0	0	1	1	1	1
10	2	2	0	0	0	1	1	1	1
10	2	2	1	0	0	1	1	1	1
10	2	2	2	0	0	1	1	1	1
10	2	2	3	0	0	1	1	1	1
10	2	2	4	0	0	1	1	1	1
10	2	2	5	0	0	1	1	1	1
10	2	2	6	0	0	1	1	1	1
10	2	2	7	0	0	1	1	1	1
10	2	2	8	0	0	1	1	1	1
10	2	2	9	0	0	1	1	1	1
10	2	2	10	0	0	1	1	1	1
10	2	2	11	0	0	1	1	1	1
10	2	2	12	0	0	1	1	1	1
10	2	2	13	0	0	1	1	1	1
10	2	2	14	0	0	1	1	1	1
10	2	2	15	0	0	1	1	1	1
10	2	2	16	0	0	1	1	1	1
10	2	2	17	0	0	1	1	1	1
10	2	2	18	0	0	1	1	1	1
10	2	2	19	0	0	1	1	1	1
10	2	2	20	0	0	1	1	1	1
10	2	2	21	0	0	1	1	1	1
10	2	2	22	0	0	1	1	1	1
10	2	2	23	0	0	1	1	1	1
10	2	2	24	0	0	1	1	1	1
10	2	2	25	0	0	1	1	1	1
10	2	2	26	0	0	1	1	1	1
10	2	2	27	0	0	1	1	1	1
10	2	2	28	0	0	1	1	1	1
10	2	2	29	0	0	1	1	1	1
10	2	2	30	0	0	1	1	1	1
10	2	2	31	0	0	1	1	1	1
10	2	2	32	0	0	1	1	1	1
10	2	2	33	0	0	1	1	1	1
10	2	2	34	0	0	1	1	1	1
10	2	2	35	0	0	1	1	1	1
10	2	2	36	0	0	1	1	1	1
10	2	2	37	0	0	1	1	1	1
10	2	2	38	0	0	1	1	1	1
10	2	2	39	0	0	1	1	1	1
10	2	2	40	0	0	1	1	1	1
10	2	2	41	0	0	1	1	1	1
10	2	2	42	0	0	1	1	1	1
10	2	2	43	0	0	1	1	1	1
10	2	2	44	0	0	1	1	1	1
10	2	2	45	0	0	1	1	1	1
10	2	2	46	0	0	1	1	1	1
10	2	2	47	0	0	1	1	1	1
10	2	2	48	0	0	1	1	1	1
10	2	2	49	0	0	1	1	1	1
10	2	2	50	0	0	1	1	1	1
10	2	2	51	0	0	1	1	1	1
10	2	2	52	0	0	1	1	1	1
10	2	2	53	0	0	1	1	1	1
10	2	2	54	0	0	1	1	1	1
10	2	2	55	0	0	1	1	1	1
10	2	2	56	0	0	1	1	1	1
10	2	2	57	0	0	1	1	1	1
10	2	2	58	0	0	1	1	1	1
10	2	2	59	0	0	1	1	1	1
10	2	2	60	0	0	1	1	1	1
10	2	2	61	0	0	1	1	1	1
10	2	2	62	0	0	1	1	1	1
10	2	2	63	0	0	1	1	1	1
10	2	2	64	0	0	1	1	1	1
10	2	2	65	0	0	1	1	1	1
10	2	2	66	0	0	1	1	1	1
10	2	2	67	0	0	1	1	1	1
10	2	2	68	0	0	1	1	1	1
10	2	2	69	0	0	1	1	1	1
10	2	2	70	0	0	1	1	1	1
10	2	2	71	0	0	1	1	1	1
10	2	2	72	0	0	1	1	1	1
10	2	2	73	0	0	1	1	1	1
10	2	2	74	0	0	1	1	1	1
10	2	2	75	0	0	1	1	1	1
10	2	2	76	0	0	1	1	1	1
10	2	2	77	0	0	1	1	1	1
10	2	2	78	0	0	1	1	1	1
10	2	2	79	0	0	1	1	1	1
10	2	2	80	0	0	1	1	1	1
10	2	2	81	0	0	1	1	1	1
10	2	2	82	0	0	1	1	1	1
10	2	2	83	0	0	1	1	1	1
10	2	2	84	0	0	1	1	1	1
10	2	2	85	0	0	1	1	1	1
10	2	2	86	0	0	1	1	1	1
10	2	2	87	0	0	1	1	1	1
10	2	2	88	0	0	1	1	1	1
10	2	2	89	0	0	1	1	1	1
10	2	2	90	0	0	1	1	1	1
10	2	2	91	0	0	1	1	1	1
10	2	2	92	0	0	1	1	1	1
10	2	2	93	0	0	1	1	1	1
10	2	2	94	0	0	1	1	1	1
10	2	2	95	0	0	1	1	1	1
10	2	2	96	0	0	1	1	1	1
10	2	2	97	0	0	1	1	1	1
10	2	2	98	0	0	1	1	1	1
10	2	2	99	0	0	1	1	1	1
10	2	2	100	0	0	1	1	1	1

$$x = 2^2 B = 1$$

$$10 \quad 2 = 1 - 1 = 0$$

$$10 - 1 = 0 = 1$$

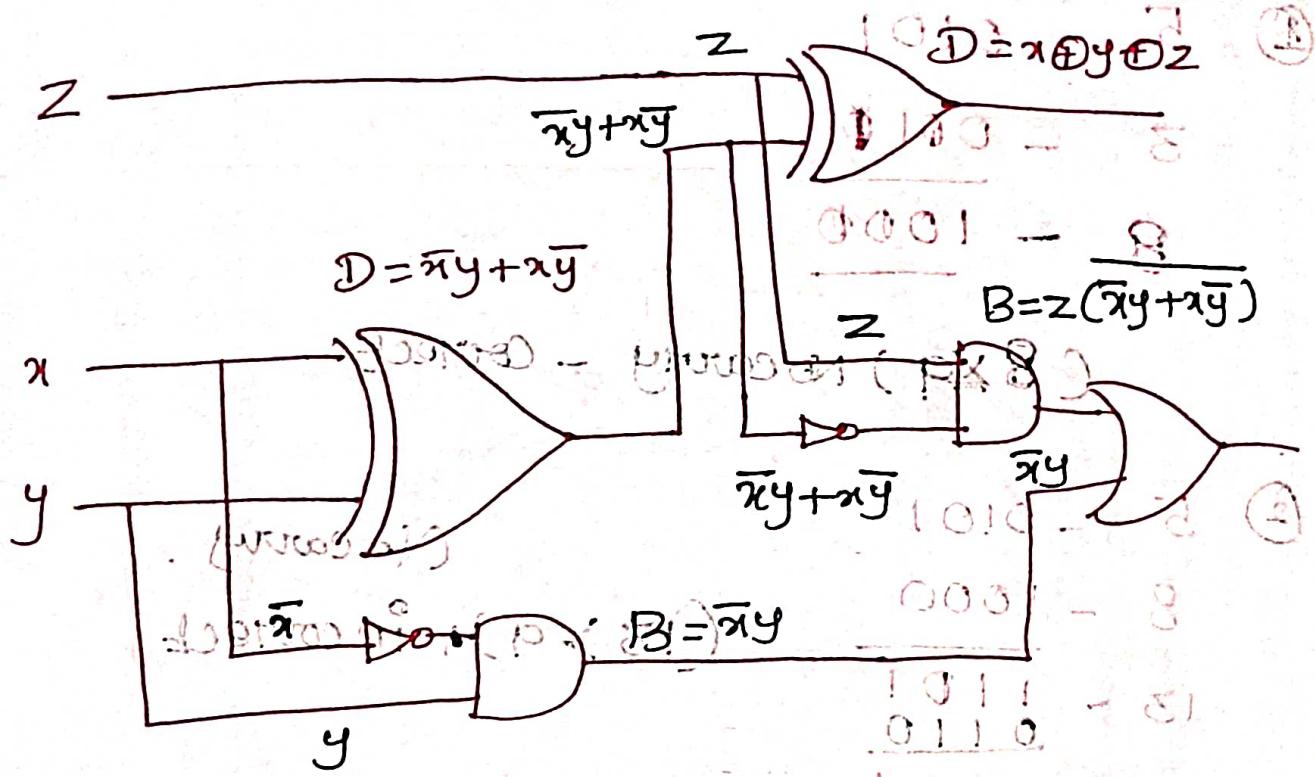
$$D = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + xy\bar{z} + \bar{x}yz$$

$$B = \bar{x}z + yz + \bar{x}y$$

$$(a) = x(\bar{y}\bar{z} + yz) + \bar{x}(yz + y\bar{z})$$

$$= x(y \oplus z) + \bar{x}(y \oplus z)$$

$$D = x \oplus y \oplus z$$



BCD Adder

BCD - Binary Coded Decimal

$$\begin{array}{r}
 3 - 0011 \\
 8^{(+)} - 1000 \\
 \hline
 1111 \\
 0110 \\
 \hline
 0101 \\
 0110 \\
 \hline
 \end{array}$$

$$\begin{array}{r}
 0011 - 3 \\
 1000 - 8 \\
 \hline
 1011 - 11 > 9 \text{ (x)} \\
 0110 - (+6) \\
 \hline
 0001 - 1
 \end{array}$$

Rules

1. Sum < 9 and Carry = 0 Correct
2. Sum < 9 and carry = 1 incorrect and (+6)
3. Sum > 9 and carry = 0 " " " "

Example

①

$$\begin{array}{r} 5 \\ \underline{- 0101} \end{array}$$

$$\begin{array}{r} 3 \\ - 0010 \\ \hline \end{array}$$

$$\begin{array}{r} 8 \\ - 1000 \\ \hline \end{array}$$

$$\begin{array}{r} 8 \\ - 1000 \\ \hline \end{array}$$

(8 \times 9) No carry - correct

②

$$\begin{array}{r} 5 \\ - 0101 \end{array}$$

$$\begin{array}{r} 8 \\ - 1000 \\ \hline \end{array}$$

$$\begin{array}{r} 13 \\ - 1101 \\ \hline 0110 \end{array}$$

$$\begin{array}{r} 1 \\ \underline{0011} - 3 \\ \hline \end{array}$$

No carry.

(13 \times 9) A incorrect

(3 $<$ 9) No carry - correct.

Ans \rightarrow Dibagi \rightarrow 108

Multiplexers

→ A Multiplexer is a circuit which has more number of inputs but only one output.

→ A digital multiplexer is a combinational circuit that selects binary information from one of the many i/p lines and directs it to a single o/p line.

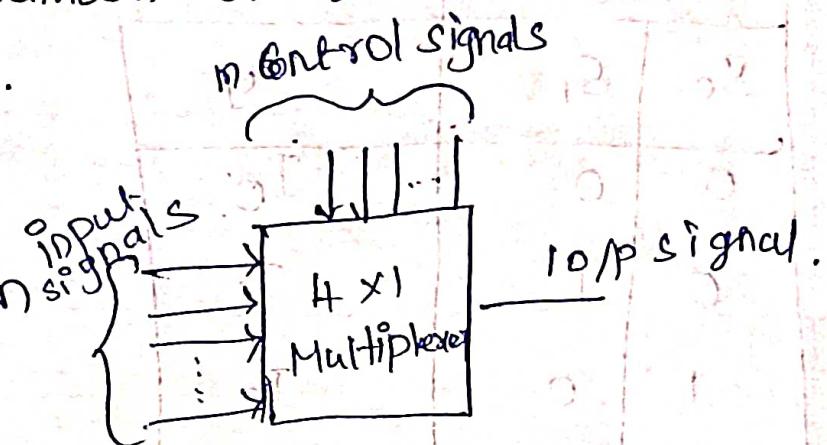
→ That has maximum of 2^n data inputs.

→ Many to one.

2^n - input lines

n - Selection Lines

Single - output line



→ One of those data inputs will be connected to the o/p based on the values of selection lines.

→ Multiplexer also called Mux.

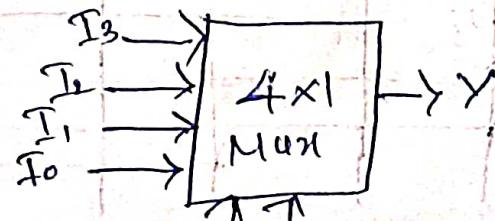
→ Data Selector

4×1 Multiplexer

→ 4 data i/B

→ Two selection lines S1 & S0

→ One o/p Y.



Advantages

1. Reduce no. of wires
2. Reduce Circuit complexity & cost.

Truth Table

Select Line		Output
S_0	S_1	y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

