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(54) **NON-VOLATILE MEMORY DEVICE AND ITS OPERATING METHOD**

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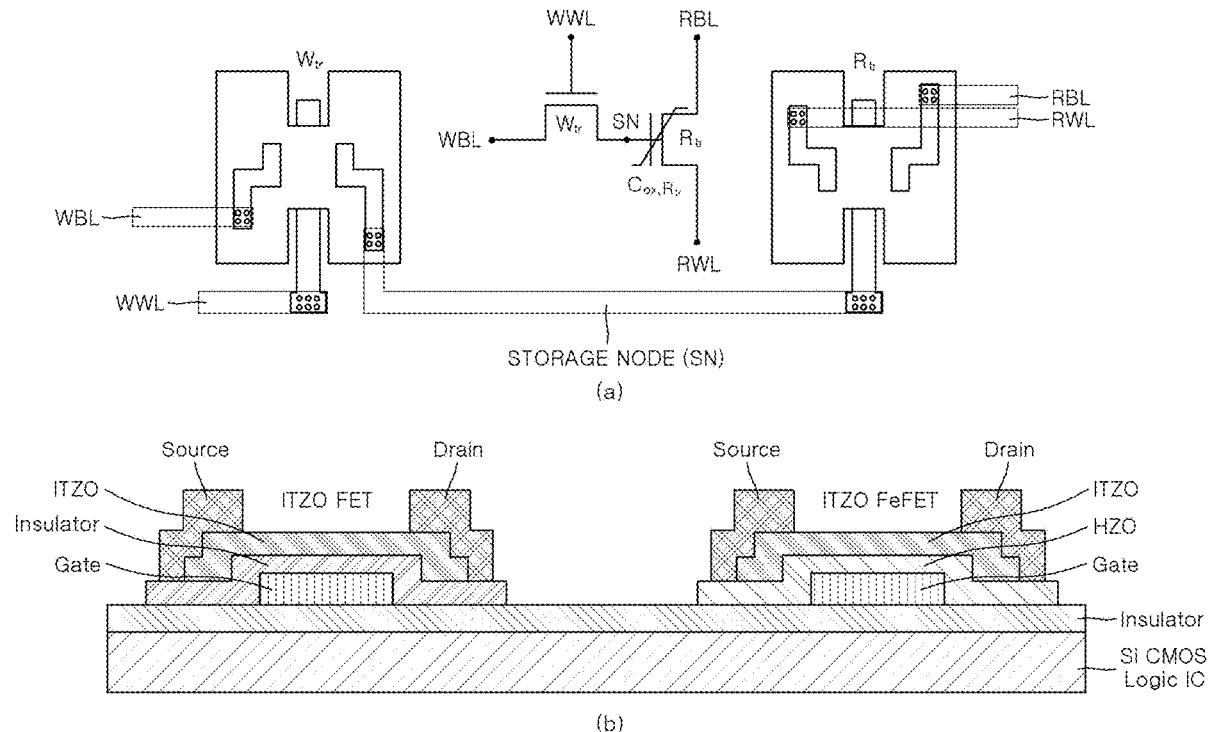
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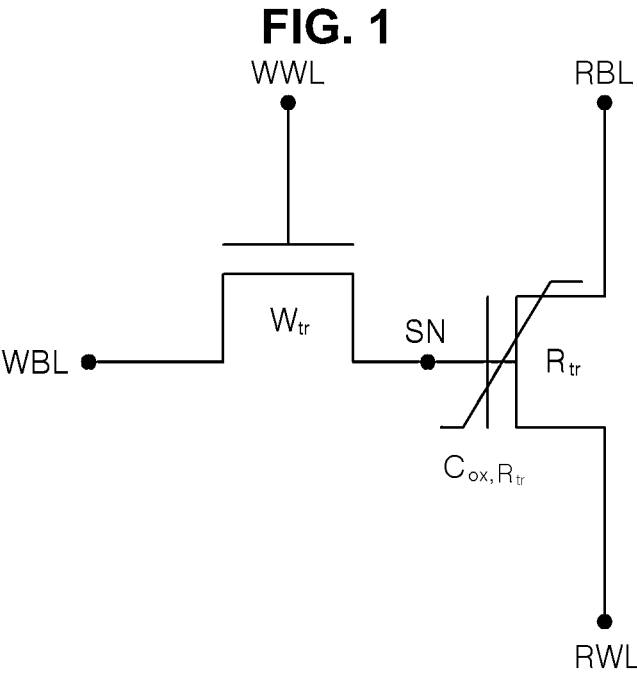
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(57) **ABSTRACT**

Disclosed herein are a non-volatile memory device and an operating method thereof. The non-volatile memory device includes a memory cell including a write transistor and a ferroelectric read transistor, a write word line connected to a gate terminal of the write transistor, a write bit line connected to a source terminal of the write transistor, a read word line connected to a source terminal of the ferroelectric read transistor, and a read bit line connected to a drain terminal of the ferroelectric read transistor, and a drain terminal of the write transistor may be connected to a gate terminal of the ferroelectric read transistor. According to the present invention, a low-power, high-density, and non-destructive dynamic random access memory (DRAM) can be implemented by realizing 2T0C FeDRAM based on a silicon complementary metal-oxide semiconductor (CMOS) process using a dielectric material.





**FIG. 2**

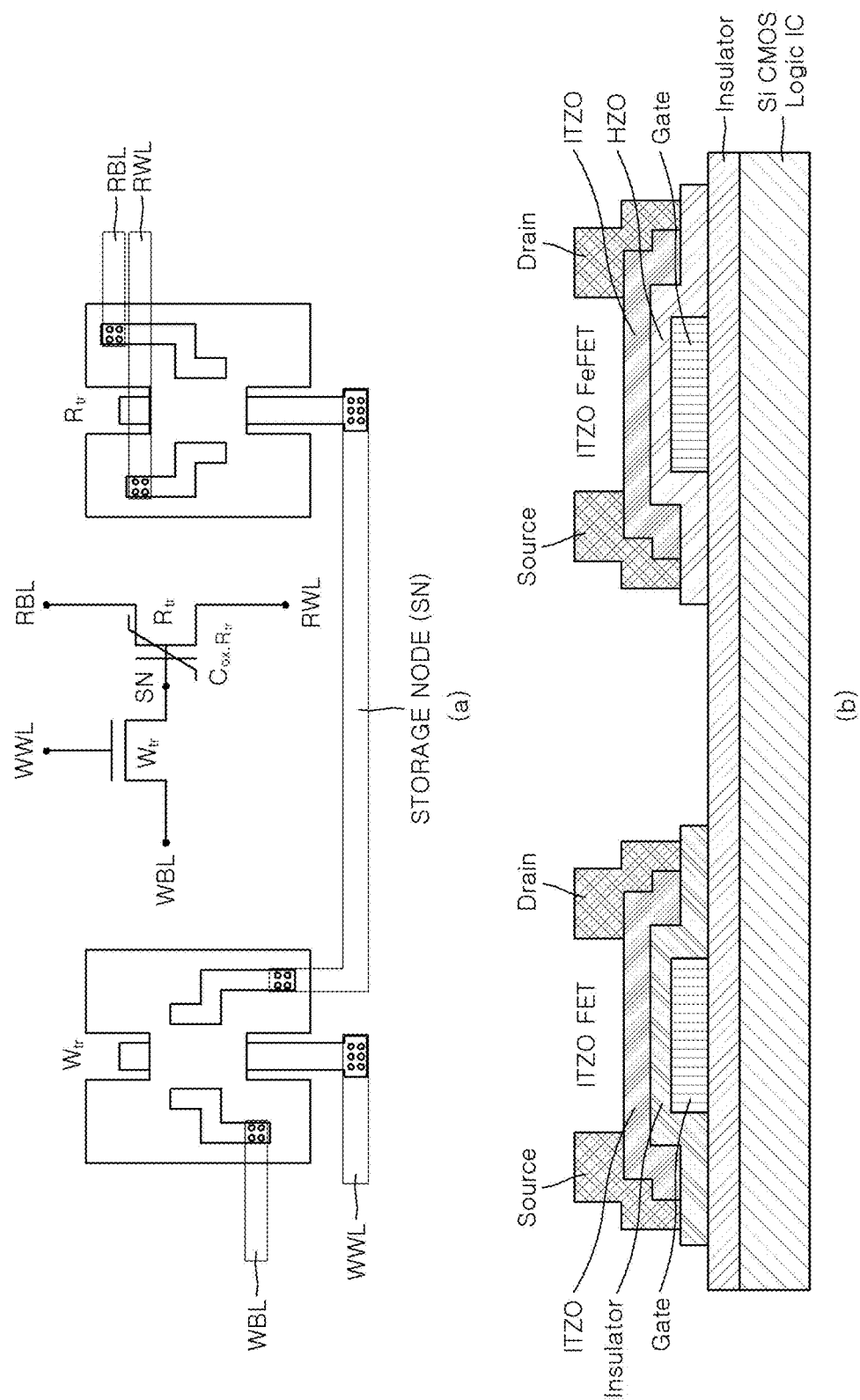
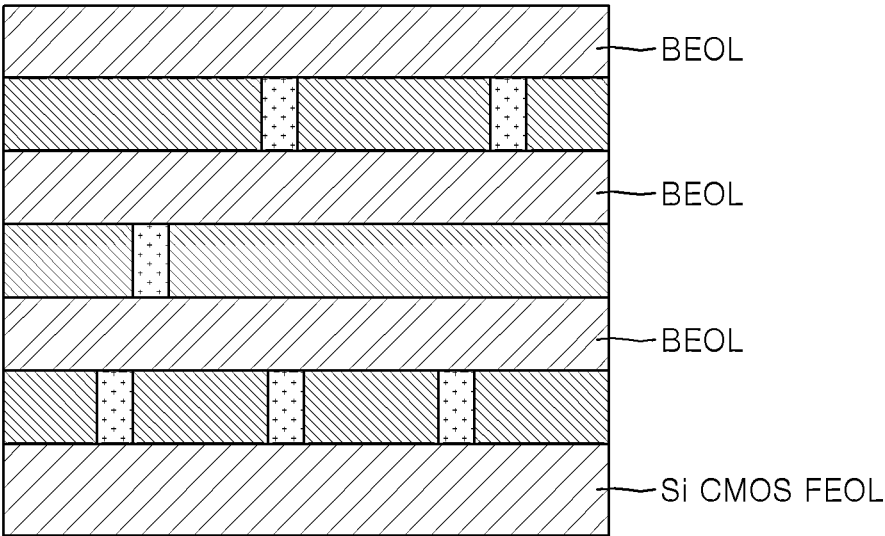


FIG. 3



**FIG. 4**

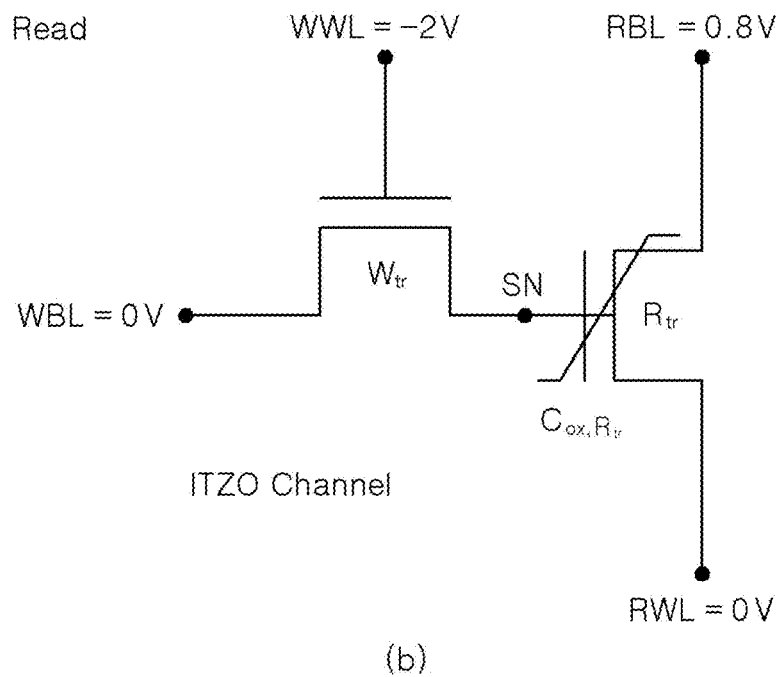
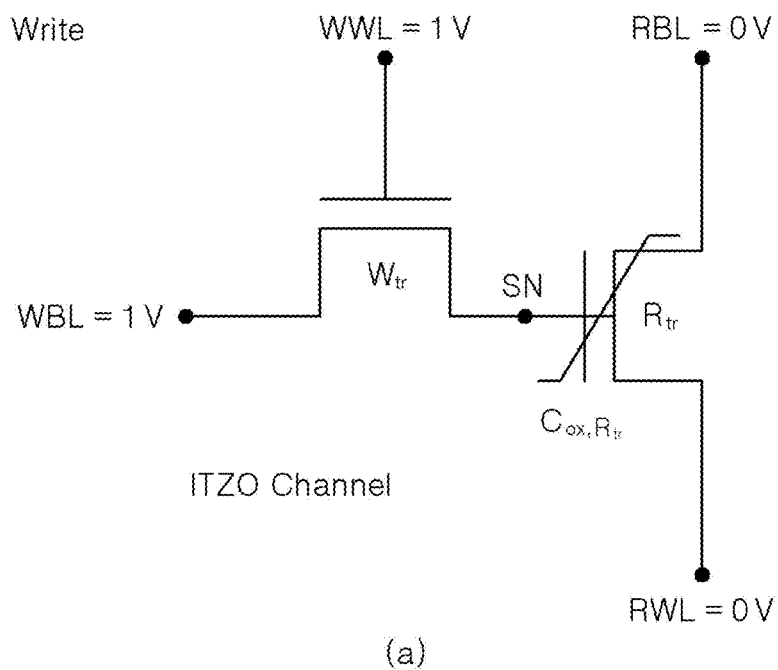


FIG. 5

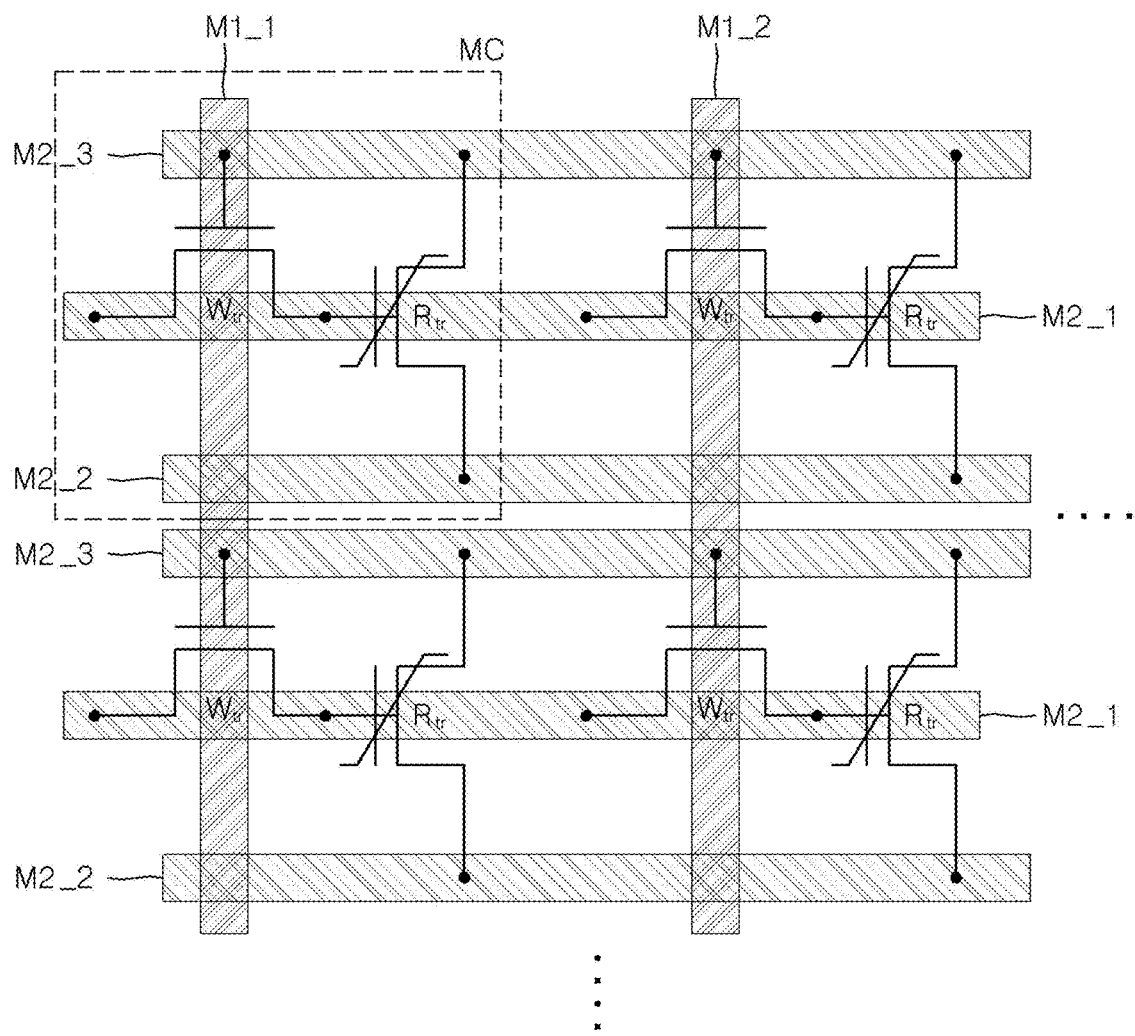


FIG. 6

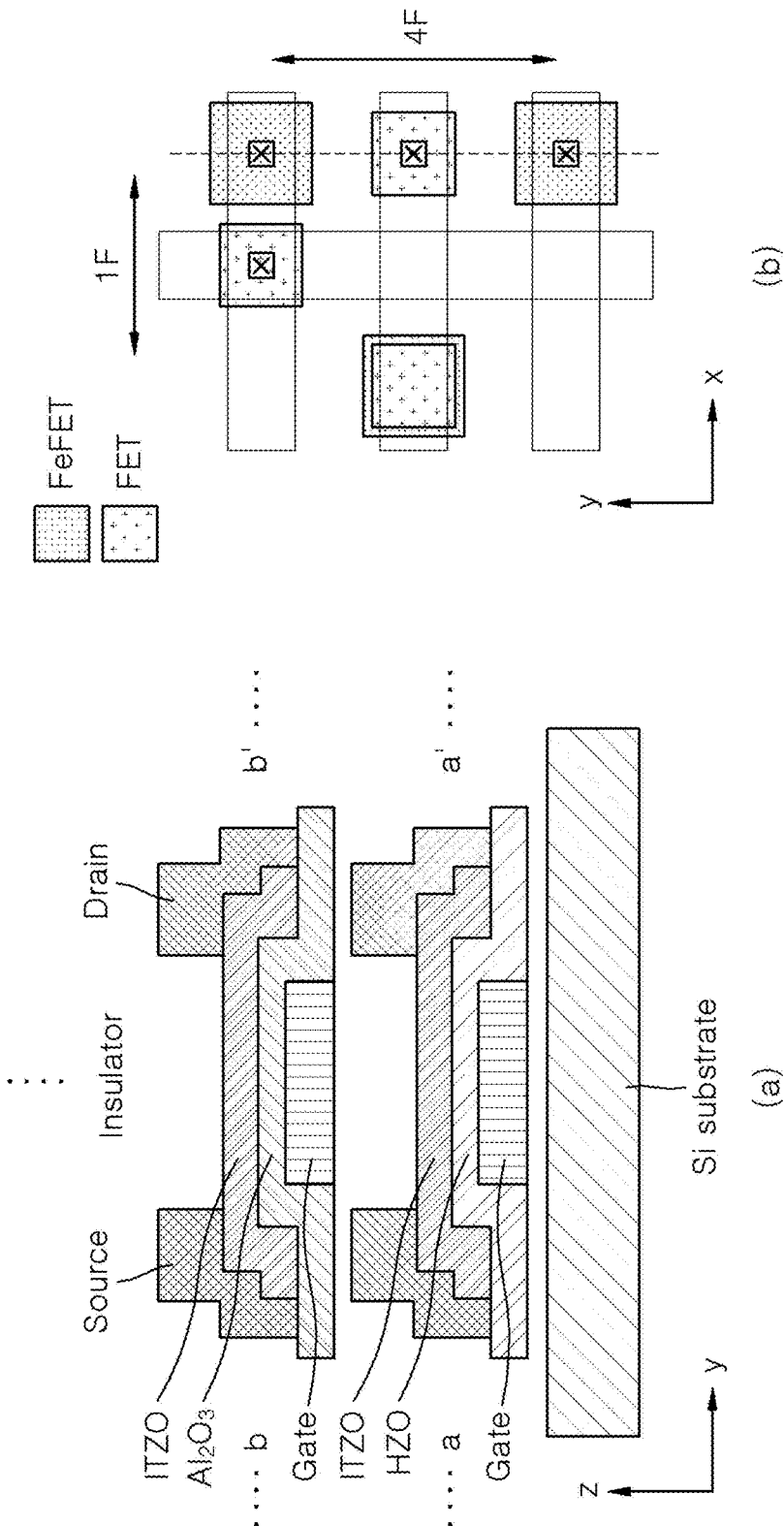


FIG. 7

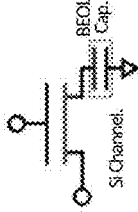
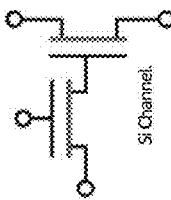
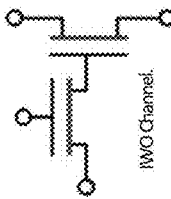
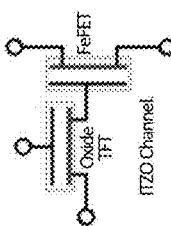
Embedded DRAM options				
Type	1T-1C [1]	2T [2]	AOS* 2T [3,4]	Nonvolatile 2T FeDRAM (This Invention)
Circuit Schematic				
Retention Time	100~2000 $\mu$ s	100~1000 $\mu$ s	1~10 s	10~160 yrs
Access Time	1~10 ns	1~10 ns	1~10 ns	1 ~ 10 ns
Destructive Read	Yes	No	No	No
Density (Mb/mm <sup>2</sup> )	10~30	1~10	80~200	80~200
Periphery	FEOL	FEOL	FEOL	FEOL
Bit Cell	FEOL/BEOL	FEOL	BEOL	BEOL



FIG. 8A

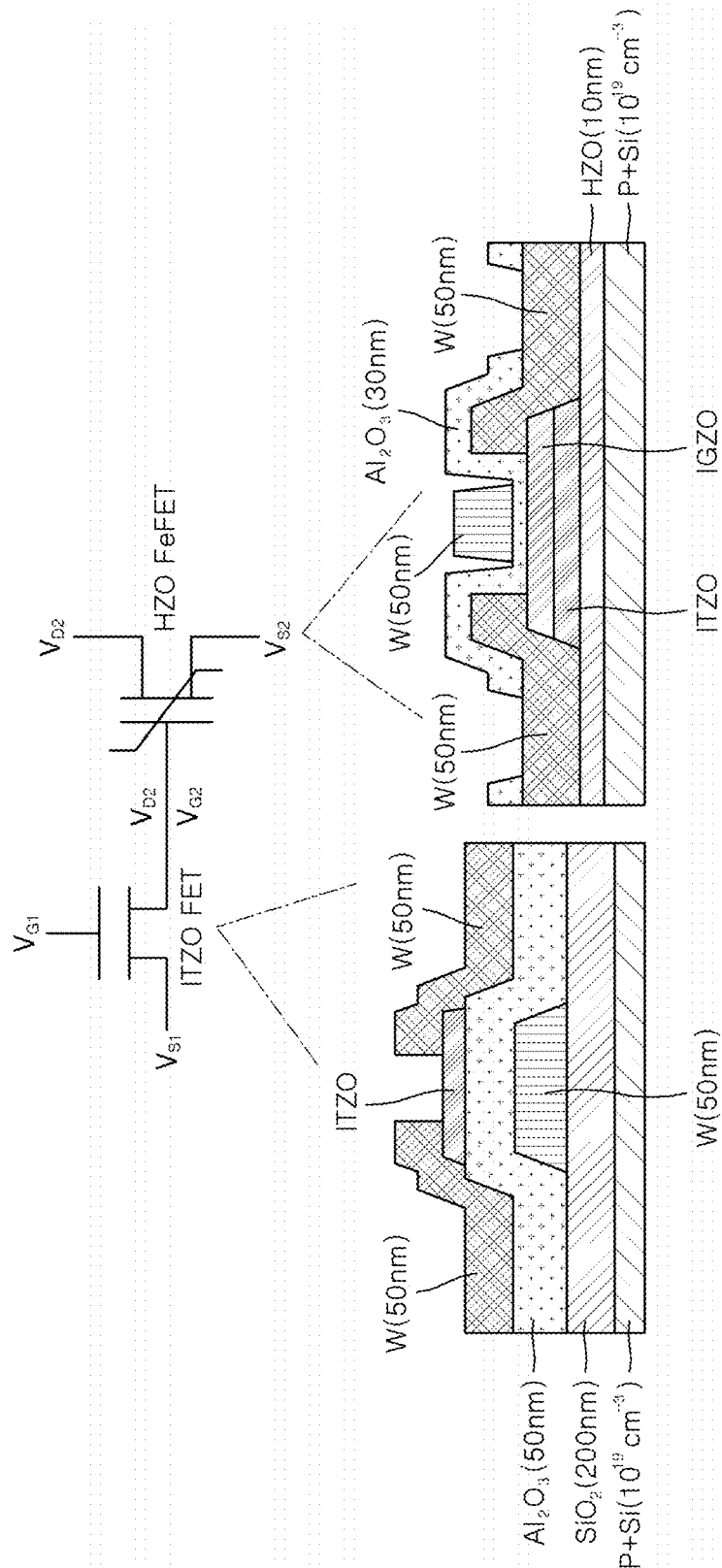


FIG. 8B

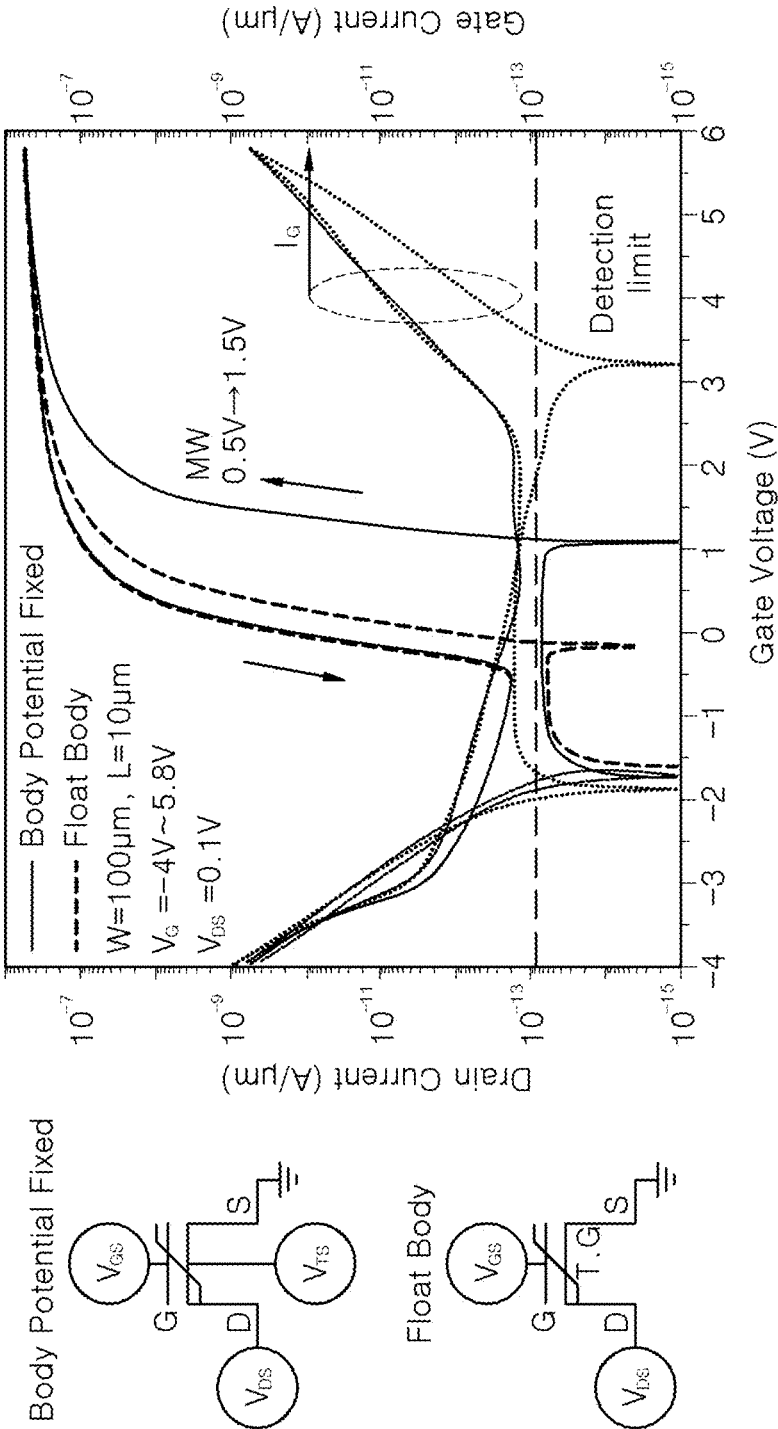
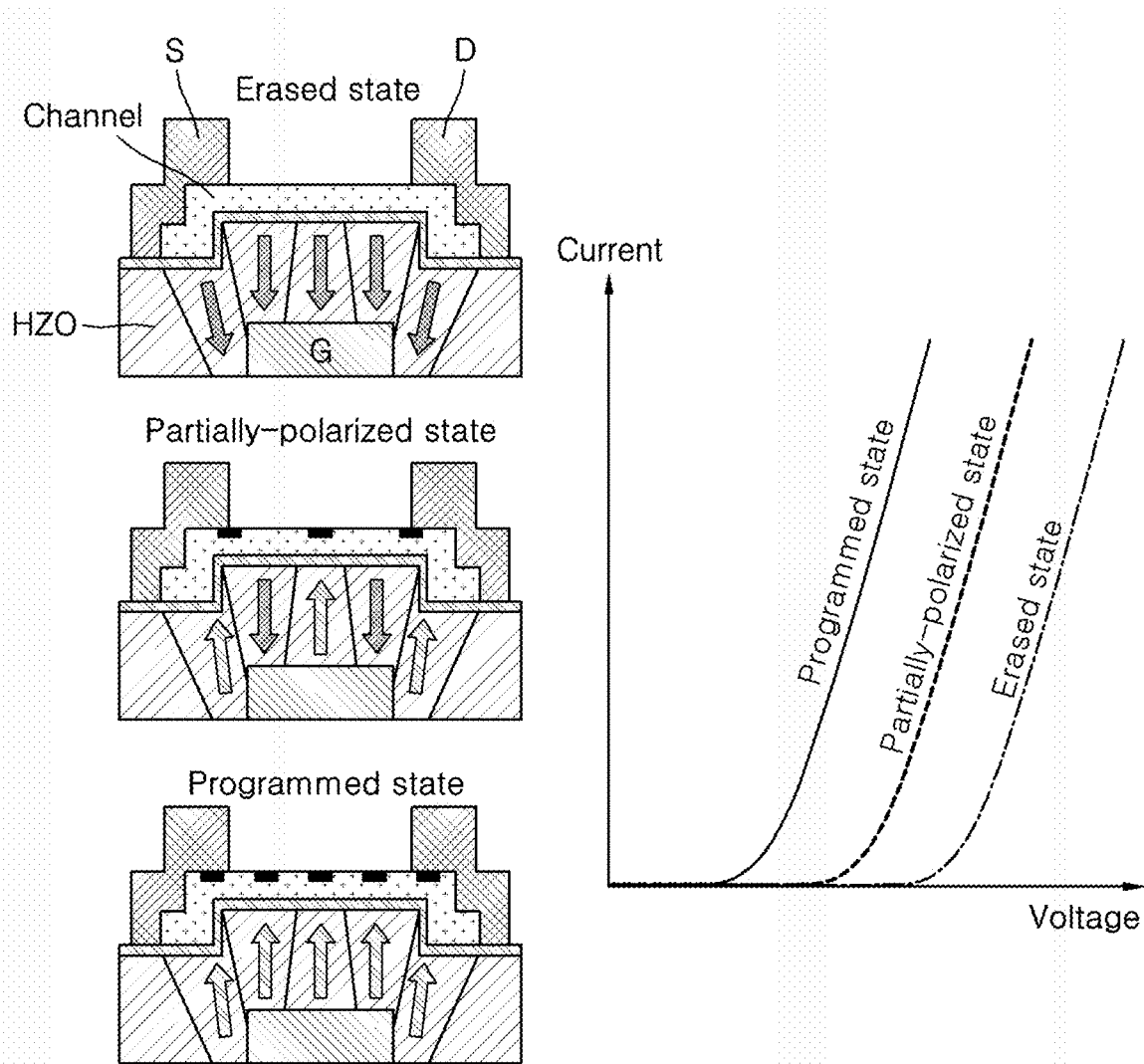


FIG. 8C



**FIG. 8D**

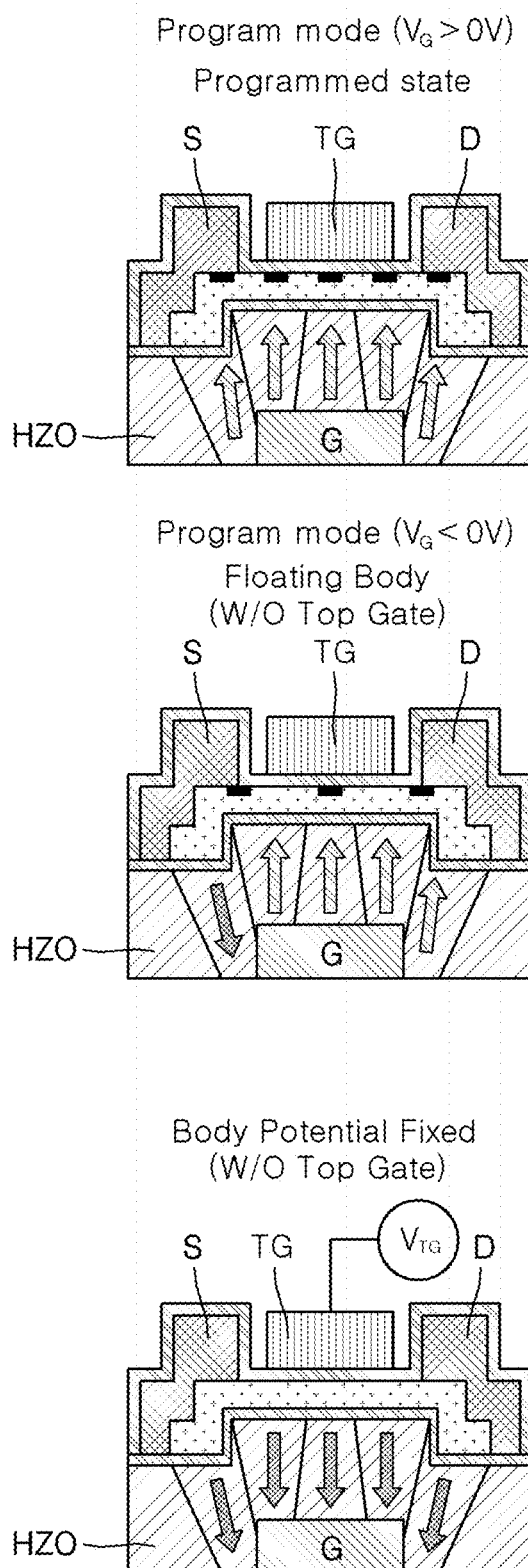
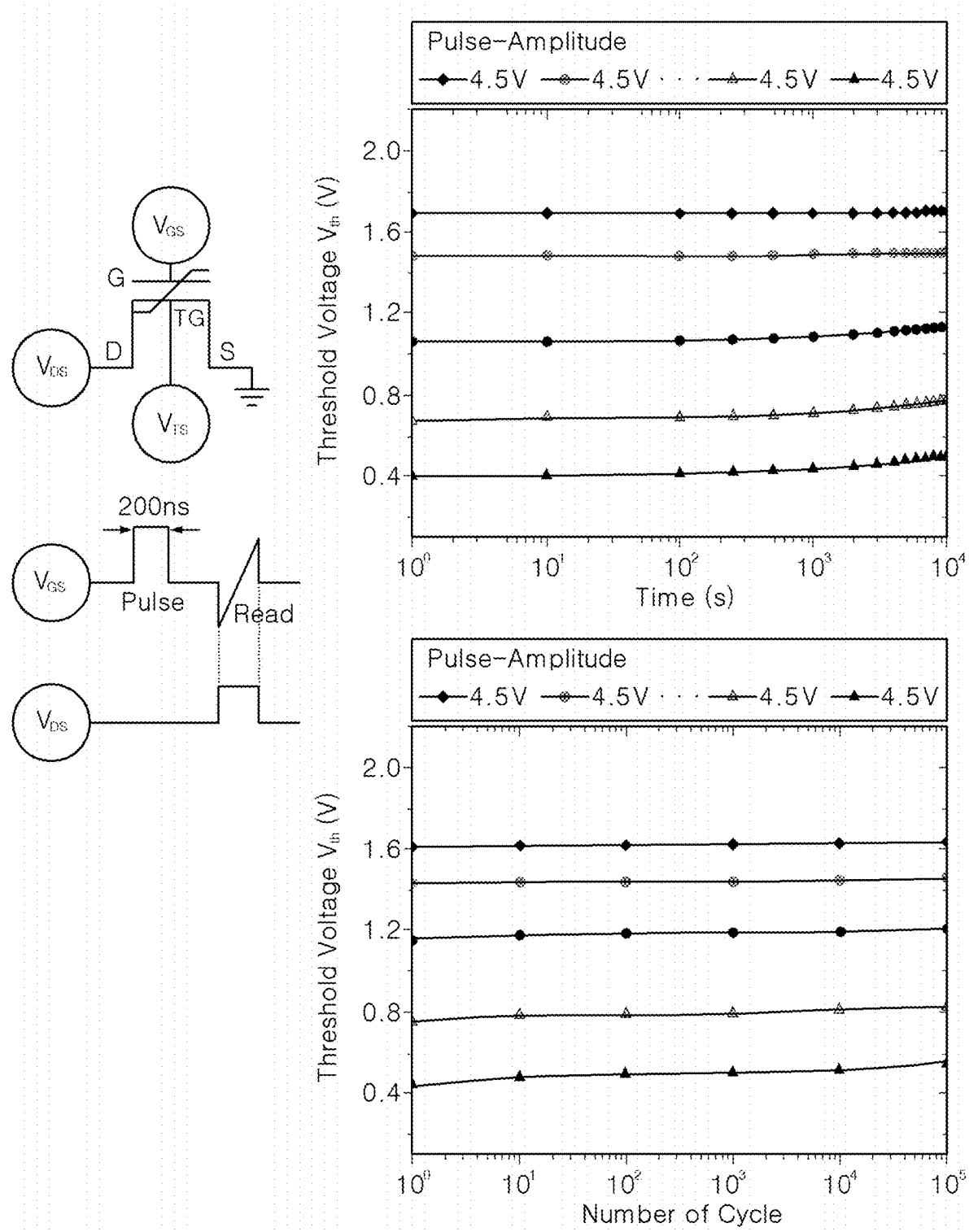
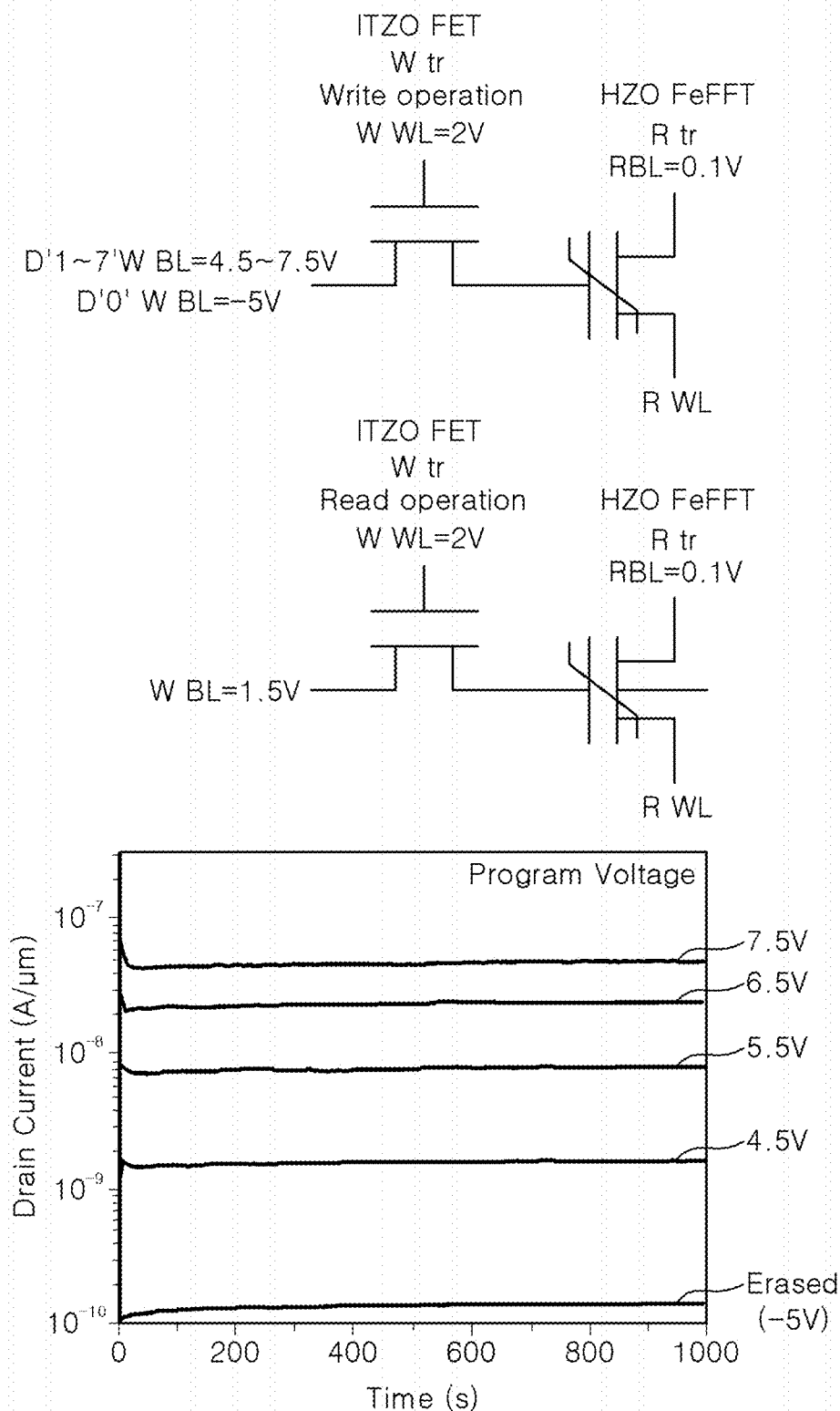


FIG. 9



**FIG. 10**



## NON-VOLATILE MEMORY DEVICE AND ITS OPERATING METHOD

### CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Republic of Korea Patent Application 10-2022-0176814 (filed 16 Dec. 2022) and Republic of Korea Patent Application 10-2023-0181567 (filed 14 Dec. 2023). The entire disclosure of both of these priority applications is hereby incorporated by reference herein.

### BACKGROUND

#### 1. Field of the Invention

[0002] The present invention relates to a non-volatile memory device and an operating method thereof, and more specifically, to a non-volatile memory device using a ferroelectric material and an operating method thereof.

#### 2. Discussion of Related Art

[0003] A dynamic random access memory (DRAM) has a simple structure and is easy to integrate, and thus it is used as a large-capacity temporary memory device. DRAMs form the mainstream of Korean semiconductor industry and are products that occupy a very large part of the semiconductor business.

[0004] Meanwhile, a DRAM has a problem of information destruction due to a physical overlap of read and write paths. For example, during a reading and writing process, because a portion where a voltage is applied and a portion where a current flows overlap and thus information is lost, a process of rewriting the information in a memory cell is necessary. This requires a non-destructive memory operation method.

[0005] In addition, a DRAM does not have a long retention time due to a limit of leakage current of a capacitor. Unlike a static random access memory (SRAM) or a flash memory, a phenomenon in which information stored in memory cells is lost over time (referred to as volatility) occurs in a DRAM. This is because a memory cell of a DRAM is formed of one transistor and one capacitor, and thus natural leakage of data stored in the capacitor occurs. Therefore, in order to prevent data loss, a refresh operation is performed to rewrite the information stored in the memory cell at regular intervals. The refresh operation may be performed by activating a word line in an active state at least once within a retention time of each memory cell to amplify data. The refresh operation consumes additional power.

[0006] Thus, in order to improve memory device performance, research is needed to enable non-destructive path implementation and increase a retention time.

### SUMMARY OF THE INVENTION

[0007] The present invention is directed to providing a non-volatile memory technology that solves the shortcomings of the existing dynamic random access memory (DRAM), which inevitably has a low retention time and a destructive operation method, by implementing a non-destructive path and using a ferroelectric material.

[0008] Meanwhile, other unspecified objects of the present invention will be additionally considered within the scope that can be easily inferred from the following detailed description and an effect thereof.

[0009] According to an aspect of the present invention, there is provided a non-volatile memory device including a memory cell including a write transistor and a ferroelectric read transistor, a write word line connected to a gate terminal of the write transistor, a write bit line connected to a source terminal of the write transistor, a read word line connected to a source terminal of the ferroelectric read transistor, and a read bit line connected to a drain terminal of the ferroelectric read transistor, wherein a drain terminal of the write transistor is connected to a gate terminal of the ferroelectric read transistor.

[0010] The drain terminal of the write transistor may be connected to the gate terminal of the ferroelectric read transistor through a storage node and may induce a polarization direction in a ferroelectric material of the ferroelectric read transistor while the write transistor is turned on.

[0011] The ferroelectric material may be hafnium-zirconium oxide.

[0012] The memory cell may be formed on a silicon complementary metal-oxide semiconductor (CMOS) logic integrated circuit through a front end of line (FEOL) process on a silicon substrate and may be stacked vertically through a back end of line (BEOL) process.

[0013] The memory cell may be stacked in an order in which the write transistor is disposed on the ferroelectric read transistor.

[0014] Indium-tin-zinc oxide (ITZO) to which a BEOL process is applicable may be applied to the write transistor as a channel layer, and hafnium-zirconium oxide (HZO) and ITZO to which a BEOL process is applicable may be applied to the ferroelectric read transistor as an insulating layer and a channel layer, respectively.

[0015] The insulating layer may be formed using ion beam sputtering during the BEOL process forming the ferroelectric read transistor.

[0016] A gate structure of the write transistor may have a structure in which a gate electrode serving as a conductive layer, an insulator serving as an insulating layer, and an amorphous oxide semiconductor layer serving as a channel layer are stacked, and a gate structure of the ferroelectric read transistor may have a structure in which a gate electrode serving as a conductive layer, a ferroelectric layer serving as an insulating layer, and an amorphous oxide semiconductor layer serving as a channel layer are stacked.

[0017] The ferroelectric layer may be any one selected from the group consisting of HZO, hafnium-lanthanum oxide (HfLaO), hafnium-Si oxide (HfSiO), and hafnium-aluminum oxide (HfAlO), and the amorphous oxide semiconductor layer may be any one selected from the group consisting of ITZO, indium-gallium-zinc oxide (IGZO), indium oxide (InO), and zinc oxide (ZnO).

[0018] The ferroelectric read transistor may be a single gate transistor.

[0019] The ferroelectric read transistor may be a double gate transistor including a bottom gate and a top gate.

[0020] Electrons may be accumulated in a channel by a write voltage applied to the bottom gate of the ferroelectric read transistor, an electric field may be applied to the ferroelectric material to store polarization, and the stored polarization may be maintained by the ferroelectric material and an operating voltage may be changed so that data is stored; and an inversion channel may be formed by an erase voltage applied to the bottom gate and the top gate, and thus

an electric field may be applied to the ferroelectric material so that the polarization may be changed and the data erased.

**[0021]** According to another aspect of the present invention, there is provided a method of operating a non-volatile memory device, which includes a memory cell including a write transistor and a ferroelectric read transistor, a write word line connected to a gate terminal of the write transistor, a write bit line connected to a source terminal of the write transistor, a read word line connected to a source terminal of the ferroelectric read transistor, and a read bit line connected to a drain terminal of the ferroelectric read transistor, a drain terminal of the write transistor being connected to a gate terminal of the ferroelectric read transistor, the method including applying a first write control voltage to the write transistor through the write word line and the write bit line, applying a second write control voltage to the ferroelectric read transistor through the read word line and the read bit line, and writing a polarization direction in the ferroelectric material of the ferroelectric read transistor; and applying a first read control voltage to the write transistor through the write word line and the write bit line, applying a second read control voltage to the ferroelectric read transistor through the read word line and the read bit line, and reading data from a drain current of the ferroelectric read transistor varying according to the polarization direction.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0022]** The above and other objects, features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing exemplary embodiments thereof in detail with reference to the accompanying drawings, in which:

**[0023]** FIG. 1 is a circuit diagram illustrating one memory cell of a non-volatile memory device according to one embodiment;

**[0024]** FIG. 2 shows a plan view and a cross-sectional view of one memory cell of the non-volatile memory device according to one embodiment;

**[0025]** FIG. 3 is a cross-sectional view illustrating a monolithic three-dimensional (3D) integrated structure of a 2T0C Fe dynamic random access memory (FeDRAM) according to one embodiment;

**[0026]** FIG. 4 is a diagram illustrating write and read operations of the 2T0C FeDRAM cell according to one embodiment;

**[0027]** FIG. 5 is a diagram illustrating an implementation example of a cell array of the 2T0C FeDRAM according to one embodiment;

**[0028]** FIG. 6 shows a cross-sectional view and a plan view of a 3D integrated 2T0C FeDRAM cell according to one embodiment;

**[0029]** FIG. 7 is a graph showing a comparison result between characteristics of the 2T0C FeDRAM according to one embodiment and the existing DRAM;

**[0030]** FIG. 8A is a diagram illustrating a structure of the 2T0C FeDRAM cell to which a double gate is applied according to one embodiment;

**[0031]** FIG. 8B is a diagram illustrating a transfer curve of a Fe field effect transistor (FeFET) used in a read transistor of the 2T0C FeDRAM of FIG. 8A for each case according to a body potential;

**[0032]** FIG. 8C is a schematic diagram illustrating an operating principle of an amorphous oxide semiconductor film-based FeFET according to one embodiment;

**[0033]** FIG. 8D is a schematic diagram illustrating a write state and an erase state of the amorphous oxide semiconductor film-based FeFET according to one embodiment;

**[0034]** FIG. 9 is a diagram showing results of non-volatile characteristics and durability characteristics of a FeFET used in the read transistor of the 2T0C FeDRAM according to one embodiment; and

**[0035]** FIG. 10 is a diagram showing non-volatile results of a multi-level state 2T0C Fe ferroelectric RAM (FeFRAM) according to one embodiment.

**[0036]** It is noted that the accompanying drawings are illustrated as references for understanding the technical spirit of the present invention, and thereby the scope of the present invention is not limited thereto.

#### DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

**[0037]** The above and other objectives, features, and advantages of the present invention will become more apparent from the following description of exemplary embodiments with reference to the accompanying drawings. However, the present invention is not limited to the embodiments disclosed herein and may be implemented in other forms. Rather, the embodiments disclosed herein are provided so that the disclosed content can be more thorough and complete and the spirit of the present invention can be sufficiently conveyed to those skilled in the art, without any intention other than to provide convenience of understanding.

**[0038]** In the present specification, when it is mentioned that certain elements or lines are connected to a target element block, it includes not only a direct connection but also an indirect connection to the target element block through some other elements.

**[0039]** In addition, the same or similar reference numerals presented in each drawing denote the same or similar components whenever possible. In some drawings, connection relationships between elements and lines are only shown for effective description of technical content, and other elements or circuit blocks can be further provided.

**[0040]** Each embodiment described and illustrated herein may also include a complementary embodiment thereof, and it is noted that a general operation of a display device or details of circuits or devices for performing the general operation are not described in detail so as not to obscure the gist of the present invention.

**[0041]** FIG. 1 is a circuit diagram illustrating one memory cell of a non-volatile memory device according to one embodiment. As shown in FIG. 1, a memory cell has a 2T0C structure and includes a write transistor  $W_{tr}$  and a ferroelectric read transistor  $R_{tr}$ . The write transistor  $W_{tr}$  may be a metal-oxide semiconductor field-effect transistor (MOSFET). The ferroelectric read transistor  $R_{tr}$  may be a ferroelectric field-effect transistor (FeFET). This is a Fe dynamic random access memory (FeDRAM) which uses ferroelectric materials, instead of capacitors used in the existing Si complementary metal-oxide semiconductor (CMOS)-based DRAM.

**[0042]** The shortcomings of the existing DRAM, which inevitably has a low retention time and a destructive operation method, are solved by implementing a non-destructive path, and a ferroelectric material with a theoretically infinite retention time is used.



**[0043]** As shown in the drawing, as metal lines, a write word line WWL, a write bit line WBL, a read word line RWL, and a read bit line RBL are connected to each transistor. Specifically, the write word line WWL is connected to a gate terminal of the write transistor  $W_{tr}$ , and the write bit line WBL is connected to a source terminal of the write transistor  $W_{tr}$ . The read word line RWL is connected to a source terminal of the ferroelectric read transistor  $R_{tr}$ , and the read bit line RBL is connected to a drain terminal of the ferroelectric read transistor  $R_{tr}$ .

**[0044]** In addition, the two transistors are connected to each other with a storage node SN interposed therebetween. Specifically, a drain terminal of the write transistor  $W_{tr}$  is connected to a gate terminal of the ferroelectric read transistor  $R_{tr}$  at the storage node SN.

**[0045]** The 2T0C FeDRAM shown in the drawing uses a ferroelectric material, and the ferroelectric material is a material that maintains polarization in a ground state at a Curie temperature or less and is applied as an insulating layer  $C_{ox}$ ,  $R_{tr}$  of the read transistor of the FeDRAM. Due to the ferroelectric material applied as the insulating layer, information of the 2T0C FeDRAM is stored in the read transistor, and once stored information has an expected retention value of about 10 years due to characteristics of the ferroelectric material.

**[0046]** A Hf-based ferroelectric material may be applied as the ferroelectric material. As an example, any one selected from the group consisting of hafnium-zirconium oxide (HZO), hafnium-lanthanum oxide (HfLaO), hafnium-Si oxide (HfSiO), and hafnium-aluminum oxide (HfAlO) may be applied as the Hf-based ferroelectric material.

**[0047]** Indium-tin-zinc oxide (ITZO), which is a type of oxide semiconductor, may be applied as a channel layer of each transistor. ITZO is a material which has a low leakage current and high mobility and which is advantageous for a low-power operation. Meanwhile, ITZO is an example, and various amorphous oxide semiconductors such as indium-gallium-zinc oxide (IGZO), indium oxide (InO), and zinc oxide (ZnO) may be applied.

**[0048]** In addition, various conductive materials may be applied to the metal materials used in the write word line WWL, the write bit line WBL, the read bit line RBL, and the read word line RWL of the 2T0C FeDRAM, as necessary.

**[0049]** FIG. 2 shows a plan view and a cross-sectional view of one memory cell of the non-volatile memory device according to one embodiment. Referring to FIG. 2A first, a source of the write transistor  $W_{tr}$  corresponds to the write bit line WBL, and a gate of the write transistor  $W_{tr}$  corresponds to the write word line WWL. A source of the read transistor  $R_{tr}$  corresponds to the read word line RWL, and a drain of the read transistor  $R_{tr}$  corresponds to the read bit line RBL. The drain of the write transistor  $W_{tr}$  and the gate of the read transistor  $R_{tr}$  are connected to each other through a storage node SN, and a device structure capable of minimizing resistance of the storage node SN is proposed.

**[0050]** Referring to FIG. 2B, a gate structure included in the write transistor  $W_{tr}$  has a stacked shape of a gate electrode Gate serving as a conductive layer, an insulator serving as an insulating layer, and ITZO serving as a channel layer. A gate structure included in the ferroelectric read transistor  $R_{tr}$  has a stacked shape of a gate electrode Gate serving as a conductive layer, a ferroelectric layer (HZO) serving as an insulating layer, and an oxide semiconductor layer (ITZO) serving as a channel layer. The reference

symbol HZO is only used to emphasize hafnium-zirconium oxide, which is a ferroelectric material, as the insulating layer, and the reference symbol ITZO is only used to emphasize indium-tin-zinc oxide, which is an amorphous oxide semiconductor, as the channel layer, and these are not necessarily used to limit the presented materials. For example, when HfLaO, HfSiO, or HfAlO is used instead of HZO, HfLaO, HfSiO, or HfAlO may be used as the reference symbol, and when IGZO, InO, or ZnO is used instead of ITZO, IGZO, InO, or ZnO may be used as the reference symbol.

**[0051]** According to one embodiment, the two transistors  $W_{tr}$  and  $R_{tr}$  may be deposited through the same process. Both the write transistor  $W_{tr}$  and the ferroelectric read transistor  $R_{tr}$  may be disposed on an insulating layer pattern Insulator of a Si CMOS logic IC. That is, the 2T0C FeDRAM is a device suitable for a silicon CMOS process and may be deposited through a process using a Si CMOS logic IC.

**[0052]** FIG. 3 is a cross-sectional view illustrating a monolithic three-dimensional (3D) integrated structure of a 2T0C Fe FeDRAM according to one embodiment. As shown in the drawing, the Si CMOS logic IC may be integrated on a silicon substrate through a front end of line (FEOL) process, and a bit cell may be stacked on the Si CMOS logic IC through a back end of line (BEOL) process. To this end, ITZO and HZO, to which the BEOL process is applicable, may be applied to each transistor.

**[0053]** FIG. 4 is a diagram illustrating write and read operations of the 2T0C FeDRAM cell according to one embodiment. FIG. 4A shows the write operation, and FIG. 4B shows the read operation.

**[0054]** Referring to FIG. 4A first, in the write operation, a first write control voltage is applied to the write transistor  $W_{tr}$  through the write word line WWL and the write bit line WBL, and a second write control voltage is applied to the ferroelectric read transistor  $R_{tr}$  through the read word line RWL and the read bit line RBL so that a polarization direction is written in a ferroelectric material  $C_{ox}$ ,  $R_{tr}$  of the ferroelectric read transistor  $R_{tr}$ . As an example, 1 V may be applied to the write word line WWL, 1 V may be applied to the write bit line WBL, 0 V may be applied to the read bit line RBL, and 0 V may be applied to the read word line RWL. In this case, a channel layer may be formed in the write transistor  $W_{tr}$  due to the write word line WWL, and information may be stored in a polarized form in the ferroelectric material  $C_{ox}$ ,  $R_{tr}$  of the ferroelectric read transistor  $R_{tr}$  through the channel layer of the write transistor  $W_{tr}$  due to the write bit line WBL. Thereafter, even when no voltage is applied, the information stored in the polarized form may be maintained.

**[0055]** Referring to FIG. 4B, in the read operation, a first read control voltage is applied to the write transistor  $W_{tr}$  through the write word line WWL and the write bit line WBL, a second read control voltage is applied to the ferroelectric read transistor  $R_{tr}$  through the read word line RWL and read bit line RBL so that data is read from a drain current of the ferroelectric read transistor  $R_{tr}$ , which varies according to the polarization direction of the ferroelectric material  $C_{ox}$ ,  $R_{tr}$  of the ferroelectric read transistor  $R_{tr}$ . As an example, -2 V may be applied to the write word line WWL, 0 V may be applied to the write bit line WBL, 0.8 V may be applied to the read bit line RBL, and 0 V may be applied to the read word line RWL. In this case, a voltage potential

barrier may be generated between the write transistor  $W_r$  and the ferroelectric read transistor  $R_r$  due to the voltage applied to the write word line WWL to prevent any unexpected reverse operation. In this state, carriers move from the read bit line RBL through the channel layer induced by the polarization generated by the writing process, and thus a current is read. In this case, the read current varies according to whether the polarization is present. In this way, it is possible to determine whether writing is performed on the device.

**[0056]** It is noted that, during the above-described write and read processes, a portion where the voltage is applied and a portion where the current flows do not overlap absolutely. The structural characteristics of the 2T0C FeDRAM according to the embodiment enable a non-destructive read method to be implemented.

**[0057]** FIG. 5 is a diagram illustrating an implementation example of a cell array of the 2T0C FeDRAM according to one embodiment. The 2T0C FeDRAM formed of the write transistor  $W_r$  and the ferroelectric read transistor  $R_r$  may be externally driven generally in an active matrix manner through two metal lines M1 and M2. Reference symbols M1\_1 and M1\_2 are referred to as M1. Reference symbols M2\_1, M2\_2, and M2\_3 are referred to as M2. A description will be made based on one cell MC indicated by a dotted line in the following drawing.

**[0058]** A first metal line M1\_1 is electrically connected to gates of write transistors  $W_r$ . By applying a voltage that is greater than or equal to a threshold voltage to the first metal line M1\_1, channel layers of the write transistors  $W_r$  may be formed. The first metal line M1\_1 may correspond to the write word line WWL.

**[0059]** The above description is based on the first metal line M1\_1 on the left side of the drawing, but the same description can be applied to a first metal line M1\_2 on the right side of the drawing.

**[0060]** Second metal lines M2\_1, M2\_2, and M2\_3 are electrically connected to sources of the write transistors  $W_r$ , sources of the read transistors  $R_r$ , and drains of the read transistors  $R_r$ . The second metal line M2\_1 at an intermediate stage in the drawing is connected to the sources of the write transistors  $W_r$ , the second metal line M2\_2 at a lower stage in the drawing is connected to the sources of the read transistors  $R_r$ , and the second metal line M2\_3 at an upper end in the drawing is connected to the drains of the read transistors  $R_r$ . The second metal lines M2\_1, M2\_2, and M2\_3 may serve to store information in the read transistor  $R_r$  during the write process and to read the stored information during the read process. The second metal line M2\_1 at the intermediate end of the drawing may be connected to the write bit line WBL, the second metal line M2\_2 at the lower end of the drawing may be connected to the read word line RWL, and the second metal line M2\_3 at the upper end of the drawing may be connected to the read bit line RBL.

**[0061]** A gap between the first metal line M1 and the second metal line M2 is filled with a passivation material, and various conductive materials may be applied as metal materials constituting the first metal line M1 and the second metal line M2, as necessary.

**[0062]** FIG. 6 shows a cross-sectional view and a plan view of a 3D integrated 2T0C FeDRAM cell according to one embodiment. FIG. 6A shows the cross-sectional view, and FIG. 6B shows the plan view.

**[0063]** First, as shown in FIG. 6A, in the 2T0C FeDRAM cell, the ferroelectric read transistor of the FeFET and the write transistor of the FET may be vertically integrated. In this case, it is noted that a high-density general-purpose memory device may be achieved by performing 3D integration by applying ITZO and HZO to which a BEOL process is applicable. That is, HZO may be applied as a ferroelectric material and ITZO may be applied as an oxide semiconductor material in the FeFET, and ITZO may be applied as an oxide semiconductor material in the FET. Meanwhile, for example, an  $\text{Al}_2\text{O}_3$  thin film with a thickness of 10 nm may be used as an insulating material in the FET.

**[0064]** When the 3D integration is performed according to one embodiment, HZO may be formed using ion beam sputtering, which allows an additional annealing process at a relatively low temperature, rather than forming HZO using atomic layer deposition (ALD). This is advantageous for a 3D process of ITZO, which requires a low-temperature process.

**[0065]** As shown in FIG. 6B, in the 2T0C FeDRAM cell, the write transistor of FET may be disposed on the ferroelectric read transistor of the FeFET. The first metal line connected to the gate of the FET extends in a y direction in the drawing. The second metal line connected to the drain of the FeFET and positioned at the upper end of the drawing extends in an x-direction in the drawing. The second metal line connected to the source of the FET and positioned at the intermediate end of the drawing extends in the x-direction in the drawing. In addition, the second metal line connected to the source of the FeFET and positioned at the lower end of the drawing extends in the x-direction in the drawing. Meanwhile, a connection portion between each transistor and the metal line is marked with an x, and since the drain of the FET and the gate of the FeFET may be connected at the storage node, a separate mark is not indicated.

**[0066]** FIG. 7 is a graph showing a comparison result between characteristics of the 2T0C FeDRAM according to one embodiment and the existing DRAM.

**[0067]** Referring to FIG. 7, a 1T-1C DRAM has a low retention time and a destructive read method and also has low integration. A 2T DRAM has a lower retention time and lower integration than the 1T-1C DRAM, but since the 2T DRAM uses a gain of the transistor, physical paths for reading and writing are separated, and thus a non-destructive method is implemented. Compared to the 1T-1C DRAM and the 2T type DRAM, an AOS 2T DRAM achieves the highest retention time using an amorphous oxide semiconductor and has non-destructive data using the gain of the transistor. In addition, 3D integration of bit cells may be possible using the BEOL process to increase integration. It can be confirmed that a 2T-0C FeDRAM according to one embodiment is non-destructive and has a retention time of a unit that is incomparable to the above three structures. In addition, the integration is very high.

**[0068]** FIG. 8A is a diagram illustrating a structure of the 2T0C FeDRAM cell to which a double gate is applied according to one embodiment. FIG. 8B shows a transfer curve of FeFET used in the read transistor of the 2T0C FeDRAM of FIG. 8A for each case (body potential fixed and float body) according to a body potential. The body potential fixed corresponds to an example in which a double gate is applied, and the floating body corresponds to an example in which a single gate is applied. In addition, FIG. 8C is a schematic diagram illustrating an operating principle of an

amorphous oxide semiconductor film-based FeFET according to one embodiment, and FIG. 8D is a schematic diagram illustrating a write state and an erase state of the amorphous oxide semiconductor film-based FeFET according to one embodiment.

**[0069]** As shown in FIG. 8A, the read transistor of the 2T0C FeDRAM is a double gate so that an electric field can be applied more efficiently to HZO.

**[0070]** Specifically, to describe the principle with reference to FIGS. 8C and 8D, when a (+) voltage is applied to the gate, electrons in the channel accumulate, and thus an electric field is efficiently applied to HZO and polarization is stored. The polarization of HZO is maintained by ferroelectricity, and thus an operating voltage  $V_{th}$  is changed and data is stored. However, since the amorphous oxide semiconductor used as the channel layer is an n-type semiconductor with many electrons and few holes, the amorphous oxide semiconductor has a characteristic of a large band gap, and a problem in which, even when a (−) voltage is applied to the gate, an inversion channel is not formed and the voltage is not efficiently applied to HZO may occur. That is, a problem with poor erase may occur. To solve the above problem, a top gate is positioned on the channel, and a voltage is applied to the top gate so that an electric field effectively acts on HZO, the polarization of HZO is changed, and thus erasing is possible. That is, in the case of a single gate, an inversion channel is not properly formed and thus a voltage cannot be efficiently applied to HZO, but in the case of a double gate, the voltage may be efficiently applied to HZO through the voltage applied to the top gate. When a transistor of a cross section shown on the left side of FIG. 8A is a single gate, like a transistor of a cross section shown on the right side, a double gate may be implemented by forming a passivation layer  $Al_2O_3$  above a source and a drain and placing a top gate on the passivation layer  $Al_2O_3$ . The source and the drain below the passivation layer may be connected to an external terminal through a via hole. Meanwhile, in the cross section shown on the right side, a lower gate is not shown for convenience of description, but the same gate as in the cross section shown on the left side may be disposed between HZO and  $P^+$  Si to serve as a lower gate.

**[0071]** As shown in FIG. 8B, it can be seen that the read transistor of the 2T0C FeDRAM is formed as a double gate so that erasing can be easily performed and a memory window can be expanded by effectively applying a voltage to a ferroelectric material. In the drawing, an example in which a memory window MW is expanded from 0.5 V to 1.5 V is shown. The number of data states capable of being written and read may increase through the expansion of the memory window. That is, it is possible to secure a large memory window due to the double gate.

**[0072]** FIG. 9 is a diagram showing results of non-volatile characteristics and durability characteristics of a FeFET used in the read transistor of the 2T0C FeDRAM according to one embodiment. A situation in which the voltage is applied to the FeFET is also shown on the left side of the drawing. In this way, unlike the existing DRAM, the 2T0C FeDRAM is expected to use less power due to having a longer data retention time. Therefore, it can be seen that low-power driving of the 2T0C FeDRAM is possible and the 2T0C FeDRAM has non-volatile characteristics. Consequently, the 2T0C FeDRAM may have durability that does not change device characteristics despite repeated operations. That is, even in the FeFET formed of the double gate,

non-volatile characteristics and durability due to an increased data retention time can be confirmed.

**[0073]** FIG. 10 is a diagram showing non-volatile results of a multi-level state 2T0C FeFRAM according to one embodiment. As shown in the drawing, due to the characteristics of FeFET, a drain current of the read transistor may be maintained for almost 1000 seconds or more during a read operation in the 2T0C FeDRAM. The operating voltage of the 2T0C FeDRAM may be adjusted to various states. Thus, the 2T0C FeDRAM may be used as a multi-level state storage device capable of storing multiple states instead of two states of 1 and 0 in the existing DRAM so that high efficiency relative to an area can be achieved. The 2T0C FeDRAM also has a probability of being used as a neuromorphic device such as a synapse that mimics the human brain.

**[0074]** According to the above-described embodiment, a new material and a structure of a DRAM can be provided. Unlike the existing DRAM, since the 2T0C FeDRAM according to one embodiment has a high retention time, the 2T0C FeDRAM has lower power usage so that a low-power and high-efficiency operation is possible unlike the existing DRAM. In the structure proposed for the 2T0C FeDRAM according to one embodiment, physical voltage application directions for reading and writing do not overlap, and thus information is not lost so that non-destructive driving is possible unlike the existing DRAM. In addition, the FeDRAM using amorphous oxide semiconductors and a ferroelectric material can be highly integrated in 3D.

**[0075]** According to the technology, a problem in which information is lost due to an overlap of read and write paths in a memory device is solved so that implementation of a non-destructive path can be achieved.

**[0076]** In addition, according to the technology, a problem of additional power consumed by a refresh operation due to a short retention time of the existing DRAM can be solved.

**[0077]** In this case, according to the technology, an integration problem is also solved.

**[0078]** In addition, according to the technology, a memory window can be expanded by effectively applying a voltage to a ferroelectric material.

**[0079]** In addition, unlike the existing DRAM, according to the technology, a data retention time is long and non-volatile characteristics are provided so that a low-power and high-efficiency operation with lower power consumption is possible.

**[0080]** In addition, according to the technology, an operating voltage can be adjusted to various states, and thus it is possible to use the device as a storage device of multi-level cells, which can store multiple states instead of two states of 1 and 0 in the existing DRAM so that high integration can be achieved.

**[0081]** While the present invention has been described with reference to specific items such as particular components, exemplary embodiments, and the accompanying drawings, these are merely provided to aid in understanding the present invention, and the present invention is not limited to these embodiments, and those skilled in the art to which the present invention pertains can perform various alterations and modifications from the description of the present invention. Therefore, the spirit of the present invention should not be limited to the above-described embodiments, and it should be construed that the appended claims

as well as all equivalents or equivalent modifications of the appended claims will fall within the scope of the present invention.

What is claimed is:

1. A non-volatile memory device comprising:
  - a memory cell including a write transistor and a ferroelectric read transistor;
  - a write word line connected to a gate terminal of the write transistor;
  - a write bit line connected to a source terminal of the write transistor;
  - a read word line connected to a source terminal of the ferroelectric read transistor; and
  - a read bit line connected to a drain terminal of the ferroelectric read transistor,
 wherein a drain terminal of the write transistor is connected to a gate terminal of the ferroelectric read transistor.
2. The non-volatile memory device of claim 1, wherein the drain terminal of the write transistor is connected to the gate terminal of the ferroelectric read transistor through a storage node and induces a polarization direction in a ferroelectric material of the ferroelectric read transistor while the write transistor is turned on.
3. The non-volatile memory device of claim 2, wherein the ferroelectric material includes hafnium-zirconium oxide.
4. The non-volatile memory device of claim 2, wherein the memory cell is formed on a silicon complementary metal-oxide semiconductor (CMOS) logic integrated circuit through a front end of line (FEOL) process on a silicon substrate and is stacked vertically through a back end of line (BEOL) process.
5. The non-volatile memory device of claim 4, wherein the memory cell is stacked in an order in which the write transistor is disposed on the ferroelectric read transistor.
6. The non-volatile memory device of claim 5, wherein indium-tin-zinc oxide (ITZO) to which a BEOL process is applicable is applied to the write transistor as a channel layer, and hafnium-zirconium oxide (HZO) and ITZO to which a BEOL process is applicable are applied to the ferroelectric read transistor as an insulating layer and a channel layer, respectively.
7. The non-volatile memory device of claim 6, wherein the insulating layer is formed using ion beam sputtering during the BEOL process forming the ferroelectric read transistor.
8. The non-volatile memory device of claim 1, wherein:
  - a gate structure of the write transistor has a structure in which a gate electrode serving as a conductive layer, an insulator serving as an insulating layer, and an amorphous oxide semiconductor layer serving as a channel layer are stacked; and
  - a gate structure of the ferroelectric read transistor has a structure in which a gate electrode serving as a conductive layer, a ferroelectric layer serving as an insulating layer, and an amorphous oxide semiconductor layer serving as a channel layer are stacked.
9. The non-volatile memory device of claim 8, wherein: the ferroelectric layer includes any one selected from the group consisting of hafnium-zirconium oxide (HZO), hafnium-lanthanum oxide (HfLaO), hafnium-Si oxide (HfSiO), and hafnium-aluminum oxide (HfAlO); and

the amorphous oxide semiconductor layer includes any one selected from the group consisting of indium-tin-zinc oxide (ITZO), indium-gallium-zinc oxide (IGZO), indium oxide (InO), and zinc oxide (ZnO).

10. The non-volatile memory device of claim 2, wherein the ferroelectric read transistor is a single gate transistor.

11. The non-volatile memory device of claim 2, wherein the ferroelectric read transistor is a double gate transistor including a bottom gate and a top gate.

12. The non-volatile memory device of claim 11, wherein: electrons are accumulated in a channel by a write voltage applied to the bottom gate of the ferroelectric read transistor, an electric field is applied to the ferroelectric material to store polarization, and the stored polarization is maintained by the ferroelectric material and an operating voltage is changed so that data is stored; and an inversion channel is formed by an erase voltage applied to the bottom gate and the top gate, and thus an electric field is applied to the ferroelectric material so that the polarization is changed and the data erased.

13. A method of operating a non-volatile memory device, which includes a memory cell including a write transistor and a ferroelectric read transistor, a write word line connected to a gate terminal of the write transistor, a write bit line connected to a source terminal of the write transistor, a read word line connected to a source terminal of the ferroelectric read transistor, and a read bit line connected to a drain terminal of the ferroelectric read transistor, a drain terminal of the write transistor being connected to a gate terminal of the ferroelectric read transistor, the method comprising:

applying a first write control voltage to the write transistor through the write word line and the write bit line, applying a second write control voltage to the ferroelectric read transistor through the read word line and the read bit line, and writing a polarization direction in the ferroelectric material of the ferroelectric read transistor; and

applying a first read control voltage to the write transistor through the write word line and the write bit line, applying a second read control voltage to the ferroelectric read transistor through the read word line and the read bit line, and reading data from a drain current of the ferroelectric read transistor varying according to the polarization direction.

14. The method of claim 13, wherein the ferroelectric read transistor is a single gate transistor.

15. The method of claim 13, wherein the ferroelectric read transistor is a double gate transistor including a bottom gate and a top gate.

16. The method of claim 13, wherein:

electrons are accumulated in a channel by a write voltage applied to the bottom gate of the ferroelectric read transistor, an electric field is applied to the ferroelectric material to store polarization, and the stored polarization is maintained by the ferroelectric material and the operating voltage is changed so that data is stored; and an inversion channel is formed by an erase voltage applied to the bottom gate and the top gate, and thus an electric field is applied to the ferroelectric material so that the polarization is changed and the data erased.

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