

A Memristor Emulation in 180-nm CMOS Process for Spiking Signal Generation and Chaos Application

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Abstract—We present a new CMOS circuit and its successful fabrication of an operational transconductance amplifier (OTA)-CMOS inverter-based memristor emulator and investigate its switching behavior from 5 MHz to 50 MHz. It could be considered the first memristor emulator based on a current mode circuit and an inverter. Primarily, the transconductance of the inverter stage transforms the bias-voltage-dependent transconductance of the OTA into an overall flux-dependent memductance of the memristor. We also demonstrate how performance measures such as frequency response, noise, post-layout simulation, and process corners impact the memristive behavior of the design. The power consumption of the proposed memristor emulator is 2.25 mW. The aforementioned power figure is based on a 1.8 V power supply and calculated on a UMC 180-nm CMOS technology node. Further, using this memristor emulator, we implement a CMOS circuit for spiking signal generation called the Memristive Integrate-and-Fire (MIF) neuron circuit that mimics a biological neuron. As far as we know, a spiking signal generation using a memristor emulator remains unreported. Later on, we went on to realize a MIF neuron based object detection application to bring out the practical significance of the MIF neuron circuit. We have fabricated a chip of the proposed memristor emulator design with the die size of L=1499.96 μm , W=1499.96 μm , and included its fabrication result to validate the theoretical derivations in the work. At last, we perform an experimental realization of a chaos circuit application with the help of the fabricated chip.

Index Terms—OTA, CMOS, memristor emulator, memristor emulator fabrication, MIF neuron, chaos.

I. INTRODUCTION

IN 1971, Leon Chua first came up with the prediction of a new passive circuit element as a missing link between the

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charge and the flux, which he named memristor [1]. Further in [2], the memristors were generalized to memristive devices (also known as generalized memristors) characterized with a hysteresis having a zero crossing property, showing memory effect while being unable to store any energy. Later in 2008, a team led by R. S. Williams at HP research lab reported the first successful fabrication of memristors [3]. The HP memristors and the nanoscale memristors such as in [4] are generalized memristors. There have been rigorous attempts by researchers to reinvigorate the memristive technology. The memristor stores information in the form of resistance. The emulators based on CMOS technology to mimic properties such as zero crossing, frequency-dependent pinched hysteresis, and non-volatility have been commonly referred to as memristor emulators. The key focus of all the CMOS memristor emulators has been to replicate the working principle of the ideal memristor [1].

To explore the switching phenomena in memristors, various memristor emulator circuits based on different design methodologies have been reported. In recent years, memristor emulator circuits based on the current mode blocks have drawn more attention. Recently, two designs [5], [6] incorporating voltage differencing transconductance amplifiers (VDTA) as the current mode (CM) block have been proposed, which operate up to 50 MHz. Experimental validation and reporting of resistorless memristor using current follower transconductance amplifier (CFTA) have been studied in [7]. A grounded memristor was explored using a second-generation current conveyor (CCII) and some passive elements in [8] with a very limited frequency range. Some memristor emulators employing analog multipliers along with passive elements have been reported in [9], [10], and [11]. A 1 kHz memristor emulator in [12] was designed using a single CCII, a multiplier, and PMOS transistors but incurred very high power consumption. Ranjan et al. proposed a memristor emulator design based on a current conveyor transconductance amplifier (CCTA) [13], which was theoretically and experimentally validated. The memristor emulator in [14], corroborated with its printed circuit board (PCB) prototype has been demonstrated as a high pass filter with its frequency holding up to 1 MHz. In particular, the Differential Voltage CCTA (DVCCTA) block was used in [15] to achieve a memristor emulator topology with 8.74 mW of power consumption. The article introduced in [16] demonstrates two voltage differencing inverting buffered amplifiers (VDIBAs) based emulator consuming 1.34 mW of power

at 1 V, but with a large transistor count of 18. Also, the aforementioned design is limited to 12.7 MHz operating frequency. The topologies of the memristor emulator that incorporated a single OTA along with few transistors and passive elements were experimented in [18] but had limited bandwidth of 24 Hz and 30 Hz respectively. Regarding [19], the major advantage of having two OTAs was an increased frequency range up to 8 MHz. The operating frequency range for spiking neural network applications would depend on the targeted application. For applications in physiological signal processing (for example, EEG signal processing), the operating frequency for spiking neural network application ranges from a few Hz to a few kHz, whereas for applications in pattern recognition, high-performance computing, edge detection, etc., the neuron models could be merited by spiking neuron models working in the range of MHz. The operating frequency of the memristor used in the spiking neuron model needs to be uplifted from a few MHz in order to facilitate even faster computation. To overcome the frequency limitations, various attempts have been made to design an emulator by cascading two CM blocks like OTA and CCII [20], OTA and current differencing transconductance amplifier (CDTA) [21], OTA and voltage differencing buffered amplifier (VDBA) [22] with working frequency as high as 26.3 MHz. OTA and voltage differencing current conveyor (VDCC) were used in [23] to emulate a memristor at 8 MHz operating frequency. A tantalum-oxide-based memristor model with improved tuning capability was studied for neural network application in [24]. Several MOSFET-only designs were adopted to implement a memristor emulator model as in [25], [26], [27], [28], [29], and [30]. Some memristor applications such as the hybrid memory scheme were proposed by Mladenov in [31]. Another application perspective of memristor emulators is extensively dealt with in [32] and [33].

We highlight our novel contribution in the following:

- 1) This article is the first to introduce a memristor emulator design that is built with an OTA and a CMOS inverter compared to other OTA-based memristor emulators shown in Table III. Our proposed memristor emulator, when compared to other OTA-based emulators has the least number of transistor counts of 13, and the highest operating frequency of 50 MHz.
- 2) This work presents an entirely different circuit architecture. The proposed emulator is balanced between the number of transistor counts and the operating frequency range.
- 3) Using the proposed emulator, we have designed a novel neuron circuit called the MIF neuron that is capable of generating spikes similar to a biological neuron. Moreover, the MIF neuron design possesses adaptive firing frequency characteristics, i.e., it can alter its spiking frequency based on the input voltage level and the duration of the pulse width. It could be made to operate in the range of microseconds as well as milliseconds and thus can be applied to various neural applications. The output spike pattern of the MIF neuron suited for different voltage levels and duty cycles is presented in Fig. 13(d). Such a spiking neuronal signal generation using a CMOS memristor emulator has not yet been

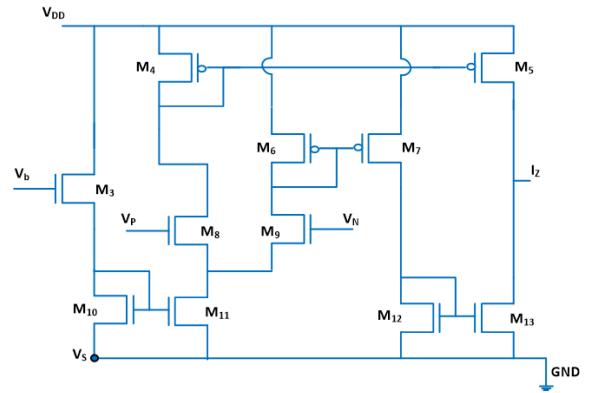


Fig. 1. MOS implementation of OTA block in Fig. 3.

reported. Further, to show the practical significance, we also present a pattern detection application using the proposed MIF neuron circuit.

- 4) We also include the simulation results of our proposed memristor emulator and compared them with the experimental test results of our fabricated memristor emulator chip. The comparison is included in Fig. 19(a)-(c) for different frequencies such as 5 MHz, 10 MHz, and 50 MHz. Thus, a more detailed comparison of the test results can be made with the literature/simulated results.
- 5) We also present an autonomous chaos implementation of Chua's circuit with our fabricated memristor emulator chip. The implementation with fabricated chip was verified by test results for single and double scroll attractors for varying ranges of potentiometer resistance 'R'.

II. OTA BLOCK AND ITS CHARACTERISTICS

The memristive behavior in the proposed article is emulated using an OTA as the CM building block. The internal structure of an OTA using 11 MOS transistors is depicted in Fig. 1. OTA is essentially a voltage-controlled current source. The transconductance (g_m) primarily transforms the difference between the input voltages (V_P and V_N) into current (I_Z) at the output side. Also, there is a provision to tune the g_m value using the bias voltage V_b . The voltage-current relationship of the OTA and the value of g_m is given by

$$I_Z = g_m (V_P - V_N), \quad g_m = \frac{k}{\sqrt{2}} (V_b - V_S - 2V_{th}) \quad (1)$$

In (1), V_S is the source voltage of transistor M_{10} , V_{th} is the threshold voltage of the MOSFETs M_3 and M_{10} , and k is the parameter described as

$$k = \mu_n C_{ox} \left(\frac{W}{L} \right) \quad (2)$$

The term μ_n is the carrier mobility of NMOS device, $\frac{W}{L}$ is the aspect ratio of M_{10} transistor, and C_{ox} denotes the gate oxide capacitance.

The frequency response of the OTA has been shown in Fig. 2(a). The setting for the input voltages was 900 mV

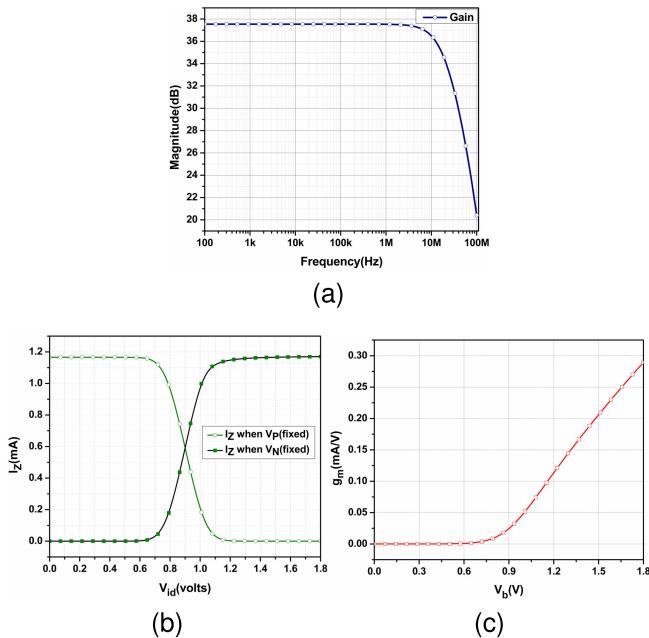


Fig. 2. (a) Frequency response of OTA (b) Simulation results for I_Z vs V_{id}
 (c) Simulation results for g_m vs V_b .

as the common mode input. The curve in Fig 2(b) shows the output current vs V_{id} (input differential voltage) where “ $V_{id} = V_P - V_N$ ”. The black line represents the output current keeping V_N fixed at 0.9 V and sweeping V_P from 0 to 1.8 V. Similarly, the green line shows the plot for output current keeping V_P fixed at 0.9 V and sweeping V_N from 0 to 1.8 V. A plot is also obtained for g_m vs the bias voltage V_b as shown in Fig. 2(c) which indicates that the g_m is directly proportional to V_b and is thus in accordance with (1).

III. DESIGN FRAMEWORK OF GROUNDED MEMRISTOR EMULATOR

The ideal memristor can be either charge-controlled or flux-controlled as described by Adhikari et al. in [34]. The memristor is charge-controlled when the memristor voltage (v) and memristor current (i) is related by

$$v = M(q)i \quad (3)$$

It is flux-controlled if the relation is given by

$$i = W(\phi) v \quad (4)$$

$M(q)$ and $W(\phi)$ are the memristance and memductance respectively, in which ' q ' denotes the charge and is defined as the time integral of current, whereas ' ϕ ' is the flux defined as the time integral of voltage. $M(q)$ and $W(\phi)$ are in turn related as

$$M(q) = \frac{1}{W(\phi)} \quad (5)$$

The design of the proposed memristor emulator is achieved by cascading a CMOS inverter with OTA as shown in Fig. 3. Here, the gate currents of M_1 and M_2 are assumed to be zero, however for non-ideal circuit elements and high-frequency AC signals, the gate currents might not be zero. There can be

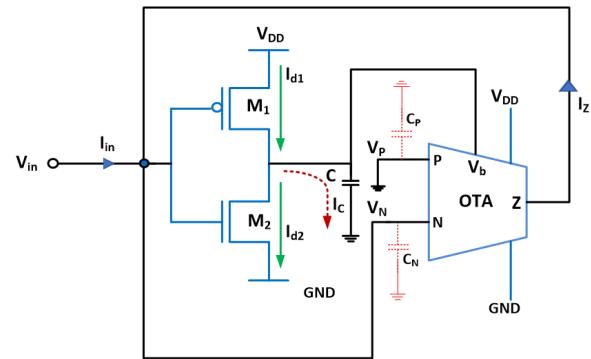


Fig. 3. Grounded memristor emulator topology.

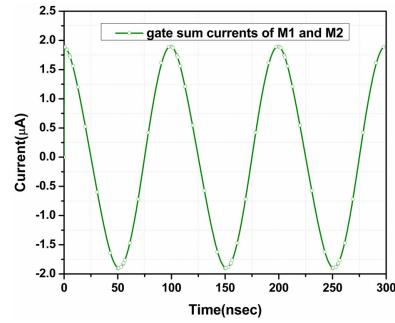


Fig. 4. Total gate currents at M_1 and M_2 .

leakage gate currents even in a steady state for large gate voltages. This has been confirmed by the sum of the gate currents of M_1 and M_2 plotted against time as shown in Fig. 4.

Input port P of the OTA is grounded while input port N, output port Z, and the input terminal of the CMOS inverter are connected together. In essence, such connection ensures the operation of the memristor emulator in grounded topology. Moreover, the proposed memristor model has been realized using a single power supply only. Another salient feature of this model in grounded configuration is that we can obtain both incremental and decremental memductance simply by interchanging the connections of the input terminals as demonstrated in the next section. These memductance states point to a continuum of several adjustable resistance states depending on the capacitor voltage. Also, by using this said topology we have further shown a MIF neuron that is able to generate spikes akin to those of biological neuronal spikes. Further, we realized the famous Chua's circuit for chaos behavior by means of this proposed grounded memristor model. In Fig. 3, the output current I_Z of the OTA is

$$I_Z = -I_{in} = g_m (0 - V_{in}) \quad (6)$$

No current flows into port N as the input impedance of port N is practically infinite.

Now, (6) can be rewritten as

$$\frac{I_{in}}{V_{in}} = g_m \quad (7)$$

From (1) and (7), we get

$$\frac{I_{in}}{V_{in}} = \frac{k}{\sqrt{2}} (V_b - V_S - 2V_{th}) \quad (8)$$

The drain current (I_D) through M_1 and M_2 develops a voltage V_C across the capacitor which is the same as bias voltage V_b . The current to V_b terminal is zero due to its high gate input impedance. The current through the capacitor I_C can be written in terms of the drain currents of M_1 and M_2 as

$$I_C = I_{d1} - I_{d2} \quad (9)$$

Now, considering the transistors M_1 and M_2 to be in saturation, and neglecting the higher-order terms, we get

$$\frac{dI_C}{dV_{in}} = k_n [(V_{tn}) - \alpha (V_{DD} + V_{tp})] = g_M \quad (10)$$

where α is the ratio of $\frac{k_p}{k_n}$. k_p and k_n are the process transconductance parameters of M_1 and M_2 respectively. When the input voltage swing moves out of the saturation region, the AC component of I_C can deviate from that of $g_M V_{in}$. However, such deviation can be made negligibly small by the proper choice of the magnitude of the voltage swing. The value of g_M obtained in (10) is a constant number as long as the voltage swing remains in the saturation region.

The potential across the capacitor is obtained as

$$V_C = V_b = \frac{1}{C} \int I_C dt = \frac{1}{C} \int g_M V_{in} dt \quad (11)$$

where g_M is the effective transconductance of the inverter stage comprising of M_1 and M_2 . Since the flux is regarded as the time integral of voltage, i.e., $\phi_{in} = \int V_{in} dt$, (11) can be rewritten as

$$V_C = V_b = \frac{1}{C} (g_M \phi_{in}) \quad (12)$$

Equation (12) shows the relation between the state variable (or flux) ϕ_{in} and V_C . Thus, it can be said that ϕ_{in} controls the capacitor voltage V_C . Analogously, it can be stated that the capacitance C is an essential parameter in determining the memory state of the memristor. We demonstrate how the capacitor C of the proposed memristor emulator could be used in the MIF neuron, which is demonstrated by computer simulation exhibiting different firing frequencies of the output spikes as shown in section VI. Substituting the value of V_b from (12) in the g_m value of (1) yields

$$g_m = \frac{k}{\sqrt{2}} \left(\frac{1}{C} (g_M \phi_{in}) - V_S - 2V_{th} \right) \quad (13)$$

Equating (7) and (13) gives

$$\frac{I_{in}}{V_{in}} = \frac{k}{\sqrt{2}} \left(\frac{1}{C} (g_M \phi_{in}) - V_S - 2V_{th} \right) \quad (14)$$

$$\Rightarrow W(\phi_{in}) = \frac{k}{\sqrt{2}} \left(\frac{1}{C} (g_M \phi_{in}) - V_S - 2V_{th} \right) \quad (15)$$

Since V_S here is grounded, on rearranging (15), the memconductance in its final form becomes

$$W(\phi_{in}) = -\frac{k}{\sqrt{2}} [2V_{th}] + \frac{k}{\sqrt{2}} \left[\frac{1}{C} (g_M \phi_{in}) \right] \quad (16)$$

where the first term on the right-hand side (RHS) of (16) is the linear time-invariant part determining the initial state of the memristor whereas the second term on the RHS signifies the linear time-variant quantity responsible for creating the

hysteresis loop and hence the memory effect. It is worth noting that the memristor defined by (16) depends on the flux ϕ_{in} and hence the proposed memristor configuration is essentially a flux-controlled memristor emulator.

Next, the frequency behavior of the memristor is analyzed wherein it is subject to a sinusoidal input $V_{in} = V_m \sin(\omega t)$. Here, V_m represents the amplitude of the input sinusoid and ω indicates the angular frequency of the sinusoidal waveform. As a consequence, (16) can be expressed as

$$W(\phi_{in}) = -\frac{k}{\sqrt{2}} [2V_{th}] + \frac{k}{\sqrt{2}} \left[\frac{V_m g_M \cos(\omega t - \pi)}{\omega C} \right] \quad (17)$$

Using $\omega = 2\pi f$ in (17) and further simplification gives

$$W(\phi_{in}) = -\frac{k}{\sqrt{2}} [2V_{th}] + \frac{k}{2\sqrt{2}} \left[\frac{V_m g_M \cos(2\pi f t - \pi)}{\pi f C} \right] \quad (18)$$

Equation (18) clearly demonstrates the frequency response of the memristor circuit where the memconductance holds an inverse relation with the frequency of the applied input. Hence, the following conclusions can be readily drawn:

- 1) With the increasing value of frequency, a shrink in the memristor-pinched hysteresis loop area is observed as the second term that is responsible for the loop decreases in value.
- 2) With frequency tending to infinity, the memory nature is completely lost, and the memristor typically transforms into a simple resistor as stated in [2].

IV. SIMULATION RESULTS

The simulation setup for the proposed work comprises Cadence Virtuoso software on the UMC 180-nm technology node. All the simulations were carried out in Analog Design Environment (ADE) window having 27°C as the nominal temperature setting. Also, the proposed work employs only a positive power supply i.e., V_{DD} which is taken to be 1.8 V. The input to the grounded memristor emulator in the simulation is a 300 mV sinusoid with a 900 mV offset. Such a value of the offset ensures that all the MOSFETs are in saturation. The aspect ratios of all the MOSFETs are presented in Table I. The value of the capacitor used in the design in order to implement the memristive behavior is 3 pF. Fig. 5(a) shows the transient behavior of the memristor emulator circuit for multiple cycles at 10 MHz, whereas Fig. 5(b) represents the pinched hysteresis loop (PHL) at 10 MHz in the voltage-current plane corresponding to Fig. 5(a). Table II contains the simulation result values. Also, observe that the PHL is actually the lissagious figure in the voltage-current plane. This pinched hysteresis can be explained by observing the peak values of applied input voltage and corresponding memristor current in Fig. 5(a). It is notable that the peaks occur at different values in time and hence give rise to such a hysteresis as seen in Fig. 5(b). The pinching of the loop occurs at (0,0.9) rather than the usual pinching at (0,0), i.e., at the origin because we have eliminated the use of a negative power supply considering the limitations of the foundry. A deviation of the PHL from the origin is observed and the causes of this deviation are

TABLE I
ASPECT RATIOS OF THE MOSFETS USED IN THE DESIGN

MOSFET	Aspect ratio (W/L) where W and L are in μm
M1	12/1
M2	1/1
M3	16.6/1
M4	20/1
M5,M7	76/1
M6	20/1
M8,M9	90/1
M10,M11	28/1
M12,M13	96/1

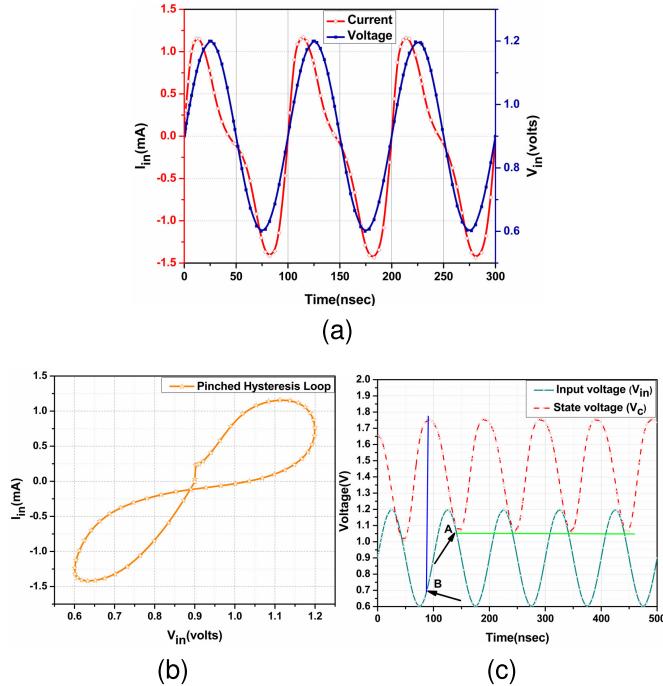


Fig. 5. (a) Transient curve (b) V-I plot (c) State evolution curve. $V_C \propto \phi_{in}(t)$ (red curve.), $\phi_{in}(t) = \int V_{in} dt$.

attributed to the parasitic effects of the DC component [6] included as an offset along with the applied input sinusoid to the memristor emulator. Since our design uses a single power supply unlike that of the usually existing emulator models that use a dual power supply, a DC offset of 900 mV was provided to obtain the required PHL and hence this shift of the DC operating point accounts for the deviation. Further, the state evolution ϕ_{in} for the V-I curve of Fig. 5(b) is plotted in Fig. 5(c). Point ‘A’ in the graph (Fig. 5(c)) is marked using an arrow, suggesting that at this point the memristor switches its state gradually from HRS to LRS. Thus, point ‘A’ represents the set state with a voltage nearly equal to 1.05 V (marked using a horizontal green line). Similarly at point ‘B’, the memristor gradually resets its state back to LRS with the reset voltage equal to 0.7 V (marked using a vertical blue line). In addition, the PHL at different frequencies presented in Fig. 6(a). and Fig. 6(b). are in accordance with the inverse relation of the loop area with increasing frequency. The two resistance states i.e LRS and HRS are clearly distinguishable up to 50 MHz. Beyond 50 MHz, the loop area shrinks considerably.

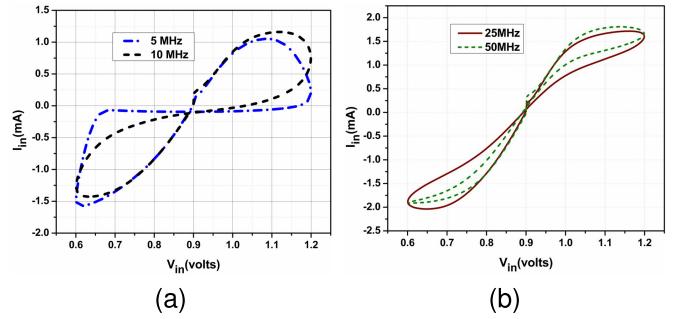


Fig. 6. (a) Nature of PHL (5 and 10) MHz (b) Nature of PHL (25 and 50) MHz.

Generally, the dimensions of the MOSFETs or any other components used in circuit simulation may differ from the actual ones due to many process steps involved in the fabrication. So, to ensure the robustness of the MOSFETs in the design to process variation and thereby ascertaining that the performance remains within the slow and fast corners, the study of process corner analysis becomes useful. Fig. 7(a) shows the different corner results such as Slow NMOS and Slow PMOS (SS), Fast PMOS and Fast NMOS (FF), and nominal cases of PMOS and NMOS. It turns out that the value of the current is maximum in the FF case and lowest in the SS case, thereby also pointing towards the fact that the deviation observed from the nominal case is marginal.

Furthermore, the power plot was calculated using the input settings as 900 mV DC offset with 300 mV amplitude of the 10 MHz sine wave. The power supply taken into consideration was 1.8 V. The power budget plot shown in Fig. 7(b) is indicative of the fact that the circuit operates with a total power consumption of approximately 2.25 mW. Such a constrained power budget could be useful in various neuromorphic applications of the presented emulator circuit.

In order to get an intuition of the major mechanisms of noise in the CMOS-based memristor emulator design which are primarily due to channel thermal and flicker noises, the total output noise simulation is included in this section. The range of noise (maximum average noise power) as plotted in Fig. 7(c) shows that the plausible value lies between 12 pV²/Hz to 1 pV²/Hz for the frequency range between 10-100 Hz. However, for the frequency range between 1 kHz up to higher MHz, the noise is negligible. Fig. 7(c) clearly depicts that within the working range of the memristor, i.e., centered at 5 MHz-50 MHz per unit of bandwidth, the effect of noise is minimal. This is a clear advantage of the design suggesting that the device presents a good signal-to-noise ratio (SNR).

Another well-established fingerprint of the memristor emulator is its non-volatile behavior. In other words, the previous resistance state should remain preserved even in the absence of stimuli. Once the input signal arrives, the previous state moves to the new value of the resistance state. An input pulse of 150 mV amplitude, pulse width of 15 ns and period of 50 ns is applied to the proposed memristor. The stair-like waveform depicted in Fig. 8 shows the memductance value at different time instants. It is noticeable that in the absence of the input

TABLE II

SIMULATION VALUES FOR ALL THE TRANSISTORS AT INPUT SETTINGS $V_{in} = 0.3$ V AT 10 MHz FREQUENCY AND DC OFFSET = 0.9 V

Parameter	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}	M_{13}
I_D	-32.37	32.37	414.2	-196.6	-750.9	196.6	-742.1	196.7	196.7	414.2	393.3	750.9	771.7
V_{GS}	-900m	900m	936.1m	-1.118	-1.118	-1.118	-1.118	557.9m	557.9m	720m	720m	616.8m	616.8m
V_{DS}	-405m	1.395	1.08	-1.118	-1.183	-1.118	-1.118	339.4m	339.4m	720m	342.1m	616.8m	900m
V_{th}	-492.9m	390.5m	504m	-492.8m	-492.8m	-492.8m	-492.8m	451.1m	451.1m	384.4m	387.3m	382.1m	380m
k	721.7 μ	293 μ	4.912m	1.145m	4.383m	1.145m	4.383m	27.02m	27.02m	8.353m	8.353m	28.72m	28.72m
g_m	134.6 μ	116.4 μ	1.72m	550.9 μ	2.105m	550.9 μ	2.072m	2.647m	2.647m	2.249m	2.089m	5.687m	5.794m

Note: I_D - drain current, V_{GS} - gate to source voltage, V_{DS} - drain to source voltage, V_{th} - threshold voltage, k - transconductance parameter, g_m - transconductance (units of V_{GS} , V_{DS} , V_{th} are in volts(V), I_D is in μ A, ' k ' is in A/V^2 and g_m is in Siemens)

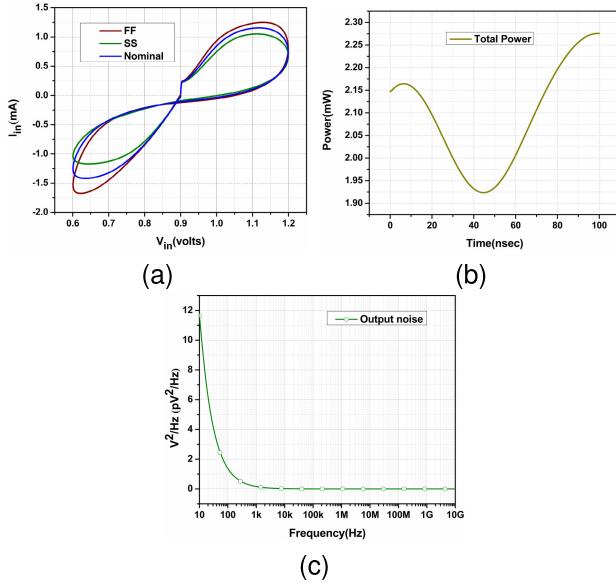


Fig. 7. (a) PHL at various process corner (b) Power budget plot (c) Total output noise.

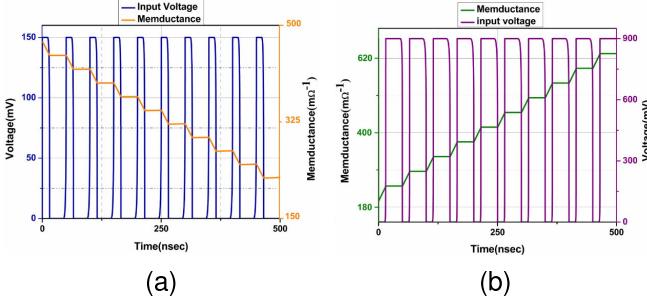


Fig. 8. (a) Non volatility (decremental) (b) Non volatility (incremental).

pulse, the waveform stays at its previous value and begins to change once the next pulse arrives. Fig. 8(a) and Fig. 8(b) confirm that the emulator designed possesses such a non-volatility and presents both decremental and incremental memductance state respectively as time advances. Analogously, it could be stated that the memristor emulator herein has a continuum of resistance states which could be well exploited in applications where the synaptic weight storage (memductance value when memristors are used as a synapse) is of primary importance such as in neural network implementation or various other learning applications.

To further validate the design precisely, the layout of the emulator is implemented as seen in Fig. 9 and the post-layout simulation has been included graphically in Fig. 10(a).

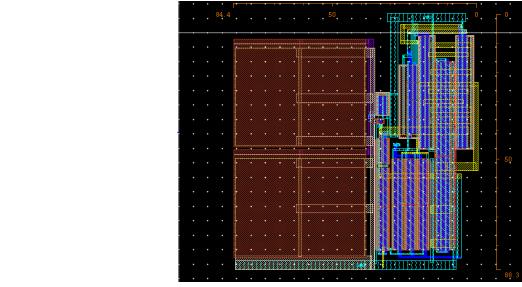


Fig. 9. Layout of the proposed model.

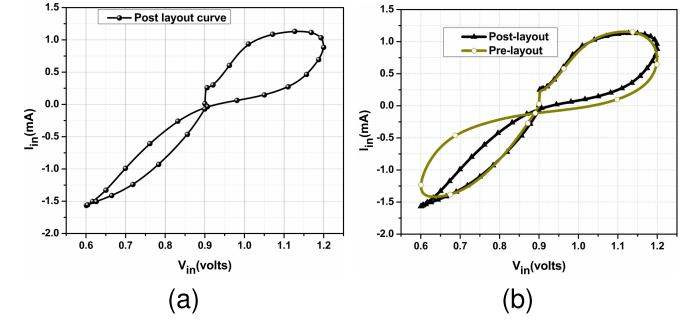


Fig. 10. Layout results (a) Post layout simulation result at 10 MHz frequency (b) Simulation results (overlapped) obtained for Post layout vs Pre layout at 10 MHz frequency.

On the other hand, Fig. 10(b) provides a pre-layout versus post-layout simulation comparison. The layout has an area of $7452.52 \mu\text{m}^2$. Even though Fig. 10(b) shows a considerable change in the post-layout loop area in the third quadrant when compared with the pre-layout result, the two memductance states are well distinguishable which indicates that the design is practically feasible. The deviation in the values of the current in the post layout from the pre-layout can be attributed to the RC parasitics [35] in the physical layout. Also, an additional grounded capacitor (shown as C_P and C_N in Fig. 3) was connected at the inputs of the memristor taking into account the parasitic capacitance that would be offered by the probes connected during testing. This further leads to the deviation in the currents. However, the parasitics do not affect the memory nature of the loop.

V. COMPARISON AND DISCUSSION

A. Memristor Emulator

A brief discussion regarding the state of the art emulators reported in various literature was presented in the

TABLE III

COMPARISON OF THE PROPOSED MEMRISTOR EMULATOR CIRCUIT WITH THE EXISTING ANALOG CM BLOCK-BASED DESIGNS

Ref. No./Year	No. of active components	No. of passive components	Power supply	Power Consumption	No. of MOS	Operating frequency	Fab. Result
[5],2019	1 - VDTA	C-1	± 0.9 V	8 μ W	16	50 MHz	×
[6],2020	1 - VDTA	R-1, C-1	± 0.9 V	NA	16	50 MHz	×
[7],2021	1 - CFTA	C-1	± 1.2 V	NA	28	9 MHz	×
[8],2017	1 - CCII, 1- Multiplier	R-1, C-1	± 10 V	NA	NA	860 kHz	×
[9],2014	4 - CCII, 1-Multiplier	R-5, C-1	± 10 V	NA	NA	20.2 kHz	×
[10],2014	4 - CCII, 1 - OPAMP, 1-Multiplier	R-10, C-1	± 15 V	NA	NA	120 Hz	×
[11],2017	4 - CCII, 1-Multiplier	R-3, C-1	± 10 V	NA	>80	40 kHz	×
[12],2020	2 - CCII, 1 - multiplier, 2-PMOS	R-2, C-1	± 10 V	NA	NA	1 kHz	×
[13],2017	1 - CCTA	R-3, C-1	± 1.5 V	NA	30	100 kHz	×
[14],2017	1 - DVCTTA	R-3, C-1	± 1.5 V	NA	29	1 MHz	×
[15],2022	1 - DVCTTA	R-1, C-2	± 1 V	8.74 mW	27	12.8 MHz	×
[16],2022	2 - VDIBA	C-1	± 1 V	1.34 mW	18	12.7 MHz	×
[17],2018	1- OTA, 3- Transistor	C-2	± 1.25 V	NA	NA	24 Hz	×
[18],2017	1- OTA, 2- PMOS	C-1	± 1 V	NA	14	30 Hz	×
[19],2018	2 - OTA	C-1	± 1.2 V	NA	34	8 MHz	×
[20],2020	1 - CCII, 1 - OTA	R-1, C-1	± 1.2 V	9.567 mW	24	26.3 MHz	×
[21],2020	1 - CDTA, 1 - OTA	C-1	± 0.9 V	NA	36	2 MHz	×
[22],2022	1 - VDBA, 1 - OTA	NIL	± 0.9 V	NA	25	5 MHz	×
[23],2023	1 - VDCC, 1 - OTA	C-1	± 0.9 V	NA	29	8 MHz	×
This work	1- OTA, 1- NMOS, 1- PMOS	C-1	1.8 V	2.25 mW	13	50 MHz	✓

introduction section. However, in the following subsection, a performance comparison of the proposed emulator with the existing emulators in terms of power consumption, transistor counts, active/passive components used in the design, power supply, and operating frequency is summarized as presented in Table III. None of the other works on the memristor emulator contain the fabrication results. This section focuses on comparing existing CM block-based emulators with the proposed one. Following are some of the inherent features of this new memristor emulator design.

- 1) This work presents a simple OTA-CMOS inverter-based memristor design with a low power budget of approx 2.25 mW only.
- 2) This grounded emulator design also eliminates the use of a dual power supply and uses a single power supply of 1.8 V instead.
- 3) The number of transistors is lowest when compared to any block-based memristor designs especially when OTA-based designs are considered.
- 4) It is also worth noting that the frequency of operation achieved with the OTA used herein is 50 MHz which is the maximum when compared with any other OTA-based emulators. This makes our design suitable for high-frequency applications.
- 5) The memristor model herein is robust to the different noises generally prevailing in the CMOS circuits.
- 6) The simulation result of this new power-efficient memristor emulator is corroborated by its fabrication result. These features could well promote its use in applications such as neuromorphic computing, signal processing, and other areas where power budget is a main concern.

B. Commercially Available Knowm Memristor

Table IV gives a brief comparison of our memristor emulator design with the commercially available Knowm memristor. The comparison is based on the parameters such as maximum

TABLE IV
COMPARISON OF THE PROPOSED MEMRISTOR EMULATOR WITH KNOWN MEMRISTOR

Memristor	Max. current	Set/reset voltage (AC)	Type	Max. Oper. Freq.
Knowm [36]	1 mA	+0.35 V/-0.5 V	Electro-forming	1 kHz
This work	>1.5 mA	+0.2 V/-0.2 V	Forming-free	50 MHz

current, operating frequency, type, and set/reset voltage. The major advantage that a CMOS-based memristor circuit offers is that it is an electro-forming free device. On the contrary, the Knowm memristor device requires initial high electro-forming voltages to form a conduction filament before being operated as a stable resistive switching device unlike that of our memristor emulator counterpart. The high operating frequency is another favorable feature of our design. The proposed memristor emulator has a maximum operating frequency of 50 MHz, whereas the Knowm memristor [36] can be operated up to a maximum frequency of only 1 kHz. Thus, the operating frequency is another aspect wherein our proposed CMOS memristor emulator outperforms the Knowm memristor.

VI. MEMRISTIVE INTEGRATE-AND-FIRE (MIF) NEURON CIRCUIT

The architecture of the proposed MIF neuron is inspired by the Leaky Integrate-and-Fire (LIF) neuron circuit as presented by Shamsi et al. in [37]. The LIF neuron circuit primarily models the spike generation mechanism or popularly known as an action potential in the biological neuron. The LIF circuit is basically divided into four segments namely the current mirror, integrator, Schmitt trigger, and reset and spike control unit. In our work, the reset section of the LIF neuron is replaced by the proposed memristor emulator (MRE) and hence called

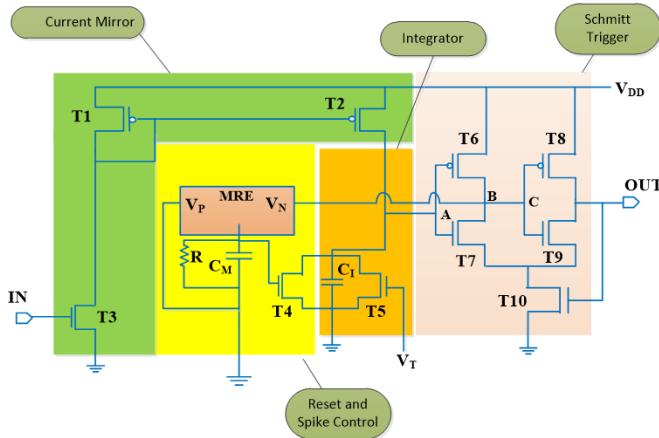


Fig. 11. The MIF neuron circuit.

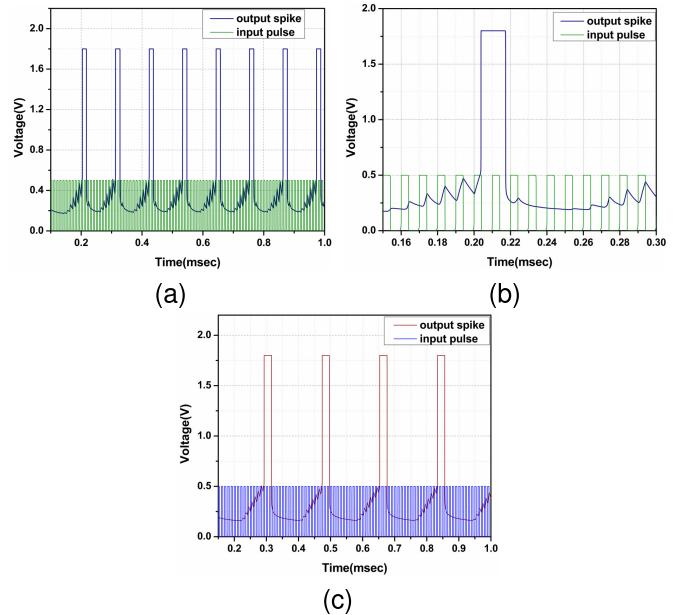
MIF neuron. By making such alterations, the MIF neuron can be used to generate a spike analogous to the biological neuronal signal and also leads to formation of the continuum of resistance states. Fig. 11 shows the design framework of the proposed MIF circuit. When an input pulse is applied at the gate of T3, the current mirror section generates and injects the current into the integration unit. The capacitor C_I then integrates this current and generates a voltage. Once this voltage (potential developed at the capacitor or analogously stated as membrane potential of the biological neuron) reaches the switching threshold of the Schmitt trigger set by V_T at transistor T5, the node A voltage is high thereby causing the Schmitt trigger section to fire. This firing generates a spike at the OUT terminal of the MIF circuit. Once the spike has been generated, at the same instant nodes B and C go low. This indeed presents a low voltage level at the input V_N of MRE in the reset section. As a result, the capacitor C_M is immediately charged to V_{DD} which turns on transistor T4, and thus the membrane potential resets to zero voltage level which eventually resets the spike. In this way, one complete formation of a spike occurs.

In another scenario, the capacitor must discharge through resistor R to allow the next spike to occur. The time taken by the capacitor C_M to discharge is determined by the time constant RC_M . The duration between two successive occurrences of the spike is termed the refractory period and it is this time constant that controls the discharging rate and hence the duration of the refractory period. It is worth noting that during the refractory period, the input pulse is incapable of generating another spike similar to the case with the biological neuron. Thus the MIF neuron circuit presented is capable of mimicking the traits of biological neuronal signals. Also, the capacitance C_M and C_I can be tuned to control the frequency of the spikes. Besides, the proposed MIF neuron circuit does not require any external logic to reset the membrane potential. The design parameters adopted to implement the MIF neuron circuit are shown in Table V.

In order to show the leaky integrate and fire and the refractory mechanism of the MIF neuron circuit, the simulations were performed for the applied input pulse of 500 mV

TABLE V
MIF NEURON CIRCUIT DESIGN PARAMETERS

Parameter	Value (W/L) where W and L are in μm
T1,T2	0.5/0.4
T3,T7	0.24/0.18
T4-T6, T8-T9	0.4/0.4
T10	0.3/0.3
R	10 k Ω

Fig. 12. Spiking MIF neuron response (a) output spike for $C_M = 40 \text{ nF}$ and $C_I = 25 \text{ pF}$ (b) magnified image showing the leaky, integrate, fire and refractory mechanism (c) output spike for $C_M = 40 \text{ nF}$ and $C_I = 50 \text{ pF}$.

amplitude. The switching threshold was set at $V_T = 0.5 \text{ V}$ and subsequent spikes were observed. Fig. 12(a) shows the spiking signal for an input pulse having 10 μs period and 40% duty cycle with C_M and C_I as 40 nF and 25 pF, respectively. The waveform in Fig. 12(b) shows a magnified version of Fig. 12(a) in order to capture the local details such as leaky phenomena, integrating action, firing, and refractory mechanism of the MIF neuron circuit. It is evident that in the absence of an input pulse, the output node leaks, and whenever an input pulse arrives, the signal keeps on integrating until it eventually fires when the switching threshold of 0.5 V is crossed. Similarly, the output spikes for $C_M = 40 \text{ nF}$ and $C_I = 50 \text{ pF}$ are shown in Fig. 12(c). It can be observed that there is a decrease in the frequency of spiking with an increasing value of C_I . Also, in the applied simulation of Fig. 13, we have kept C_I fixed at 500 pF and input pulse is applied for a time period of 10 ms with 40% duty cycle. Different spiking rates are observed for $C_M = 40 \text{ nF}$, $C_M = 30 \text{ nF}$ and $C_M = 100 \text{ nF}$ as depicted in Fig. 13(a), 13(b) and 13(c), respectively. The firing rate of the MIF neuron output response is maximum for $C_M = 30 \text{ nF}$ and lowest for $C_M = 100 \text{ nF}$. This is because the time constant RC_M is maximum for $C_M = 100 \text{ nF}$, resulting in a larger refractory period and hence the tendency for the neuron to fire in a given time instant decreases. Similarly with $C_M = 30 \text{ nF}$, the value of RC_M is minimum and hence the refractory

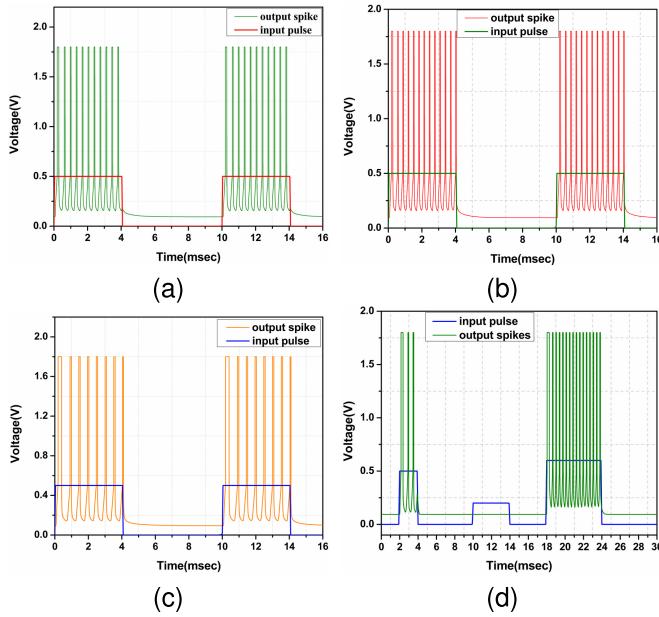


Fig. 13. Spiking MIF neuron response (a) output spike for $C_M = 40$ nF and $C_I = 500$ pF (b) output spike for $C_M = 30$ nF and $C_I = 500$ pF (c) output spike for $C_M = 100$ nF and $C_I = 500$ pF (d) output spike at different duty cycle and amplitude for $C_M = 100$ nF and $C_I = 500$ pF.

period is minimum, resulting in an increased firing rate of a neuron. Furthermore, it should be noted that multiple spikes are generated during the ON period of the applied input pulse when the time period is set in the milliseconds range. Next, in Fig. 13(d), we show the adaptive firing frequency nature of the MIF neuron that depends on the voltage level and the pulse width. In the plot of Fig. 13(d), the duty cycle immediately after the zero input (in the duration 0 to 2 milliseconds) is 25% (in the duration 2-10 milliseconds) with 500 mV amplitude, afterward from 10-14 milliseconds the amplitude is set to a value that is below the threshold, i.e., < 500 mV and the last input pulse is a square wave of 50% duty cycle, i.e., from 18-30 milliseconds. Such a graph with varying duty cycles as well as the amplitude corresponds towards a more practical scenario where the typical spikes are asynchronous in nature. Finally, it can be noted that with the simple adjustment of C_M and C_I , the spike rate can be controlled as explained earlier.

A. MIF Neuron vs LIF Neuron: Pursuit to in-Memory Computation

In our design of MIF neuron, the charging and discharging of C_M causes the spike to autonomously reset and leads to the onset of the refractory period. Moreover, any change in the voltage of C_M directly alters the memductance of the memristor. Thus, with every charging of C_M , there arises a new memductance state while every discharging of C_M ensures that the previous state is maintained. This phenomenon is depicted in Fig. 14. Both the processing of the data and its storage occur at the same place similar to what happens in the human brain. Thus, in evaluating the MIF neuron's capability over LIF neuron, the former can significantly benefit the future computing system by replacing the Von-Neumann model which is regarded as a bottleneck in terms of area and

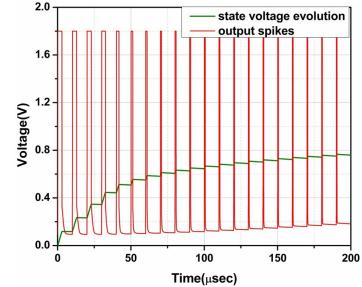


Fig. 14. MIF neuron spiking response (red) and corresponding state voltage (green) showing different state voltages for each output spikes.

power. In the LIF neuron model, the in-memory computation still remains elusive.

B. MIF Neuron vs LIF Neuron: Energy and Static Power Consumption Comparison

In this section, we evaluate the energy consumption of MIF neuron in generating a complete single spike. In order to compare energy and power figures with that of the existing state-of-the-art spiking neuron models, we simulate the MIF neuron circuit for $C_M = 1$ nF and $C_I = 100$ fF. A 500 mV input pulse was applied for a duration of 1 ms having a period of 10 μs with 40% duty cycle. The energy consumption per spike was calculated according to the formula

$$E_{\text{spike}} = \frac{\int_{t_0}^{t_1} V_{DD} \cdot i(t) dt}{N} \quad (19)$$

where N represents the total number of spikes between t_0 to t_1 , $i(t)$ denotes the current from the power supply. For the period from $t_0 = 0$ to $t_1 = 1$ ms and by inspection, a total of 100 spikes were generated as seen in Fig. 15(a). The value of the numerator part of (20) is calculated from the supply current ($i(t)$) plotted in Fig. 15(b). This yields the energy per spike as

$$E_{\text{spike}} = \frac{19.57}{100} nJ \approx 196 \text{ pJ/spike} \quad (20)$$

The value of E_{spike} obtained is reasonably close to that of the LIF neuron model in [37] although the transistor count of the core circuit has been doubled. Both MIF neurons and LIF neurons use CMOS technology. But the LIF neuron counterpart requires significant additional circuit overheads such as lateral inhibitory terminals for reset, a threshold detection module, and external logic for switching such as the Schmitt trigger. Although an energy consumption per spike that is around 7.3 pJ, the LIF neuron model does not include any information on the energy consumed by external circuits for threshold detection and switching control circuitry. In contrast, our MIF model has approximately 196 pJ/spike as the E_{spike} , while requiring only a Schmitt trigger as the external circuit for logic switching. The E_{spike} of the Schmitt trigger is approximately 0.77 pJ. Even though, the E_{spike} for the LIF neuron model is reported to be only 7.3 pJ without considering peripheral circuits, it is to be kept in mind that the MIF serves dual purposes, i.e., processing as well as storage at the same location within the constrained energy

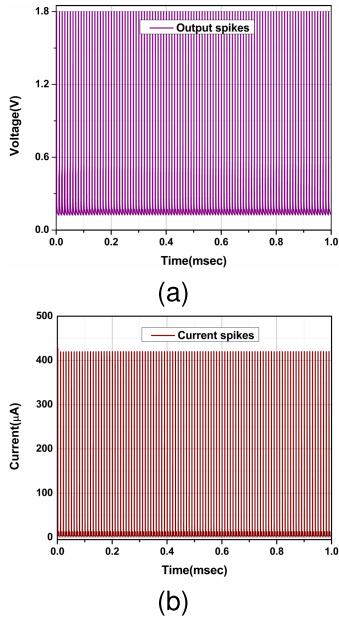


Fig. 15. (a) Spiking voltage output vs time (b) Supply current spikes vs time.

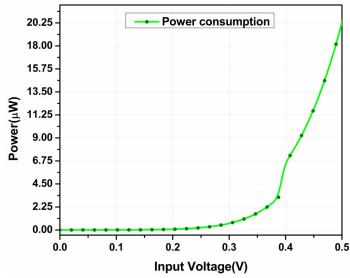


Fig. 16. Power consumption of the MIF neuron circuit vs the input voltage.

budget of only 196 pJ/spike. Additionally, for the CMOS LIF neuron architecture to suit the neuromorphic computing needs, external storage units are needed which would eventually shoot up their energy requirements, and this seems to be a major pitfall.

Similarly, in order to determine the total power consumption of the proposed MIF neuron architecture, we run the simulation for 1 ms and consider the case where C_M and C_I are taken as 1 nF and 100 fF respectively. The applied input voltage is varied from 0 to 500 mV. From Fig. 15(b), the average supply current is found to be $10.87 \mu\text{A}$. Thus, the dynamic power consumption of the MIF neuron is $19.56 \mu\text{W}$ whereas the static power consumption is typically around 443 pW. In this regard, the total power consumption of the MIF neuron circuit with respect to time is approximately $19.6 \mu\text{W}$. Fig. 16 shows the simulated total power consumption vs. the applied input voltage from 0 to 500 mV and shows a total power consumption of $20.25 \mu\text{W}$ while the average is around $3.31 \mu\text{W}$.

C. MIF Neuron vs LIF Neuron: Circuit Overhead

A vital downside that the LIF circuit carries is the use of additional circuitry in its voltage level monitoring such as a lateral inhibitory terminal (T_{INH}) for the reset action

TABLE VI
NEURON CIRCUIT COMPARISON

Ref.	No. of MOS	Energy	Static power	Refract. period	In-memory
Indiveri, et al.[39]	>22	900 pJ/spike	-	✓	✗
Albrecht, et al.[40]	16	0.4 pJ/spike	-	✗	✗
Wu, et al.[41]	>35	9.3 pJ/spike	-	✗	✗
Shamsi, et al.[37]	14	$\approx 7.3 \text{ pJ/spike}$	182 pW	✓	✗
This work	25	$\approx 196 \text{ pJ/spike}$	$\approx 443 \text{ pW}$	✓	✓

Note: LIF numbers do not include the overhead circuit numbers

and additional input supply from T_{EX} as in [37]. Our MIF neuron, on the other hand, is devoid of any adaptive mechanism external to the MIF neuron model which is a major advantage over the LIF neuron counterpart which in general requires sophisticated external overheads for its voltage level monitoring [38].

Table VI presents a comparison between some of the existing state of art LIF neuron circuits [39], [40], [41] and the proposed MIF neuron model. The basis of comparison is based on factors such as transistor count, energy consumption per spike, ability to show the refractory period phenomena, static power consumption, and capability to perform in-memory computation. While the design may appear counter-productive, the ability to perform in-memory computation through storage of adjustable memductance states is an inherent feature possessed by this MIF neuron circuit. Analogously, the design could be adopted in learning applications such as memristive synapse where the continuum of resistance states could be altered depending on the input spike pattern and stored in the form of adjustable synaptic weight accordingly.

VII. MEASUREMENT RESULTS

The memristor emulator fabrication was done on a UMC 180-nm technology node, the chip micrograph image of which has been shown in Fig. 17. The die size is approx $L=1499.96 \mu\text{m} \times W=1499.96 \mu\text{m}$. For characterization, transient analysis is carried out with 1.2 V peak-to-peak sinusoidal input at 10 MHz fed to the memristor emulator chip as shown in the Mixed Signal Oscilloscope (MSO) screen of Fig. 18(a). Additionally, the MSO's screen depicting the non-linear behavior of memristor PHL at 5 MHz, 10 MHz and 50 MHz has been captured as shown in Fig. 18(b), Fig. 18(c), and Fig. 18(d). The measured results correctly corroborate with the fingerprints of the memristor as a shrink in the loop area with increasing frequency is clearly evident from the plots. Furthermore, a comparison between the simulated and experimentally tested memristor emulator chip is included in Fig. 19(a), Fig. 19(b), and Fig. 19(c) so that the experimental results can be compared with the literature results with much clarity. As seen in Fig. 19, deviation in the loop area between the simulated and tested results exists along with

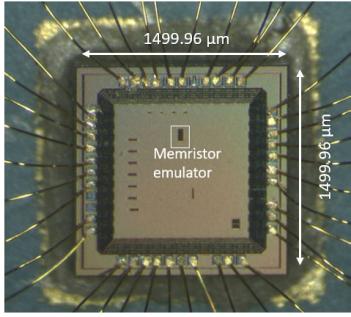


Fig. 17. Chip micrograph.

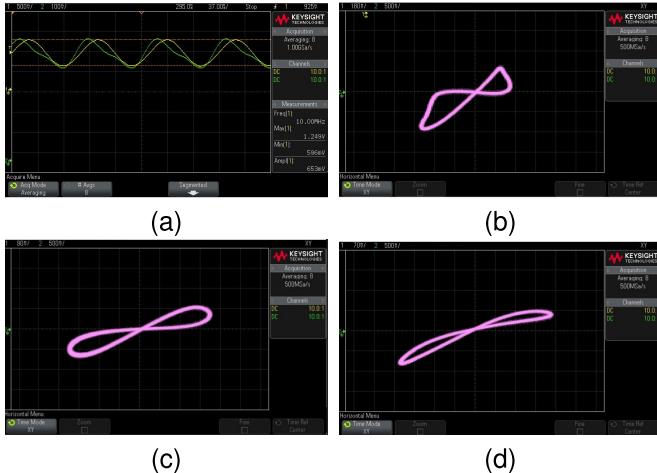


Fig. 18. Experimentally tested result of the fabricated chip (a) Transient curve of the test chip at 10 MHz (b) PHL of the test chip at 5 MHz (c) PHL of the test chip at 10 MHz (d) PHL of the test chip at 50 MHz.

a DC shift of the origin. Parasitics occurring as a result of large interconnections/wirings and parasitic capacitances offered by the probes during testing account for such deviations. However, the signal integrity is maintained as the LRS and HRS are still distinguishable and nearly the same for all the cases. Thus it can be inferred that the measurement result from the fabricated chip presents a faithful replication of the simulated waveform and hence confirms the operation of the proposed memristor design both theoretically and practically.

VIII. APPLICATION

A. MIF Neuron Circuit Featuring Pattern Detection

Fig. 14 illustrates that each spike occurring at different instants of time points towards different C_M voltage or state voltage. These different state voltages represent different memductance states. Thus, the MIF neuron circuit overall is capable of producing spiking output as well as showing various tunable memductance states. In the application of pattern detection, we aim to exploit various analog state voltages (analogously the memductance states) of the MIF neuron circuit. For this, we consider DC inputs to the MIF neuron circuit in the 12×1 MIF neuron array shown in Fig. 20(a) capable of generating a voltage across C_M above the threshold of the MIF neuron which is set as 500 mV. Such input voltages represent the black cell in the image of 4×3 pixels as shown in Fig. 20(b), whereas the voltage that fails to charge the C_M above the threshold is

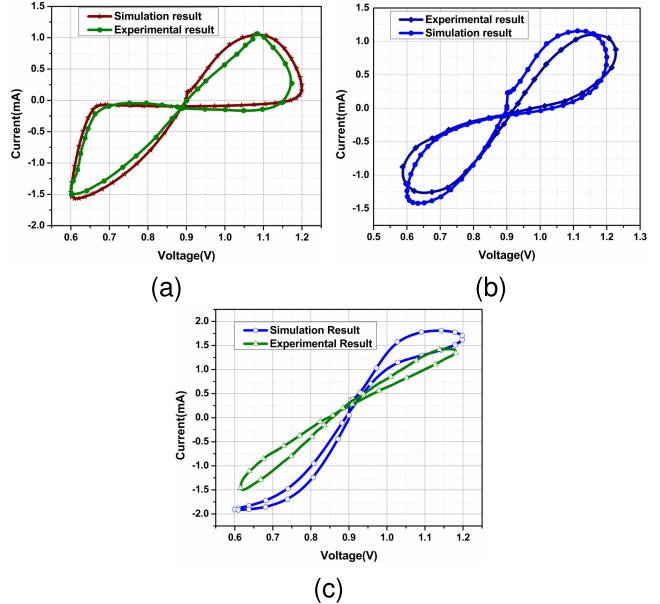
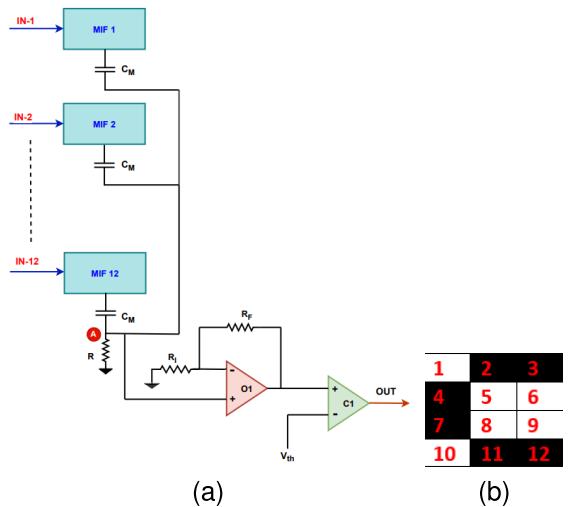


Fig. 19. Comparison between simulated and tested result (a) 5 MHz (b) 10 MHz (c) 50 MHz.

Fig. 20. Pattern detection scheme using the proposed MIF neuron (a) 12×1 MIF neuron array (b) Single pattern for detection using 4×3 pixels.

indicated by white cells in 4×3 pixels. Thus, each cell in 4×3 pixels represents an input voltage to the MIF neuron. Hence, an image of 4×3 pixels would require 12 MIF neurons. The circuit has been configured in the form of a 12×1 MIF neuron array in the proposed application. The currents through individual capacitors in turn generate a net current at node A as shown in Fig. 20(a). The corresponding voltage at node A is then analyzed to generate the final out for the pattern detection scheme.

In order to show the practical significance of the proposed MIF neuron, we investigate a pattern detection scheme using the proposed MIF neuron circuit. For this, we consider a 4×3 pixel image representing the letter 'C' as shown in Fig. 20(b). The black pixels signify a high input (voltage above 500 mV) whereas the white pixels correspond to a low input (voltage below 500 mV). From Fig. 20(b) cell or pixel number

TABLE VII

COMPARISON OF THE PATTERN DETECTION USING 12×1 MIF NEURON AND 12×1 LIF NEURON FOR A SINGLE OUTPUT PATTERN OF 4×3 PIXELS

Circuit	Total no. of transistors	passive elements
LIF neuron [42]	336	48
Proposed MIF neuron	276	Nil

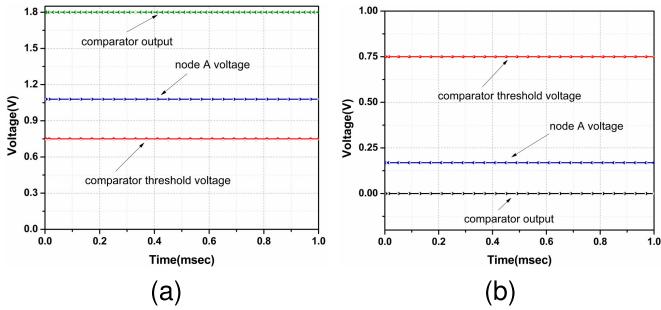


Fig. 21. Pattern detection results (a) Successful detection (b) Failed detection.

2,3,4,7,11 and 12 represents black pixels and thus input IN-2, IN-3, IN-4, IN-7, IN-11, and IN-12 in the 12×1 MIF neuron array is set to high input voltage, while the remaining inputs are subjected to low input voltages. The currents of the 12×1 MIF neuron array corresponding to the above pattern are then summed up at node A. The corresponding voltage at node A is then amplified using a non-inverting OP-AMP ‘O1’ and then compared with the threshold voltage (V_{th}) of the comparator. The value of (V_{th}) is chosen as 750 mV. If the input to the comparator ‘C1’ is above (V_{th}), a high logic (1.8 V) is generated else a low logic (0 V) is obtained. The high logic output signifies successful pattern detection as in Fig. 21(a), which is indicated by a green line whereas the low logic output suggests a failed pattern detection indicated by a black line in Fig. 21(b). It should be noted that if the black pixels are more than 6, still the pattern would be detected signifying the presence of a pattern in a pixel array, however the pattern would be different. In such a case, to differentiate between the patterns, more sophisticated pattern recognition would be required. In another scenario where the black pixels are less than 6, the output of ‘O1’ is not enough to cross the comparator threshold voltage and hence a low logic is generated at the OUT terminal of ‘C1’ indicating a failed pattern detection.

We have also explored a few advantages in terms of the transistor count and passive elements while comparing the pattern detection for a single pattern using the proposed MIF neuron and the LIF neuron counterpart. As seen in Table VII, to implement a pattern detection scheme comprising of 12×1 MIF neuron array, the MIF neuron requires only 276 (i.e., 23 transistors in each MIF \times 12 MIF neurons) with no passive elements whereas the single pattern detection using 12×1 LIF neuron array as in [42] would require 336 transistors (i.e., 14 transistors in each LIF \times 12 LIF neurons, 6 transistors \times 12 STDP synapse, 8 transistors in each delay block \times 12 delay blocks) in addition to 48 passive elements (i.e., 2 \times 12 resistors and 2 \times 12 capacitors in the STDP). Thus, the MIF neuron has a clear advantage in terms

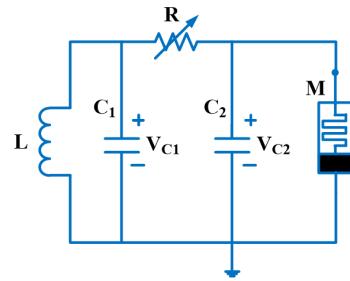


Fig. 22. The chaos circuit using proposed memristor emulator.

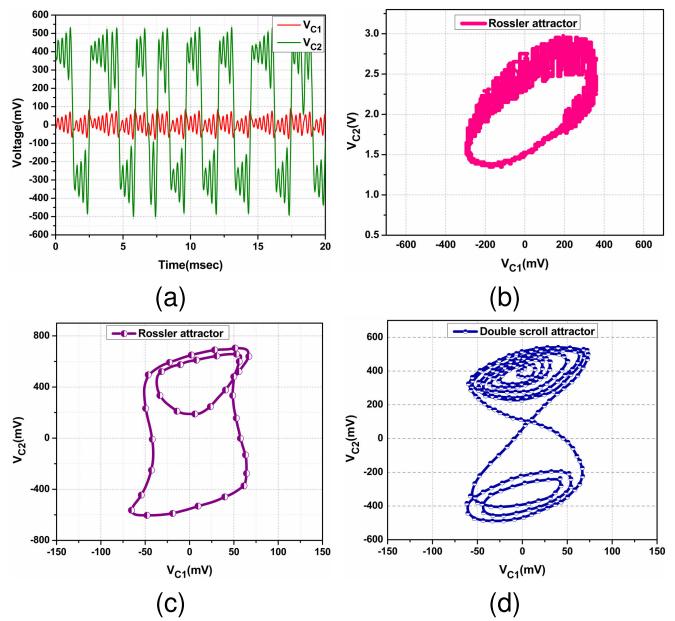


Fig. 23. Response of Chua's circuit based on fabricated memristor emulator (a) Transient response (b) Rossler attractor at $R=1.82$ k Ω (c) Rossler attractor at $R=1.77$ k Ω , (d) Double scroll attractor obtained for the chaotic implementation using the fabricated test chip at $R=1.45$ k Ω .

of transistor counts and passive elements over the LIF neuron counterpart for pattern detection in a 4×3 pixel image.

B. Chaos Implementation

Chaos nature can be generally seen in a third or higher order dynamic systems having one or more non-linearities [43]. Such chaos systems are oscillatory in nature and have many favorable features that are very useful. Aperiodicity is one of its traits. At first instance, these chaos behaviors may seem periodic and predictable, but after a while, they seemingly start getting random and unpredictable. Despite being a stable system, they show orbital trajectories that revolve inside a tight band around several attractors spiraling all over an unstable fixed point. If considered over a long duration of time these trajectories seem to occupy the band in a purely random manner [44].

Lately, chaos systems such as the design of several chaotic oscillators have drawn the attention of analog IC design engineers owing to its various possible applications in the area of secured communication networks, signal processing, cryptography, etc., [45] and [46].

Chua's circuit is said to exhibit numerous chaos, hyperchaos, bifurcations, and attractors suitable for different nonlinear dynamic systems. The classical Chua's circuits are commonly used for chaos generation [47]. Here we show a chaos behavior experimentally as an application of the proposed memristor emulator. We have replaced the Chua's diode with our fabricated memristor emulator denoted by "M" in the well-known Chua circuit as seen in Fig. 22. The value of the fixed capacitors C_1 and C_2 are 100 nF and 10 nF, respectively and the value of the inductor is 17.6 mH. The resistor (R) used in the circuit is a potentiometer. A series of bifurcations are observed by varying the potentiometer resistance value between 1 k Ω to 2 k Ω . To show the experimental output of the chaotic phenomena, we have considered the voltage V_{C1} vs V_{C2} trajectories. Fig. 23(a) shows the transient response of V_{C1} and V_{C2} with respect to time. It is observed that for $R = 1.82$ k Ω and 1.77 k Ω , Rossler-type attractors are generated in Fig. 23(b) and Fig. 23(c) respectively whereas for $R = 1.45$ k Ω double scroll attractor is generated as shown in Fig. 23(d). The topological mixing reveals that the Rossler attractors are the simplest chaotic attractors, whereas the shape of the double scroll attractors appears as a Saturn ring attached by means of swirling lines.

IX. CONCLUSION

This article features a simple grounded OTA-CMOS inverter-based memristor emulator that operates up to 50 MHz with a 2.25 mW power consumption in 180-nm CMOS technology. We have presented a new circuit configuration of the emulator with a fairly low transistor count, i.e., 13 transistors. The experimental results signify that the design has a favorable noise performance. The simulation results are in agreement with the fingerprints of the ideal memristor. This manuscript is the first ever to report a MIF neuron circuit implemented in full CMOS technology and with a few simplifying presumptions, the energy consumption per spike and static power that this MIF neuron circuit dissipates falls roughly around 196 pJ and 443 pW respectively. Thus, our work attains an energy efficiency alike to most of the modern designs, while being realizable in full CMOS. Moreover, the spiking signal traits offered by the MIF circuit are physiologically alike to that of a biological neuronal signal. In addition, we have also implemented a MIF neuron based pattern detection circuit to bring out the practical significance of the proposed MIF neuron design. The work is also corroborated by the fabrication of a MOS chip of the proposed design having a die size of L=1499.96 μm & W=1499.96 μm . The test results for the fabricated memristor emulator are in good agreement with the simulation results. To show the chaos behavior, we have also conducted an experiment from an application perspective of the fabricated memristor emulator chip. The introduction of the proposed memristor emulator and MIF neuron circuit may provide new applications of memristor technologies, especially in the field of neuromorphic computing.

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