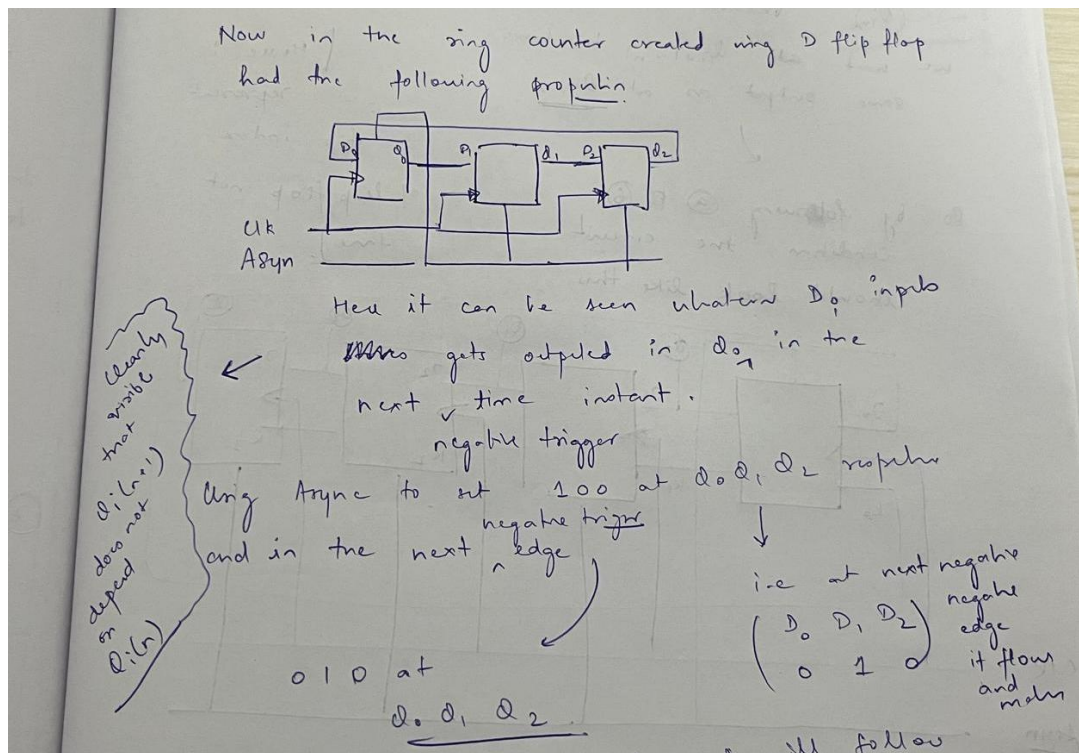


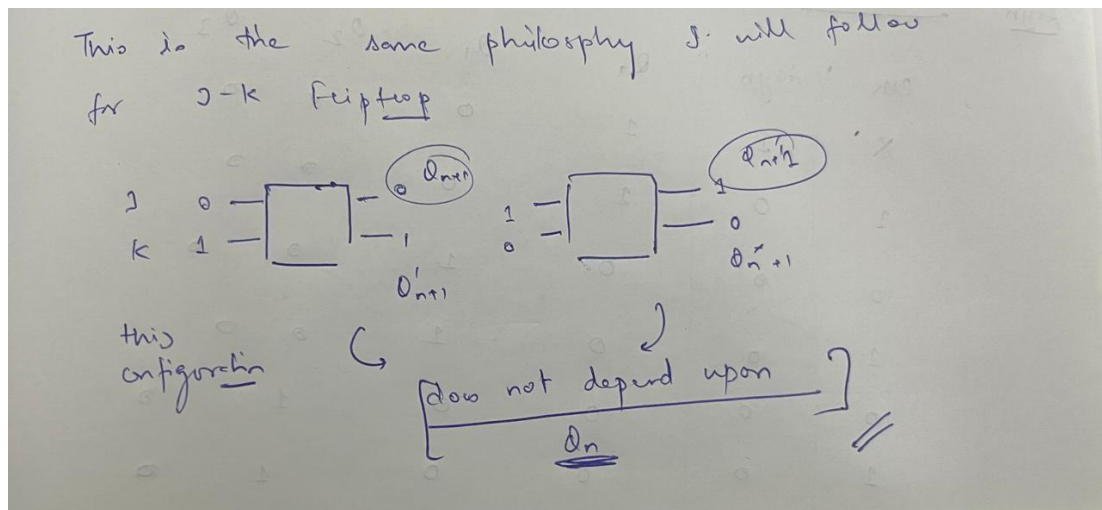
Assignment-3

Name: Aditya Rathor
Roll No: B22AI044

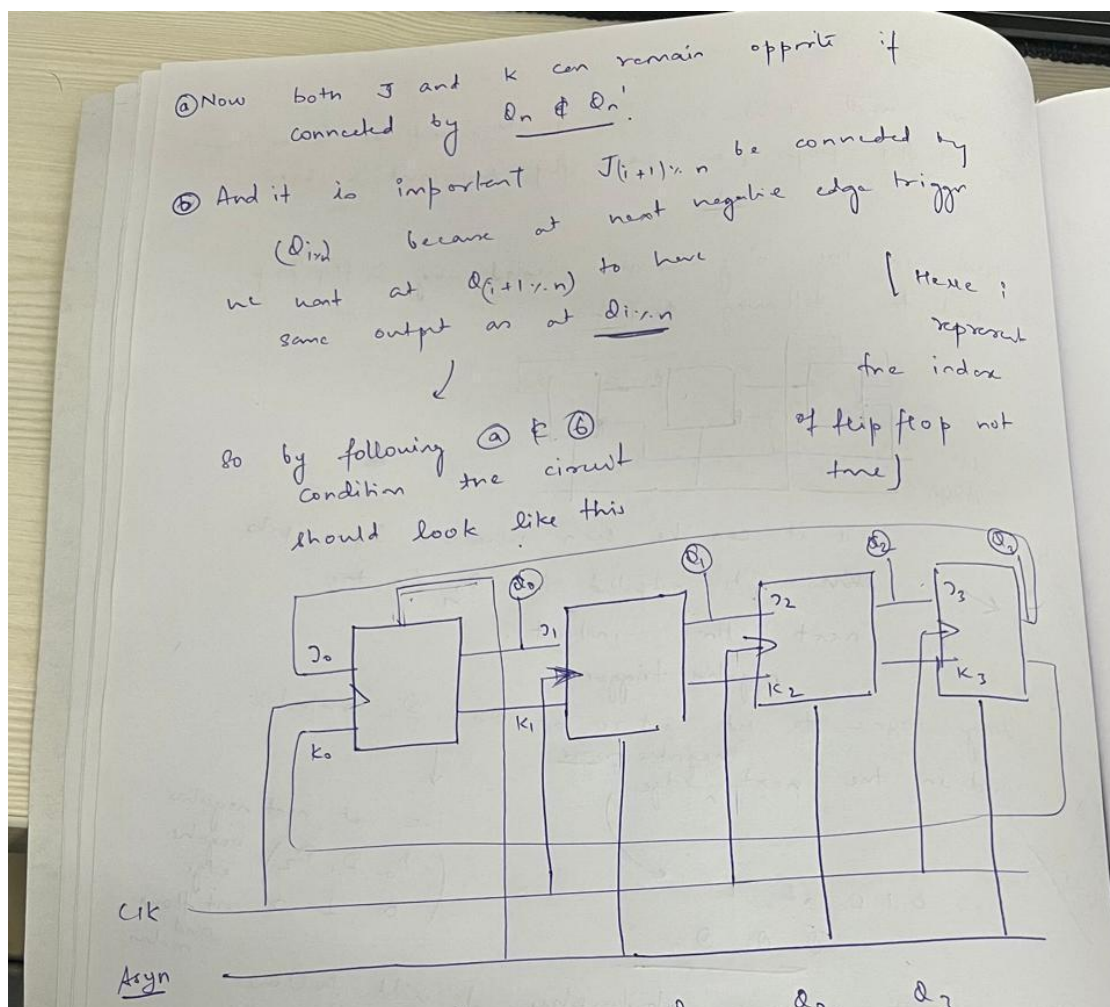
Q1(Ring Counter)

Since 4bit ring counter is needed so there will be a requirement of 4 bit flip-flop as each flip flop represents a bit in the counter





And using that I designed the circuit:



In this when preset==1 then output is always 1 and clear ==1 then output is always 0 independent of the clock signal as in the case where $Q_0 = 1$ and rest are set to 0

And the truth tabel for it:

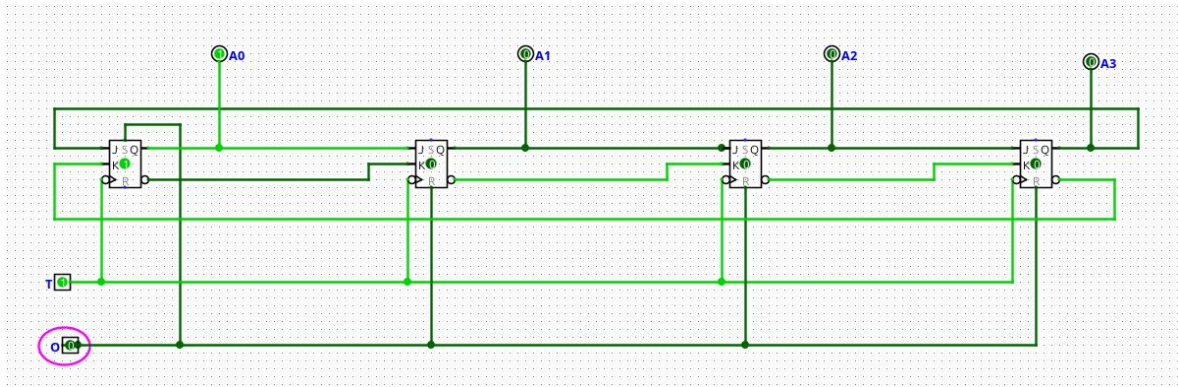
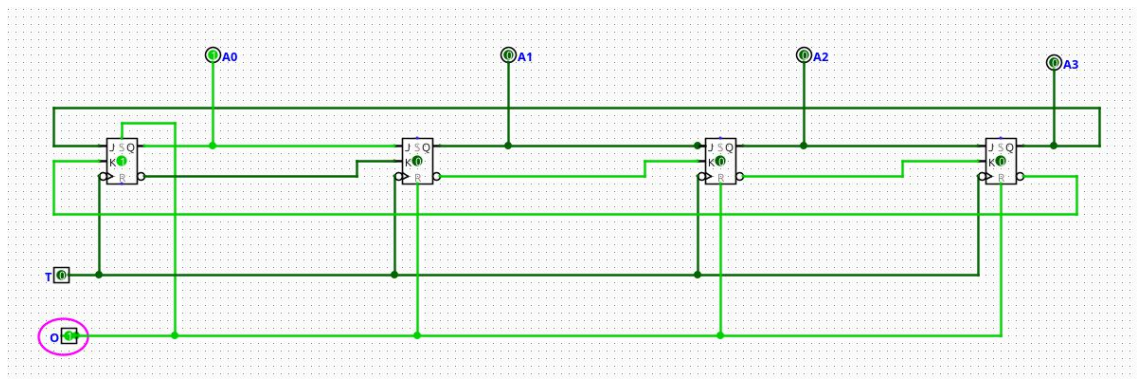
Here Q_i is the state after clock change

clk	Asyn	Q_0	Q_1	Q_2	Q_3
X	1	1	0	0	0
1	0	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	0	0	0	1	0
1	0	0	0	1	0

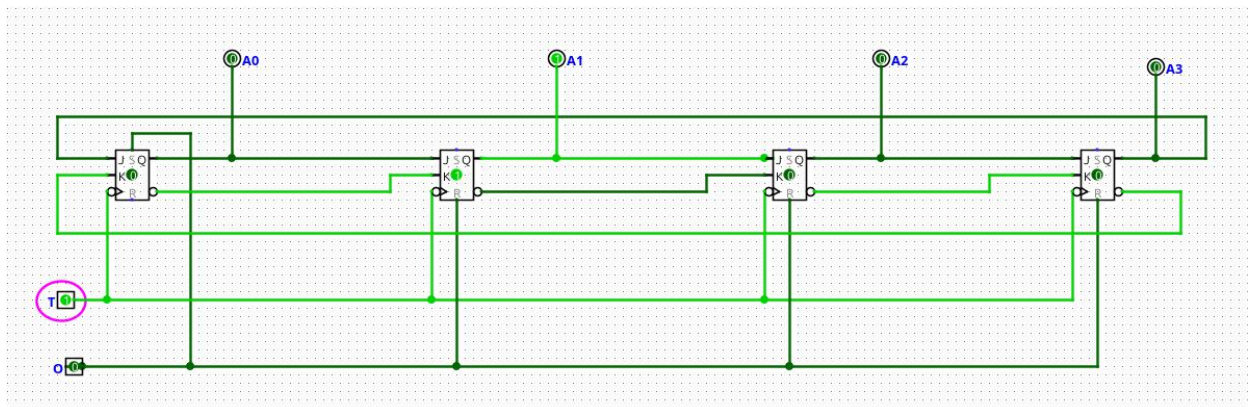
0	0	0	0	0	1
1	0	0	0	0	1
0	0	1	0	0	0

Considering Q_0 to be LSB it starts from $1 \rightarrow 2 \rightarrow 4 \rightarrow 8$

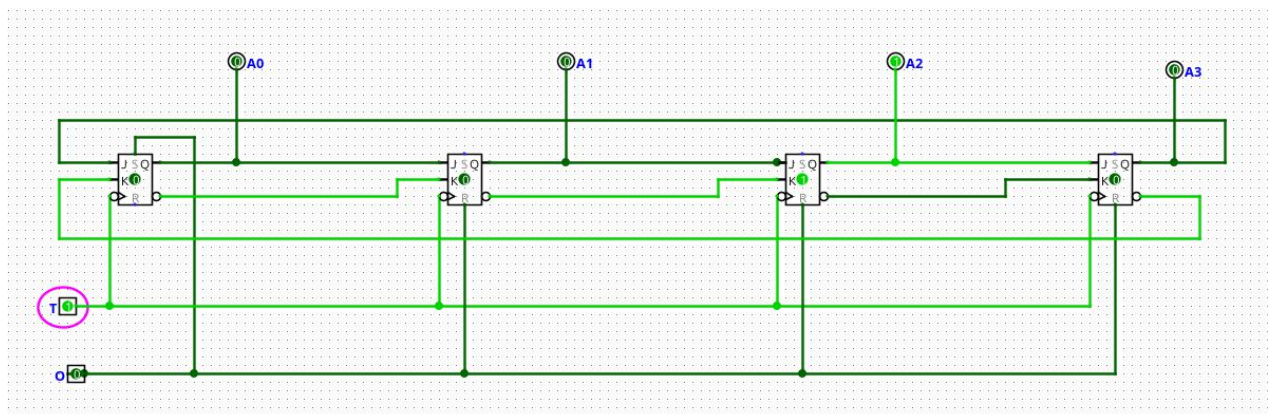
The below is the circuit for the above test vector

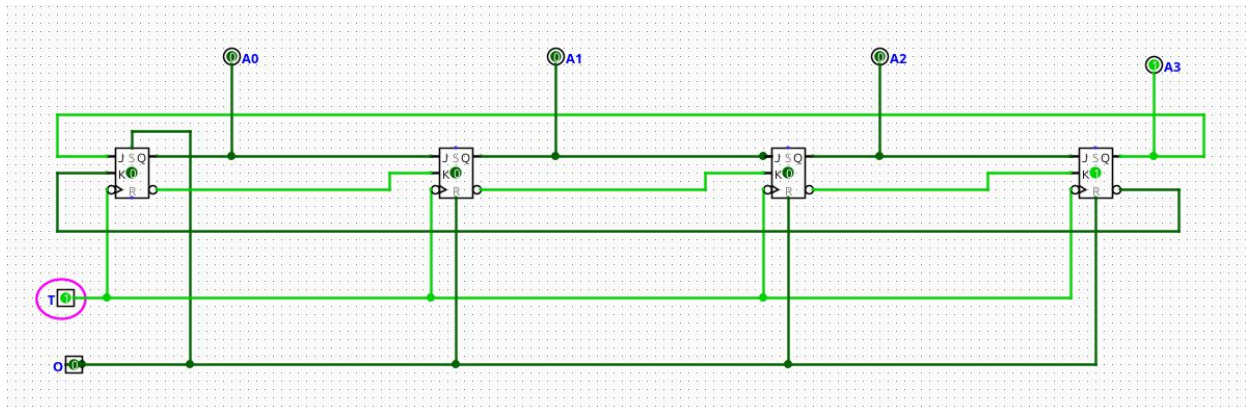


In the next negative edge trigger it is moving to the next flip flop which is A1

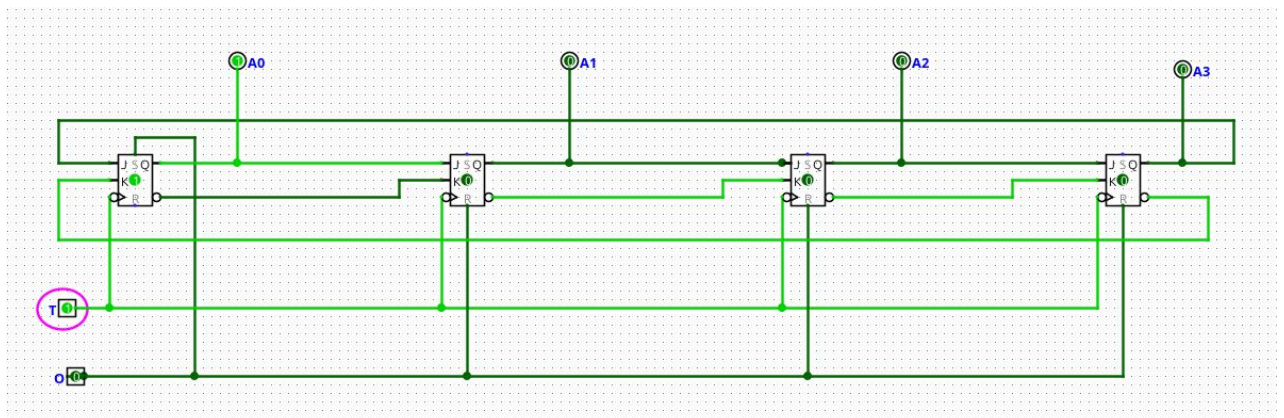


Moving to A2





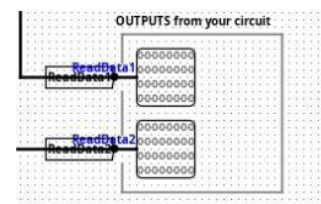
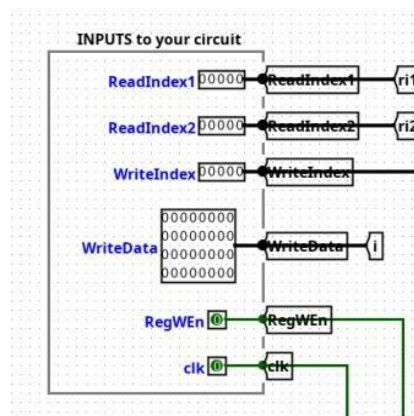
And again moving to the starting A0 in the next negative edge trigger



Q2(Register File)

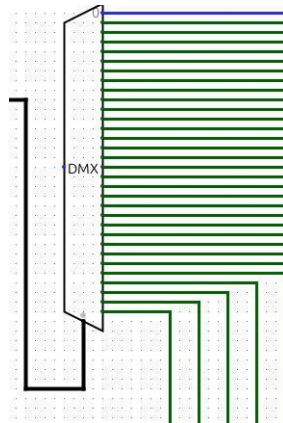
ReadIndex1 and ReadIndex2:

(used for getting the register number to be read which in R type instruction and I type are s,t and s respectively) are connected to the selection lines of both mux using a tunnel and is connected further to the output section of the circuit as the input line are carrying 32 bit data sent from the register whose value is to be read



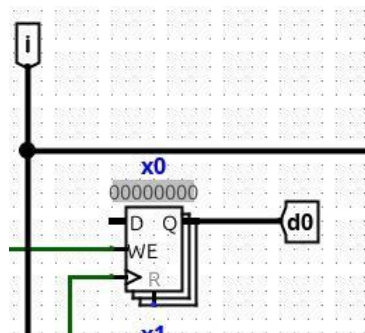
Next WriteIndex is used as a selection line for the demux

Here demux role is to select that line connected further to that register whose data needs to be written



The writeData in the input contains the data that needs to be written in the register and is connected using the tunnel of i such that further it is connected to each register's data line except x0 as in it data is always zero as shown below

x0 register

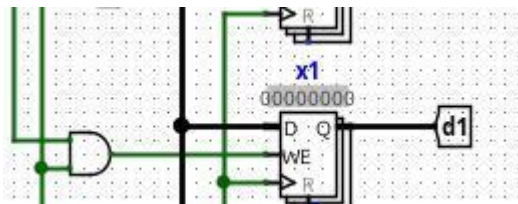


Now since i tunnel is connected to every register (except x0) so how to ensure that data only goes into the desired register whenever required

There I made use of the enable pin in the register such that it is connected by an AND gate such that the inputs to it are

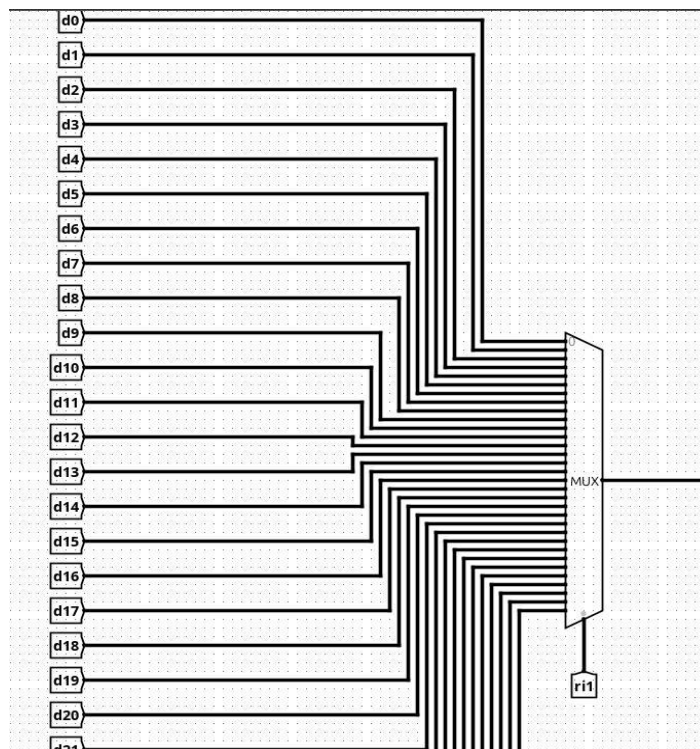
1. the selected line from demux connecting to the register
2. and RegWEn which is a type of control signal which controls that whether write operation are allowed in the register file or not

This is shown below:



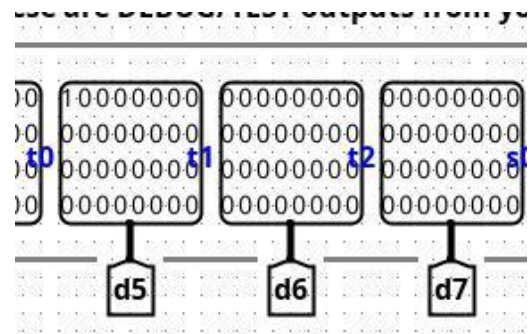
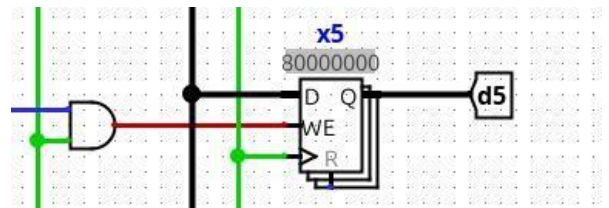
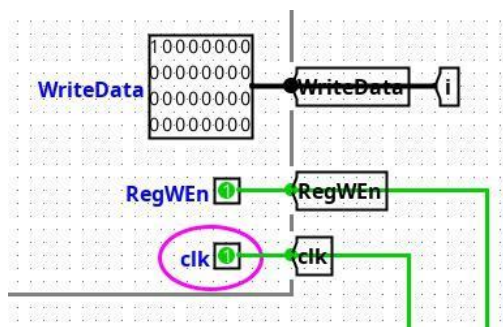
R line in the register is connected with the clock line such that operations are performed in the desired register on edge trigger here the register is positive edge trigger

Q line (Output from the register) connected with the mux which is used for selecting the register on which read operation needs to be performed



Testing:

- Write operation in register x5 after trigger clk from 0 to 1 and output visible in the debugging section in t0 as data goes into d5



- Performing read operation
writing in x4 and then reading it

