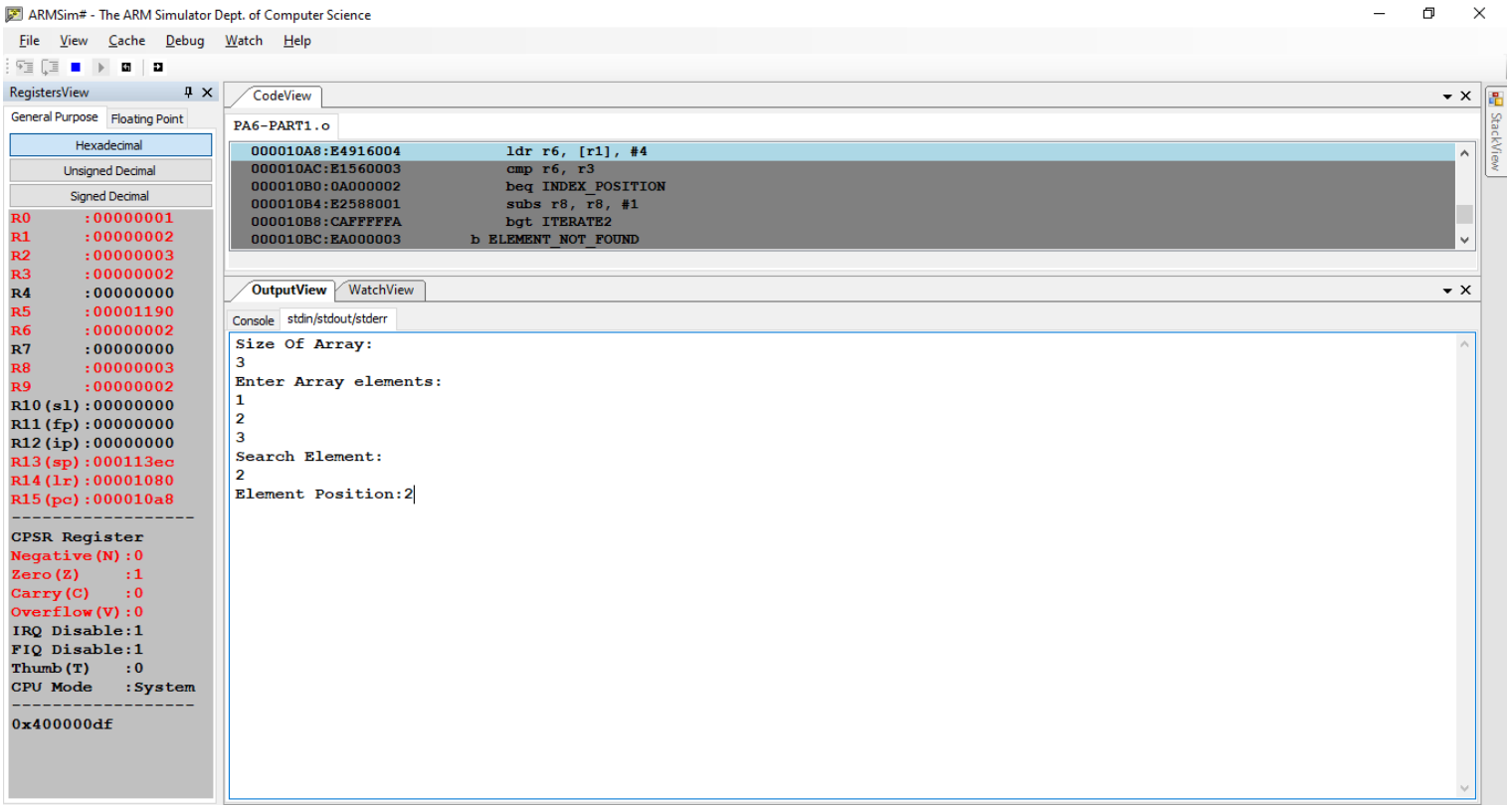
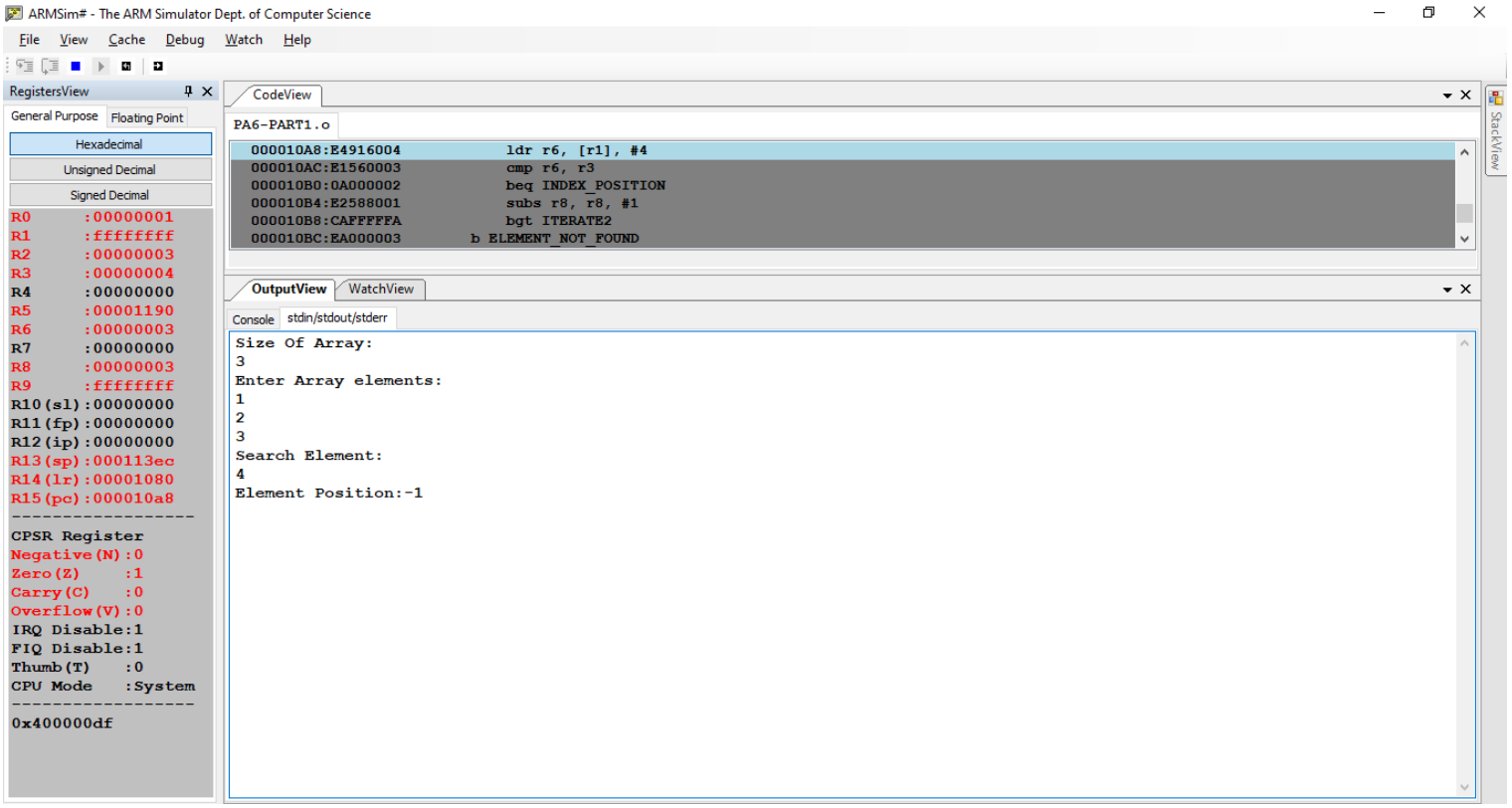
Part1:

Positive Case:

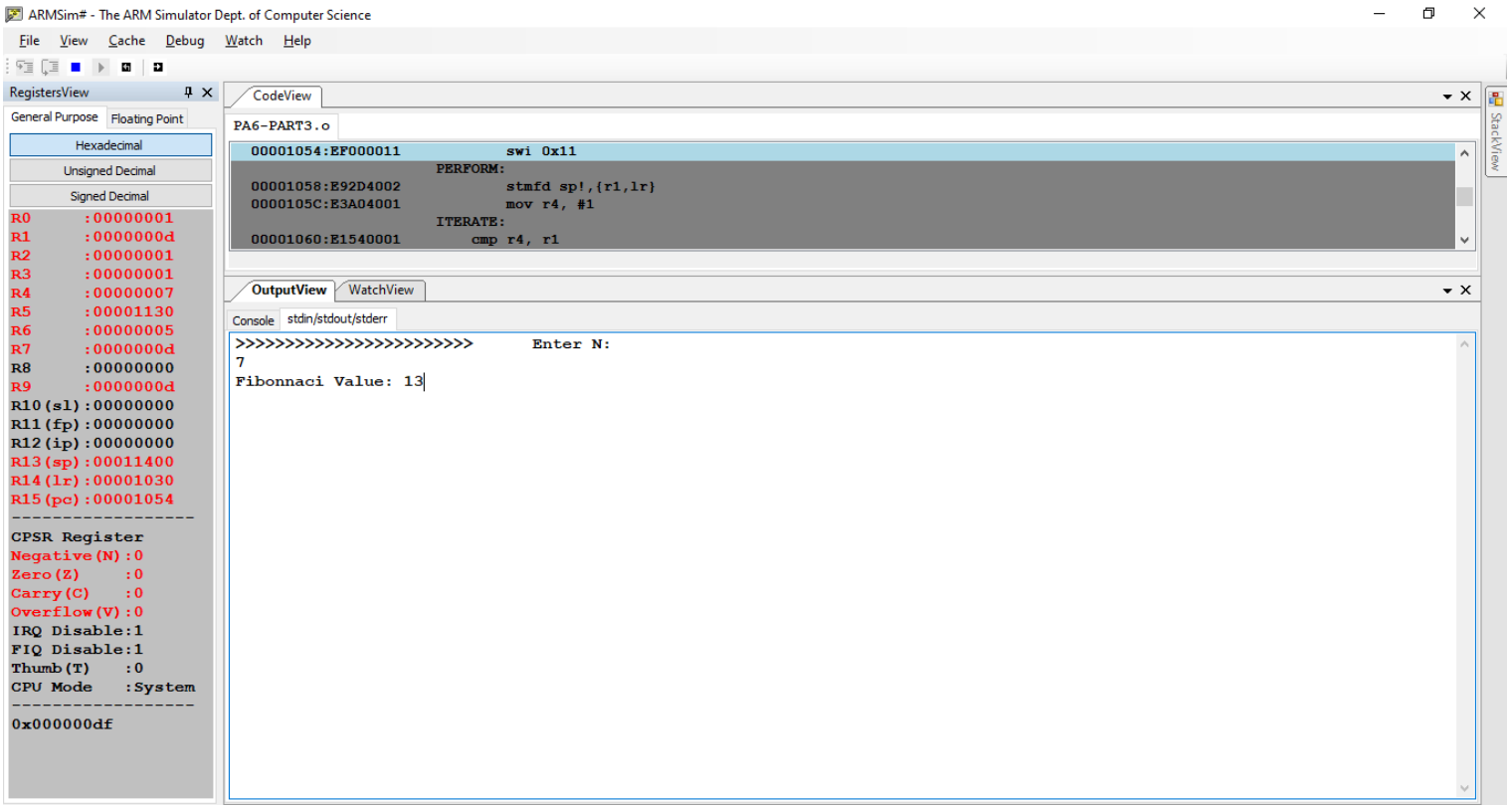


Negative Case:

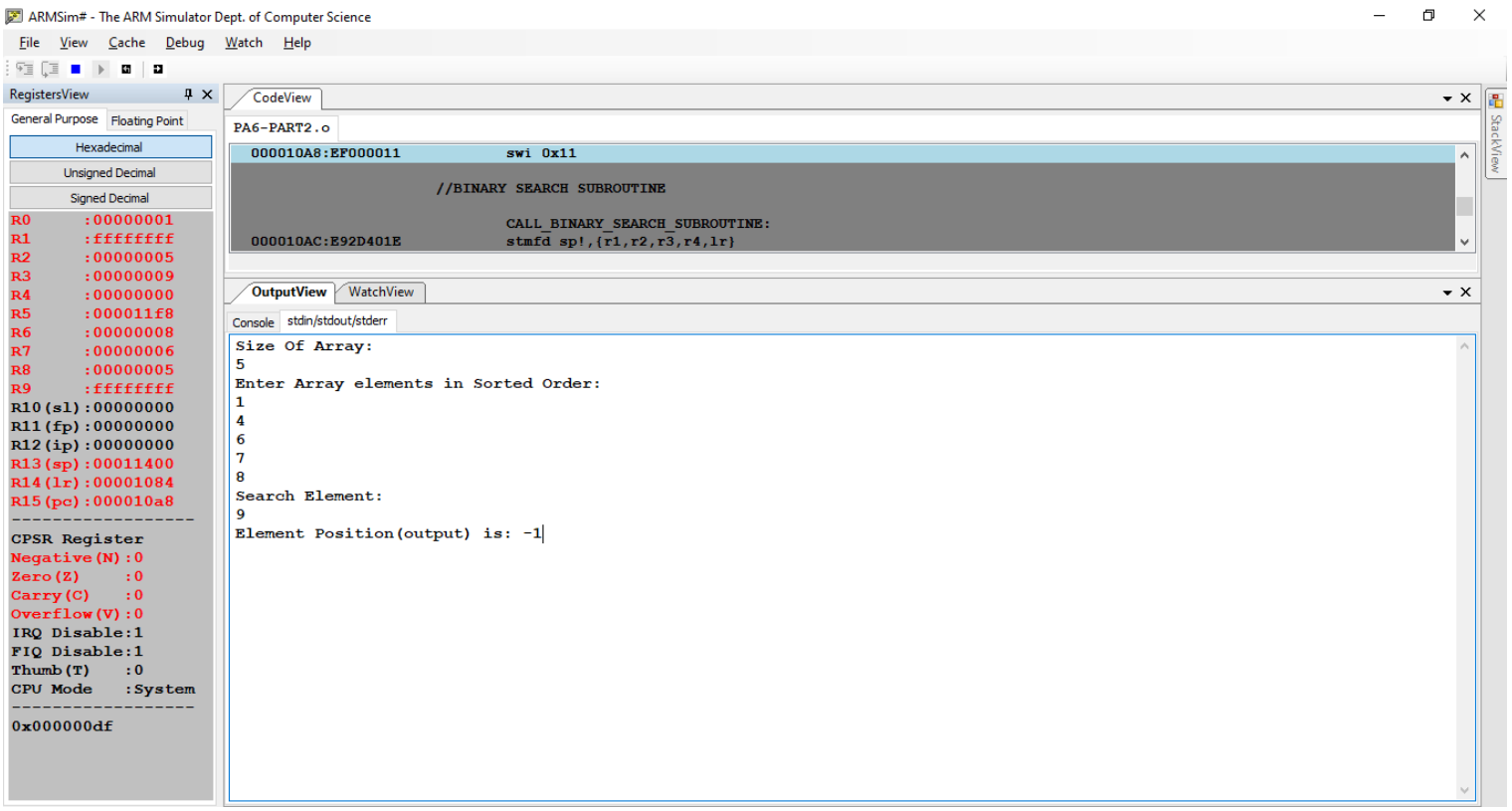


Part 2:

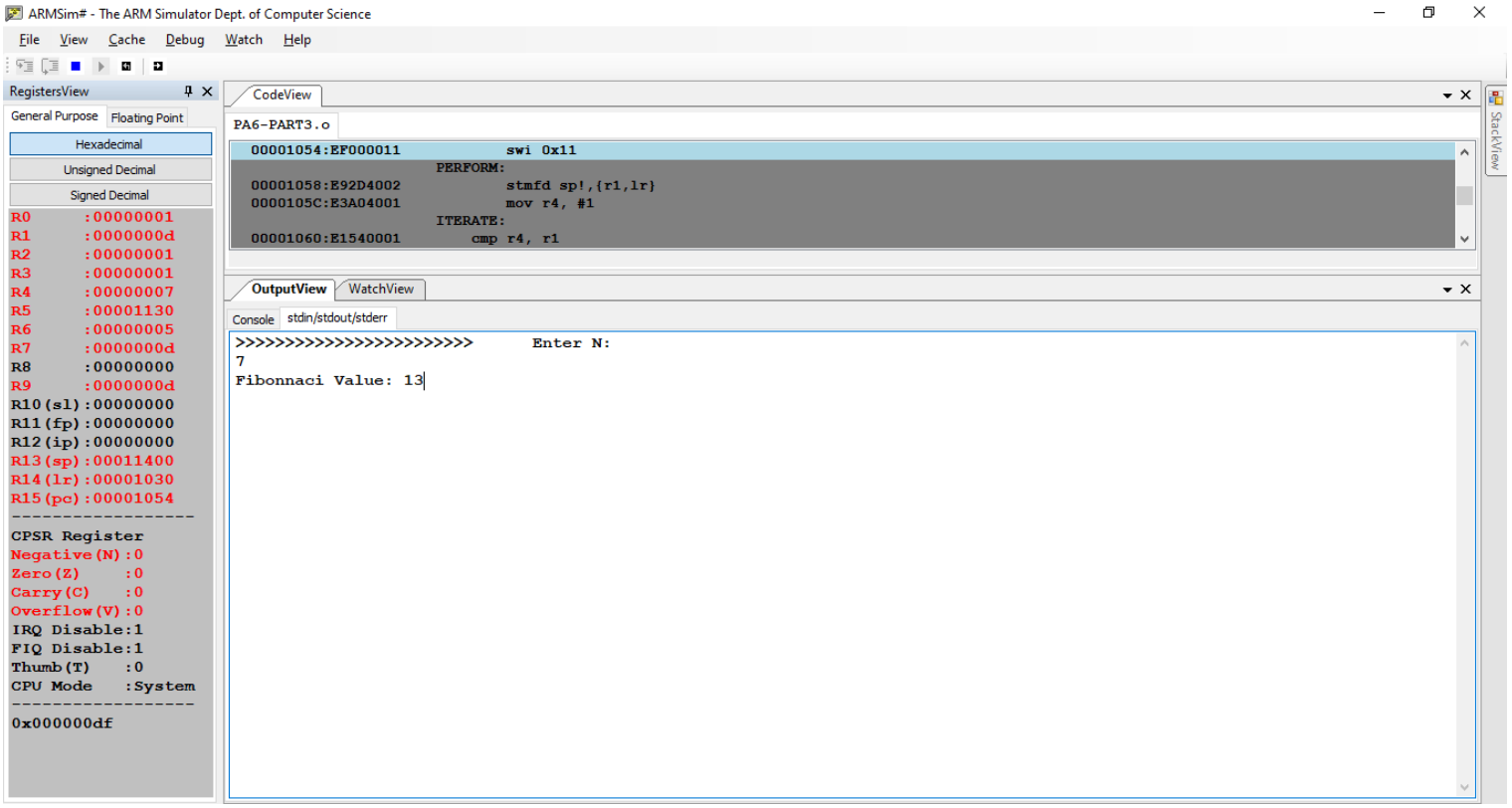
Positive Case:



Negative Case:



Part 3:


ARMSim# - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000001
R1 :0000000d
R2 :00000001
R3 :00000001
R4 :00000007
R5 :00001130
R6 :00000005
R7 :0000000d
R8 :00000000
R9 :0000000d
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00011400
R14(lr):00001030
R15(pc):00001054
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
CodeView
PA6-PART3.o
00001054:EF000011 swi 0x11
PERFORM:
00001058:E92D4002 stmfd sp!,{r1,lr}
0000105C:E3A04001 mov r4, #1
ITERATE:
00001060:E1540001 cmp r4, r1
OutputView WatchView
Console stdin/stdout/stderr
>>>>>>>>>>>>>>>>>>>>>>>> Enter N:
7
Fibonnaci Value: 13
StackView