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CSEN 702: Microprocessors
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Practice assignment 3

Exercise 1

Assume we have a computer where the cycles per instruction (CPI) is 1.0 when all memory accesses hit in the cache.
The only data accesses are loads and stores, and these total 50% of the instructions.
If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits?

Exercise 2

Assume that the cache miss penalty is 200 clock cycles, and all instructions normally take 1.0 clock cycles (ignoring memory stalls).
Assume that the average miss rate is 2%, there is an average of 1.5 memory references per instruction, and the average number of cache misses per 1000 instructions is 30.
What is the impact on performance when behavior of the cache is included? Also what's the impact when no cache is used at all.
Hint: Calculate the impact using both misses per instruction and miss rate.

Exercise 3

What is the impact of two different cache organizations on the performance of a processor? Assume that the CPI with a perfect cache is 1.6, the clock cycle time is 0.35 ns, there are 1.4 memory references per instruction, the size of both caches is 128 KB, and both have a block size of 64 bytes. One cache is *direct mapped* and the other is *two-way set associative*.
Since the speed of the processor can be tied directly to the speed of a cache hit, assume the processor clock cycle time must be stretched 1.35 times to accommodate the added selection hardware of the set associative cache.
The cache *miss penalty* is 65 ns for either cache organization.
Assume the *hit time* is 1 clock cycle, the *miss rate* of a direct-mapped 128 KB cache is 2.1%, and the *miss rate* for a two-way set associative cache of the same size is 1.9%.

1) Calculate the average memory access time. Discuss the result.
2) Calculate the processor performance. Discuss the result.

Exercise 4

Compare the two below schemes by comparing A) the miss rates and B) average memory access time.

- **Scheme 1:** 16 KB *instruction cache* with a 16 KB *data cache*
- **Scheme 2:** 32 KB unified cache
  - Both caches are write-through, use the table below for misses per 1000 instructions
  - 36% of the instructions are data transfer instructions.
  - Assume a hit takes 1 clock cycle and the miss penalty is 200 clock cycles.
  - A load or store hit takes **1 extra clock** cycle on a unified cache if there is only one cache port to satisfy two simultaneous requests.

Table 1. Misses per 1000 instructions

Size (KB)	Instruction cache	Data cache	Unified cache
8	8.16	44.0	63.0
16	3.82	40.9	51.0
32	1.36	38.4	43.3