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CSEN 702: Microprocessors
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Practice assignment 2

Exercise 1

Consider the following code:

```
Loop: LD R1,0(R2)          #load R1 from address 0+R2
DADDI R1, R1, 1            #R1=R1+1
SD R1, 0(R2)                     #store R1 at address 0+R2
DADDI R2, R2, 4            #R2=R2+4
DSUB R4,    R3,    R2            #R4=R3-R2
BNEZ R4,    Loop           #branch to Loop if R4!=0
```

Assume that the initial value of R3 is R2 + 396.

A) List all data dependencies, regardless if they cause a hazard or not.

B) Show the timing of this instruction sequence for the 5-stage RISC pipeline without any forwarding or bypassing hardware but assuming that a register read and a write can happen in the same clock cycle as mentioned in the lecture. Assume branches are handled by stalling the pipeline until the outcome is known. Branch outcomes are known at the end of EX stage.

C) Show the timing of this instruction sequence for the 5-stage RISC pipeline with full forwarding and bypassing hardware. Assume that the branch is handled by predicting it as **not taken**. Branch outcomes are known at the end of Decode stage.

D) Show the timing of this instruction sequence for the 5-stage RISC pipeline with full forwarding and bypassing hardware. Assume that the branch is handled by predicting it as **taken**.

Exercise 2

Complete the timing sequence of this code.
Each (…) represents a normal integer instruction with no dependency. Notice the floating point operations. What are the issues that you faced?

Instruction
MUL.D F0,F4,F6
...
...
ADD.D F2,F4,F6
...
...
L.D F2,0(R2)

Exercise 3

A microprocessor is designed to have an adjustable voltage. It was observed that reducing the voltage to 80% would result in a 25% reduction of the frequency. Calculate the impact of this reduction on power and energy.

Exercise 4

Suppose we have made the following measurements.

- Frequency of FP operations = 20%
- Average CPI of all FP operations = 5.0
- Average CPI of other instructions = 1.5.
- Frequency of FP division is 4% out of the entire program, with a CPI of 14.

A) Compute the average CPI.
B) Consider two enhancements E1 and E2, where in E1, we try to minimize the CPI of FP divisions to 4, while in E2, we try to minimize the overall FP CPI to 2.5. Compare the impact of both enhancements on the performance.

Exercise 5

Consider the following benchmark execution times for processors A and B, against the reference processor R.

Benchmark	**R**	**A**	**B**
wupwise	1600	45	55
swim	900	40	20

A) Compare the performance of processors A and B, using the geometric mean.
B) Discuss the result.

Exercise 6 [optional]

Consider the following prices and measures:

- Cost of wafer: 50$
- A wafer can be divided into 1200 dies. 34% of them are usually defective on average.
- Testing costs 4$ and packaging cost an extra 3$
- A final yield test is found to be 97%.

Calculate the cost of the integrated circuit.