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Dept. of Computer Science and Engineering
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CSEN 702: Microprocessors
Winter 2024
Quiz 1 version 1 (30 min)

Name	ID	Tutorial

Question 1	Question 2	Total
8	12	20

Formula sheet

Pipelining
CPI pipelined = Ideal CPI + Pipeline stall clock cycles per instruction
$\text{Speedup} = \frac{\text{Pipeline depth}}{1 + \text{Pipeline stall cycles per instruction}}$

Execution time = IC x CPI x CCT

Exercise 1 (8 pts)

Consider a pipelined processor with full forwarding. It's found that, due to data hazards, we incur 3 stalls every 10 instructions. Furthermore, due to structural hazards, it was found that, on average, we have 10 stalls per 100 instructions.
The processor uses an always-taken scheme for its branches, which are computed in the execute stage.

A) Given that 12% of the instructions are branches, and 70% of the branches are found to be taken, compute the CPI.

CPI = 1 + 3/10 + 0.1 + 0.12 x 0.3 (misprediction) x 2 (2 cycles penalty since exec stage)
= 1.472

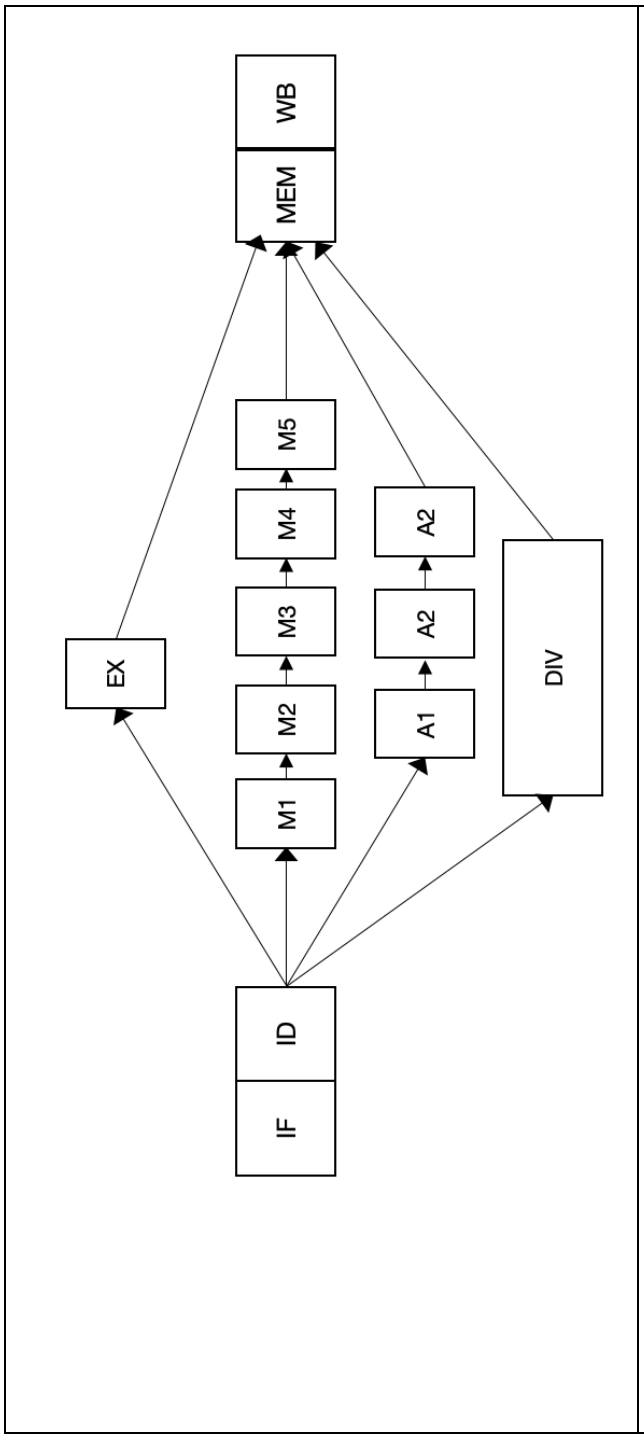
B) We wish to decrease the CPI found in part (A) by 3%, by changing the prediction scheme and computing the branch in the decode stage. What should be the minimum prediction accuracy of that scheme, given that changing the scheme would require extending the clock cycle by 5%?

New required cpi = 1.472 x 0.97 = 1.427
1.427 = 1.4 + 0.12 x M x 1, where M is the misprediction rate.
M = 0.225 or 22.5%
So prediction accuracy = 77.5%
N.B. Clock cycle time doesn't play a role here.

Exercise 2 (12 pts)

Consider this modified version of the floating MIPS where the multiplier is pipelined into 5 stages, the floating point adder into 3, and the divider is not pipelined but needs 6 cycles to finish. Forwarding is applied everywhere. Register file can write and read in the same cycle. A special hardware is present to detect true structural hazards.

Fill in the timing diagram up to cycle 20, if needed. For stall cycles, leave cell empty or place a dash (-)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
L.D F1, 6(R2)																				
MUL.D F2, F1, F1																				
ADD.D F3, F4, F5																				
DIV.D F6, F2, F3																				
S.D F6, 6(R2)																				

SOLUTION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
L.D F1,6(R2)	F	D	X	M	W													
MUL.D F2,F1,F1		F	D		M1	M2	M3	M3	M5	M	W							
ADD.D F3,F4,F5			F		D	A1	A2	A3	M	W								
DIV F6,F2,F3					F	D				DIV	DIV	DIV	DIV	DIV	DIV	M	W	
S.D F6,6(R2)						F				D	X					M	W	