Faculty of Media Engineering and Technology
Dept. of Computer Science and Engineering
Dr. Milad Ghantous

CSEN 702: Microprocessors
Winter 2022
Quiz 2 Version 1 - solution

Name: _____ ID: _____ Group: _____

Question 1- (8 pts) Consider a CPU that uses the Tomasulo architecture. At some clock cycle X, the following is observed in the reservation stations and the register file.
Explain each one of them in a sentence. (6 pts)

RS A1:

1	ADD	2.8		0	M1

Explanation:
An ADD instruction is issued to RS A1, Vj field = 2.8 while Qj =0 means 2.8 is valid and was grabbed from the register file, while Vk = 3 and Qk=M1(!=0) meaning that 3 is invalid and this ADD must wait for M1 to be able to start executing.

RS M1:

1	DIV	2.8	3	0	0

Explanation:
this is a DIV instruction that is currently executing since both fields Q are zeros.

Store buffer:

1	10+R5		A1

Explanation: store is issued with address 10(R5) and it is waiting for A1 to finish.

Register file:

Reg	Q
F2	M1
F3	A1
F4	0

Explanation:
Register F2 will be computed by M1 (DIV) when it finishes, while F3 is the destination of the ADD instruction in A1, and F4 is currently valid and no one is producing it.

Part B) Reverse engineer into assembly. Take any necessary assumptions. (2 pts)

```
DIV.D   F2, F7,F8
SUB.D   F3,F7, F2
S.D     F3, 10(R5)
```

Question 2- Consider the following code to be scheduled on a Tomasulo's architecture with 2 add/sub reservation stations, 2 mult/div reservation stations, 2 load buffers and 2 store buffers.

Multiplication takes 2 execution cycles, addition takes 1 execution cycles, loads and stores take 1 execution cycles each, but the first load misses and takes 3 cycles to execute.

F5 is available in the register file and contains the value 9.0. Also register R2 is available and contains value 2. (12 pts)

```
L.D   F2, 10(R2)
ADD.D F3, F2 ,F2
ADD.D F4, F3, F3
MUL.D F5, F5, F5
S.D   F4, 10(R2)
```

- Fill in the contents of the corresponding components on pages 3 to 6, each clock cycle, starting with cycle 1 up until cycle 7 inclusive. (8 pts)
- However, fill the table on Page 2, fully, *until code completion.* (4 pts)
- Write down a summary of events in each cycle inside the discussion box.
- Note that the A field is omitted in the RS of Add and Mult.
- If 2 instructions want to write result in the same cycle, use FIFO order.

	Issue	Execute	Write result
L.D F2, 10(R2)	1	2…4	5
ADD.D F3, F2 ,F2	2	6	7
ADD.D F4, F3, F3	3	8	9
MUL.D F5, F5, F5	4	5…6	8
S.D F4, 10(R2)	5 (6 is also accepted)	10	11

6 in case someone considers the load published in 5 and exits, so the store, having the same address can now be issued)

Cycle 1

	Busy	op	Vj	Vk	Qj	Qk
A1	0					
A2	0					

	busy	op	Vj	Vk	Qj	Qk
M1	0					
M2	0					

	Busy	Address
L1	1	12
L2	0	

	busy	Address	V	Q
S1	0			
S2	0			

	Qi	Reg value	Discussion
F2	L1		Load is issued
F3			
F4			
F5	0	9	

Cycle 2

	Busy	op	Vj	Vk	Qj	Qk
A1	1	add			L1	L1
A2						

	busy	op	Vj	Vk	Qj	Qk
M1						
M2						

	Busy	Address
L1	1	12
L2	0	

	busy	Address	V	Q
S1	0			
S2	0			

	Qi	Reg value	Discussion
F2	L1		Add is issued Load starts will finish at 6
F3	A1		
F4			
F5	0	9	

Cycle 3

	Busy	op	Vj	Vk	Qj	Qk
A1	1	add			L1	L1
A2	1	add			A1	A1

	busy	op	Vj	Vk	Qj	Qk
M1						
M2						

	Busy	Address
L1	1	12
L2	0	

	busy	Address	V	Q
S1	0			
S2	0			

	Qi	Reg value	Discussion
F2	L1		Second add is issued
F3	A1		
F4	A2		
F5	0	9	

Cycle 4

	Busy	op	Vj	Vk	Qj	Qk
A1	1	add			L1	L1
A2	1	add			A1	A1

	busy	op	Vj	Vk	Qj	Qk
M1	1	mult	9	9		
M2						

	Busy	Address
L1	1	12
L2	0	

	busy	Address	V	Q
S1	0			
S2	0			

	Qi	Reg value	Discussion
F2	L1		mult is issued
F3	A1		
F4	A2		
F5	M1	9	

Cycle 5

	Busy	op	Vj	Vk	Qj	Qk
A1	1	add	Mem[12]	Mem[12]		
A2	1	add			A1	A1

	busy	op	Vj	Vk	Qj	Qk
M1	1	mult	9	9		
M2						

	Busy	Address
L1	0	
L2	0	

	busy	Address	V	Q
S1	1	12		A2
S2	0			

	Qi	Reg value	Discussion
F2	0	Mem[12]	Load publishes, taken by A1 Mult is executing Store is issued
F3	A1		
F4	A2		
F5	M1	9	

Cycle 6

	Busy	op	Vj	Vk	Qj	Qk
A1	1	add	Mem[12]	Mem[12]		
A2	1	add			A1	A1

	busy	op	Vj	Vk	Qj	Qk
M1	1	mult	9	9		
M2						

	Busy	Address
L1	0	
L2	0	

	busy	Address	V	Q
S1	1	12		A2
S2	0			

	Qi	Reg value	Discussion
F2	0	Mem[12]	• Nothing happens in terms of values. • A1 is executing and will publish in 7 • Mult is executing and will publish in 8 (because A1 publishes in 7) • Store is also executing and will write result in 7 (this is ok since store doesn't use the bus)
F3	A1		
F4	A2		
F5	M1	9	

Cycle 7

	Busy	op	Vj	Vk	Qj	Qk
A1	0					
A2	1	add	2*m[12]	2*m[12]		

	busy	op	Vj	Vk	Qj	Qk
M1	1	mult	9	9		
M2						

	Busy	Address
L1	0	
L2	0	

	busy	Address	V	Q
S1	0			
S2	0			

	Qi	Reg value	Discussion
F2	0	Mem[12]	• A1 published taken by A2 and reg file.
F3	0	2*Mem[12]	
F4	A2		
F5	M1	9	