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CSEN 702: Microprocessors
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Practice assignment 7-Solution

Consider the following code:

```
MUL R3, R1, R2
ADD R5, R3, R4
ADD R7, R2, R6
ADD R10, R8, R9
MUL R11, R7, R10
ADD R5, R5, R11
```

Assume multiplication takes 6 cycles and addition takes 4 cycles, to execute. Both units are pipelined.

a) Consider the regular pipeline with forwarding. Compute the number of cycles needed to execute this code. (Show the steps)

b) Re-execute this code using Tomasulo using 3 add reservation stations and 2 multiply reservation stations (Assume tomasulo is used for integer instructions) and compute the number of cycles needed. (Show all the steps and consider R1, R2, R4, R6, R8, R9 are available initially)
Also, if two instructions finish in the same cycle, discuss your opinion on who publishes on CDB first.

Solution

A) M is mem, W is write back

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**
MUL	IF	ID	1	2	3	4	5	6	M	W																
ADD		IF	ID	-	-	-	-	-	1	2	3	4	M	W												
ADD			IF	-	-	-	-	-	ID	1	2	3	4	M	W											
ADD									IF	ID	1	2	3	4	M	W										
MUL										IF	ID	-	-	-	1	2	3	4	5	6	M	W				
ADD											IF	-	-	-	ID	-	-	-	-	-	1	2	3	4	M	W

TOTAL= 26 cycles.

B) Applying Tomasulo algorithm

```
MUL R3, R1, R2
ADD R5, R3, R4
ADD R7, R2, R6
ADD R10, R8, R9
MUL R11, R7, R10
ADD R5, R5, R11
```

Cycle 1:

	Issue	Execute	Write result
MUL R3, R1, R2	1		
ADD R5, R3, R4			
ADD R7, R2, R6			
ADD R10, R8, R9			
MUL R11, R7, R10			
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1						
A2						
A3						

	op	Vj	Vk	Qj	Qk	busy
M1	**mul**	**Reg[R1]**	**Reg[R2]**			**1**
M2						

	Qi
R1	
R2	
R3	**M1**
R4	
R5	
R6	
R7	
R8	
R9	

R10	
R11	

Cycle 2:

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…	
ADD R5, R3, R4	2		
ADD R7, R2, R6			
ADD R10, R8, R9			
MUL R11, R7, R10			
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	**add**		**Reg[R4]**	**M1**		**1**
A2						
A3						

	op	Vj	Vk	Qj	Qk	busy
M1	**mul**	**Reg[R1]**	**Reg[R2]**			**1**
M2						

	Qi
R1	
R2	
R3	**M1**
R4	
R5	**A1**
R6	
R7	
R8	
R9	
R10	
R11	

- **Since multiply M1 started in cycle 2, it will finish in cycle 7 (it needs 6 cycles)**

Cycle 3:

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…	
ADD R5, R3, R4	2		
ADD R7, R2, R6	3		
ADD R10, R8, R9			
MUL R11, R7, R10			
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	add		Reg[R4]	M1		1
A2	add	Reg[R2]	Reg[R6]			1
A3						

	op	Vj	Vk	Qj	Qk	busy
M1	mul	Reg[R1]	Reg[R2]			1
M2						

	Qi
R1	
R2	
R3	M1
R4	
R5	A1
R6	
R7	A2
R8	
R9	
R10	
R11	

Cycle 4:

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…	
ADD R5, R3, R4	2		
ADD R7, R2, R6	3	4…	
ADD R10, R8, R9	4		
MUL R11, R7, R10			
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	add		Reg[R4]	M1		1
A2	add	Reg[R2]	Reg[R6]			1
A3	add	Reg[R8]	Reg[R9]			1

	op	Vj	Vk	Qj	Qk	busy
M1	mul	Reg[R1]	Reg[R2]			1
M2						

	Qi
R1	
R2	
R3	M1
R4	
R5	A1
R6	
R7	A2
R8	
R9	
R10	A3
R11	

A3 issued.
A2 starts executing and needs 4 cycles so will finish in cycle 7.

Cycle 5:

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…	
ADD R5, R3, R4	2		
ADD R7, R2, R6	3	4…	
ADD R10, R8, R9	4	5…	
MUL R11, R7, R10	5		
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	add		Reg[R4]	M1		1
A2	add	Reg[R2]	Reg[R6]			1
A3	add	Reg[R8]	Reg[R9]			1

	op	Vj	Vk	Qj	Qk	busy
M1	mul	Reg[R1]	Reg[R2]			1
M2	mul			A2	A3	1

	Qi
R1	
R2	
R3	M1
R4	
R5	A1
R6	
R7	A2
R8	
R9	
R10	A3
R11	M2

Multiply M2 is issued.
A3 starts executing and will finish cycle 8.

Cycle 6:

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…	
ADD R5, R3, R4	2		
ADD R7, R2, R6	3	4…	
ADD R10, R8, R9	4	5…	
MUL R11, R7, R10	5		
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	add		Reg[R4]	M1		1
A2	add	Reg[R2]	Reg[R6]			1
A3	add	Reg[R8]	Reg[R9]			1

	op	Vj	Vk	Qj	Qk	busy
M1	mul	Reg[R1]	Reg[R2]			1
M2	mul			A2	A3	1

	Qi
R1	
R2	
R3	M1
R4	
R5	A1
R6	
R7	A2
R8	
R9	
R10	A3
R11	M2

The last `add` cannot be issued due to structural hazard so it must wait until one of the adds finishes.

All other operations are executing in parallel now

Cycle 7:

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	
ADD R5, R3, R4	2		
ADD R7, R2, R6	3	4…7	
ADD R10, R8, R9	4	5…	
MUL R11, R7, R10	5		
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	add		Reg[R4]	M1		1
A2	add	Reg[R2]	Reg[R6]			1
A3	add	Reg[R8]	Reg[R9]			1

	op	Vj	Vk	Qj	Qk	busy
M1	mul	Reg[R1]	Reg[R2]			1
M2	mul			A2	A3	1

	Qi
R1	
R2	
R3	M1
R4	
R5	A1
R6	
R7	A2
R8	
R9	
R10	A3
R11	M2

M1 and A2 both finish in this cycle and will need to publish their results on the CDB in cycle 8. But one of them can publish. One possible scheme is to check who can execute if M1 is published and who can execute if A2 is published.
If M1 is published, A1 can start right away.
If A2 is published, it will be grabbed by M2 but cannot start because it still needs A3. So priority is for M1 to be published here.

Cycle 8:

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2		
ADD R7, R2, R6	3	4…7	
ADD R10, R8, R9	4	5…8	
MUL R11, R7, R10	5		
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	add	=(R1*R2)	Reg[R4]			1
A2	add	Reg[R2]	Reg[R6]			1
A3	add	Reg[R8]	Reg[R9]			1

	op	Vj	Vk	Qj	Qk	busy
M2	mul			A2	A3	1

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	A1	
R6		
R7	A2	
R8		
R9		
R10	A3	

R11	M2	

Cycle 9: A2 still hasn't published yet, and A3 needs to publish too. Again, we have to choose. There's no preference here so A2 will publish because it was meant to publish earlier than A3. It will be grabbed by M2.
A1 can start executing, will finish cycle 12.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…	
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	
MUL R11, R7, R10	5		
ADD R5, R5, R11			

	op	Vj	Vk	Qj	Qk	busy
A1	add	=(R1*R2)	Reg[R4]			1
A2	add	Reg[R2]	Reg[R6]			1
A3	add	Reg[R8]	Reg[R9]			1

	op	Vj	Vk	Qj	Qk	busy
M2	mul	=R2+R6			A3	1

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	A1	

R6		
R7	0	=R2+R6
R8		
R9		
R10	A3	
R11	M2	

Cycle 10: A3 will publish and grabbed by M2. M2 can start executing in cycle 11. Also The last Add that was stalled can now be issued.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…	
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5		
ADD R5, R5, R11	10		

	op	Vj	Vk	Qj	Qk	busy
A1	add	=(R1*R2)	Reg[R4]			1
A2	add			A1	M2	1
A3	add	Reg[R8]	Reg[R9]			1

	op	Vj	Vk	Qj	Qk	busy
M2	mul	=R2+R6	=R8+R9			1

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	A2	
R6		

R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	M2	

Cycle 11: m2 starts and will finish cycle 16

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…	
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5	11…	
ADD R5, R5, R11	10		

	op	Vj	Vk	Qj	Qk	busy
A1	add	=(R1*R2)	Reg[R4]			1
A2	add			A1	M2	1
A3						0

	op	Vj	Vk	Qj	Qk	busy
M2	mul	=R2+R6	=R8+R9			1

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	A2	

R6		
R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	M2	

Cycle 12: The first ADD in A1 finishes, will publish its results in cycle 13.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…12	
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5	11…	
ADD R5, R5, R11	10		

	op	Vj	Vk	Qj	Qk	busy
A1	add	=(R1*R2)	Reg[R4]			1
A2	add			A1	M2	1
A3						0

	op	Vj	Vk	Qj	Qk	busy
M2	mul	=R2+R6	=R8+R9			1

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2

R4		
R5	A2	
R6		
R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	M2	

Cycle 13: A1 publishes its results and grabbed by A2.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…12	13
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5	11…	
ADD R5, R5, R11	10		

	op	Vj	Vk	Qj	Qk	busy
A1	add	=(R1*R2)	Reg[R4]			1
A2	add	=R3+R4			M2	1
A3						0

	op	Vj	Vk	Qj	Qk	busy
M2	mul	=R2+R6	=R8+R9			1

	Qi	Reg value

R1		
R2		
R3	0	=R1*R2
R4		
R5	A2	
R6		
R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	M2	

Skip to Cycle 16: mul finishes execution. Will publish in 17.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…12	13
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5	11…16	
ADD R5, R5, R11	10		

	op	Vj	Vk	Qj	Qk	busy
A1						0
A2	add	=R3+R4			M2	1
A3						0

	op	Vj	Vk	Qj	Qk	busy
M2	mul	=R2+R6	=R8+R9			1

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	A2	
R6		
R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	M2	

Cycle 17: mul publishes in 17. And grabbed by A2.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…12	13
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5	11…16	17
ADD R5, R5, R11	10		

	op	Vj	Vk	Qj	Qk	busy
A1						0
A2	add	=R3+R4	=R7*R10			1
A3						0

	op	Vj	Vk	Qj	Qk	busy

M2	mul	=R2+R6	=R8+R9			1

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	A2	
R6		
R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	0	=R7*R10

Cycle 18: A2 can start and will finish cycle 21.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…12	13
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5	11…16	17
ADD R5, R5, R11	10	18…	

	op	Vj	Vk	Qj	Qk	busy
A1						0
A2	add	=R3+R4	=R7*R10			1
A3						0

	op	Vj	Vk	Qj	Qk	busy
						0
M2						0

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	A2	
R6		
R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	0	=R7*R10

Skip to Cycle 22: finish.

	Issue	Execute	Write result
MUL R3, R1, R2	1	2…7	8
ADD R5, R3, R4	2	9…12	13
ADD R7, R2, R6	3	4…7	9
ADD R10, R8, R9	4	5…8	10
MUL R11, R7, R10	5	11…16	17
ADD R5, R5, R11	10	18…21	22

	op	Vj	Vk	Qj	Qk	busy
A1						0
A2	add	=R3+R4	=R7*R10			1
A3						0

	op	Vj	Vk	Qj	Qk	busy
						0
M2						0

	Qi	Reg value
R1		
R2		
R3	0	=R1*R2
R4		
R5	0	=R5+R11
R6		
R7	0	=R2+R6
R8		
R9		
R10	0	=R8+R9
R11	0	=R7*R10