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Dept. of Computer Science and Engineering
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CSEN 702: Microprocessors
Winter 2024
Quiz 1 version 2 (30 min)

Name	ID	Tutorial

Question 1	Question 2	Total
8	12	20

Formula sheet

Pipelining
CPI pipelined = Ideal CPI + Pipeline stall clock cycles per instruction
$\text{Speedup} = \frac{\text{Pipeline depth}}{1 + \text{Pipeline stall cycles per instruction}}$

Execution time = IC x CPI x CCT

Exercise 1 (8 pts)

Consider an unpipelined processor P, with a 1 GHz clock, in which, memory operations require 5 cycles, ALU operations 4 cycles and branches 3 cycles. On average, 10% of the codes are branches, while 50% are ALU operations.

A) Compute the CPI of processor P.

CPI = 0.1 x 3 + 0.5 x 4 + 0.4 x 5 = 4.3 cycles.

B) If you are to choose between 2 compilers C1 and C2 where C1 produces the percentages above while C2 produces a code shorter than C1 by 2% but with 10% more memory operations same number of branches as C1. Which one would you choose and why?
C1-CPI = 4.3
C2-CPI = 44% x 5 + 10% x 3 + 46% x 4 = 4.34

Exec 1 = IC1 x 4.3 x CCT
Exec 2 = 0.98 x IC1 x 4.34 x CCT = 4.25 x IC1 x CCT
Compiler 2 is better.

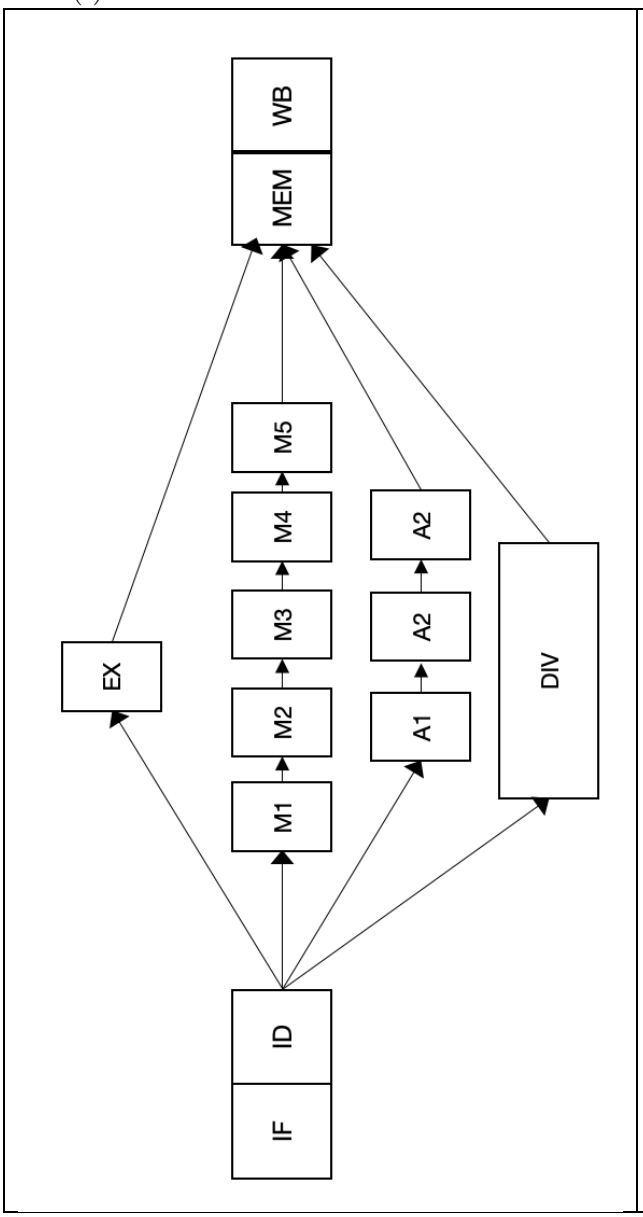
C) Using part (A), assume we pipeline processor P into 7 balanced stages. Due to pipelining, data stalls and structural stalls were found to be one every 3 instructions, and 2 every 11 instructions respectively. A dynamic branch prediction is employed with 95% accuracy. Branches penalty is 2 cycles. Compute the speedup and show your work.

Speedup = 7 / (1 + 1/3 + 2/11 + 0.1 x 0.05 x 2) = 4.58

Exercise 2 (12 pts)

Consider this modified version of the floating MIPS where the multiplier is pipelined into 5 stages, the floating point adder into 3, and the divider is not pipelined but needs 6 cycles to finish. Forwarding is applied everywhere. Register file can write and read in the same cycle. No extra hardware is present.

Fill in the timing diagram up to cycle 20, if needed. For stall cycles, leave cell empty or place a dash (-)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
L.D F1, 6(R2)																				
MUL.D F2, F1, F1																				
MUL.D F3, F4, F5																				
DIV.D F6, F2, F3																				
S.D F6, 6(R2)																				

SOLUTION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
L.D F1, 6(R2)	F	D	X	M	W															
MUL.D F2, F1, F1		F	D		M1	M2	M3	M4	M5	M	W									
MUL.D F3, F4, F5			F		D	M1	M2	M3	M4	M5	M	W								
DIV.D F6, F2, F3					F	D					DIV	DIV	DIV	DIV	DIV	DIV	M	W		
S.D F6, 6(R2)						F					D	X						M	W	