Experiment 4
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Aim

To study the PN junction diode as Clampers, Peak to Peak detectors and Voltage multipliers.

Results

Positive clamper circuit

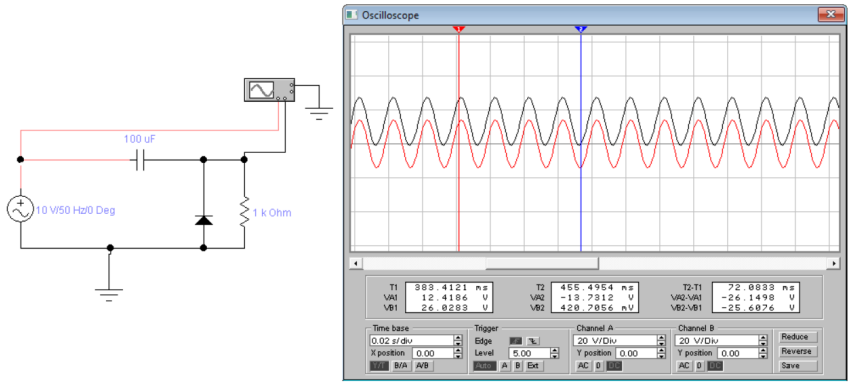


Figure 1: Positive clamper circuit

The circuit shifts the AC signal to a positive a positive DC level without changing the waveform. In the negative half cycle, the capacitor is charged to the peak negative value and the diode is forward biased. In the positive half cycle, the capacitor is charged to the positive peak value as the ideal diode is reverse biased and therefore an open circuit.

Positive clamper with positive reference voltage

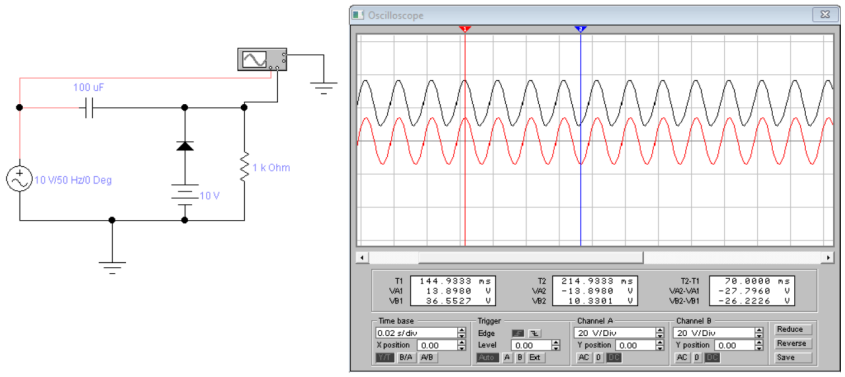


Figure 2: Positive clamper with positive reference voltage

This also works the same way as above, the positive reference voltage sums up with the output to raise the clamped level and shift the output by $V_p + V_r$

Positive clamper with negative reference voltage

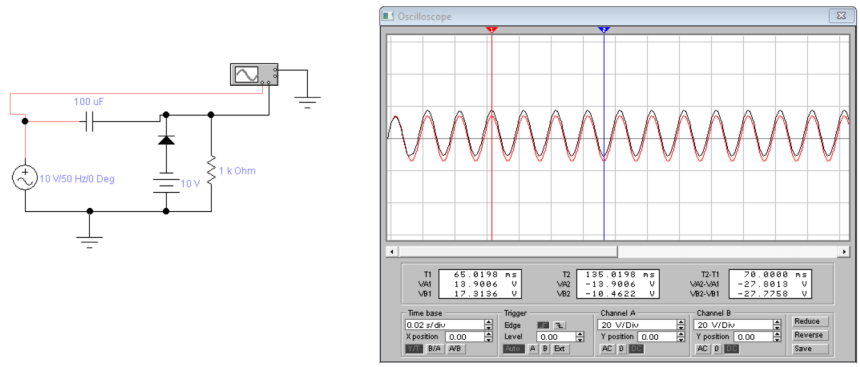


Figure 3: Positive clamper with negative reference voltage

This also works the same as above, the negative reference sums up with the output to lower the clamped level and shift the output by $V_p - V_r$

Negative clamper circuit

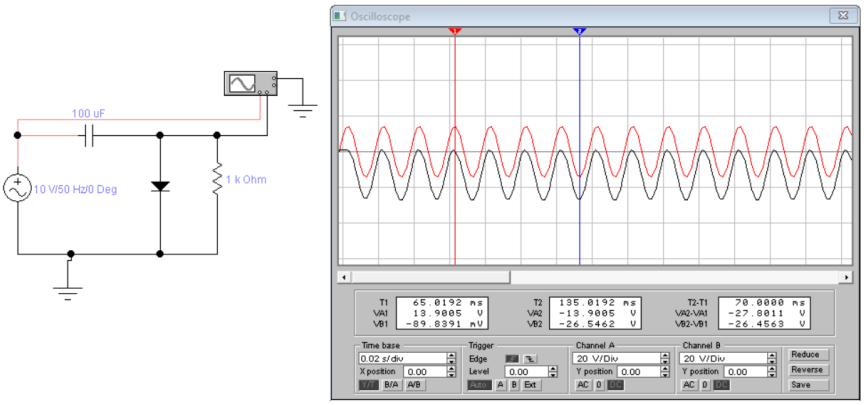


Figure 4: Negative clamper circuit

The circuit shifts the AC signal to the negative DC level without changing the waveform.
During the positive half cycle, the diode is forward biased and the capacitor is charged to its positive peak value. In the negative half cycle, the diode is reverse biased and therefore open circuited leading to the capacitor getting charged to the negative value of V_p.

Negative clamper with positive reference voltage

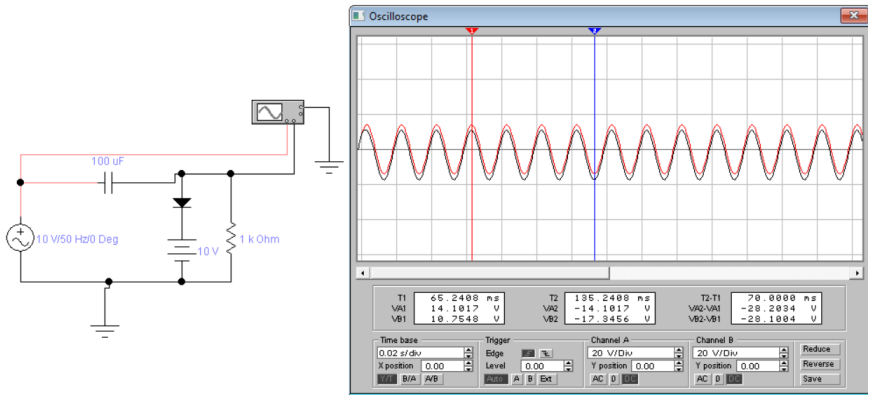


Figure 5: Negative clamper with positive reference voltage

This circuit works the same as above. The reference voltage adds to the negative of the clamped voltage (V_p), shifting the output to the negative side. ($V_p - V_r$)

Negative clamper with negative reference voltage

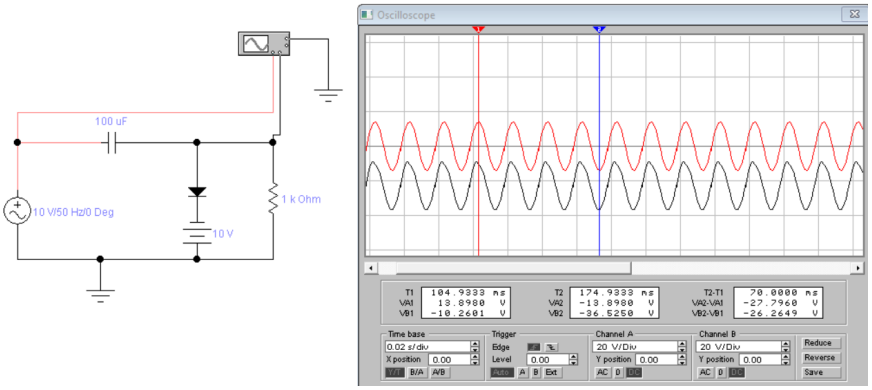
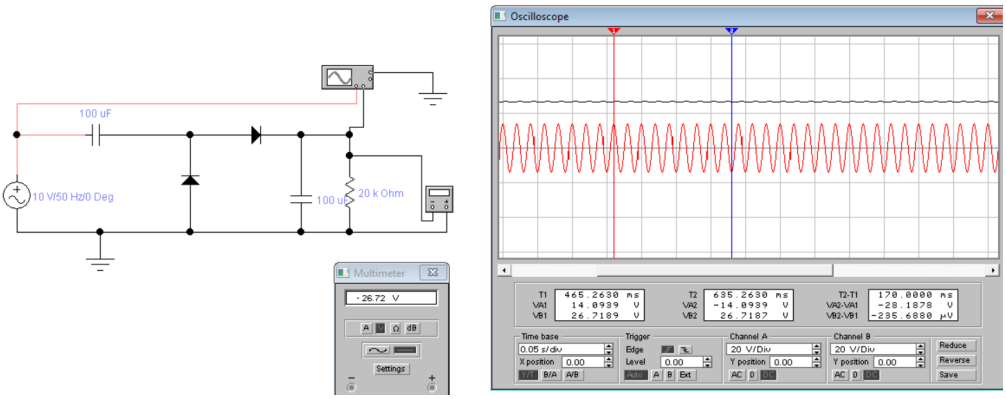


Figure 6: Negative clamper with negative reference voltage

This circuit also works the same as above. The negative reference voltage sums up with the negative output to raise the clamped level and shift the output to the negative side by $V_p + v_r$

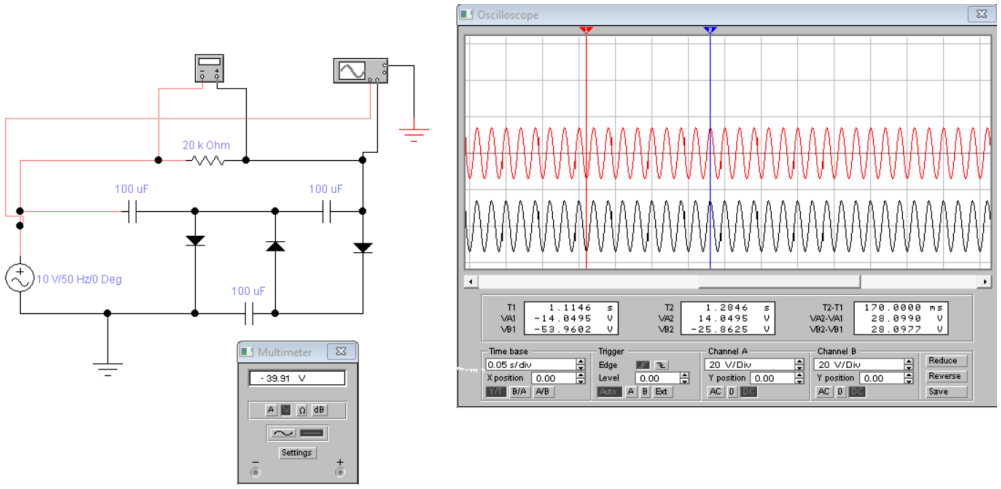
Clamper combination circuit 7 (Connect a load resistance of $R = 20k\Omega$ across the output)



This is a half-wave voltage doubler circuit. It gives a DC output which is twice the input.
During the negative half cycle, the first diode is forward biased charging up the first capacitor to its peak value. This capacitor remains fully charged. The second diode via the first diode charged up the second capacitor.

During the positive half cycle, the first diode is reverse biased which blocks the discharging of the first cap. while the second capacitor charges up as the second diode is forward biased. The second cap. charges to twice the peak and when it discharges, gives back twice the input.

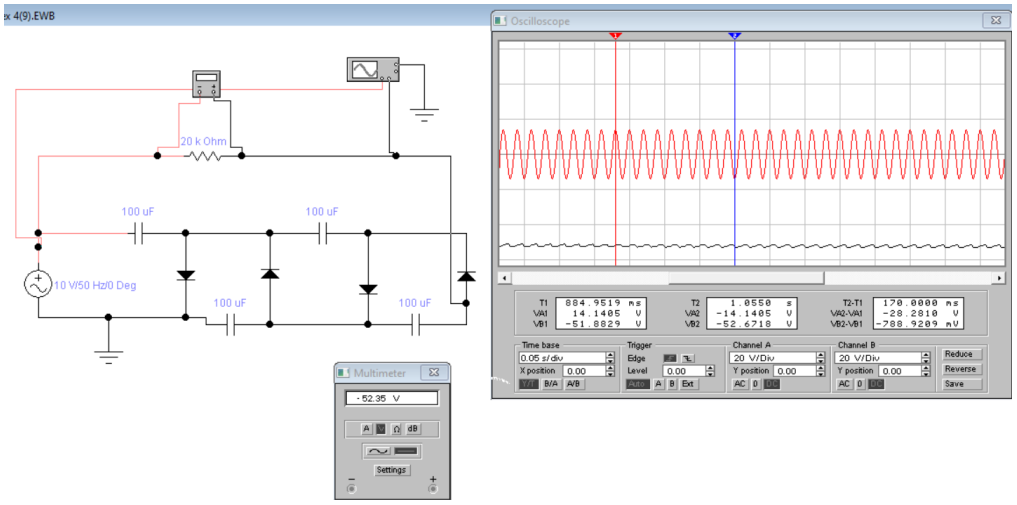
Clamper combination circuit 8 (Connect a load resistance of $R = 20k\Omega$ across the output)



This is a voltage tripler circuit.
During the negative half cycle, the first diode is reverse biased blocking the first capacitor, the second is forward biased charging the second capacitor, the third is reverse biased charging the third capacitor via the second diode.

Then during the positive half cycle, the first diode is forward biased and charges the first capacitor to V_p. The second diode is reverse biased blocking the discharging of the second capacitor which is at V_p. The third diode is forward biased charging the third capacitor by another V_p to $2V_p$.
When the first and third capacitors discharge through the resistor, the output is $3V_p$.

Clamper combination circuit 9 (Connect a load resistance of $R = 20k\Omega$ across the output)



The circuit is a voltage quadrupler, Its just two voltage doubler circuits connected side by side.