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0200CST202042503

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R,S) (FT/WP) / (S2 PT) Exam April 2025 (2019 Scheme)

Course Code: CST 202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		Differentiate between One-address, Two-address, and Three-address Instructions with examples	3
2		Describe the role of the following special purpose registers: 1. MAR 2. PC 3. IR	3
3		What will be the output when the binary value 11100111 undergoes 1. Circular right shift 2. Logical right shift	3
4		List and briefly explain the different types of arithmetic micro-operations.	3
5		Design 3 X 2 array multiplier and label it.	3
6		How does a pipelined processor differ in terms of speed and efficiency from a non-pipelined processor? Quantify the difference between the two for a task with n instructions and a pipelined processor with k stages.	3
7		A microprogrammed control unit offers flexibility. Justify this statement.	3
8		Describe the 'one flip-flop per state' method of control organization.	3
9		Under what circumstances are ROMs used to store data? Differentiate between EPROM and EEPROM.	3
10		Why dynamic RAMs need constant refreshing? Draw the structure of a DRAM cell and explain.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Illustrate the single bus organization of processor unit with the help of suitable diagrams.	9
	b)	Write the control sequence (micro-operations) to execute the instruction LOAD 10(R2),R1.	5
12	a)	Draw and explain the internal architecture of a basic CPU and illustrate how data	8

flows from memory to the ALU during execution and the role of the different registers in this.

b) Evaluate the importance of each condition code in the design of instruction sets for decision making in processors. 6

Module -2

13 a) What is a scratchpad memory? Draw the block diagram of a processor employing scratchpad memory. 6

b) Give example of an arithmetic/logic operation that will cause the following scenarios: 8

1. The carry flag will be set.
2. The zero flag will be set.
3. The overflow flag will be set.
4. The sign flag will be set.

14 a) Design an adder circuit with one selection variable, S and two inputs A and B. The circuit operates as given below. 8

S	Y (Output)
0	A + B
1	A + B′ + 1

b) With a neat diagram, describe the structure and working principle of a 4-bit combinational shifter. 6

Module -3

15 a) Illustrate the working of the restoring division method with an example. Draw the flowchart and explain how the algorithm handles division step by step. 10

b) Differentiate between instruction and arithmetic pipelines. 4

16 a) Describe in detail about structural, control and data hazards in pipelined processors. Give any one method to overcome this. 7

b) In what way does Booth's algorithm reduce the number of operations in signed binary multiplication? Explain the logic behind its working with an example. 7

Module -4

17 a) Illustrate the working of a micro program sequencer with the help of a diagram. 10

b) Compare instruction formats of horizontal and vertical microinstructions in terms of its organisation, memory and speed. 4

18 a) Given the state transition diagram of a control unit, explain the different ways to 10

implement a hardwired control unit from the state diagram.

b) Define and differentiate the following terms: Control Word, Micro Routine, Micro Program, Micro Instruction. 4

Module -5

19 a) Define interrupts and illustrate the sequence of actions that occur in a processor when an interrupt is triggered. 7

b) Illustrate the concept of DRAM and compare its two main types, highlighting the key differences between them. 7

20 a) Outline the implementation of Direct Memory Access (DMA). Differentiate between cycle stealing DMA and burst mode DMA, providing their advantages and disadvantages. 5

b) Illustrate direct, associative and set associative cache mapping techniques and compare them in terms of speed of access and miss rate. 9

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