SUMMER TRAINING IN VLSI AND MICROELECTRONICS

JADAVPUR UNIVERSITY

Targets

1. Learn the implementation of Digital Electronic components using Verilog and test them
2. Learn Verilog , its usage , different data types, keeywords for proper ability to code in Verilog HDL
3. Understand the shortcomings of Verilog and hence understand the basics of System Verilog, some of their unique operators.
4. Learn and understand the Synopsys tools and use them for Design Abstraction

Lab Tasks

1. Run the verilog codes in different modeling styles for Half Adder in Synplify_Pro and view waveform using Verdi.
2. Code for Half Subtractor and do the same.
3. Run the verilog codes in different modeling styles for Full Adder in Synplify_Pro and view waveform using Verdi.
4. Code for Full Subtractor and do the same.
5. Run the verilog codes in different modeling styles for 16 bit Ripple Carry Adder in Synplify_Pro and view waveform using Verdi.
6. Run the verilog codes in different modeling styles for D Flip Flop in Synplify_Pro and view waveform using Verdi.

Assignment

Design a 32 bit Ripple Carry Adder Subtractor using 4bit Adder Subtractor blocks. Write the testbench for checking results. Check using random values. Provide a small analysis based report (PHYSICAL COPY) comparing Resource Usage, Timing Diagram, etc. with a 32 bit Full Adder. There must remain a control bit in top level module controlling the unit’s operation(addition or subtraction) externally.

Further Practice (Not for Assesment)

1. Run codes for Universal Shift Register, Asynchronous and Synchronous Counters and understand their operations.
2. It is sectioned separately as Further Practices.

Resources

1. Iverilog https://steveicarus.github.io/iverilog/ Best for Linux based systems. You can also use in Windows. Very light.
2. AMD Vivado https://www.xilinx.com/support/download.html Best among freeware Very bulky
3. ModelSIM https://www.intel.com/content/www/us/en/software-kit/750368/modelsim-intel-fpgas-standard-edition-software-version-18-1.html KInda in between both. Easy learning curve