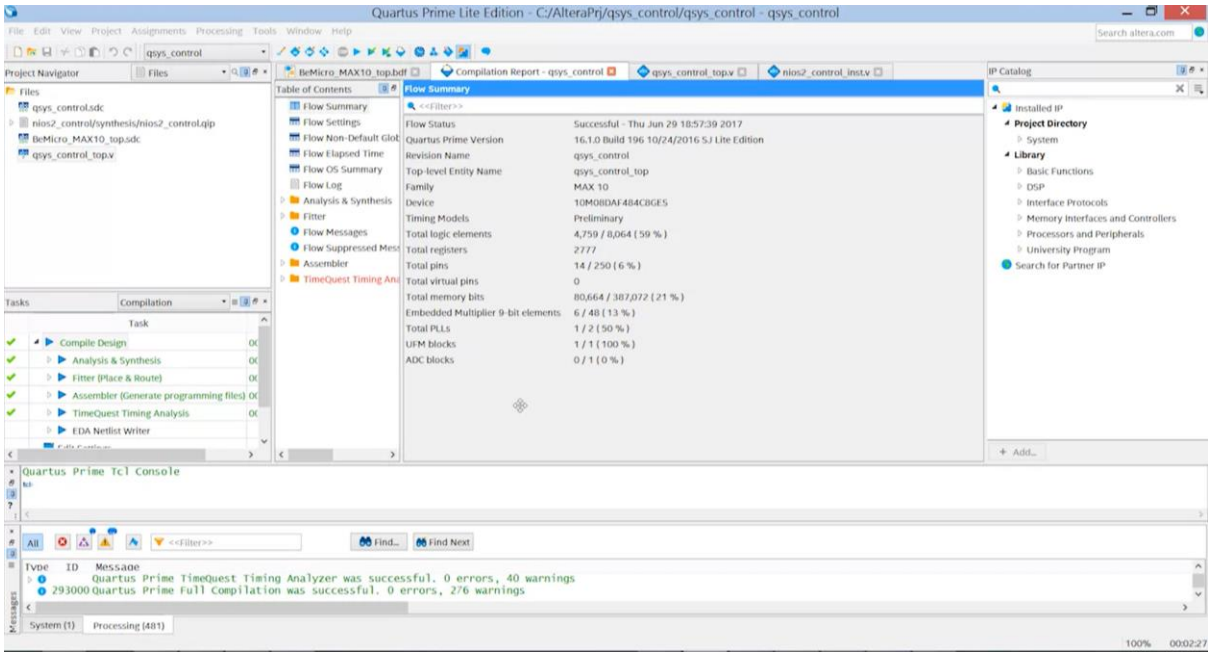
Quartus Prime Lite Edition - C:/AlteraPrj/qsys_control/qsys_control - qsys_control
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
qsys_control
Project Navigator
Files
qsys_control.sdc
nios2_control/synthesis/nios2_control.qip
BeMicro_MAX10_top.sdc
qsys_control_top.v
BeMicro_MAX10_top.bdf
Compilation Report - qsys_control
qsys_control_top.v
nios2_control_inst.v
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Glob
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Flow Messages
Flow Suppressed Mess
Assembler
TimeQuest Timing Ana
Flow Summary
<<Filter>>
Flow Status Successful - Thu Jun 29 18:57:39 2017
Quartus Prime Version 16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name qsys_control
Top-level Entity Name qsys_control_top
Family MAX 10
Device 10M08DAF484CBGES
Timing Models Preliminary
Total logic elements 4,759 / 8,064 (59 %)
Total registers 2777
Total pins 14 / 250 (6 %)
Total virtual pins 0
Total memory bits 80,664 / 387,072 (21 %)
Embedded Multiplier 9-bit elements 6 / 48 (13 %)
Total PLLs 1 / 2 (50 %)
UFM blocks 1 / 1 (100 %)
ADC blocks 0 / 1 (0 %)
IP Catalog
Installed IP
Project Directory
System
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
+ Add...
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Quartus Prime Tcl Console
All
<<Filter>>
Find...
Find Next
Type ID Message
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 40 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 276 warnings
Messages
System (1)
Processing (481)
100%
00:02:27