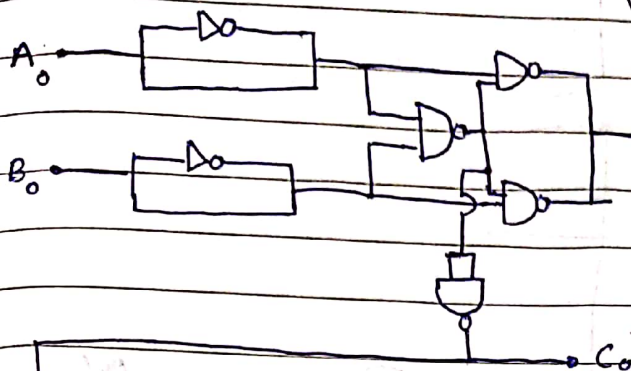


# COURSERA - INTRODUCTION TO FPGA

## (1) 2 Bit Full Adder



2bit  
Half-  
Adder

2bit  
Full-  
Adder

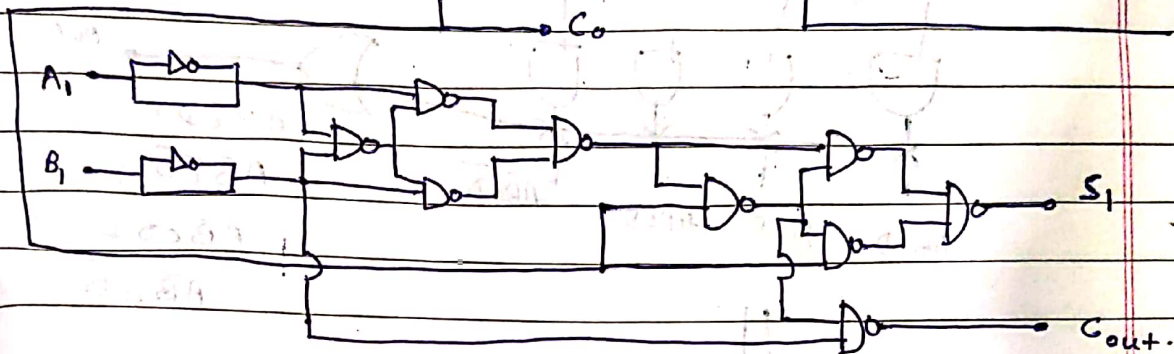
### BOOLEAN EXPRESSION

$$(1) (\bar{A}_0 B_0) + (A_0 \bar{B}_0) = S_0$$

$$(2) A_0 B_0 = C_0$$

$$(3) (\bar{A}_1 B_1 + A_1 \bar{B}_1) \text{ XOR } C_0 = S_1$$

$$(4) A_1 B_1 + C_0 (A_1 + B_1) = C_{out}$$



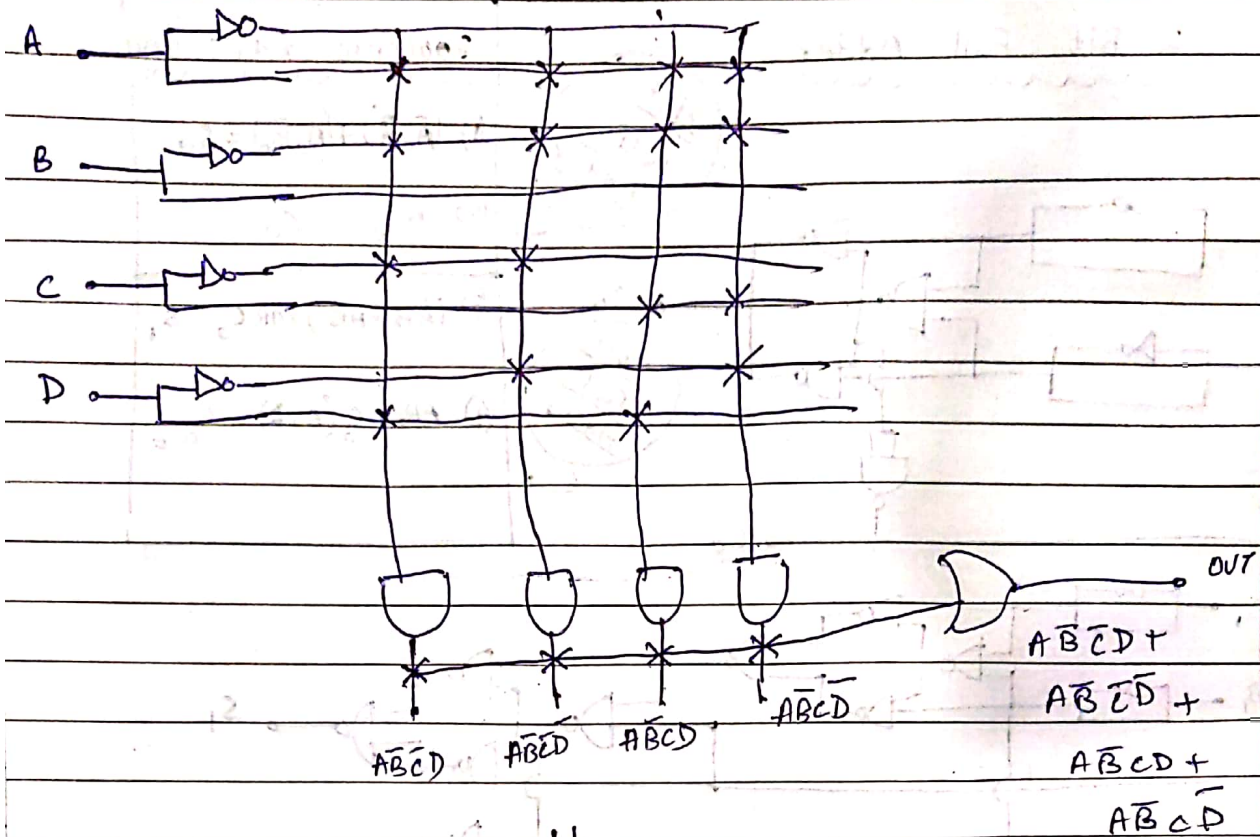
## (2) (A AND NOT(B)) OR (C AND NOT(D))

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D}$$

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D}$$

# of prog. AND gate = # of min terms = 4



CORRECT DIAGRAM =

