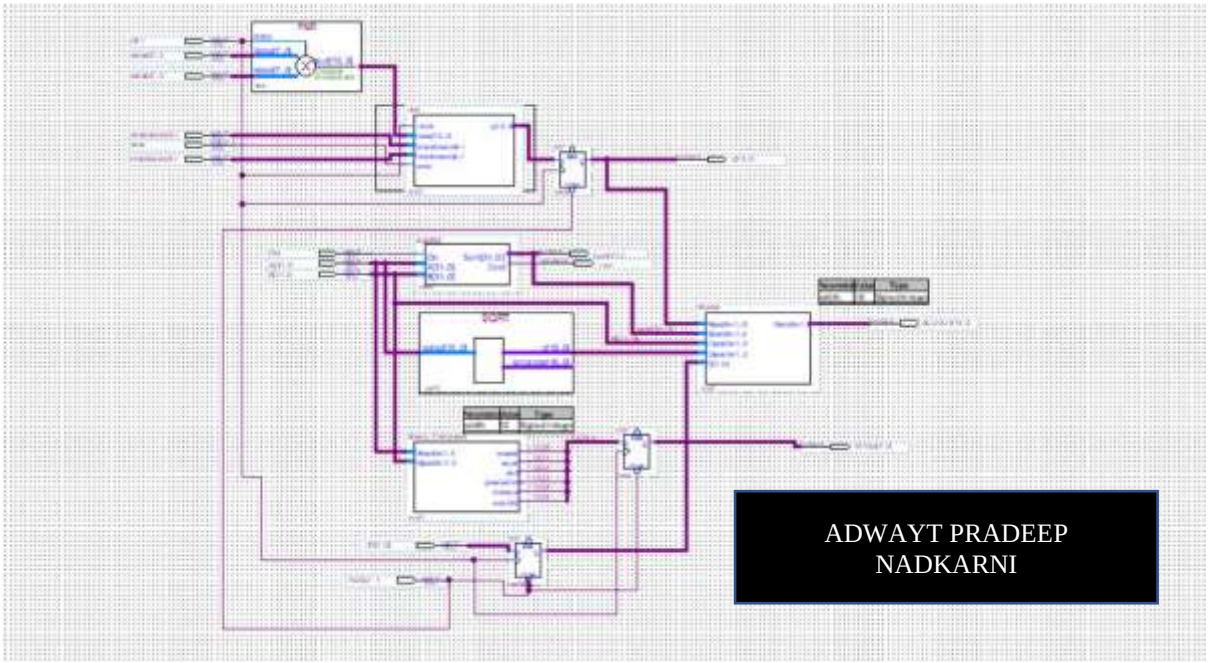
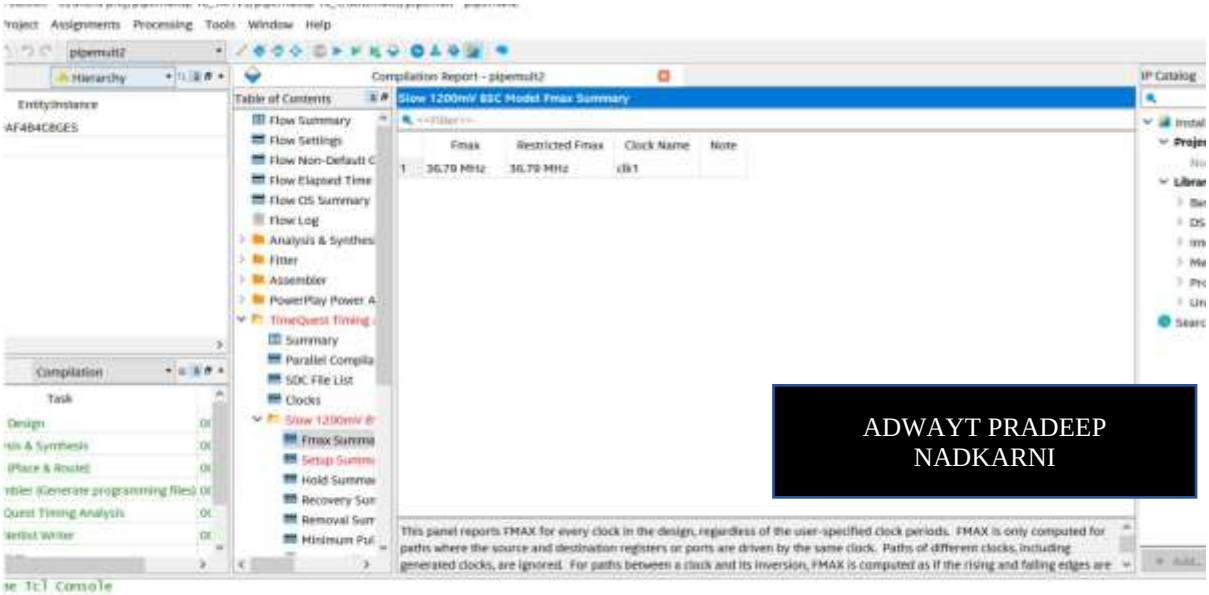
QUESTIONS

The goal of this assignment is to extend your knowledge of schematic design using Quartus Prime by using pipelining and IP blocks to improve design performance. The student should be following the video instructions and creating the example as they go along. Their progress is checked at milestones by presenting screenshots which are matched to the solution screenshots to verify their work. Milestones checked are design schematic creation, timing improvement with pipelining, pin assignment, timing analysis and simulation.

This assignment is required. Peers must review 3 submissions to pass the
assignment.

SOLUTIONS:




Project Assignments Processing Tools Window Help
Compilation Report - pipemult2
Slow 1200mV 85C Model Fmax Summary
Fmax
Restricted Fmax
Clock Name
Note
36.79 MHz
36.79 MHz
clk1
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are
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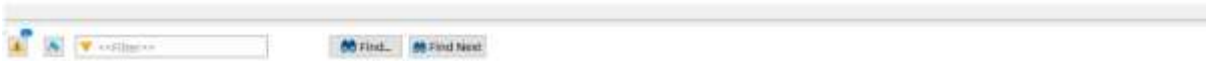
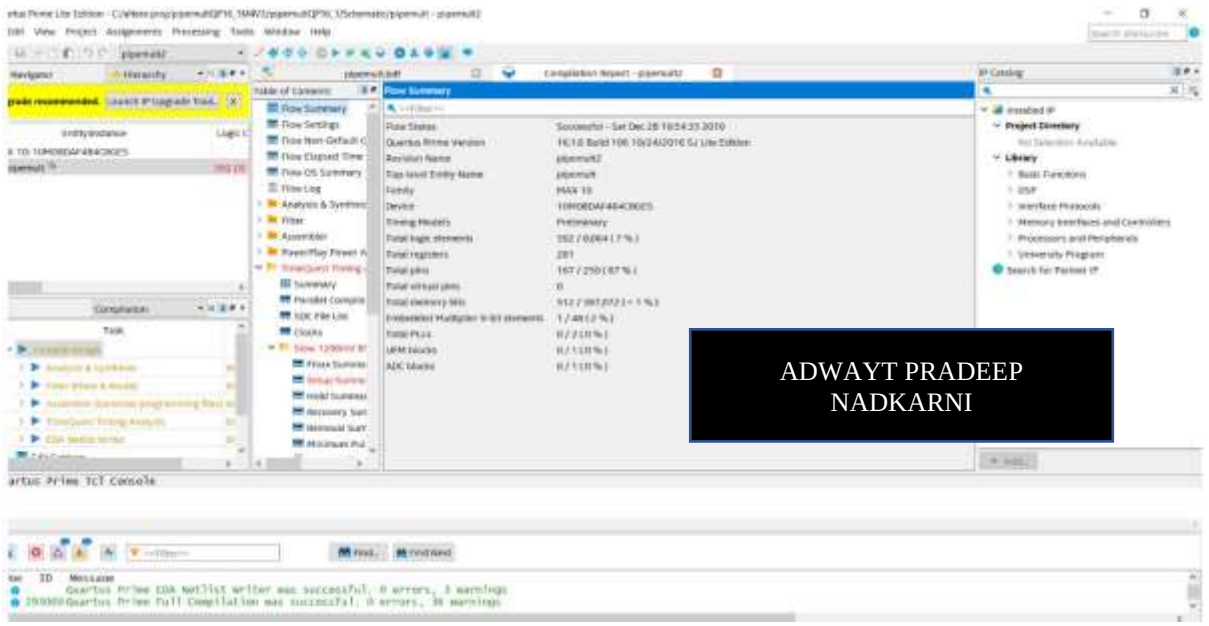

Find...
Find Next


Flow Summary
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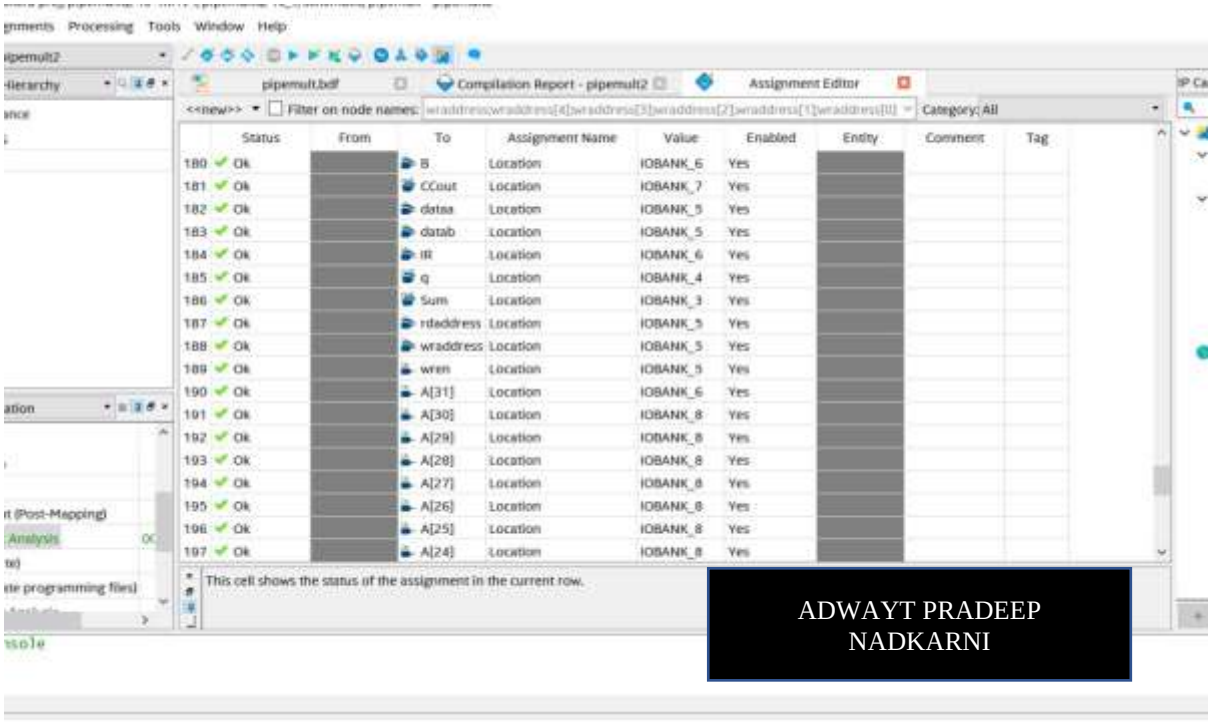
Find...
Find Next


Processing Tools Window Help
pipemult.bdf
Compilation Report - pipemult2
Assignment Editor
Filter on node names:
Category: All
Status From To Assignment Name Value Enabled Entity Comment Tag
180 Ok B Location IOBANK_6 Yes
181 Ok CCout Location IOBANK_7 Yes
182 Ok dataa Location IOBANK_5 Yes
183 Ok datab Location IOBANK_5 Yes
184 Ok IR Location IOBANK_6 Yes
185 Ok q Location IOBANK_4 Yes
186 Ok Sum Location IOBANK_3 Yes
187 Ok rdaddress Location IOBANK_5 Yes
188 Ok wraddress Location IOBANK_5 Yes
189 Ok wren Location IOBANK_5 Yes
190 Ok A[31] Location IOBANK_6 Yes
191 Ok A[30] Location IOBANK_8 Yes
192 Ok A[29] Location IOBANK_8 Yes
193 Ok A[28] Location IOBANK_8 Yes
194 Ok A[27] Location IOBANK_8 Yes
195 Ok A[26] Location IOBANK_8 Yes
196 Ok A[25] Location IOBANK_8 Yes
197 Ok A[24] Location IOBANK_8 Yes
This cell shows the status of the assignment in the current row.
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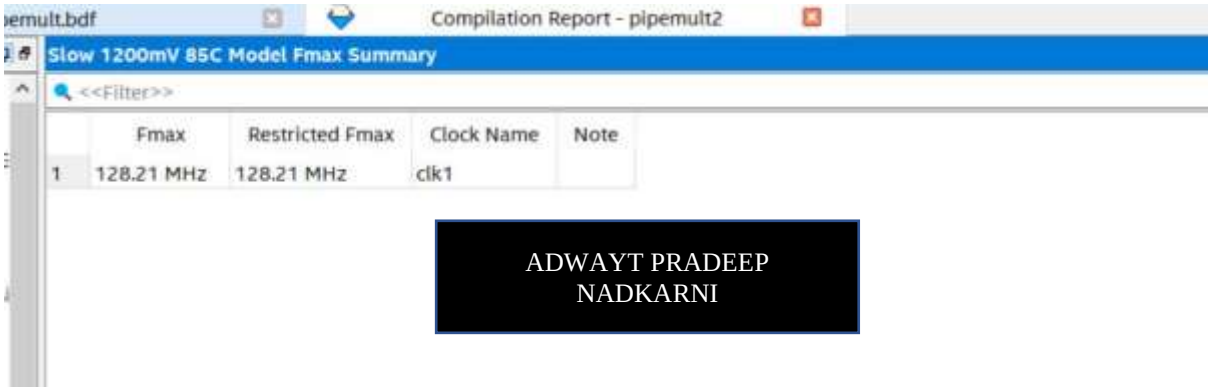
pipemult.bdf
Compilation Report - pipemult2
Slow 1200mV 85C Model Fmax Summary
<<Filter>>
Fmax Restricted Fmax Clock Name Note
1 128.21 MHz 128.21 MHz clk1
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