

# Altera CPLDs and Small FPGAs



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# Altera CPLDs and Small FPGAs

- ⇒ MAX V
- ⇒ MAX 10
- ⇒ Cyclone V



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In this video we will continue our survey of modern programmable logic devices, with CPLDs and Small FPGAs from Altera, including the MAX V, the MAX 10 and the Cyclone V.

## Programmable Logic Device Selection Criteria

1. Reprogrammability (Configuration Memory Type)
2. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
3. Cost per logic gate
4. Speed (Maximum clock frequency)
5. Power Consumption (static and dynamic)
6. Cost per I/O (I/O Density) and extent of supported I/O standards
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
10. Endurance (number of programming cycles and years of retention)
11. Design and Data Security



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The goal in programmable logic device selection is to pick the best fit part for our requirements. We will use the programmable logic device selection criteria we established earlier to evaluate these devices as listed here.

Feature	5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
LEs	40	80	160	240	570	1,270	2,210
Typical Equivalent Macrocells	32	64	128	192	440	980	1,700
User Flash Memory Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192	8,192
Global Clocks	4	4	4	4	4	4	4
Internal Oscillator	1	1	1	1	1	1	1
Maximum User I/O pins	54	79	79	114	159	271	271
$t_{PD1}$ (ns) (1)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
$f_{CNT}$ (MHz) (2)	152	152	152	152	152	304	304
$t_{SU}$ (ns)	2.3	2.3	2.3	2.3	2.2	1.2	1.2
$t_{CO}$ (ns)	6.5	6.5	6.5	6.5	6.7	4.6	4.6

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Here's a portion of the Altera MAX V CPLD family device handbook. The Altera MAX V has reprogrammable FLASH configuration and User memory, although the routing switches are based on SRAM. On power up, the device transfers the configuration memory in FLASH to the SRAM in about half a millisecond.

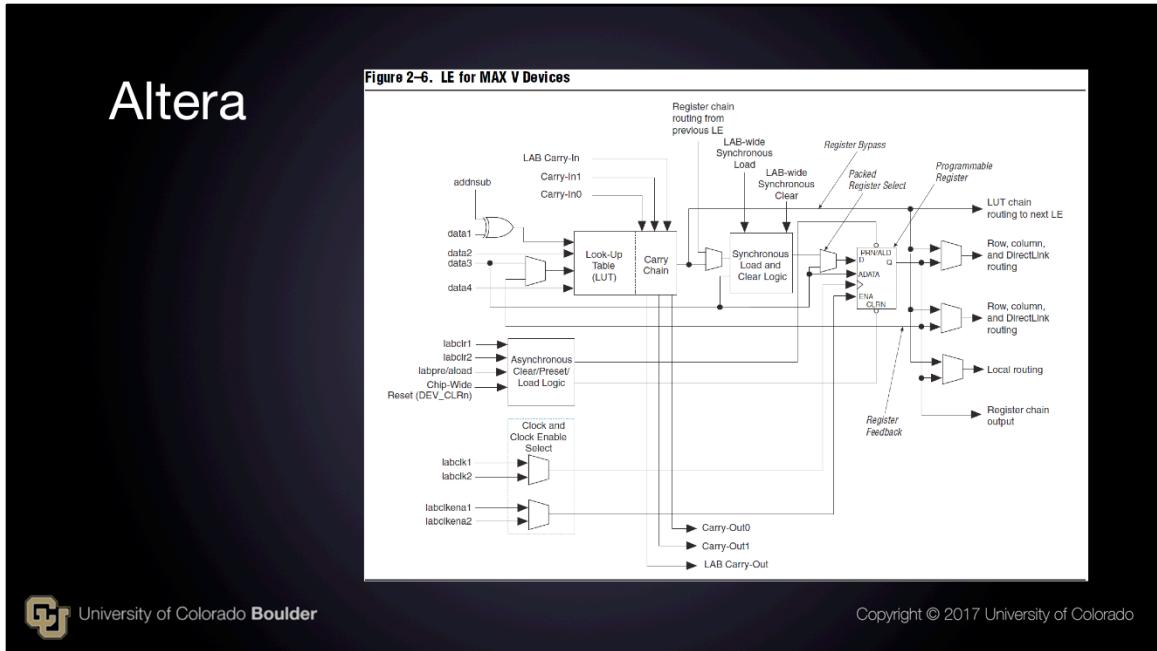
Note equivalent gates up to 2210 logic elements, more logic than the other CPLDs we have considered. [Annotate]

Speed is limited to 304 MHz on global clock buffers, which is about par with other CPLDs. [Annotate]

Maximum static power draw is between 0.09 and 2 mA depending on part size, so these are low power parts. Dynamic power is not specified, use the Power Play Analyzer tool to determine it.

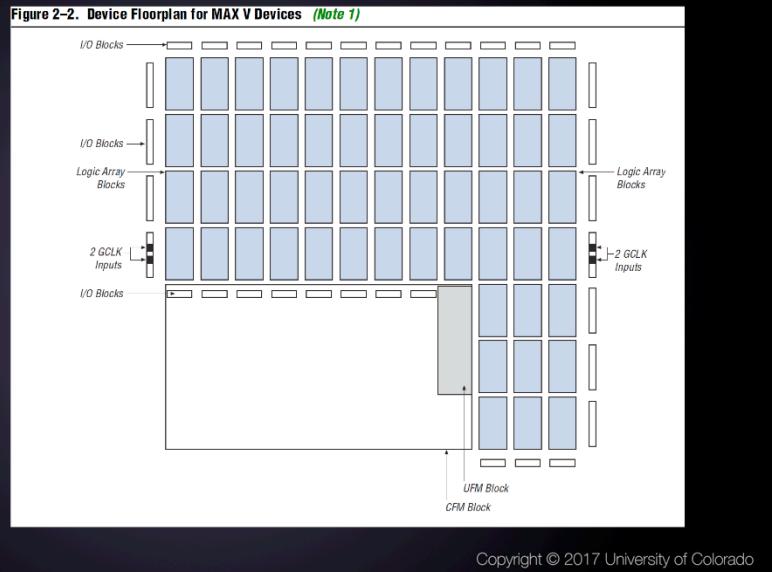
This device has up to 271 IO pins, a 8:1 ratio of logic cells to I/O. There are 9 supported I/O standards. [Annotate]

Data retention is not specified, 100 programming cycles endurance is minimal.



This is a picture of the MAX V logic element. It looks more like an FPGA logic element than a CPLD, as the heart of this LE is a 4-input LUT and Flip-flop. This is because the MAX V was designed as a “crossover” device between a CPLD and an FPGA. In reality it’s more like an FPGA than a CPLD.

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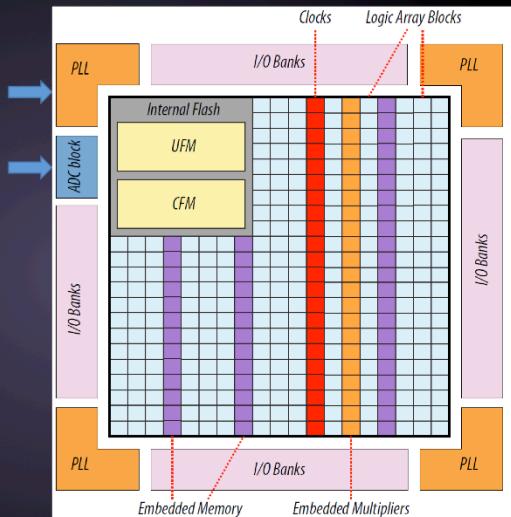
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This next picture shows the overall layout of the MAX V device, which is basically a sea of Logic Array Blocks (LABs) connected by row and column routing. Each LAB contains 10 logic elements.

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MAX10 Floorplan

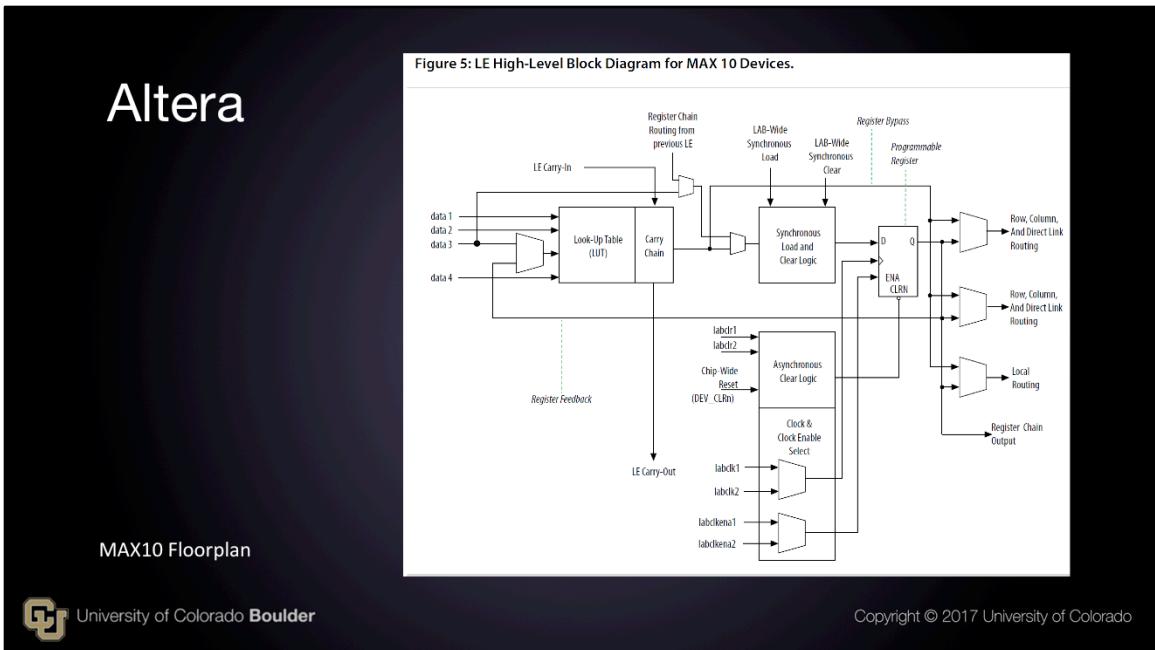


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Contrast the MAX V floorplan with this floorplan for the MAX 10. It looks more sophisticated, which it is, and better yet, it is in color. The MAX 10 is a more recent part, and consistent with the trend, includes more hard IP blocks, like the PLLs [Annotate] and an ADC [Annotate]. This is a mixed signal part, with both analog and digital functions on chip.

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Here is the logic element diagram for the MAX 10. It is almost identical to the MAX V LE, with 4-input LUT and flip-flop at the heart and some carry chains and mux signal selection. Even though the MAX family has been a CPLD family, Altera finally dropped all pretense with the MAX 10 and does call it an FPGA.

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**MAX 10 FPGAs Product Table**

Product Line	10M02	10M04	10M08	10M16	10M25	10M40	10M50
(E) I/O	2	4	8	16	25	40	50
Block memory (kB)	108	169	378	549	675	1,260	1,638
User flash memory <sup>1</sup> (kB)	12	16 - 156	32 - 172	32 - 296	32 - 400	64 - 736	64 - 736
18 x 18 multipliers	16	20	34	45	55	125	144
TMR <sup>2</sup>	1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
External configuration	Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC)	-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
Temperature sensing diode (TSD) <sup>3</sup>	-	-	-	-	-	-	-
External memory interface (EMI) <sup>4</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>
Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transceiver/Receiver							
V36 (D)	WLCP (3 mm, 0.8 mm pitch) WLCS (4 mm, 0.4 mm pitch)	C, 22, 3/7	-	-	-	-	-
V81 (D)	-	-	CA, 56, 7/17	-	-	-	-
F226 (D)	-	CA, 178, 13/54					
U324 (D)	UEGA (17 mm, 0.8 mm pitch)	CA, 162, 9/47	CA, 246, 15/81	CA, 246, 15/81	-	-	-
F484 (D)	FBGA (23 mm, 1.0 mm pitch)	-	CA, 256, 15/83	CA, 320, 2/116	CA, 360, 24/136	CA, 360, 24/136	CA, 360, 24/136
1672 (D)	FBGA (27 mm, 1.0 mm pitch)	-	-	-	-	CA, 500, 30/182	CA, 500, 30/182
E144 (S) <sup>6</sup>	EGFP (22 mm, 0.5 mm pitch)	C, 101, 7/27	CA, 101, 10/27	CA, 101, 10/27	CA, 101, 10/27	CA, 101, 10/28	CA, 101, 10/28
M132 (S)	MBGA (8 mm, 0.5 mm pitch) <sup>7</sup>	C, 112, 9/29	CA, 112, 9/29	-	-	-	-
U169 (S)	UEGA (11 mm, 0.8 mm pitch)	C, 130, 9/38	CA, 130, 9/38	CA, 130, 9/38	-	-	-



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Here is the logic element diagram for the MAX 10. It is almost identical to the MAX V LE, with 4-input LUT and flip-flop at the heart and some carry chains and mux signal selection. Even though the MAX family has been a CPLD family, Altera finally dropped all pretense with the MAX 10 and does call it an FPGA.

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Table 4: Maximum Resource Counts for Cyclone V E Devices

Resource	Member Code				
	A2	A4	A5	A7	A9
Logic Elements (LE) (K)	25	49	77	150	301
ALM	9,434	18,480	29,080	56,480	113,560
Register	37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860
	MLAB	196	303	424	836
Variable-precision DSP Block		25	66	150	156
18 x 18 Multiplier		50	132	300	312
PLL		4	4	6	7
					8



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Next let's look at the product table for the Cyclone V small FPGA.

The Altera MAX 10 has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

Notice there are up to 300,000 logic elements, a considerable amount for a small FPGA. [Annotate]

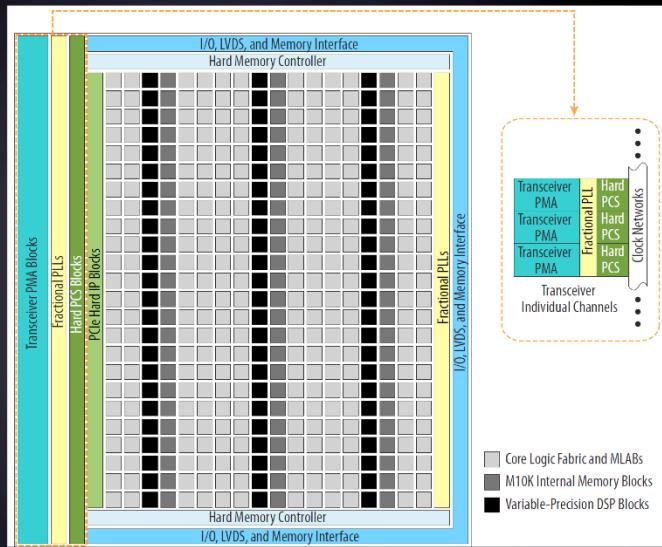
Speed is limited to 550 MHz on global clock buffers, very good for a small FPGA.

Power is not specified, use the Power Play Analyzer tool to determine it.

This device has up to 480 IO pins, a 600:1 ratio of logic cells to I/O. There are 34 supported I/O standards.

A number of hard IP blocks have been added, including Block memory [Annotate], Multipliers [Annotate], PLLs [Annotate], DSP blocks [Annotate], High Speed Transceivers and External Memory Interfaces.

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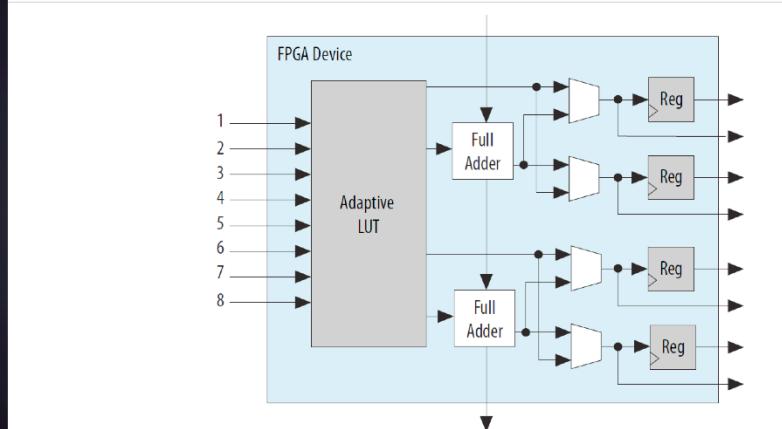


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This shows the layout of the overall Cyclone V, with the logic cells, RAM blocks, DSP blocks, PLLs, Transceiver, and Memory Interfaces.

Figure 8: ALM for Cyclone V Devices

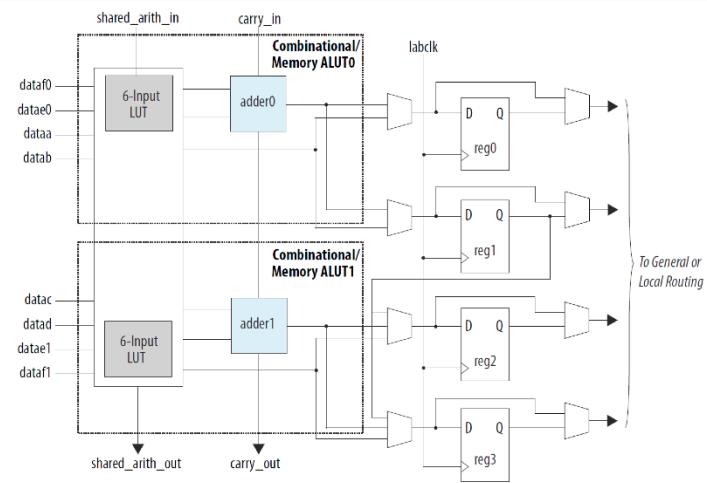
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The basic logic element for the Cyclone V is the Adaptive Logic Module or ALM. It consists of an 8-input adaptive LUT, 2 full adders, and 4 flip-flop registers. This register-rich logic element allows more design packing capability than previous generations. The LUT can also be configured as a  $32 \times 3$  dual port SRAM. The ALM can become a 3-input adder by combining the full adders with LUT arithmetic.

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Figure 1-5: ALM High-Level Block Diagram for Cyclone V Devices

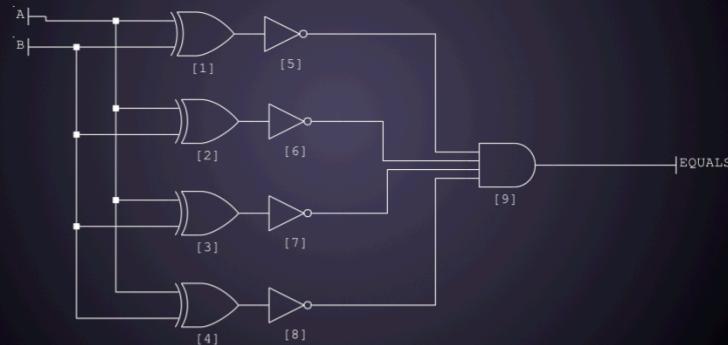


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This is a picture of the ALM in the normal mode.

## How large of a comparator can be made using a MAX 10 or Cyclone V Logic Cell?



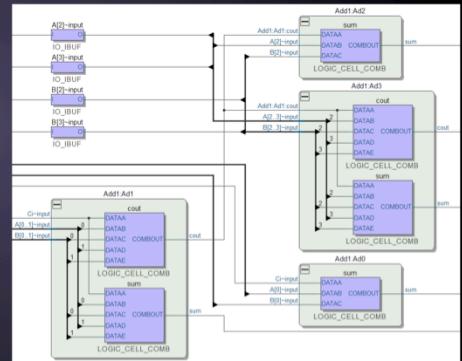
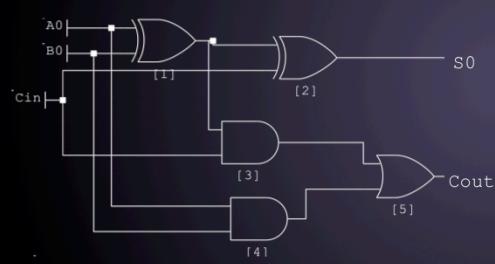
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Recall the 4-bit comparator.

How many comparator bits can be implemented in a LUT? In the MAX 10 case, there are only 4 inputs, so only a 2-bit comparator can be created. Larger comparators require that the LUTs be cascaded. Although the logic is efficiently used, there is added delay relative to the CPLD implementation. In the Cyclone V case, the 6 independent input LUT will handle 3 bits of comparator, so wider comparators can be made with less delay.

## How many full adders can be created in a MAX 10 or Cyclone V logic cell?



How many full adders can be made in a logic cell? For the MAX10 each LUT can create one full 1-bit adder because of the addition of the carry chain logic. 1 LE = 1 bit adder. However, from a previous video we used 3 Cyclone ALMs to implement a 4-bit adder, so each ALM creates about 1.33 adders.

## Altera CPLDs and Small FPGAs Summary

- ⇒ Altera offers the MAX V CPLD and MAX 10 and Cyclone V FPGA families for smaller logic designs.
- ⇒ The MAX V and MAX 10 are single chip solutions with more I/O combined with reasonable logic density and efficient 4-input LUT logic cells.
- ⇒ The MAX 10 adds analog signal processing via an on-chip ADC.
- ⇒ The Cyclone V is a good entry level FPGA with good speed and logic density combined with a considerable amount of hard IP blocks, including Block memory, PLLs, Multipliers and DSP blocks, High Speed Transceivers and External Memory Interfaces.



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In this video we have learned

- Altera offers the MAX V CPLD and MAX 10 and Cyclone V FPGA families for smaller logic designs.
- The MAX V and MAX 10 are single chip solutions with more I/O combined with reasonable logic density and efficient 4-input LUT logic cells.
- The MAX 10 adds analog signal processing via an on-chip ADC.
- The Cyclone V is a good entry level FPGA with good speed and logic density combined with a considerable amount of hard IP blocks, including Block memory, PLLs, Multipliers and DSP blocks, High Speed Transceivers and External Memory Interfaces.