

Compile a Design with Quartus Prime



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≡ In this presentation, you will compile an FPGA design in Quartus Prime.



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In this presentation, you will compile an FPGA design in Quartus Prime.

Design files are provided so that you can follow along and perform each step along the way.

Feel free to pause the video as you enter commands into Quartus Prime.

Agenda for this Video

1. How to specify compiler settings to get the results you want
2. How to run full compilation
3. How to analyze compilation results
4. How to create a design revision
5. How to archive a project



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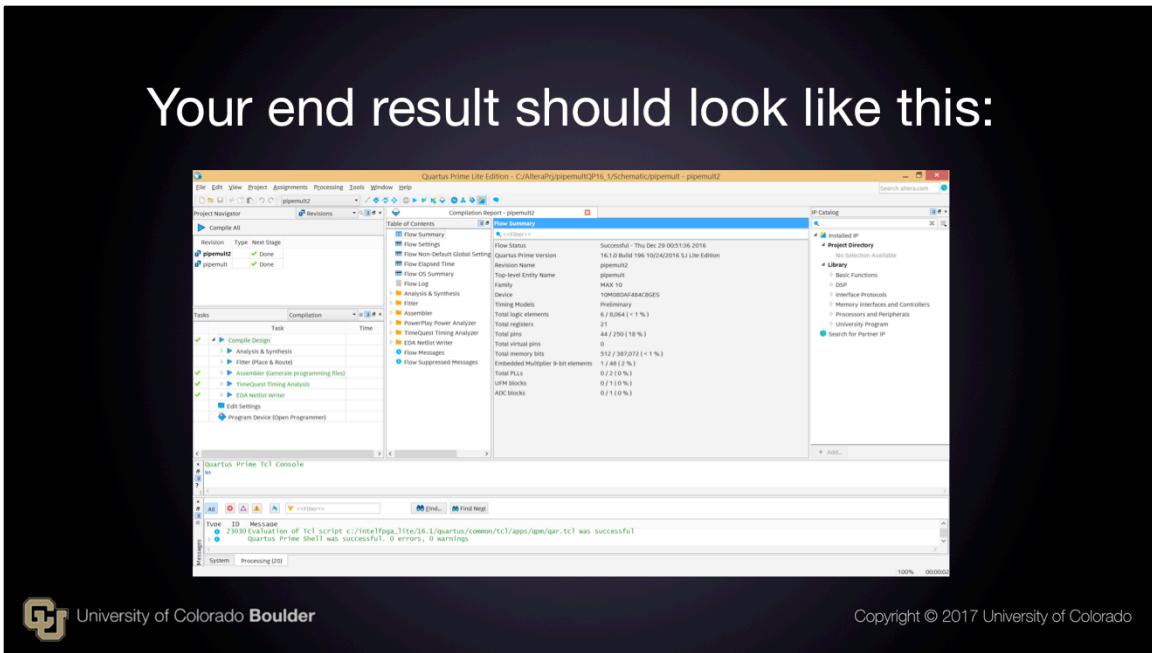
The Quartus Prime compiler is a set of software modules that:

- =D- Performs synthesis , fitting, assembly, and analysis
- =D- Generates programming output files
- =D- Runs modules together or independently
- =D- Optimizes results through compiler settings
- =D- Generates reports for analysis

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Your end result should look like this:



You end result should look something like this.

In this video, you have learned:

- ⇒ How to specify compiler settings to get the results you want
- ⇒ How to run full compilation
- ⇒ How to analyze compilation results
- ⇒ How to create a design revision
- ⇒ How to archive a project



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In this video, you have learned:

1. The various ways design entry can be performed for FPGAs
2. How to select and configure an IP core multiplier
3. How to create schematic symbols from HDL source files
4. How to create a schematic of logic and IP blocks for FPGA implementation