

Xilinx Large FPGAs



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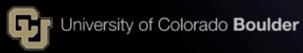
We will use the programmable logic device selection criteria we established earlier to evaluate these devices.

To reiterate, there are 11 criteria:

1. Reprogrammability (Configuration Memory Type)
2. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
3. Cost per logic gate
4. Speed (Maximum clock frequency)
5. Power Consumption (static and dynamic)
6. Cost per I/O (I/O Density)
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
10. Endurance (number of programming cycles and years of retention)
11. Design and Data Security

Xilinx Large FPGAs

- =D- Artix-7 FPGA Family
- =D- Kintex-7 FPGA Family
- =D- Virtex-7 FPGA Family
- =D- Kintex-Ultrascale FPGA Family
- =D- Virtex-Ultrascale FPGA Family



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In this video we will continue our survey of modern programmable logic devices, with Large FPGAs from Xilinx, including the Artix 7, Kintex 7, and Virtex 7; and the Kintex and Virtex Ultrascale device families.

Programmable Logic Device Selection Criteria

1. Reprogrammability (Configuration Memory Type)
2. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
3. Cost per logic gate
4. Speed (Maximum clock frequency)
5. Power Consumption (static and dynamic)
6. Cost per I/O (I/O Density) and extent of supported I/O standards
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
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The screenshot shows a portion of the Xilinx Artix-7 product selection guide. At the top, the Xilinx logo is displayed. Below it is a table comparing Artix-7 FPGAs across various models: XC7A12T, XC7A15T, XC7A25T, XC7A35T, XC7A50T, XC7A75T, XC7A100T, and XC7A200T. The table includes sections for Logic Resources (Logic Cells, Slices, CLB Flip-Flops), Memory Resources (Maximum Distributed RAM, Block RAM/FIFO), Clock Resources (CMTs, Maximum Single-Ended I/O, Maximum Differential I/O Pairs), I/O Resources (DSP Slices, PCIe® Gen2®, Analog Mixed Signal (AMS) / XADC), Embedded Hard IP Resources (Configuration AES / HMAC Blocks, GTP Transceivers (6.6 Gb/s Max Rate)), and Speed Grades (Commercial, Extended, Industrial). Red arrows point to specific columns in the table.

Artix®-7 FPGAs									
Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)									
	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (kb)	171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 kb each)	20	25	45	50	75	105	135	365
	Total Block RAM (kb)	720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs	72	120	72	120	120	144	144	240
	DSP Slices	40	45	80	90	120	180	240	740
Embedded Hard IP Resources	PCIe® Gen2®	1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate) ^[2]	2	4	4	4	4	8	8	16
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3							
	Industrial	-1, -2, -1L							

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Here's a portion of the Xilinx 7-series product selection guide providing an overview of the Artix-7 midrange FPGA. At this stage of development the FPGA selection process has become so bewildering that the vendors are producing selection guides in addition to datasheets and user's guides.

The Artix-7 has reprogrammable SRAM configuration which requires an external nonvolatile memory, usually a FLASH memory, to load the configuration at power up. The delay before the device becomes active is several milliseconds.

The size of these devices goes to 215,000 logic cells. [Annotate] This is sufficient to build a large 32-bit CPU on the FPGA.

Speed is limited to 628 MHz on clock buffers and a 1412 MHz toggle frequency, which is much faster than previous devices. Transceivers now run to 6.6 Gbps.

Maximum static power draw is between 48 and 328 mA at 1 volt depending on part size. Dynamic power is not specified, power estimation tools are used to determine this now.

This device has up to 500 IO pins, a 400:1 ratio of logic cells to I/O. [Annotate] There

The table is titled "Kintex-7 FPGAs" and is "Optimized for Best Price-Performance (1.0V, 0.95V, 0.9V)". It compares seven Xilinx Kintex-7 parts: XC7K70T, XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, and XC7K480T. The table includes columns for Part Number, EasyPath™ Cost Reduction Solutions⁽²⁾, Slices, Logic Cells, CLB Flip-Flops, Maximum Distributed RAM (Kb), Block RAM/FIFO w/ ECC (36 Kb each), Total Block RAM (Kb), CMOS (1 MMCM + 1 PLL), Maximum Single-Ended I/O, Maximum Differential I/O Pairs, DSP48 Slices, PCIe® Gen2⁽³⁾, Analog Mixed Signal (AMS) / XADC, Configuration AES / HMAC Blocks, and GTX Transceivers (12.5 Gb/s Max Rate). Red arrows point to the Total Block RAM (Kb) column for XC7K480T, the Maximum Single-Ended I/O column for XC7K480T, and the GTX Transceivers row.

Optimized for Best Price-Performance (1.0V, 0.95V, 0.9V)								
	Part Number	XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
Logic Resources	EasyPath™ Cost Reduction Solutions ⁽²⁾	—	—	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
Memory Resources	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
	Maximum Distributed RAM (Kb)	838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)	135	325	445	715	795	835	955
Clock Resources	Total Block RAM (Kb)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
	CMOS (1 MMCM + 1 PLL)	6	8	10	6	10	8	8
	Maximum Single-Ended I/O	300	400	500	300	500	400	400
I/O Resources	Maximum Differential I/O Pairs	144	192	240	144	240	192	192
	DSP48 Slices	240	600	840	1,440	1,540	1,680	1,920
	PCIe® Gen2 ⁽³⁾	1	1	1	1	1	1	1
Integrated IP Resources	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)	8	8	16	24	16	32	32

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Here's a portion of the Xilinx 7-series product selection guide providing an overview of the Kintex-7 large FPGA.

The Kintex-7 has reprogrammable SRAM configuration which requires an external nonvolatile memory, to load the configuration at power up.

The size of these devices goes to 477,000 logic cells, twice as large as the Artix-7. [Annotate]

Speed is limited to 741 MHz on clock buffers and a 1818 MHz toggle frequency, which is much faster than previous devices. Transceivers now run to 12.5 Gbps.

Maximum static power draw is between 201 and 1080 mA at 1 volt depending on part size. Dynamic power is not specified, power estimation tools are used to determine this now.

This device has up to 500 IO pins, almost a 1000:1 ratio of logic cells to I/O. [Annotate] There are 36 supported I/O standards.

The screenshot shows a portion of the Xilinx Virtex-7 FPGAs product selection guide. At the top, it says "Optimized for Highest System Performance and Capacity (1.0V)". Below is a table comparing various Xilinx Virtex-7 devices across different categories:

	XC7V585T	XC7V200I	XC7VX330I	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690I	XC7VX980I	XC7VX1140I	XC7VH580I	XC7VH870I	
Logic Resources	EasyPath™ Cost Reduction Solutions ⁽¹⁾	XCE7V585T	—	XCE7VX330I	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690I	XCE7VX980I	—	—	
	Slices	91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells	582,720	1,954,560	—	412,160	485,760	551,240	693,120	979,200	1,139,200	580,480	876,160
Memory Resources	Maximum Distributed RAM (kb)	6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Block RAM/FIFO w/ ECC (36 kb each)	728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Clocking I/O Resources	Total Block RAM (Gb)	28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
	CMLs (1 MMCM + 1 PLL)	18	24	14	12	14	20	20	18	24	12	18
	Maximum Single-Ended I/O	850	1,200	—	600	700	600	1,000	900	1,100	600	300
	Maximum Differential I/O Pairs	400	576	336	288	336	288	480	432	528	288	144
Integrated IP Resources	DSP Slices	1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCIe® Gen2 ⁽²⁾	3	4	—	—	4	—	—	—	—	—	—
	PCIe Gen3 ⁽³⁾	—	—	2	2	—	2	3	3	4	2	3
	Analog Mixed Signal (AMIS) / XADC ⁽⁴⁾	1	1	1	1	1	1	1	1	1	1	1
	Configuration AES7/HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate) ⁽⁵⁾	36	36	—	—	56	—	—	—	—	—	—
	GTH Transceivers (13.1 Gb/s Max Rate) ⁽⁶⁾	—	—	28	48	—	80	80	72	96	48	72
	GTZ Transceivers (28.05 Gb/s Max Rate)	—	—	—	—	—	—	—	—	—	8	16

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Here's a portion of the Xilinx 7-series product selection guide providing an overview of the Virtex-7 large FPGA.

The Virtex-7 has reprogrammable SRAM configuration which requires an external nonvolatile memory, to load the configuration at power up.

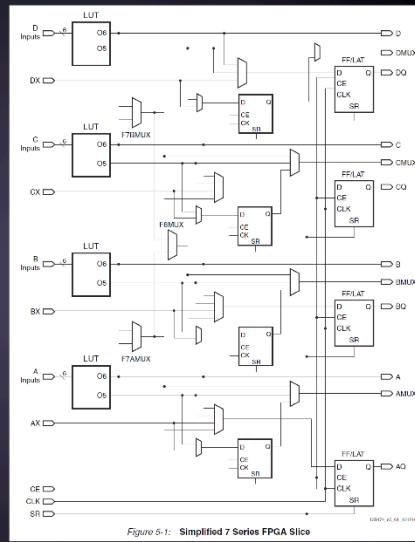
The size of these devices goes to almost 2 million logic cells, 4 times as large as the Kintix-7! [Annotate]

Speed is limited to 741 MHz on clock buffers and a 1818 MHz toggle frequency, which is much faster than previous devices. Transceivers now run to 28.05 Gbps. [Annotate]

Maximum static power draw is between 1012 and 3756 mA at 1 volt depending on part size. Dynamic power is not specified, power estimation tools are used to determine this now. These device can consume up to the range of 100 watts, so heat sinks are often necessary.

This device has up to 1100 IO pins, almost a 2000:1 ratio of logic cells to I/O. [Annotate] There are 36 supported I/O standards.

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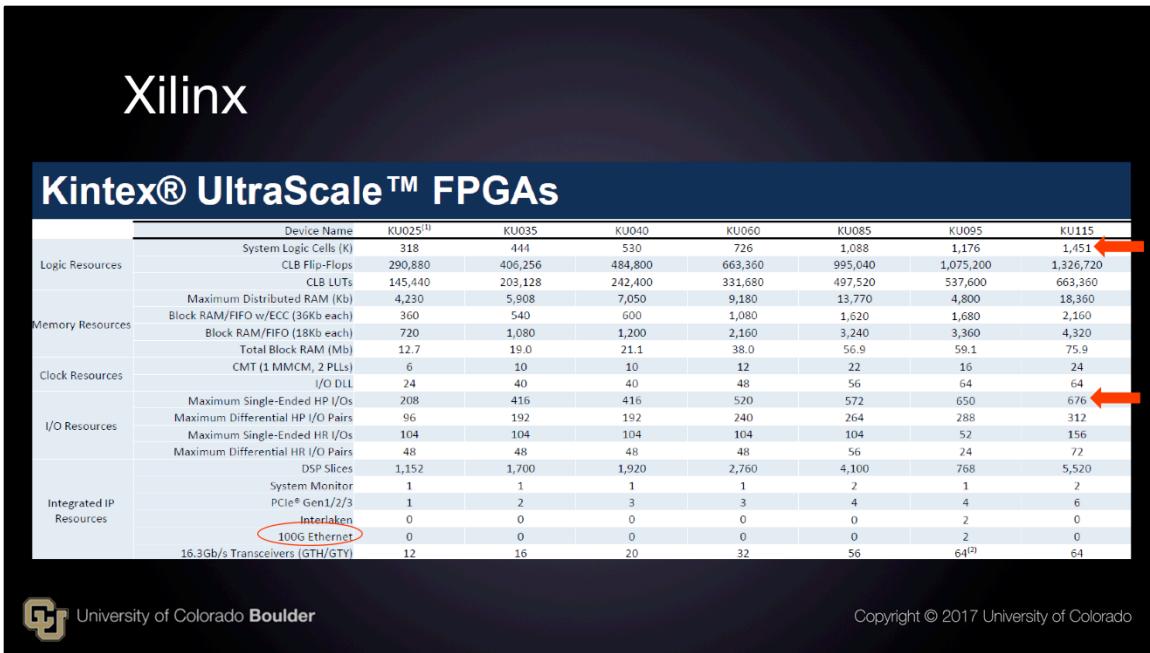


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Here is a simplified diagram of the Series 7 Slice, which is the same as the slice in the Spartan 6. It's not a big surprise that it is the same, given the time and effort that the designers have put in to optimize the logic cell. Once they find something that works, they tend to repeat it.

It is based on 4 6-input LUTs and 8 flip-flops. It can create 1 single bit full adder per LUT, and each LUT can be a 32-bit shift register.



The image shows a portion of the Xilinx Kintex UltraScale FPGAs Product Selection Guide. The guide is a table comparing various device models: KU025⁽¹⁾, KU035, KU040, KU060, KU085, KU095, and KU115. The table is organized by resource type: Logic Resources, Memory Resources, Clock Resources, I/O Resources, and Integrated IP Resources. Red arrows point to specific values in the table: one arrow points to the value '1,451' in the 'System Logic Cells (K)' row for KU115; another arrow points to the value '676' in the 'Maximum Single-Ended HP I/Os' row for KU115.

	Device Name	KU025 ⁽¹⁾	KU035	KU040	KU060	KU085	KU095	KU115
Logic Resources	System Logic Cells (K)	318	444	530	726	1,088	1,176	1,451
	CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
Memory Resources	CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
	Maximum Distributed RAM (Kb)	4,230	5,908	7,050	9,180	13,770	4,800	18,360
	Block RAM/FIFO w/ECC (36kb each)	360	540	600	1,080	1,620	1,680	2,160
Clock Resources	Block RAM/FIFO (18kb each)	720	1,080	1,200	2,160	3,240	3,360	4,320
	Total Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
	CMT (1 MMC, 2 PLLs)	6	10	10	12	22	16	24
I/O Resources	I/O DLL	24	40	40	48	56	64	64
	Maximum Single-Ended HP I/Os	208	416	416	520	572	650	676
	Maximum Differential HP I/O Pairs	96	192	192	240	264	288	312
	Maximum Single-Ended HR I/Os	104	104	104	104	104	52	156
Integrated IP Resources	Maximum Differential HR I/O Pairs	48	48	48	48	56	24	72
	DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
	System Monitor	1	1	1	1	2	1	2
	PCIe® Gen1/2/3	1	2	3	3	4	4	6
	Interlaken	0	0	0	0	0	2	0
	100G Ethernet	0	0	0	0	0	2	0
	16.3Gb/s Transceivers (GTB/GTY)	12	16	20	32	56	64 ⁽²⁾	64

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Here's a portion of the Xilinx Ultrascale product selection guide providing an overview of the Kintex Ultrascale large FPGA.

The Kintex Ultrascale has reprogrammable SRAM configuration which requires an external nonvolatile memory, to load the configuration at power up.

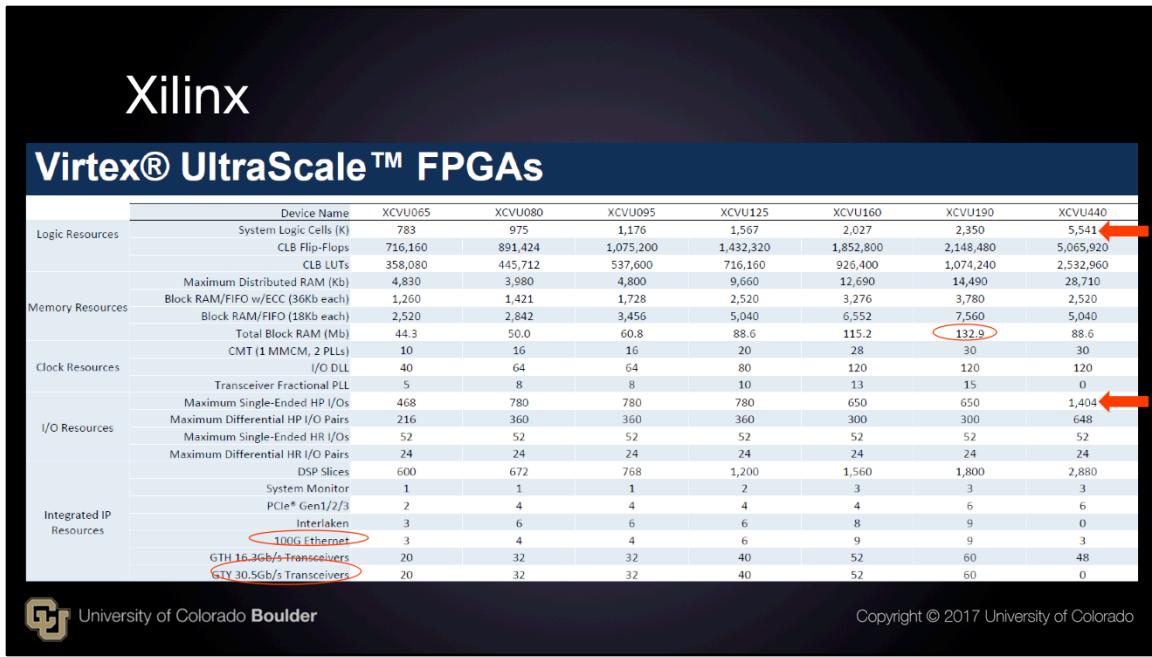
The size of these devices goes to 1.4 million logic cells. [Annotate]

Speed is limited to 8501 MHz on clock buffers, which is faster than previous devices. Transceivers run to 16.3 Gbps.

Maximum static power draw is between 1097 and 3181 mA at 1 volt depending on part size. Dynamic power is not specified, power estimation tools are used to determine this now.

This device has up to 676 IO pins, almost a 2000:1 ratio of logic cells to I/O. There are 41 supported I/O standards. [Annotate]

Hard IP blocks are the same as the 7 series, with the notable addition of the 100G



The image shows a portion of the Xilinx Virtex UltraScale FPGAs Product Selection Guide. The guide is titled "Virtex® UltraScale™ FPGAs" and includes a table comparing seven device models: XCVU065, XCVU080, XCVU095, XCVU125, XCVU160, XCVU190, and XCVU440. The table provides detailed technical specifications for Logic Resources, Memory Resources, Clock Resources, I/O Resources, and Integrated IP Resources. Red circles highlight specific data points: 5,541 logic cells for XCVU440, 1,404 I/O pins for XCVU190, and two entries for 100G Ethernet and GTH 16.3Gb/s Transceivers. The University of Colorado Boulder logo and copyright information are also visible.

	Device Name	XCVU065	XCVU080	XCVU095	XCVU125	XCVU160	XCVU190	XCVU440
Logic Resources	System Logic Cells (K)	783	975	1,176	1,567	2,027	2,350	5,541
	CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
	CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Memory Resources	Maximum Distributed RAM (Kb)	4,830	3,980	4,800	9,660	12,690	14,490	28,710
	Block RAM/FIFO w/ECC (36Kb each)	1,260	1,421	1,728	2,520	3,276	3,780	2,520
	Block RAM/FIFO (18Kb each)	2,520	2,842	3,456	5,040	6,552	7,560	5,040
	Total Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
	I/O DLL	40	64	64	80	120	120	120
	Transceiver Fractional PLL	5	8	8	10	13	15	0
I/O Resources	Maximum Single-Ended HP I/Os	468	780	780	780	650	650	1,404
	Maximum Differential HP I/O Pairs	216	360	360	360	300	300	648
	Maximum Single-Ended HR I/Os	52	52	52	52	52	52	52
	Maximum Differential HR I/O Pairs	24	24	24	24	24	24	24
Integrated IP Resources	DSP Slices	600	672	768	1,200	1,560	1,800	2,880
	System Monitor	1	1	1	2	3	3	3
	PCIe® Gen1/2/3	2	4	4	4	4	6	6
	Interlaken	3	6	6	6	8	9	0
	100G Ethernet	3	4	4	6	9	9	3
	GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
	GY 30.5Gb/s Transceivers	20	32	32	40	52	60	0

Here's a portion of the Xilinx Ultrascale product selection guide providing an overview of the Virtex Ultrascale large FPGA.

The Virtex-Ultrascale has reprogrammable SRAM configuration which requires an external nonvolatile memory, to load the configuration at power up.

The size of these devices goes to over 5 million logic cells, 2 times as large as the Kintix-Ultrascale. [Annotate]

Speed is limited to 850 MHz on clock buffers. Transceivers now run to 30.5 Gbps, with aggregate bandwidth to an amazing 3.66 Tera bits per second. [Annotate]

Maximum static power draw is between 1581 and 7988 mA at 1 volt depending on part size. Dynamic power is not specified, power estimation tools are used to determine this now. These device can consume up to the range of 100 watts, so heat sinks are often necessary.

This device has up to 1400 IO pins, almost a 4000:1 ratio of logic cells to I/O. There are 36 supported I/O standards. [Annotate]

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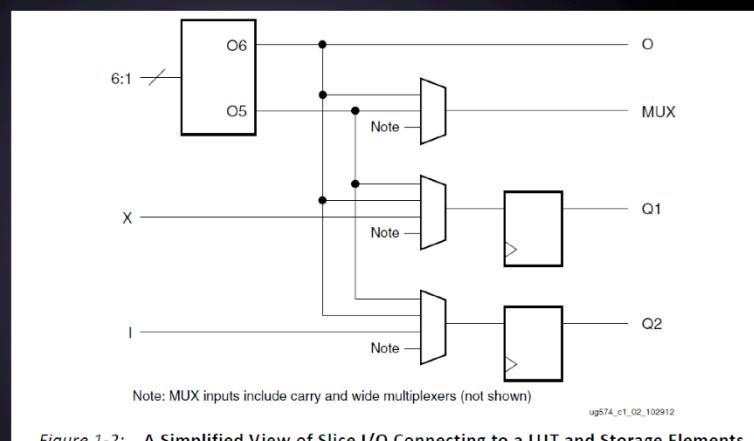


Figure 1-2: A Simplified View of Slice I/O Connecting to a LUT and Storage Elements

This is a picture of the logic cell in the Ultrascale FPGA family. It is very similar to the Series 7 logic cell, with a 6-input LUT and 2 flip-flops with intervening carry logic. However, there are 8 of these cells in a single logic slice instead of 4 as there was in the series 7. When used as distributed RAM, these LUTs are more capable, providing up to 64 bits of RAM per LUT, up to 512 bits per slice. In a type M slice, the LUTs can also provide 32 bits of shift register each.

Xilinx summary

⇒ <https://www.xilinx.com/products/silicon-devices/fpga.html>

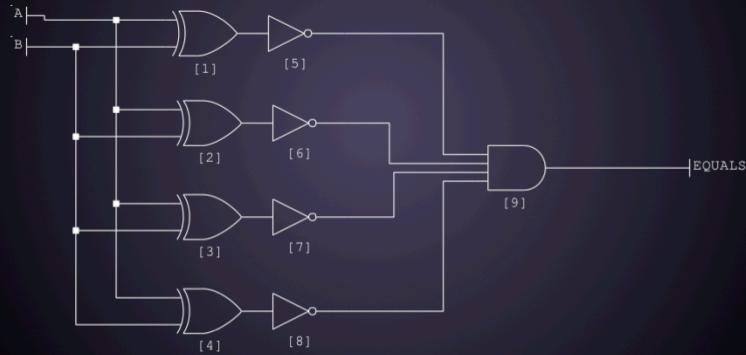


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You can find up to date information about all Xilinx FPGAs at
<https://www.xilinx.com/products/silicon-devices/fpga.html>.

How large of a comparator in bits can be made using a Virtex Ultrascale Logic Cell?



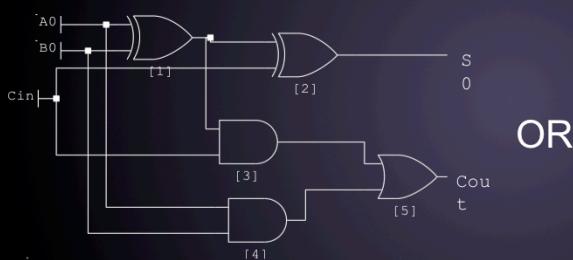
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Recall the 4-bit comparator.

How many comparator bits can be implemented in a LUT? In the Ultrascale architecture, the 6 input LUT will handle 3 bits of comparator, so wider comparators can be made with less delay.

How many full adders can be created
in a Virtex Ultrascale logic cell?



OR

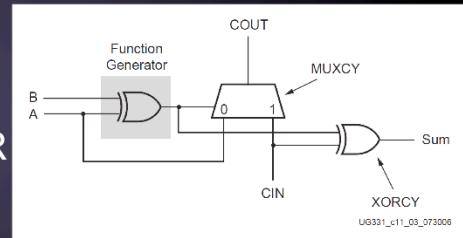


Figure 9-3: Carry Logic in Spartan-3 Generation FPGAs



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How many full adders can be made in an Ultrascale logic cell? Given there are 2 outputs, each cell should be able to easily generate a full adder per cell using the standard approach. This is also true of the carry look-ahead approach, which also provides faster performance.

Xilinx Large FPGAs Summary

- ⇒ Xilinx offers several large FPGA families, including the Artix-7, Kintex-7 and Virtex-7 as well as the Kintex Ultrascale and Virtex Ultrascale. These are large devices with up to 5 million logic cells.
- ⇒ Speed has increased greatly with these large FPGAs, with internal clock trees running up to 850 MHz and Transceivers at 30 Gbps with aggregate bandwidth of 3.66 Tbps.
- ⇒ Xilinx large FPGAs are rich in added hard IP blocks, which include Memory, PLLs, DSP, PCIe Gen 1/2/3 Transceivers, 100G Ethernet Interface, and even 12 bit ADCs in some cases.



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In this video we have learned

- Xilinx offers several large FPGA families, including the Artix-7, Kintex-7 and Virtex-7 as well as the Kintex Ultrascale and Virtex Ultrascale. These are large devices with up to 5 million logic cells.
- Speed has increased greatly with these large FPGAs, with internal clock trees running up to 850 MHz and Transceivers at 30 Gbps with aggregate bandwidth to 3.66 Tbps.
- Xilinx large FPGAs are rich in added hard IP blocks, which include Memory, PLLs, DSP, PCIe Gen 1/2/3 Transceivers, 100G Ethernet Interface, and even 12 bit ADCs in some cases.