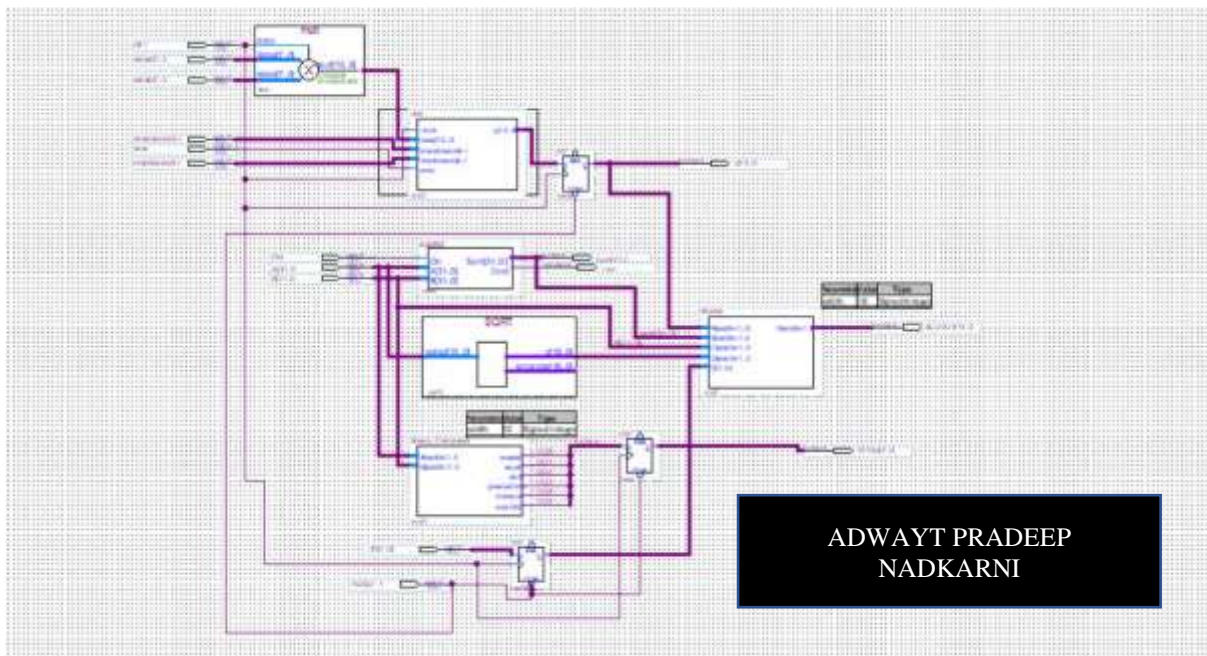


QUESTIONS

The goal of this assignment is to extend your knowledge of schematic design using Quartus Prime by using pipelining and IP blocks to improve design performance. The student should be following the video instructions and creating the example as they go along. Their progress is checked at milestones by presenting screenshots which are matched to the solution screenshots to verify their work. Milestones checked are design schematic creation, timing improvement with pipelining, pin assignment, timing analysis and simulation.

This assignment is required. Peers must review 3 submissions to pass the assignment.

SOLUTIONS:



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- Fmax Summary
- Setup Summ
- Hold Summ
- Recovery Sum
- Removal Sum
- Minimum Pul

Slow 1200MHz B3C Model Fmax Summary

Fmax	Restricted Fmax	Clock Name	Note
1	36.70 MHz	clk1	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are

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Flow Summary

Flow Status	Success
Quartus Prime version	16.1.0 Build 106 10/24/2016 GJ (Site Edition)
Revision Name	pipemult2
Top-level Entity Name	MAX10
Family	10K10K04F484C80ES
Timing Models	Preliminary
Total logic elements	352 / 6064 (1.7 %)
Total registers	281
Total pins	167 / 250 (6.7 %)
Total output pins	0
Total memory bits	512 / 381,012 (0.1 %)
Unimplemented Multiplexers	1 / 48 (0.2 %)
Total Fmax	0 / 1.00 %
SRAM blocks	0 / 1.00 %
ALU blocks	0 / 1.00 %

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ipemult2

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Assignment Editor

Category: All

	Status	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
180	Ok		B	Location	IOBANK_5	Yes			
181	Ok		CCout	Location	IOBANK_7	Yes			
182	Ok		dataa	Location	IOBANK_5	Yes			
183	Ok		dataib	Location	IOBANK_5	Yes			
184	Ok		IR	Location	IOBANK_6	Yes			
185	Ok		q	Location	IOBANK_4	Yes			
186	Ok		Sum	Location	IOBANK_3	Yes			
187	Ok		rtfaddress	Location	IOBANK_5	Yes			
188	Ok		wrtfaddress	Location	IOBANK_5	Yes			
189	Ok		wren	Location	IOBANK_5	Yes			
190	Ok		A[31]	Location	IOBANK_6	Yes			
191	Ok		A[30]	Location	IOBANK_8	Yes			
192	Ok		A[29]	Location	IOBANK_8	Yes			
193	Ok		A[28]	Location	IOBANK_8	Yes			
194	Ok		A[27]	Location	IOBANK_8	Yes			
195	Ok		A[26]	Location	IOBANK_8	Yes			
196	Ok		A[25]	Location	IOBANK_8	Yes			
197	Ok		A[24]	Location	IOBANK_8	Yes			

This cell shows the status of the assignment in the current row.

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Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	128.21 MHz	128.21 MHz	clk1	

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