

# Lattice FPGAs



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# Lattice

- ECP5
- ECP3
- MACHXO3
- MACHXO2
- ICE40 Ultra

In this video we will continue our survey of modern programmable logic devices, with Large FPGAs from Altera, including the Arria V, the Stratix V, the Arria 10, and the Stratix 10.

## Programmable Logic Device Selection Criteria

	Selection Criteria	SRAM CPLDs	SRAM FPGAs
1	Reprogrammability (Configuration Memory Type)	Yes	Yes
2	Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)	Small	Moderate
3	Cost per logic gate	Low	Low
4	Speed (Maximum clock frequency)	388 MHz	400 MHz
5	Power Consumption (static and dynamic)	Very Low	Moderate
6	Cost per I/O (I/O Density) and extent of supported I/O standards	Low, Good	Low, Good
7	Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)	Very Good	Good
8	Deterministic timing (timing is consistent in every implementation)	No	No
9	Reliability (FIT rate)	Fair	OK
10	Endurance (number of programming cycles and years of retention)	100K/ 20 year	NA
11	Design and Data Security	Fair	Fair



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The goal in programmable logic device selection is to pick the best fit part for our requirements. We will use the programmable logic device selection criteria we established earlier to evaluate these devices as listed here.

# Lattice ECP5

Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U-12	LFE5U-25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages and SERDES Channels / I/O Combinations							
285 cFBGA (10 x 10 mm <sup>2</sup> , 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 cBGA (17 x 17 mm <sup>2</sup> )	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 cBGA (23 x 23 mm <sup>2</sup> )	—	4/245	4/259	—	—	0/245	0/259
756 cBGA (27 x 27 mm <sup>2</sup> )	—	—	4/365	—	—	—	0/365



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To start, let's look at the product table for the Arria V mid-range FPGA. The Altera Arria V has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

Notice there are up to 500,000 logic elements, about double that of a Cyclone V.  
[Annotate]

Speed is limited to 625 MHz on global clock buffers.

Power is not specified, use the Power Play Analyzer tool to determine it.

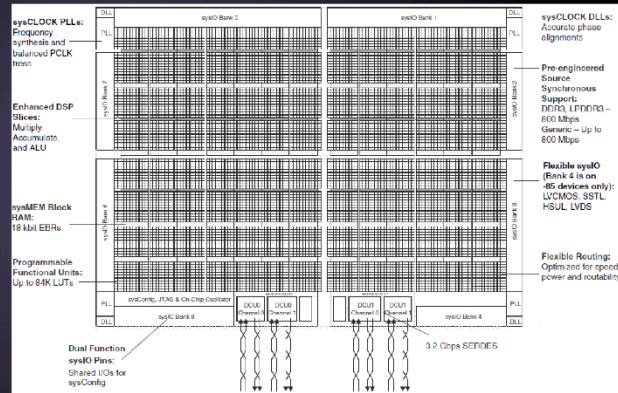
This device has up to 704 IO pins, a 715:1 ratio of logic cells to I/O. [Annotate]

A number of hard IP blocks have been added, including Block memory [Annotate], DSP blocks [Annotate], High Speed Transceivers at 6.6 Gbps [Annotate] standard, with transceiver parts to 12.5 Gbps, and External Memory Interfaces up to DDR3 at 1600 Mbps. [Annotate].

# ECP5 Architecture

Each ECP5 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC).

Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices



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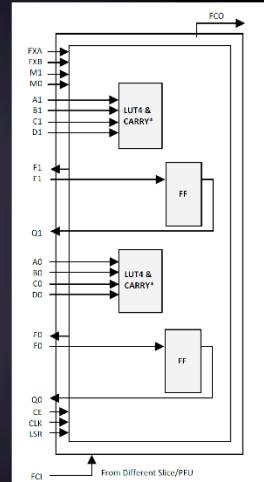
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## ECP5 Slice (Logic Element)

Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM.



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## ECP5 DSP Slice

The ECP5 sysDSP Slice supports many functions that include the following:

- Full double data rate support - Higher operation frequency (throughput of up to 370 Mbps)
- Dual-multiplier architecture.
- Fully cascadable DSP across slices.
- Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)
- Multiply (36x36 by cascading across two sysDSP slices)
- Multiply Accumulate - one 18x36 or two 18x18

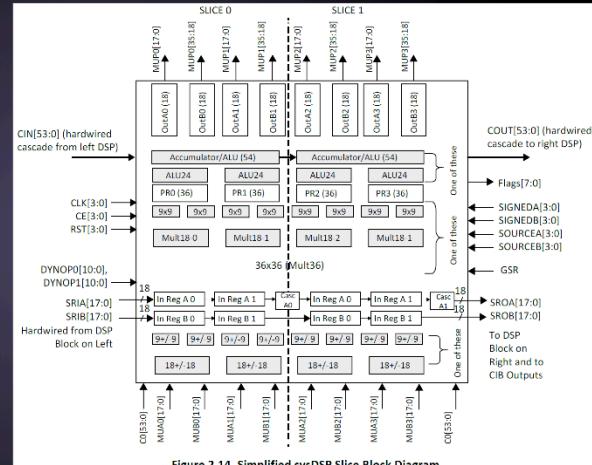


Figure 2.14. Simplified sysDSP Slice Block Diagram

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# Lattice ECP3

Table 1-1. LatticeECP3™ Family Selection Guide

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
328 csBGA (10 x 10 mm)	2 / 116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586



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To start, let's look at the product table for the Arria V mid-range FPGA. The Altera Arria V has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

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[Annotate]

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Speed is limited to 625 MHz on global clock buffers.

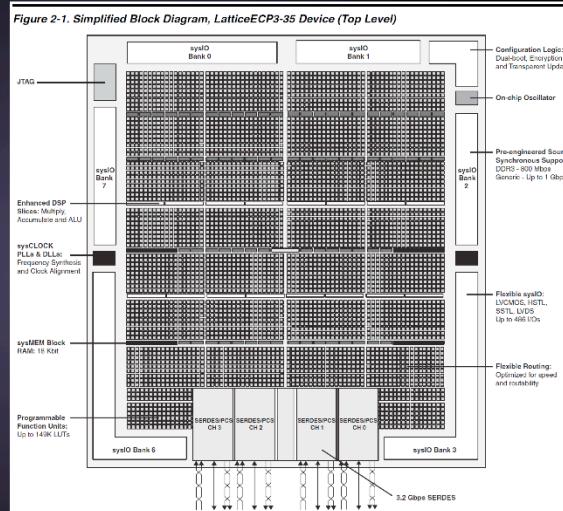
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# ECP3 Architecture

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing slices



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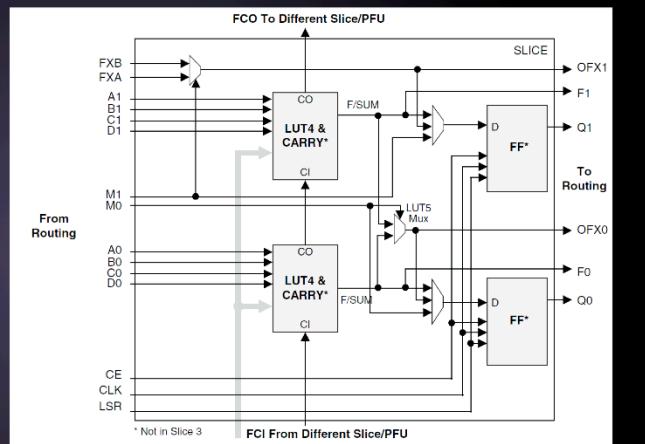
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## ECP3 Slice (Logic Element)

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. Slice 0 through Slice 2 can be configured as distributed memory.



To start, let's look at the product table for the Arria V mid-range FPGA. The Altera Arria V has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

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## Lattice MACHX02

	XO2-256	XO2-640	XO2-640U <sup>1</sup>	XO2-1200	XO2-1200U <sup>1</sup>	XO2-2000	XO2-2000U <sup>1</sup>	XO2-4000	XO2-7000
LUTs	256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbytes)	2	5	5	10	10	16	16	34	54
EBR SRAM (kbytes)	0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbytes/block)	0	2	7	7	8	8	10	10	26
UFM (kbytes)	0	24	64	64	80	80	96	96	256
Device Options:	HC <sup>2</sup>	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE <sup>3</sup>					Yes	Yes	Yes	Yes
	ZE <sup>4</sup>	Yes	Yes		Yes	Yes		Yes	Yes
Number of PLLs	0	0	1	1	1	1	2	2	2
Hardened Functions:	I <sup>2</sup> C	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1



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[Annotate]

Speed is limited to 625 MHz on global clock buffers.

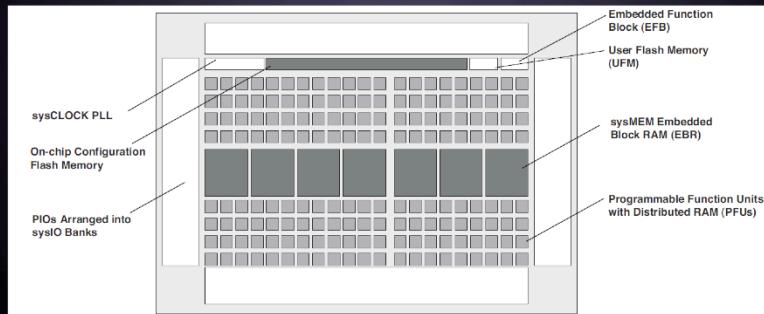
Power is not specified, use the Power Play Analyzer tool to determine it.

This device has up to 704 IO pins, a 715:1 ratio of logic cells to I/O. [Annotate]

A number of hard IP blocks have been added, including Block memory [Annotate], DSP blocks [Annotate], High Speed Transceivers at 6.6 Gbps [Annotate] standard, with transceiver parts to 12.5 Gbps, and External Memory Interfaces up to DDR3 at 1600 Mbps. [Annotate].

## MACHXO2 Architecture

The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have PLLs and blocks of Embedded Block RAM (EBRs).



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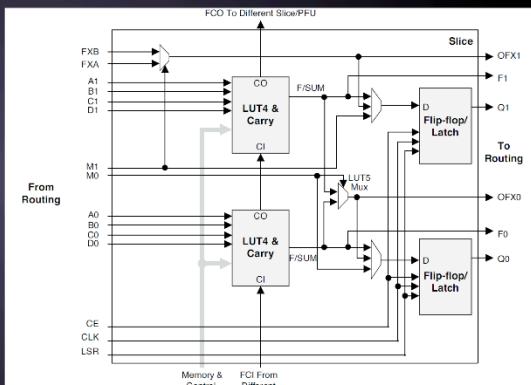
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## MACHXO2 Slice (Logic Element)

The registers in the slice can be configured for positive/ negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU).

There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU).



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## Lattice MACHX03

Features	MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs	640	1300	2100	4300	6900	9400
Distributed RAM (kbytes)	5	10	16	34	54	73
EBR SRAM (kbytes)	64	64	74	92	240	432
Number of PLLs	1	1	1	2	2	2
Hardened Functions:						
I <sup>2</sup> C	2	2	2	2	2	2
SPI	1	1	1	1	1	1
Timer/Counter	1	1	1	1	1	1
Oscillator	1	1	1	1	1	1
MIPI D-PHY Support	Yes	Yes	Yes	Yes	Yes	Yes
Multi-Time Programmable NVM	MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash	MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400



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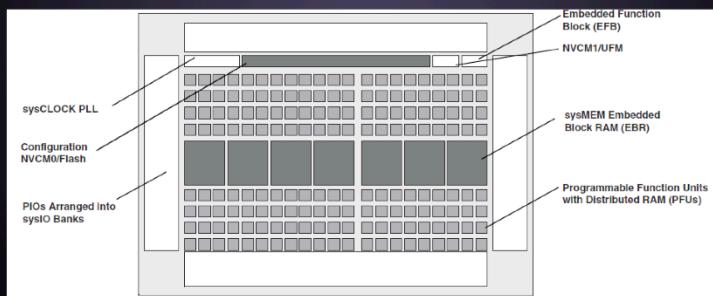
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# MACHXO3L Architecture

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have PLLs and Embedded Block RAM (EBRs).



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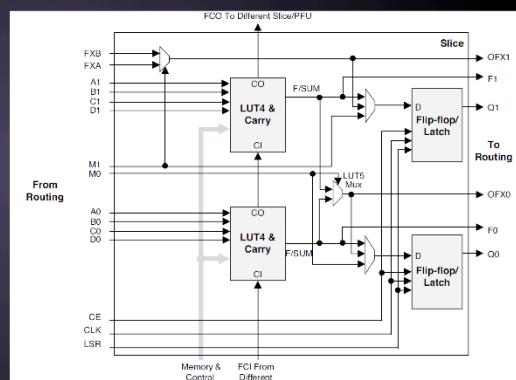
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## MACHXO3L Slice (Logic Element)

The MACHXO3 logic element is a slice with 2 LUT4s and 2 flip-flops, identical to the slice in the MACHXO2.



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## Lattice ICE40 Ultra

Part Number	iCE5LP1K	iCE5LP2K	iCE5LP4K
Logic Cells (LUT + Flip-Flop)	1100	2048	3520
EBR Memory Blocks	16	20	20
EBR Memory Bits	64 k	80 k	80 k
PLL Block	1	1	1
NVCM	Yes	Yes	Yes
DSP Blocks (MULT16 with 32-bit Accumulator)	2	4	4
Hardened I2C, SPI	1,1	2,2	2,2
HF Oscillator (48 MHz)	1	1	1
LF Oscillator (10 kHz)	1	1	1
24 mA LED Sink	3	3	3
500 mA LED Sink	1	1	1
Embedded PWM IP	Yes	Yes	No
Packages, ball pitch, dimension	Total User I/O Count		
36-ball WLCSP, 0.35 mm, 2.078 mm x 2.078 mm	26	26	26
36-ball ucfBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26	26
48-ball QFN Package, 0.5 mm, 7.0 mm x 7.0 mm	39	39	39



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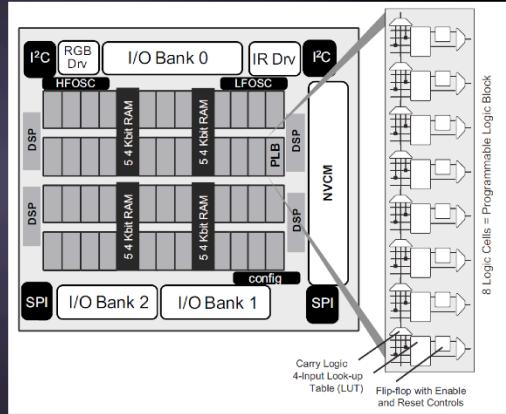
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# ICE40 Architecture

The iCE40 Ultra family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I2C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO).



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[Annotate]

Speed is limited to 625 MHz on global clock buffers.

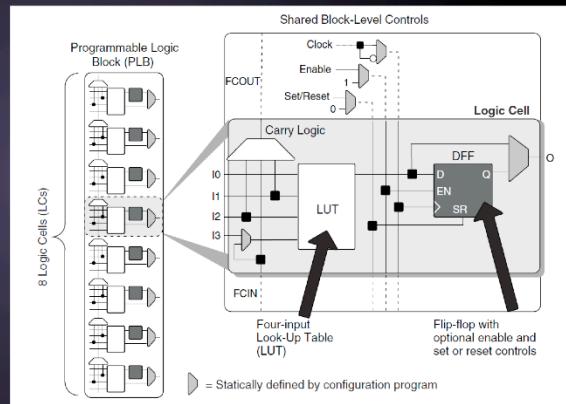
Power is not specified, use the Power Play Analyzer tool to determine it.

This device has up to 704 IO pins, a 715:1 ratio of logic cells to I/O. [Annotate]

A number of hard IP blocks have been added, including Block memory [Annotate], DSP blocks [Annotate], High Speed Transceivers at 6.6 Gbps [Annotate] standard, with transceiver parts to 12.5 Gbps, and External Memory Interfaces up to DDR3 at 1600 Mbps. [Annotate].

## ICE40 Slice (Logic Element)

The core of the iCE40 Ultra device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown. Each LC contains one LUT and one register.



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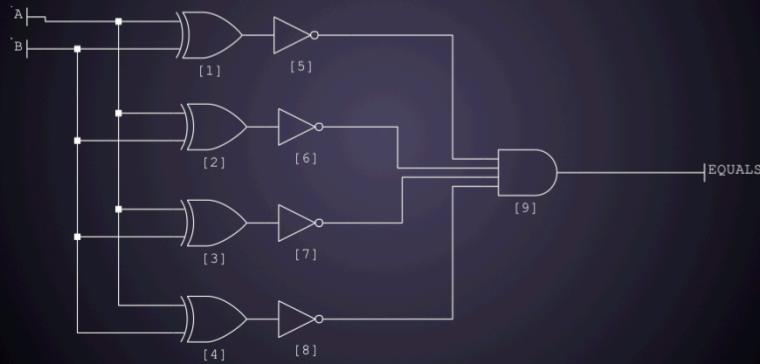
To start, let's look at the product table for the Arria V mid-range FPGA. The Altera Arria V has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

Notice there are up to 500,000 logic elements, about double that of a Cyclone V.  
[Annotate]

Speed is limited to 625 MHz on global clock buffers.  
Power is not specified, use the Power Play Analyzer tool to determine it.  
This device has up to 704 IO pins, a 715:1 ratio of logic cells to I/O. [Annotate]

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## How large of a comparator can be made using a Lattice logic Cell?



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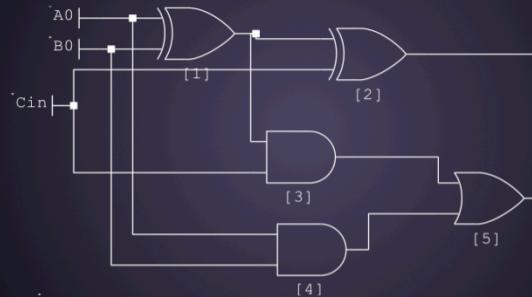
To start, let's look at the product table for the Arria V mid-range FPGA. The Altera Arria V has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

Notice there are up to 500,000 logic elements, about double that of a Cyclone V.  
[Annotate]

Speed is limited to 625 MHz on global clock buffers.  
Power is not specified, use the Power Play Analyzer tool to determine it.  
This device has up to 704 IO pins, a 715:1 ratio of logic cells to I/O. [Annotate]

A number of hard IP blocks have been added, including Block memory [Annotate], DSP blocks [Annotate], High Speed Transceivers at 6.6 Gbps [Annotate] standard, with transceiver parts to 12.5 Gbps, and External Memory Interfaces up to DDR3 at 1600 Mbps. [Annotate].

## How many full adders can be created in a Lattice logic element?



1 bit full adder

To start, let's look at the product table for the Arria V mid-range FPGA. The Altera Arria V has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

Notice there are up to 500,000 logic elements, about double that of a Cyclone V.  
[Annotate]

Speed is limited to 625 MHz on global clock buffers.  
Power is not specified, use the Power Play Analyzer tool to determine it.  
This device has up to 704 IO pins, a 715:1 ratio of logic cells to I/O. [Annotate]

A number of hard IP blocks have been added, including Block memory [Annotate], DSP blocks [Annotate], High Speed Transceivers at 6.6 Gbps [Annotate] standard, with transceiver parts to 12.5 Gbps, and External Memory Interfaces up to DDR3 at 1600 Mbps. [Annotate].

## Lattice FPGAs Summary

- Lattice specializes in low cost high value small to medium size programmable logic parts, including the iCE40, MACHXO2, MACHXO3, ECP3 and ECP5 families
- The MACHXO2 and MACHXO3 devices are single chip solutions with on-chip nonvolatile configuration memory storage, but routing controlled by SRAM cells that must be loaded on power up. These devices feature low power, very small size down to 2.5 x 2.5 mm, and several hard IP blocks.
- The iCE40 family includes an abundance of hard IP functions for such a small part, and very low power consumption.
- Lattice devices all have logic elements based on a 4 input LUT and register, adequate but somewhat less capable than other offerings.



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To start, let's look at the product table for the Arria V mid-range FPGA. The Altera Arria V has reprogrammable SRAM configuration and routing, so it needs an external nonvolatile configuration memory. On power up, the device transfers the configuration information to the internal SRAM.

Notice there are up to 500,000 logic elements, about double that of a Cyclone V.  
[Annotate]

Speed is limited to 625 MHz on global clock buffers.  
Power is not specified, use the Power Play Analyzer tool to determine it.  
This device has up to 704 IO pins, a 715:1 ratio of logic cells to I/O. [Annotate]

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