

Create a Design with Quartus Prime



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Title Slide

≡D- In this presentation, you will be introduced to the methods used to enter FPGA designs in Quartus Prime



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In this presentation, you will be introduced to the methods used to create FPGA designs in Quartus Prime, including:

- Schematic Capture,
- Import of IP blocks
- HDL text entry, including VHDL, Verilog, and System Verilog.
- State machine entry
- Import of EDIF files

How to select one of these methods to use in the design will be demonstrated. Files are provided so that you can follow along and perform each step along the way. If you haven't already, please download them now from the link provided.

Feel free to pause the video as you enter commands into Quartus Prime.

Agenda for this Video

1. Create a schematic file for the top-level design.
2. Create a schematic symbol from an IP core multiplier.
3. Create a schematic symbol from an HDL file.
4. Wire the symbols together and then to device pins to complete the schematic design entry.



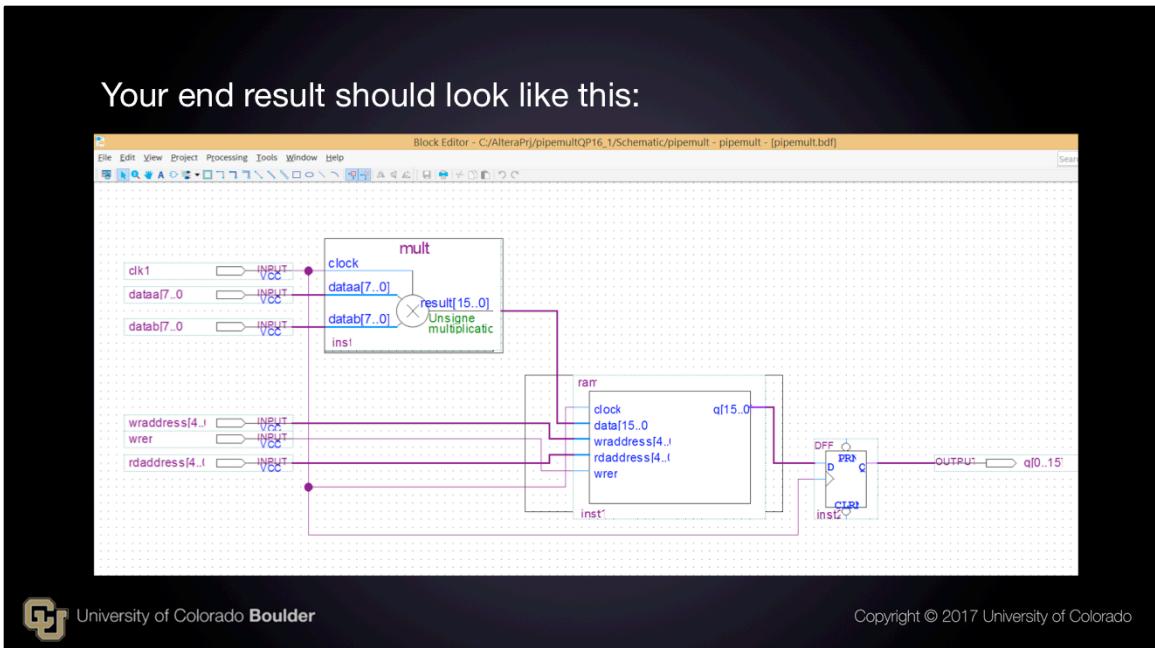
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Your end result should look like this:



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In this video, you have learned:

- The various ways design entry can be performed for FPGAs
- How to select and configure an IP core multiplier
- How to create schematic symbols from HDL source files
- How to create a schematic of logic and IP blocks for FPGA implementation



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