

Xilinx Small FPGAs



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Let's take a closer look and FPGA Architecture to see how these devices are put together and why.

Xilinx Small FPGAs

▫ Spartan-3AN FPGA Family

▫ Spartan 6 Family



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In this video we will continue our survey of modern programmable logic devices, with Small FPGAs from Xilinx, including the Spartan-3AN and the Spartan 6.

Programmable Logic Device Selection Criteria

1. Reprogrammability (Configuration Memory Type)
2. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
3. Cost per logic gate
4. Speed (Maximum clock frequency)
5. Power Consumption (static and dynamic)
6. Cost per I/O (I/O Density) and extent of supported I/O standards
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
10. Endurance (number of programming cycles and years of retention)
11. Design and Data Security



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We will use the programmable logic device selection criteria we established earlier to evaluate these devices.

To reiterate, there are 11 criteria:

1. Reprogrammability (Configuration Memory Type)
2. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
3. Cost per logic gate
4. Speed (Maximum clock frequency)
5. Power Consumption (static and dynamic)
6. Cost per I/O (I/O Density)
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
10. Endurance (number of programming cycles and years of retention)
11. Design and Data Security

Here's a portion of the Xilinx Spartan-3AN FPGA family datasheet. The Spartan-3AN has reprogrammable FLASH configuration and User memory. Note equivalent gates up to 1.4 M, 25k logic cells, considerably more logic than the CPLDs have. This part is designed for low cost.

Speed is limited to 350 MHz on global clock buffers, which is faster than the CPLDs.

Maximum power draw is between 20 and 200 mA depending on part size.

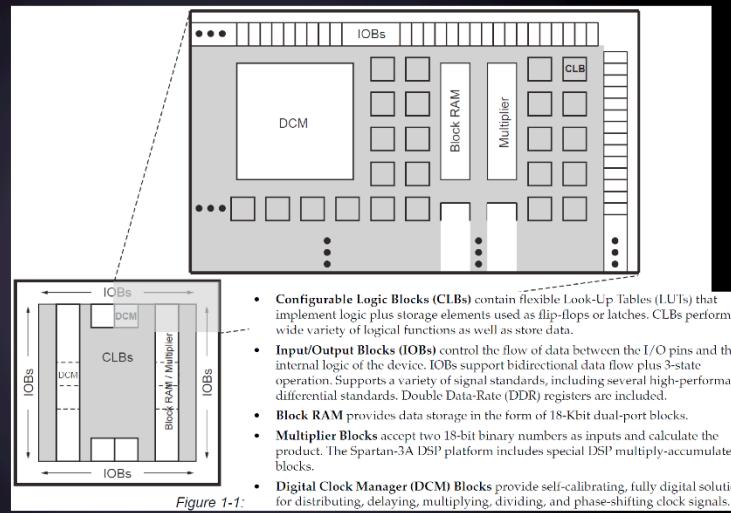
This device has up to 502 IO pins, a 50:1 ratio of logic cells to I/O. There are 23 supported I/O standards.

20 years data retention is good, as is 100000 programming cycles endurance.

Design security is enhanced by the integration of the configuration memory on a single chip.

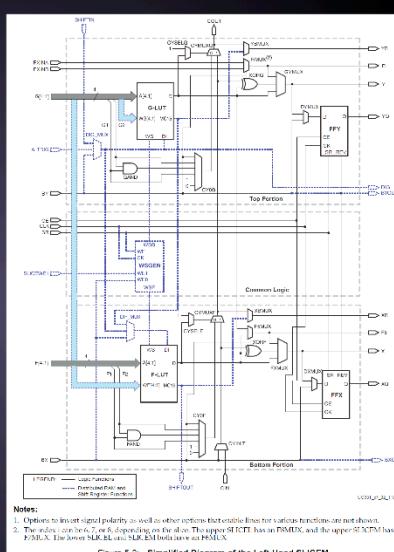
Hard IP blocks have been added, including RAM blocks, Multipliers, and Digital Clock Managers.

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Here is the overall architecture of the Spartan 3. IO is on the outside, and it includes Logic blocks, RAM, Multipliers, and Clock manager.

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Here is a picture of a Spartan 3 Slice (one half of a logic block). The heart of the slice is 2 4-input LUTs and 2 Flip Flop outputs. It also has some carry-chain logic for creating adders, and shift clock generation to help make shift registers.

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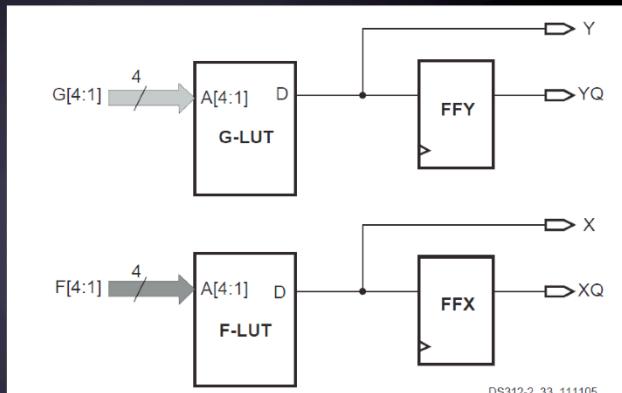


Figure 5-5: LUT Resources in a Slice

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Spartan-6 FPGA Feature Summary

Table 1: Spartan-6 FPGA Feature Summary by Device

Device	Logic Cells ⁽¹⁾	Configurable Logic Blocks (CLBs)			DSP48A1 Slices ⁽³⁾	Block RAM Blocks		CMTs ⁽⁵⁾	Memory Controller Blocks (Max) ⁽⁶⁾	Endpoint Blocks for PCI Express	Maximum STP Transceivers	Total IO Banks	Max User I/O
		Slices ⁽²⁾	Flip-Flops	Max Distributed RAM (Kb)		18 Kb ⁽⁴⁾	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576
XC6SLX25T	24,051	3,758	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	498
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	540



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Here's a portion of the Xilinx Spartan-3AN FPGA family datasheet.
The Spartan-6 has reprogrammable SRAM configuration which requires an external nonvolatile memory, usually a FLASH memory, to load the configuration at power up.
The delay before the device becomes active is several milliseconds.

Note it has up to 147k logic cells, considerably more logic. This part is designed for low cost.

Additional Hard IP blocks are included, including
180 DSP slices
Almost 5000 kB of Block RAM
And up to 8 high-speed transceivers.

This device has up to 540 IO pins, a 300:1 ratio of logic cells to I/O. There are 55 supported I/O standards.

Speed is limited to 400 MHz on global clock buffers, which is faster than the CPLDs.

Maximum static power draw is between 20 and 51mA depending on part size.

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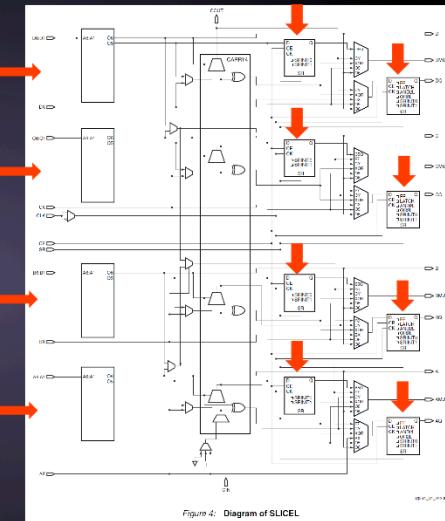


Figure 4: Diagram of SLICEL.



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Here is a picture of a Spartan 6 Slice (one quarter of a logic block). The heart of the slice is 4 6-input LUTs and 8 Flip Flops. It also has some carry-chain logic for creating adders. There are 3 types of slices, with varying capabilities. As you can see, the logic is becoming more and more complex.

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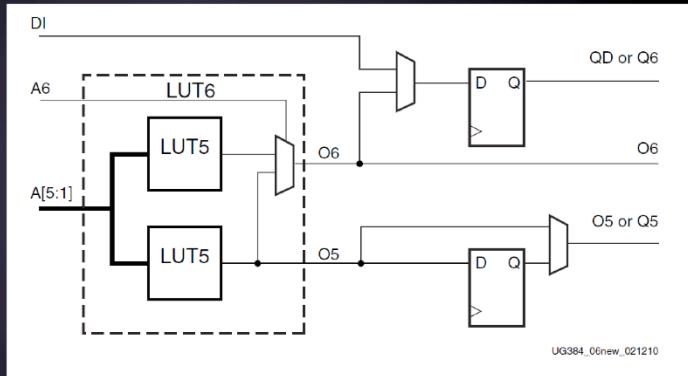
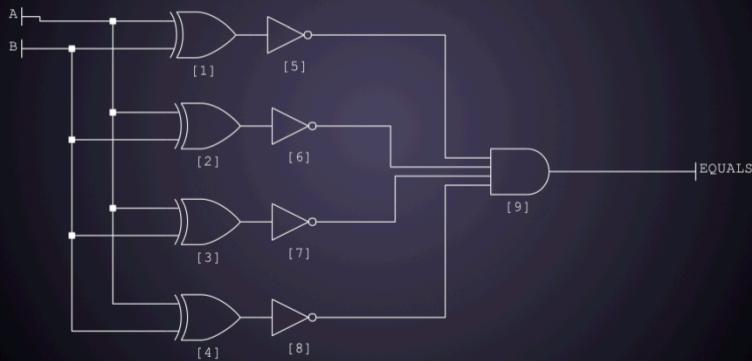


Figure 6: LUT6

This is a simplified picture of the LUT resources in a slice. The LUTs can also be used as distributed memory (each slice can create up to a 256 x 1 RAM or ROM) or as a 32-bit shift register per slice.

How large of a comparator in bits can be made using a Spartan Logic Cell?



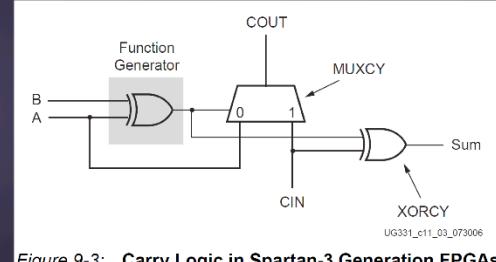
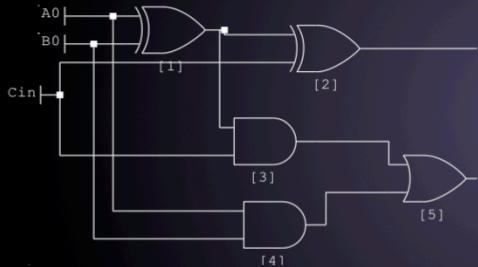
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Recall the 4-bit comparator.

How many comparator bits can be implemented in a LUT? In the 3AN case, there are only 4 inputs, so only a 2-bit comparator can be created. Larger comparators require that the LUTs be cascaded. Although the logic is efficiently used, there is added delay relative to the CPLD implementation. In the Spartan 6 case, the 6 input LUT will handle 3 bits of comparator, so wider comparators can be made with less delay.

How many full adders can be created in a Spartan logic cell?



How many full adders can be made in a logic cell? For the Spartan 3AN at first blush, it would seem to require 2 LUTS per one adder. The logic on the left can be implemented in two LUTs with three inputs each to generate Sum and Carry. The problem with this implementation is that it requires two LUTs for every input bit, and the Carry propagates through the full LUT delay for each bit.

A better implementation is to "look ahead" and determine if the input Carry signal needs to be propagated (the inputs are different) or generated (both inputs are High).

This is shown on the left. To optimize the implementation of this logic, the Spartan-3 generation CLB provides a dedicated XOR gate outside the LUT to generate the Sum, called XORCY, and a dedicated mux to provide the Carry, called MUXCY. In this way each LUT can implement 1 full adder bit.

This structure makes more efficient use of logic resources than what was seen in the CPLDs. This is also true of shift registers, which can be implemented entirely using the LUT, 16 bits per LUT for the Spartan 3AN, 32 bits per Slice for the Spartan 6.

Xilinx Small FPGAs Summary

- ⇒ Xilinx offers several smaller FPGA families, including the Spartan -3AN and Spartan 6 which are both currently available.
- ⇒ The Spartan 3AN uses on-chip FLASH configuration memory, so it a single-chip solution. The Spartan 6 uses SRAM configuration memory, so it needs an additional nonvolatile memory device to hold the configuration.
- ⇒ The Spartan 3AN has a logic cell based on a 4-input LUT and flip-flop, with additional logic to help efficiently create adders and shift registers. The Spartan 6 has a 6-input LUT with 2 flip-flops per logic cell.
- ⇒ Xilinx small FPGAs are more efficient in implementation of adders or shift registers than CPLDs.



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In this video we have learned

- Xilinx offers several smaller FPGA families, including the Spartan -3AN and Spartan 6 which are both currently available.
- The Spartan 3AN uses on-chip FLASH configuration memory, so it a single-chip solution. The Spartan 6 uses SRAM configuration memory, so it needs an additional nonvolatile memory device to hold the configuration.
- The Spartan 3AN has a logic cell based on a 4-input LUT and flip-flop, with additional logic to help efficiently create adders and shift registers. The Spartan 6 has a 6-input LUT with 2 flip-flops per logic cell.
- Xilinx small FPGAs are more efficient in implementation of adders or shift registers than CPLDs.
- Xilinx small FPGAs include additional Hard IP blocks, including Multipliers and DSP, RAM blocks, Clock generation, and Hi-speed Transceivers.