

# Xilinx CPLD Devices



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# Xilinx CPLD Devices

▷ XC9500XL CPLD Family

▷ CoolRunner II Family



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In this video we will start our survey of modern programmable logic devices, beginning with CPLDs from Xilinx.

## Programmable Logic Device Selection Criteria

1. Reprogrammability (Configuration Memory Type)
2. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
3. Cost per logic gate
4. Speed (Maximum clock frequency)
5. Power Consumption (static and dynamic)
6. Cost per I/O (I/O Density)
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
10. Endurance (number of programming cycles and years of retention)
11. Design and Data Security



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We will use the programmable logic device selection criteria we established earlier to evaluate these devices.

To reiterate, there are 11 criteria:

1. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
2. Cost per logic gate
3. Speed (Maximum clock frequency)
4. Power Consumption (static and dynamic)
5. Reprogrammability
6. Cost per I/O (I/O Density)
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
10. Endurance (number of programming cycles and years of retention)
11. Design and Data Security

Here's the Xilinx XC9500XL CPLD family datasheet.

Why do you look at the datasheet? Generally we are trying to determine if we can use this part in our design by looking at its specified performance characteristics.

I'd like to highlight some of the significant characteristics of this device that relate directly to our selection criteria.

Deterministic timing – 5 ns pin to pin delay

5V I/O. Everyone say that with gusto! These parts used as voltage translators – especially in automotive applications where much legacy equipment still runs on 5 volts. I have used a XC9572XL in the design of an industrial product for this very reason.

This is a device with FLASH cell for routing.

It is reprogrammable.

20 years data retention is good, as is 10000 programming cycles endurance.

Note the limit in the amount of logic – 288 macrocells, 6400 gates, 288 Flip Flops.

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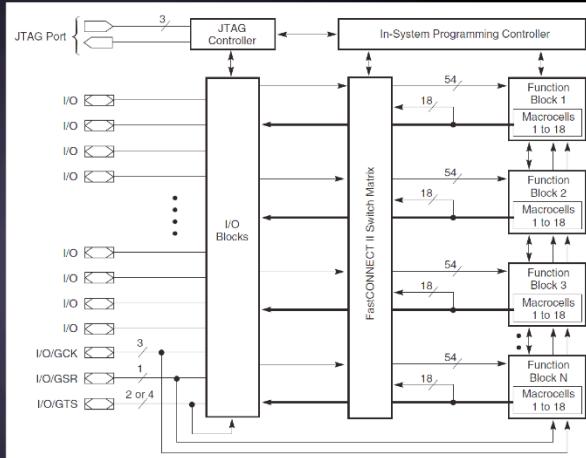


Figure 1: XC9500XL Architecture

Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.



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Here is an overall top-level view of the architecture. Up to 288 Macrocells are connected through the routing matrix to the I/O.

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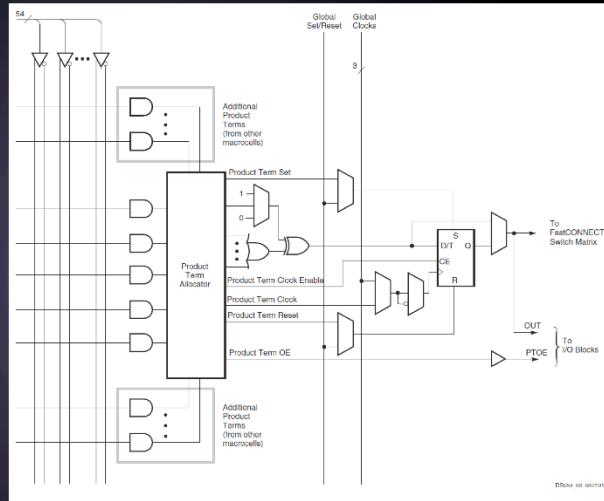


Figure 3: XC9500XL Macrocell Within Function Block



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The next figure shows a more detailed view of the Macrocell architecture. The Macrocell can AND up to 54 signals, and the OR together 5 of these plus 5 from an adjacent macrocell, which may itself have an additional number for other macrocells. Choice of clock, enables, resets, etc. are programmable, either local or global. The macrocell has only 2 outputs to I/O blocks

The image shows the front cover of the Xilinx CoolRunner-II CPLD Family Datasheet (DS090 v3.1, September 11, 2008). The cover features the Xilinx logo and the product name. Several orange arrows point from the text below to specific sections on the cover: one arrow points to the 'Features' section, another to the 'Product Specification' section, and three arrows point to the table of key parameters.

**Xilinx**

**CoolRunner-II CPLD Family**

DS090 (v3.1) September 11, 2008

**Features**

- Optimized for 1.8V systems
- Industry's fastest low power CPLD
- Densities from 32 to 512 macrocells
- Advanced architecture for high speed CPLD
- Optimized architecture for effective logic synthesis
- Multivoltage I/O operation – 1.5V to 3.3V
- Advanced In System Programming
- Fastest in system programming
- 1 MTF using IEEE 1152 JTAG interface
- On-chip 100% JTAG TAP
- IEEE1149.1 JTAG Boundary Scan Test
- Optional Schmitt trigger input (per pin)
- Multiple global output enables
- Unsurpassed low power management
- DataGATE external signal control
- Flash-based internal memory
- Optional DualEDGE triggered registers
- Clock domain crossing
- Global signal options with macrocell control
- Multiple global clocks with phase selection per macrocell
- Multiple global output enables
- Global output drivers
- Abundant product term clocks, output enables and set/reset
- Efficient control term clocks, output enables and set/reset for each macrocell and shared across function blocks
- Advanced design security
- Open-drain output option for Wired-OR and LED applications
- Optional bus-hold, 3-state or weak pullup on selected I/O pins
- Optional configurable grounds on unused I/Os
- Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all parts

**Product Specification**

- SSTL2, 1.5SSTL2, 1, and HSTL\_1 on 128 macrocell and denser devices
- Hot pluggable
- Programmable
- Superior prototyp retention
- 100% product term rotatability across function block
- Wide temperature range operating life pth:
- Chip Scale Package (CSP) BGA, Fine Line BGA, TQFP, POFP, VQFP and QFN packages
- Pb-free available for all packages
- Design verification using Xilinx and industry standard CAE tools
- Free software support for all densities using Xilinx® WebPACK tool
- Industry leading nonvolatile 0.18 micron CMOS process
- Guaranteed 1,200 program/erase cycles
- Guaranteed 20 year data retention

**Family Overview**

Xilinx CoolRunner™-II CPLDs deliver the high speed and ease of use associated with the XC9500XL™ CPLD family, but in a much smaller footprint. The XPA3 family in a single CPLD. This means that the exact same parts can be used for high-speed data communications/switching, as well as low-power control applications, with the added benefit of In System Programming. Low power consumption and high-speed operation are compatible with a variety of packages and assembly techniques. Clocking techniques and other power saving features extend the performance envelope. The XPA3 parts are supported starting with Xilinx ISE® 4.1i WebPACK tool. Additional details can be found in [Further Reading](#).

**Table 1. CoolRunner-II CPLD Family Parameters**

	XC2C2Z	XC2C4A	XC2C12B	XC2C256	XC2C384	XC2C512
Macrocells	32	64	128	256	384	512
Max I/O	33	64	100	184	240	270
$T_{PD}$ (ns)	3.8	4.6	5.7	5.7	7.1	7.1
$T_{SU}$ (ns)	1.9	2.0	2.4	2.4	2.9	2.6
$T_{CO}$ (ns)	3.7	3.9	4.2	4.5	5.8	5.8
F <sub>SYSTEM</sub> (MHz)	323	263	244	256	217	179

Table 1 shows the macrocell capacity and key timing parameters for the CoolRunner-II CPLD family. The parts are Pb-free and support 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all pins.

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Here's the Xilinx CoolRunner II CPLD family datasheet.

Here are some of the significant characteristics of this device that relate directly to our selection criteria.

This part was designed with low power in mind, hence the name, and includes several low power features.

Note the limit in the amount of logic – 512 macrocells, 512 Flip Flops.

This device has up to 270 IO pins, so lots of I/O per register – almost 1:2. This is an I/O rich device as well.

Deterministic timing – 5 ns pin to pin delay

Speed limited to 323 MHz. It's faster for the smaller parts – why do you suppose this is? The parts with more macrocells will have more routing, more capacitance, and therefore slower speeds. This is an example of the scaling problems inherent in CPLDs.

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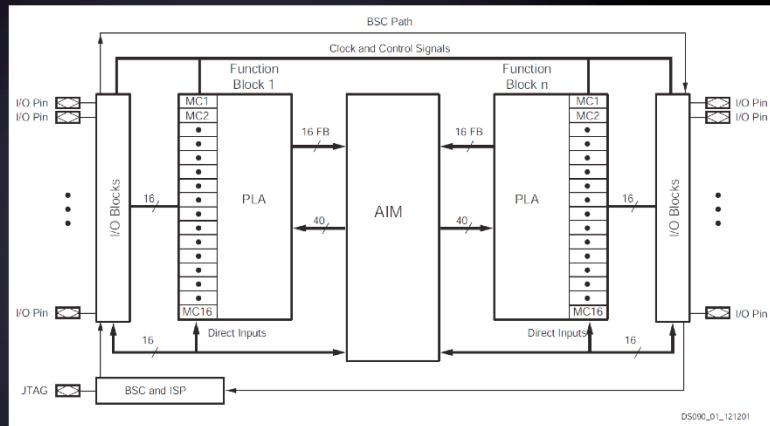


Figure 1: CoolRunner-II CPLD Architecture

Here is an overall top-level view of the architecture. Up to 512 Macrocells are connected through the Advanced Interconnect Matrix or AIM, with each function block connected to the I/O.

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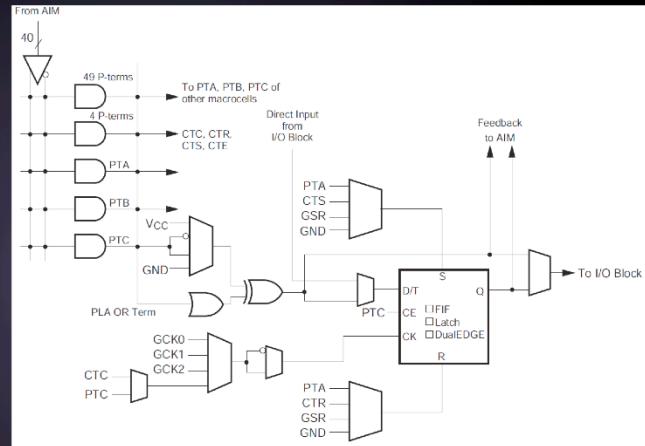


Figure 3: CoolRunner-II CPLD Macrocell

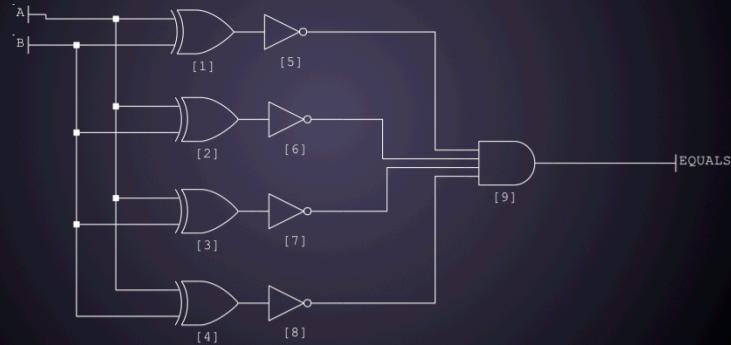
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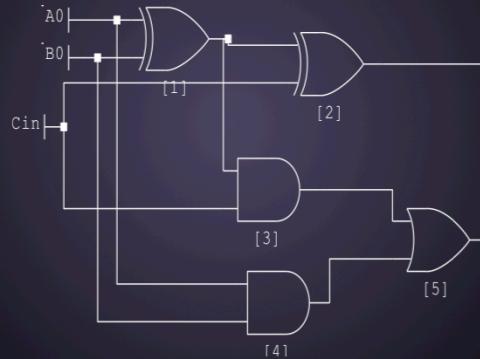
The next figure shows a more detailed view of the CoolRunner II Macrocell architecture, which is very similar to the XC9500XL. The Macrocell can AND up to 40 signals, and then OR together 5 of these. Feedforward from other macrocells is through the AND array. Choice of clock, enables, resets, etc. are programmable, either local or global. The macrocell has only 1 output to the I/O blocks

How large of a comparator in bits can be made using a XC95xx or CoolRunner II Macrocell?



Remember the 4-bit comparator? How wide of a comparator can you build with one macrocell? In theory, since 5 signals are combined each macrocell could generate 5 bits of comparator, a fairly efficient use of the available logic. From this one could also conclude that implementation of address decoders will be efficient.

How large of a comparator in bits can be made using a XC95xx or CoolRunner II Macrocell?



How many full adders can be made in a macrocell? Just 1, as there is only one output. If the EXOR output is used for the sum out, then the carry out can be routed to the next macrocell, just as the carry in comes from the previous one. However, this only uses about 9 gates in one macrocell, which isn't very efficient. Likewise, when implementing a shift register, only the register in each macrocell is used, so the big PLA structures are superfluous.

## Xilinx CPLD Devices Summary

- Xilinx offers 2 CPLD families, the XC9500XL and CoolRunner II. Both are reprogrammable, with deterministic timing and rich in I/O, but are limited in speed and logic density.
- The XC9500XL family has 5 volt tolerant I/O, which can be important in industrial and automotive applications.
- The CoolRunner II is a lower power CPLD family.
- Xilinx CPLDs are efficient in implementation of comparators and decoders, but not efficient in implementation of adders or shift registers.



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In this video we have learned

- Xilinx offers 2 CPLD families, the XC9500XL and CoolRunner II. Both are reprogrammable, with deterministic timing and rich in I/O, but are limited in speed and logic density.
- The XC9500XL family has 5 volt tolerant I/O, which can be important in industrial and automotive applications.
- The CoolRunner II is a lower power CPLD family.
- Xilinx CPLDs are efficient in implementation of comparators and decoders, but not efficient in implementation of adders or shift registers.