Analyze a Design with Quartus Prime

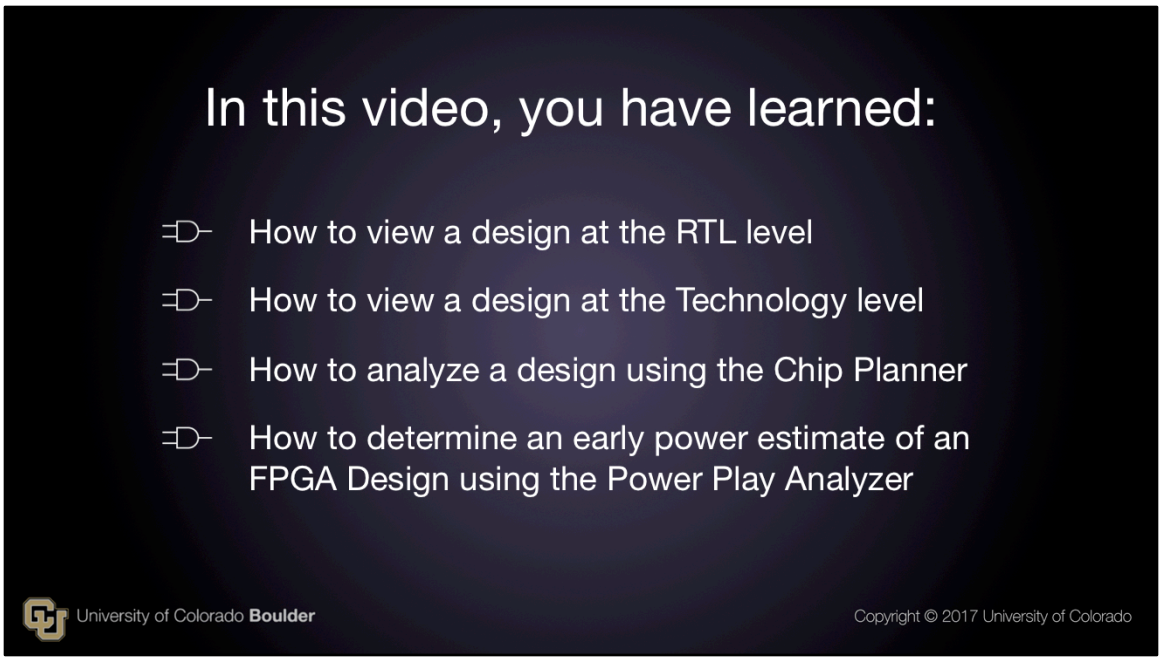
University of Colorado **Boulder**

In this presentation, you will compile an FPGA design in Quartus Prime.

You will use design files from the previous video, Compile a Design in Quartus Prime, so that you can follow along and perform each step along the way.
Feel free to pause the video as you enter commands into Quartus Prime.

Agenda for this Video

1. View a design at the RTL level
2. View a design at the Technology level
3. Analyze a design using the Chip Planner
4. Analyze a design with the Power Play Power Analyzer



In this video, you have learned:

- How to view a design at the RTL level
- How to view a design at the Technology level
- How to analyze a design using the Chip Planner
- How to determine an early power estimate of an FPGA Design using the Power Play Analyzer