

# Altera CPLDs and Small FPGAs

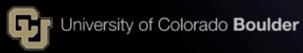


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# Microsemi FPGAs

- IGLOO
- IGLOO2
- Accelerator
- RTAX



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In this video we will continue our survey of modern programmable logic devices, with Large FPGAs from Altera, including the Arria V, the Stratix V, the Arria 10, and the Stratix 10.

## Programmable Logic Device Selection Criteria

	Selection Criteria	FLASH FPGAs	Anti-Fuse
1	Reprogrammability (Configuration Memory Type)	Yes	No
2	Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)	Moderate	Moderate
3	Cost per logic gate	Moderate to high	High
4	Speed (Maximum clock frequency)	400 MHz	870 MHz
5	Power Consumption (static and dynamic)	Very Low	Moderate
6	Cost per I/O (I/O Density) and extent of supported I/O standards	Low, Good	Low, Good
7	Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)	Extensive	Good
8	Deterministic timing (timing is consistent in every implementation)	No	Yes
9	Reliability (FIT rate)	Excellent	Best Available
10	Endurance (number of programming cycles and years of retention)	10K/ 20 year	1/ 20 year
11	Design and Data Security	Best Available	Excellent



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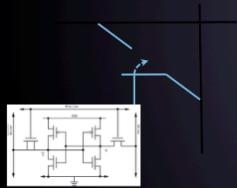
The goal in programmable logic device selection is to pick the best fit part for our requirements. We will use the programmable logic device selection criteria we established earlier to evaluate these devices as listed here.

## FLASH Interconnection Technologies

FPGA Interconnect Technologies are FSRAM, FLASH, and Antifuse

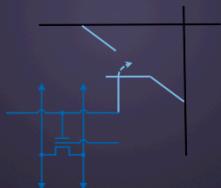
Microsemi manufactures FLASH and Antifuse FPGAs

SRAM



Reprogrammable  
And Volatile

FLASH



Reprogrammable  
and Non-Volatile

Antifuse



One-time Programmable  
and Non-Volatile



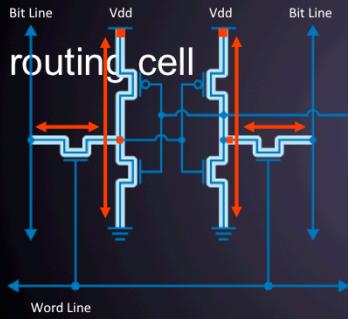
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## Microsemi FLASH Technology Advantages

### FPGA SRAM routing Cell



### FLASH



1000x Lower Leakage Leakage  
Very low static current



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## Microsemi FLASH Technology Advantages

1. True FLASH-Based Technology
2. Live at Power-up
3. Integration provides lower total system cost
4. Low power across the board
5. Best Design Security
6. Superior Reliability



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# Microsemi IGLOO nano

IGLOO nano Devices	AGLN010	AGLN015 <sup>1</sup>	AGLN020	AGLN030Z <sup>1</sup>	AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices <sup>1</sup>				AGLN060Z <sup>1</sup>	AGLN125Z <sup>1</sup>	AGLN250Z <sup>1</sup>	
System Gates	10,000	15,000	20,000	30,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	128	172	256	512	1,024	2,048
VersaTiles (D-flip-flops)	260	384	520	768	1,536	3,072	6,144
Flash*Freeze Mode (typical, $\mu$ W)	2	4	4	5	10	16	24
RAM Kbits (1,024 bits) <sup>2</sup>	—	—	—	—	18	36	36
4,608-Bit Blocks <sup>2</sup>	—	—	—	—	4	8	8
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1
Secure (AES) ISP <sup>2</sup>	—	—	—	—	Yes	Yes	Yes
Integrated PLL in CCCs <sup>2,3</sup>	—	—	—	—	1	1	1
VersaNet Globals	4	4	4	6	18	18	18
I/O Banks	2	3	3	2	2	2	4
Maximum User I/Os (packaged device)	34	49	52	77	71	71	68
Maximum User I/Os (Known Good Die)	34	—	52	83	71	71	68



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# Microsemi IGLOO nano

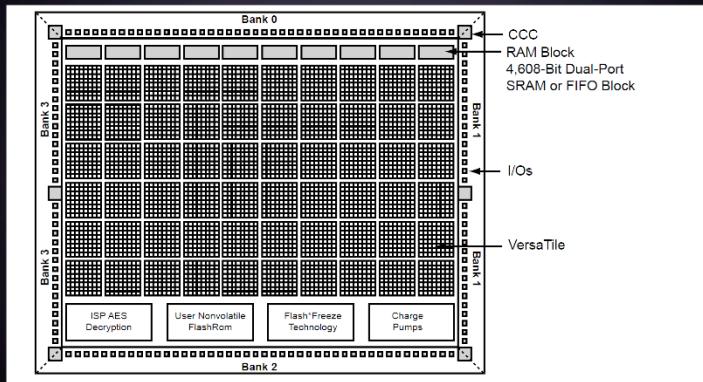


Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)



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# Microsemi IGLOO nano

LUT-3 Equivalent



D-Flip-Flop with Clear or Set



Enable D-Flip-Flop with Clear or Set

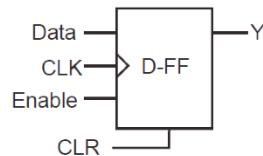


Figure 1-6 • VersaTile Configurations



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## Microsemi SmartFusion

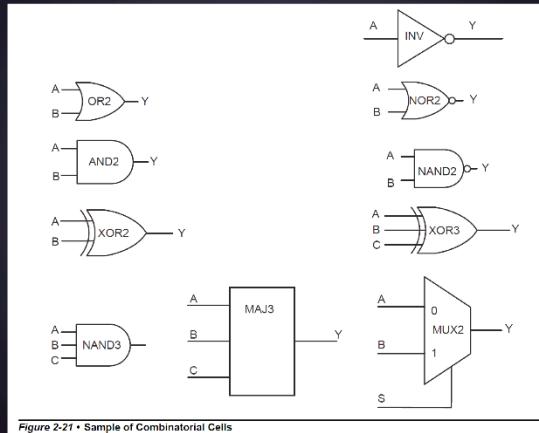


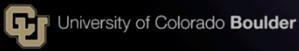
Figure 2-21 • Sample of Combinatorial Cells

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# Microsemi IGLOO2

Table 1 • IGLOO2 FPGA Product Family

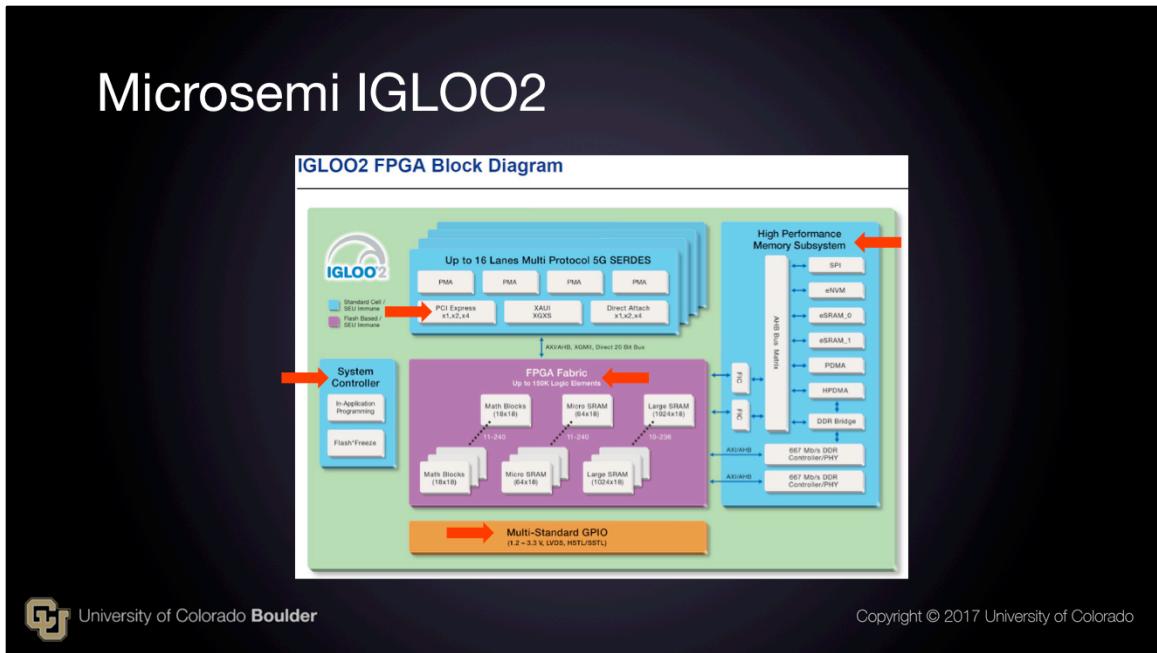
	M2GL005 (S)	M2GL010 (B/T/TB)	M2GL025 (T/TB)	M2GL050 (T/TB)	M2GL060 (T/TB)	M2GL090 (T/TB)	M2GL150 (T/TB)
Features <sup>2,3</sup>							
Maximum Logic Cells (4LUT + DFF) <sup>4</sup>	8,080	12,084	27,896	56,340	58,520	88,164	148,124
Math Nodes (18x18)	11	22	34	72	72	84	240
PoC/DS							
PLLs and CCs	2			6			8
SPI/HW/PCIe/RDMA				1 each			
Fabric Interface Controller (FCo)	1		2		1		2
Data Security				AES256, SHA256, RNG		AES256, SHA256, RNG, ECC, PUF	
eNVM (K Bytes)	128			256			512
LSRAM 16K Blocks	10	21	31	69	69	109	238
Memory							
uSRAM/MK Blocks	11	22	34	72	72	112	240
eDRAM (K Bytes)				64			
Memory							
Total RAM (K bits)	703	912	1104	1828	1828	2588	5000
DDR Controllers			1x16	2x36	1x16	1x16	2x36
SERDES Lanes (T)	0		4	8	4	4	16
User I/Os							
PCIe End Points	0		1		2		4
MSIO (3.3 V)	119	123	157	139	271	309	292
MSIOD (2.5 V)	28	40	40	62	40	40	106
DCDIO (2.5 V)	66	70	70	176	76	76	176
Total User I/O	209	233	267	377	387	425	514
Grades	Commercial (C), Industrial (I), Military (M), Automotive (A), T1/T2	C, I, M, T1, T2	C, I, M, T1, T2			C, I, M	



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# Microsemi IGLOO2



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# Microsemi IGLOO2

## Security

- Design Security Features (available on all devices)
  - Intellectual Property (IP) Protection through Unique Security Features and Use Models New to the PLD Industry
  - Encrypted User Key and Bitstream Loading, Enabling Programming in Less-Trusted Locations
  - Supply-Chain Assurance Device Certificate
  - Enhanced Anti-Tamper Features
  - Zeroization
- Data Security Features (available on premium devices)
  - Non-Deterministic Random Bit Generator (NRBG)
  - User Cryptographic Services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) Engine)
  - User Physically Unclonable Function (PUF) Key Enrollment and Regeneration
  - CRI Pass-Through DPA Patent Portfolio License
  - Hardware Firewalls Protecting Microcontroller Subsystem (HPMS) Memories

## Reliability

- Single Event Upset (SEU) Immune
  - Zero FIT FPGA Configuration Cells
  - Junction Temperature: 125°C – Military Temperature, 100°C – Industrial Temperature, 85°C – Commercial Temperature
- Single Error Correct Double Error Detect (SECDED) Protection on the Following:
  - Embedded Memory (eSRAMs)
  - PCIe Buffer
  - DDR Memory Controllers with Optional SECDED Modes
  - Buffers Implemented with SEU Resistant Latches on the Following:
    - DDR Bridges (HPMS, MDDR, FDDR)
    - SPI FIFO
  - NVM Integrity Check at Power-Up and On-Demand
  - No External Configuration Memory Required—Instant-On, Retains Configuration When Powered Off



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# Microsemi IGLOO2

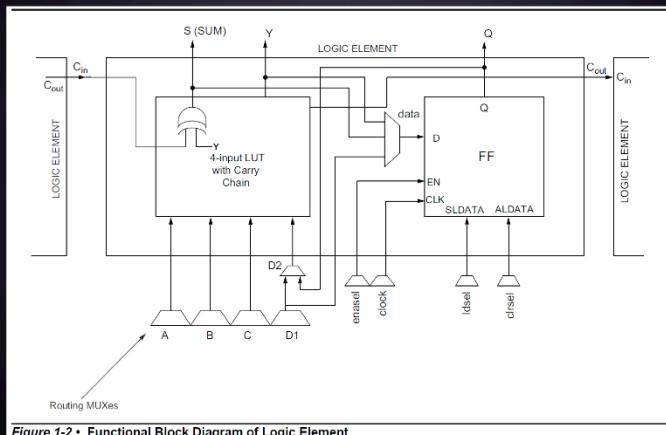


Figure 1-2 • Functional Block Diagram of Logic Element

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# Microsemi Accelerator FPGA Family

Table 1 • Accelerator Family Product Profile

Device	AX125	AX250	AX500	AX1000	AX2000
Capacity (in Equivalent System Gates)	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Modules					
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Maximum Flip-Flops	1,344	2,816	5,376	12,096	21,504
Embedded RAM/FIFO					
Number of Core RAM Blocks	4	12	16	36	64
Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Clocks (Segmentable)					
Hardwired	4	4	4	4	4
Routed	4	4	4	4	4
PLLs	8	8	8	8	8
I/Os					
I/O Banks	8	8	8	8	8
Maximum User I/Os	168	248	336	516	684
Maximum LVDS Channels	84	124	168	258	342
Total I/O Registers	504	744	1,008	1,548	2,052
Package					
PQ		208	208	729	
BG				484, 676, 896	
FG	256, 324	256, 484	484, 676	352	896, 1152
CQ		208, 352	208, 352	624	256, 352
CG					624



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# Microsemi Accelerator Layout

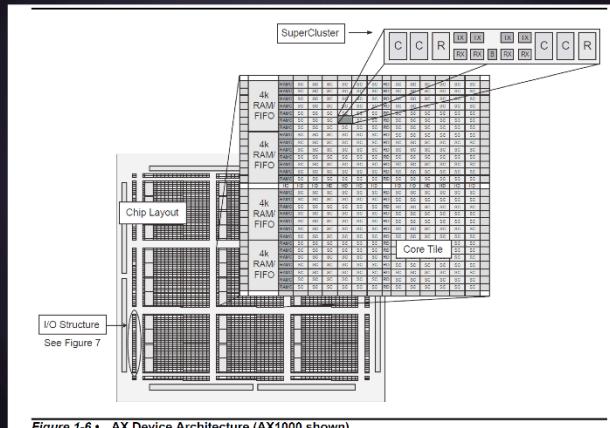


Figure 1-6 • AX Device Architecture (AX1000 shown)

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# Microsemi Accelerator Layout

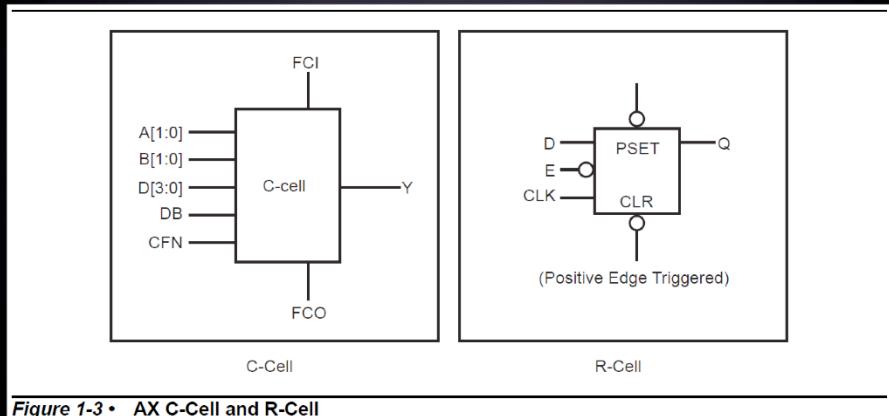


Figure 1-3 • AX C-Cell and R-Cell



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# Microsemi RTAX Rad-Hard FPGA Family

Table 1 • RTAX Family Product Profile

Device	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL	RTAX2000D/DL	RTAX4000D/DL
<b>Capacity</b>						
Equivalent System Gates	250,000	1,000,000	2,000,000	4,000,000	2,000,000	4,000,000
ASIC Gates	30,000	125,000	250,000	500,000	250,000	500,000
<b>Modules</b>						
Register (R-cells)	1,408	6,048	10,752	20,160	9,856	18,480
Combinatorial (C-cells)	2,816	12,096	21,504	40,320	19,712	36,960
<b>Embedded RAM/FIFO (w/o EDAC)</b>						
Core RAM Blocks	12	36	64	120	64	120
Core RAM Bits (K = 1,024)	54 k	162 k	288 k	540 k	288 k	540 k
<b>Embedded Multiply/Accumulate Blocks</b>	—	—	—	—	64	120
<b>Clocks (segmentable)</b>						
Hardwired	4	4	4	4	4	4
Routed	4	4	4	4	4	4
<b>I/Os</b>						
I/O Banks	8	8	8	8	8	8
User I/Os (maximum)	198	418	684	840	684	840
I/O Registers	744	1,548	2,052	2,520	2,052	2,520
<b>Package</b>						
CG/LG	624	624	624, 1,152	1,272	1,272	1,272
CQ	208, 352	352	256, 352	352	352	352



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## Microsemi RTAX Logic

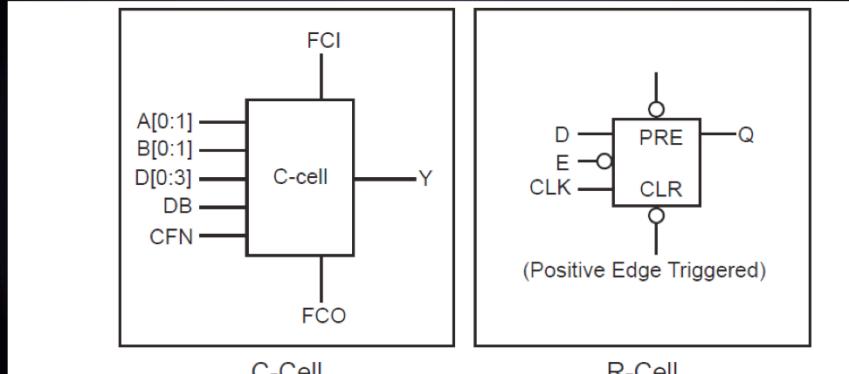


Figure 1-3 • RTAX C-Cell and R-Cell

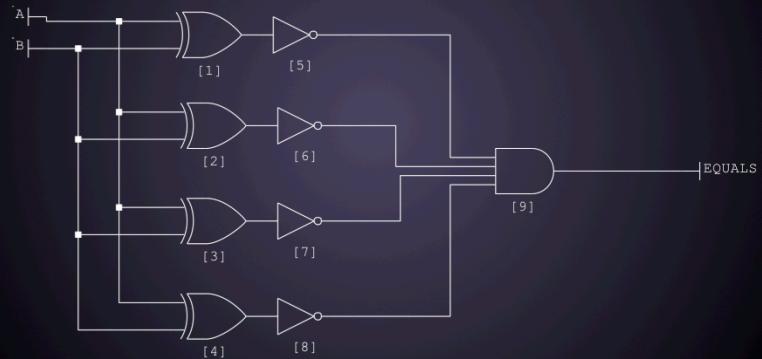


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## How large of a comparator can be made using an IGLOO Logic Cell?

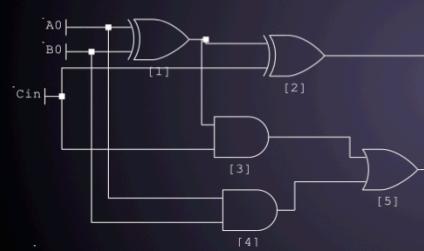


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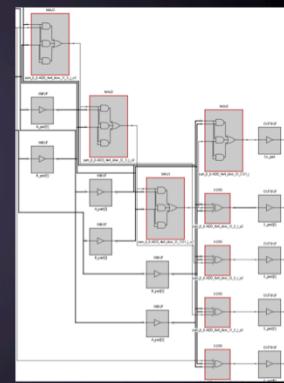
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How many full adders can be created in a IGLOO?



1 bit full adder



4 bit adder in 8 Versatiles



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## Microsemi FPGAs Summary

- ⇒ Microsemi offers both FLASH and Antifuse FPGAs. Each type has different capabilities and limitations.
- ⇒ The current Microsemi FLASH FPGA offering, the IGLOO and IGLOO2, are instant-on single chip solutions that are reprogrammable, with very good low power performance and high reliability and security.
- ⇒ Microsemi Antifuse FPGAs are designed for rugged environments and high reliability, including the Accelerator family and the RTAX radiation tolerant family.
- ⇒ The Microsemi IGLOO2 has a wealth of hard IP cores included, including memory controllers, high-speed transceivers, RAMs, DSP blocks, and many security enhancements.
- ⇒ If security or reliability or low power are design requirements, Microsemi FPGAs are worth consideration.



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