Interactive Transcript



Help us translate!

0:00

Let's take a closer look at FPGA architecture to see how

these devices are put together and why.

In the first module we introduced programmable logic devices in the FPGA.

0:12

In module two, we used Quartus Prime to work through a sample FPGA design.

0:17

In this module, we will extend our knowledge of FPGA capabilities so

that we can choose the right one when working on a design.

0:26

Designing digital devices is a creative process,

much like cooking up a new recipe or painting a new picture.

To be proficient,

we need to know what ingredients are available to make our new creation.

0:39

Xilinx, Altera, Microsemi and Lattice all make great programmable logic devices,

but none of them will work for every application.

Each vendor has their specialities.

Have you ever wondered why use this one instead of that one?

If so you're in luck, because we are going to answer this question.

In this module we'll look at a set of criteria to evaluate these devices.

To help us decide which one is best for a particular application.

1:07

What are the essential capabilities that we need to get from an FPGA?

First, it needs to provide ample amounts of logic.

The more the better, as the value tends to rise faster than cause as FPGAs get large.

Smaller FPGA process geometries usually translate in the higher logic density.

The amount of logic is measured in a number of ways, system gates,

logic elements, slices, macrocells, LABs, ALMs, etc.

The course if the part cost too much for a design budget,

then the benefits from the logic device won't be accrued.

So cost and particularly cost per gate is important.

Another essential FPGA characteristic is processing speed,

often measured by the maximum clock frequency or fmax.

Speed is also important in the IO, as well as the fabric.

In direct opposition to speed is the requirement for low power consumption.

FPGAs consume considerable power, both when operating at high frequencies but

also the path does nothing it draws static power.

Depending on architecture and the configuration memory type,

power consumption can vary from microwatts to hundreds of watts.

2:23

Reprogrammability is also dependent on the configuration memory type.

SRAM and Flash are reprogrammable antifuses node.

Reprogrammability makes development much easier,

as new designs can be programmed into the same part over and over again.

In addition to internal capabilities,

external interfaces to the FPGA are also important.

Modern FPGAs can be tied to a large variety of I/O types.

One measure of value is the cost per I/O and

the I/O density relative to the logic on a part.

2:59

Another way to increase the value of an FPGA is by inclusion of Hard IP cores,

like those for Memory, DSP Blocks, Transceivers, and even hard processors.

Some devices, particularly CPLDs and

smaller FPGAs, are structured so that the timing is deterministic.

It remains consistent for a function,

even as the part is rerouted based on a new design.

3:24

In some applications, like safety critical designs, reliability

is a major concern measured by the fit rate or mean time between failure.

3:35

Endurance of the Configuration Memory can be an issue for

long lifetime products, and is an important parameter in FLASH based FPGAs.

3:46

Increasingly important is the ability to protect design information held in

the FPGA bit pattern, and also the data that travels through the FPGA.

In summary,

here is the Programmable Logic Device Selection Criteria we'll use as we survey

available FPGA devices and technology from all the major vendors.

There are eleven criteria, Reprogrammability, or

Configuration Memory Type.

4:15

Size or Logic Density, the amount o logic in system gates, or LEs,

or Slices, or ALMs.

Cost per logic gate, Speed or Maximum clock frequency.

Power Consumption, both Static and Dynamic.

Cost per I/O relative to I/O density.

4:36

Hard IP available on the chip, like Memory, DSP Blocks, Transceivers, etc.

4:43

Deterministic timing, where timing is Consistent in every implementation.

4:49

Reliability measured by the FIT rate.

4:53

Endurance, the number of programming cycles and years of retention, and

Design and Data Security.

Interactive Transcript



Help us translate!

0:00

In this video, we will start our survey of modern programmable logic devices,

beginning with CPLDs from Xilinx.

We will use the programmable logic device selection criteria we established earlier

to evaluate these devices.

To reiterate, there are 11 criteria, size or logic density,

which is the amount of logic in system gates, or LEs, or slices, or ALMs.

Cost per logic gate, speed, which is the maximum clock frequency,

0:34

power consumption, static and dynamic, reprogrammability.

0:42

Cost per I/O, or I/O density, Hard IP available on chip,

like memory, DSP blocks, transceivers, etc, deterministic timing,

where the timing is consistent in every implementation.

1:00

Reliability, which can be measured by the FIT rate, endurance, which is the number

of programming cycles and years of retention, design and data security.

1:13

Here's the XILINX XC9500XL CPLD Family Data Sheet,

which you can find on the xilinx.com website.

Why do you look at the data sheet?

Generally, we're trying to determine if we can use this part in our design

by looking at its specified performance characteristics.

I'd like to highlight some of the significant characteristics of this device

that relate directly to our selection criteria.

1:43

Deterministic timing, 5 ns pin-to-pin delay, 5V I/O, say that with gusto.

These products are used as voltage translators, especially in automotive

applications, where much legacy equipment still runs on 5V.

2:00

I myself have used an XC9572XL in the design of

an industrial product for this very reason.

2:10

This is a device with FLASH cells for routing.

It is reprogrammable.

2:17

20 years data retention is good, as is 10,000 programming cycles endurance.

2:24

Note the limit in the amount of logic, 288 macrocells,

6,400 gates, 288 footflops.

2:33

The speed is also limited to 208 MHz.

This device has up to 192 I/O pins, so

lots of I/O per register, almost one to one.

This is an I/O rich device, unlike an EPIGA,

which would be register rich and I/O scarce.

2:52

Here's an overall top level view of the architecture.

2:55

Up to 288 macrocells are connected through the routing matrix to the I/O.

3:02

The next figure shows a more detailed view of the macrocell architecture.

The macrocell can and up to 54 signals and

then or together 5 of these plus 5 from an adjacent macrocell,

which may itself have an additional number for other macrocells.

Choice of clock enables, resets, etc, are programmable.

They're either local or global.

The macrocell has only two outputs to the I/O blocks.

3:32

Here is the XILINX CoolRunner-II CPLD Family Data Sheet.

Here are some of the significant characteristics of this device

that relate directly to our selection criteria.

3:44

This part was designed with low power in mind, hence the name, and

includes several low power features.

3:52

Note the limit in the amount of logic, 512 macrocells, 512 flip flops.

4:00

This device has up to 270 I/O pins, so

lots of I/O per register, almost one to two.

This is an I/O rich device as well.

4:11

It has deterministic timing, 5 ns pin to pin delay.

The speed's limited to 323 MHz, it's faster for smaller parts.

Why do you suppose this is?

The parts with the more macrocells will have more routing, more capacitance, and

therefore, slower speeds.

This is an example of the scaling problems inherent in CPLDs.

This is a device with non-volatile configuration memory that

is transferred to SRAM cells for routing, it is reprogrammable.

20 years data retention is good, as is 1,000 programming cycles endurance.

4:49

Here's an overall top level view of the architecture.

Up to 512 macrocells are connected through the advanced interconnected matrix,

or AIM, with each function block connected to the I/O.

5:03

The next figure shows a more detailed view of the CoolRunner-II Macrocell

architecture, which is very similar to the XC9500XL.

The macrocell can and up to 40 signals and then or together 5 of these.

Feed forward from other macrocells is through the and array.

Choice of clock enables, resets, etc, are programmable, either local or global.

The macrocell has only one output to the I/O blocks.

Remember the 4-bit comparator?

How wide of a comparator can you build with one macrocell?

In theory, since 5 signals are combined, each macrocell could generate 5

bits of comparator, a fairly efficient use of available logic.

From this, one could also conclude

that the implementation of address decoders will be efficient.

5:54

How many full adders can be made in a macrocell?

Just one, as there is only one output.

If the XOR output is used for the sum-out, then the carry-out can be routed to

the next macrocell, just as the carry-in comes from the previous one.

However, this will only uses about nine gates in one macrocell,

which isn't very efficient.

LIkewise, when implementing a shift register,

only the register in each macrocell is used.

So the big PLA structures are superfluous.

6:24

In this video, we have learned Xilinx offers two CPLD families,

the XC9500XL and the CoolRunner II.

Both are reprogrammable with deterministic timing and rich in I/O,

but are limited in speed and logic density.

The XC9500XL family has 5 volt tolerant I/O,

which can be important in industrial and automotive applications.

6:50

The CoolRunner II is a lower power CPLD family.

6:55

Xilinx CPLDs are efficient in the implementation of comparators and

decoders, but not efficient in the implementation of adders or

shift registers.

Interactive Transcript



Help us translate!

0:00

In this video, we will continue our survey of modern programmable logic devices

with small FPGAs from Xilinx including the Spartan 3AN and the Spartan 6.

We will use the Programmable Logic Device Selection Criteria we

established earlier to evaluate these devices.

As a reminder, there are 11 criteria.

Size or Logic Density, the amount of logic

in systems gates or LEs or Slices or ALMs.

Cost per logic gate, the Speed, their maximum clock frequency,

Power Consumption, both static and dynamic, Reprogrammability or

the configuration memory type, cost per I/O or I/O Density,

Hard IP available on chip, the memory, DSP, Blocks, Transceivers, etc.

Deterministic timing (timing is consistent in every implementation), Reliability,

measured by the FIT rate, Endurance, the number of programming cycles and

years of retention, and Design and Data Security.

Here's a portion of the Xilinx Spartan 3AN FPGA family data sheet.

The Spartan 3AN has reprogrammable flash configuration and user memory.

Note the equivalent gates up to 1.4 million.

25 K logic cells, considerably more logic than the CPLDs have.

This part is designed for low cost.

If you need more logic than this,

then you need to select the larger part that will meet your requirements.

We'll talk about larger parts as we continue in this module.

The speed is limited to 350 megahertz on global

clock buffers, which is faster than CPLDs.

Maximum power draw is between 20 and 200 milliamps depending on part size.

This device has up to 502 I/O pins, a 50 to 1 ratio of logic cells to I/O.

There are 23 supported I/O standards.

20 years data retention is good, as is 100,000 programming cycles endurance.

Design security is enhanced by the integration of the configuration

memory on a single chip.

Hard IP blocks have been added including RAM blocks,

multipliers, and Digital Clock Managers.

Initially, programmable logic devices specify most information in

the data sheet.

However, now not all the information is found in the data sheet.

Some is found in the corresponding user's guide or handbook.

Here is the overall architecture of the Spartan 3.

I/O is on the outside and includes logic blocks,

RAM, multipliers and clock manager.

Here is a picture of a Spartan 3 slice, one-half of a logic block.

The heart of the slice is 2 4-input LUTs and 2 flip-flop outputs.

It also has some carry chain logic for creating adders and

shift clock generation to make shift registers.

This is a simplified picture of the LUT resources in a slice.

The LUTs can also be used as distributed memory.

Each LUT is 16-bits of RAM, or has a 16-bit shift register.

Here is a portion of the Xilinx Spartan 6 FPGA family data sheet.

The Spartan 6 has reprogrammable SRAM configuration,

which requires an external nonvolatile memory,

usually a flash memory, to load the configuration at power up.

The delay before the device becomes active is several milliseconds.

Note it has up to a 147 K logic cells, considerably more logic.

This part is designed for low cost.

Additional Hard IP blocks are included, including 180 DSP slices,

almost 5,000 kilobytes of Block RAM, and

up to 8 High-Speed Transceivers.

This device has up to 540 I/O pins, a 300 to 1 ratio of logic cells to I/O.

There are 55 supported I/O standards.

Speed is limited to 400 megahertz on global clock buffers

which is faster than CPLDs.

Maximum static power draw is between 20 and 51 milliamps depending on part size.

Dynamic power is not specified.

Other information is found in several user's guides.

Here is a picture of a Spartan 6 slice, one-quarter of a logic block.

The heart of the slice is 4 6-input LUTs and 8 flip-flops.

It also has some carry chain logic for creating adders.

There are three types of slices with varying capabilities.

As you can see, the logic is becoming more and more complex.

This is a simplified picture of the LUT resources in the slice.

The LUTs can also be used as distributed memory.

Each slice can create up to a 256 by 1 RAM or

ROM or as a 32-bit shift register per slice.

Recall, the 4-bit comparator.

How many comparator bits can be implemented in a LUT?

In the 3AN case there are only 4-inputs, so only a 2-bit comparator can be created.

Larger comparators require that the LUTs be cascaded.

Although the logic is efficiently used,

there is an added delay relative to the CPLD implementation.

In the Spartan 6 case, the 6-input LUT will handle 3-bits of comparators,

so wider comparators can be made with less delay.

How many full adders can be made in a logic cell?

For a Spartan 3AN at first blush, it would seem to require 2 LUTs per 1 adder.

The logic on the left can be implemented in 2 LUTs with

3-inputs each to generate the sum and the carry.

The problem with this implementation, that it requires 2 LUT for every input bit,

and the carry propagates through the full LUT delay for each bit.

A better implementation is to use look ahead and determine if the input carry

signal needs to be propagated where the inputs are different, or

generated when both inputs are high.

This is shown on the left.

To optimize the implementation of this logic, the Spartan-3 Generation CLB

provides a dedicated XOR gate outside the LUT, to generate the sum called

the XORCY and a dedicated MUX to provide the carry called the MUXCY.

In this way, each LUT can implement 1 full adder bit.

This structure makes more efficient use of logic resources

than what was seen in the CPLDs.

This is also true of shift registers,

which can be implemented entirely using the LUT, 16-bits per LUT for

a Spartan 3AN, 32-bits per slice for the Spartan 6.

In this video, we have learned Xilinx offers several smaller FPGA families,

including the Spartan 3AN and Spartan 6, which are both currently available.

The Spartan 3AN uses a on-chip FLASH configuration memory,

so it is a single-chip solution.

The Spartan 6 uses SRAM configuration memory, so

it needs an additional nonvolatile memory device to hold the configuration.

The Spartan 3AN has a logic cell based on a 4-input LUT and a flip-flop,

with additional logic to help efficiently create adders and shift registers.

The Spartan 6 has a 6-input LUT with 2 flip-flops per logic cell.

Xilinx small FPGAs are more efficient in implementation of adders or

shift registers than CPLDs.

Xilinx small FPGAs include additional Hard IP blocks, including Multipliers and

DSP, RAM blocks, Clock generation, and High-Speed Transceivers.

Interactive Transcript



Help us translate!

0:00

In this video, we will continue our survey of modern programmable logic

devices with large FBGA and Xylinks, including the Artex-7, Kentex-7,

and the Vertex-7, and the Kentex and Vertex ultra-scale device families.

We will again use the rogrammable logic device selection criteria we

established earlier to evaluate these devices.

0:24

To reiterate, there are 11 criteria, size or logic density,

which is the amount of logic in systems gates, LEs, Slices, or

ALMs, cost per logic gate, speed or

the maximum clock frequency, power consumption, both static and

dynamic, reprogrammability and the configuration memory type,

cost per I/O or I/O density,

hard IP available on chip which include memory, DSP blocks, transceivers etc.

1:01

Deterministic timing where the time is consistent in every implementation

1:07

reliability measured by the FIT rate, endurance or the number

of programming cycles and years of retention, and design and data security.

1:19

He's a portion of the Xilinx 7 series product selection guide

providing an overview of the Artix-7 mid-range FPGA.

At this stage of development, the FPGAs selection process has become so

bewildering that the vendors are producing selection guides in addition to the data

sheets and users guides.

1:40

The Artix-7 has reprogrammable SM configuration

which requires an external non vault or memory,

usually a flash memory, throughout the configuration of power up.

The delay before the device becomes active is several milliseconds.

The size of these devices goes to 215,000 logic sales.

This is sufficient to build a large 32 bit CPU on the FPGA.

2:05

Speed is limited to 628 megahertz on clock buffers.

And a 1,412 mega hertz toggle frequency

which is much faster than previous devices.

Transceivers now run to 6.6 gigabits per second.

2:21

Maximum static power draws between 48 and

320 milliamps of one volt depending port size.

Dynamic power is not specified.

Power estimation tools are used to determine this now.

This device has up to 500 I/O pins, a 400 to 1 ratio of logic cells to I/O.

There are 36 supported IO standards.

Hard IP blocks have been added, including RAM blocks.

2:48

Clock management tiles with face lock loops, DSP slices,

PCIe transceivers, and even an analog-to-digital converter.

3:00

There's also a DDR3 interface that runs at 1,066 megabits per second.

3:07

Here's a portion of the XYLEX 7 series product selection guide providing

an overview of the Kintex-7 large FPGA.

The Kintex-7 has reprogrammable SRAM configuration which

requires an external nonvolatile memory to load the configuration at power up.

3:26

The size of these devices goes to 477,000 logic cells,

twice as large as the Arctic 7.

The speed is limited to 741 mega hertz on clock buffers.

And an 1,818 megahertz toggle frequency which is much faster than previous

devices.

Transceivers now run to 12.5 gigabits per second.

The maximum static power draw is between 201 and

1,080 milliamps at one volt, depending on the part size.

Dynamic power is not specified.

Power summation tools are used to determine this now.

This device is up to 500 I/O pins, almost a 1000 to 1 ratio of logic cells to I/O.

There are 36 supported I/O standards.

Hard IP blocks are the same as Arctic seven including RAM blocks,

clock management tiles, the clock face lock loops, DSP slices,

PCIe transceivers, and an analog-to-digital converter.

There's also a DDR3 interface that runs at 1,866 megabits per second.

4:35

Here's a portion of Zynec Seven series product selection guide.

Providing an overview of the Virtex-7 large FPGA.

The Virtex-7 has reprogrammable SRAM configuration, which requires

an external non-volatile memory to load the configuration and power up.

The size of these devices goes to almost two million logic cells,

four times as large as a Kintex-7.

5:00

Speed is limited to 741 megahertz on collect buffers, and

in 1,818 megahertz toggle frequency, which is much faster than previous devices.

Transceivers now run to 28.05 gigabits per second.

5:16

Maximum static power draw is between 1,012 and

3,756 milliamps at one volt depending on part size.

Dynamic power is not specified.

Prior estimation tools are used to determine this now.

These devices consume up to a range of 100 watts.

So heat sinks are often necessary.

5:39

This device has up to 1,100 I/O pins,

almost a 2,000 to 1 ratio of logic cells to I/O.

There are 36 supported I/O standards.

Hard IP blocks are the same as Arctic 7 including RAM blocks.

Clock management tiles of phase lock loops.

DSP Slices PCIe transceivers and an analog to digital converter.

There's also a DDR three interface that runs at 1,866 megabits per second.

6:10

Here's a simplified diagram of the series seven slice,

which is the same as the slice in the Spartan six.

It's not a big surprise that it is the same.

Given the time and effort that designers have put into optimizing the logic cell.

Once they find something that works they tend to repeat it.

6:28

It is based on four six input lots and eight foot flops.

It can create one single bit full adder per lot and

each lot can become a 32 bit shift register.

6:40

Here's a portion of the Xilinx UltraScale product selection guide,

providing an overview of the Kintex UltraScale FPGA.

6:48

The Kintex UltraScale has a reprogrammable s ramp configuration which requires

an external non-volatile memory to load the configuration at power up.

6:58

The size of these devices goes to 1.4 million logic cells.

7:03

Speed is limited to 850 megahertz like clock buffers

which is faster than previous devices.

Transceiver run up to 16.3 gigabits per second.

The max-min static power draw is between 1,097 and

3,181 milliamps or one volt depending on part size.

Dynamic power is not specified,

power estimation tools are used to determine this now.

This device is up to 676 I/O pins, almost to 2,000 to 1 ratio of logic cells to I/O.

There are 41 supported I/O standards.

7:40

Hard IP blocks are the same as the seven series,

with the notable addition of the 100 gigabit ethernet interface.

There's also a DDR4 interface that runs at 2,400 megabits per second.

7:54

Everything is bigger and faster in the UltraScale.

7:57

Here's a portion of the Xilinks UltraScale product selection guide providing

an overview of the Virtex UltraScale large FPGA.

The Virtex UltraScale has reprogrammable SRAM configuration which requires

an external non-volatile memory to load the configuration at power up.

8:14

The size of these devices goes to over 5 million logic sales.

Two times as large as the Kintex UltraScale.

8:22

Speed is limited to 850 megahertz on clock buffers.

Transceivers, now, run to 30.5 gigabits per second

with aggregate bandwidth to an amazing 3.66 terabytes per second.

The maximum static power draw is between 1,581 and

7,988 milliamps at one volt, depending on part size.

8:45

Dynamic power is not specified.

Power summation tools are used to determine this now.

These devices consume up to the range of 100 watts.

So heat sinks are often necessary, this device has up to 1,400 I/O pins almost

a 4,000 to one ratio of logic cells to I/O, there are 36 supported I/O standards.

9:08

Hard IP blocks the same as the seven series with the noble addition of the 100

gigabit ethernet interface, block RAM now totals to 132 megabits.

There's also a DDR4 interface that runs at 2,400 megabits per second.

9:25

This is a picture of the logic cell and the UltraScale FPGA family.

It's very similar to series 7 logic cell.

With a six input LUT and two flip flops with intervening carry logic.

However, there are eight of these cells in a single logic slice instead of four as

there was in the series seven.

When used a distributed RAM, these LUTs are more capable of providing

up to 64 bits of RAM per LUT up to 512 bits per slice.

In a type M slice, the lets can also provide 32bits of shift registry each.

9:58

You can find up to date information on all Xilinx FPGAs at

www.xilinx.com/products/silicon-devices/f- pga.

Recall the 4bit comparator.

How many comparator bits can be implemented in a lot?

In the Ultrascale architecture the six input levels will handle three bits of

comparator.

So wider comparators can be made with less delay.

10:24

How many full adders can be made in Ultrascale logic cell?

Given there are two outputs each cell should be able to easily generate

a full adder per cell using the standard approach.

This is also looking at approach which provides faster performance.

10:41

In this video, we have learned Xilinx offers several large FPGA families,

including the Artix-7, Kintex-7, and

Virtex-7 as well as the Kintex Ultrascale and Virtex Ultrascale.

These are large devices with up to five million logic cells.

Speed has increased greatly with these large FPGAs,

with internal clock trees running up to 850 megahertz and transceivers

at 30 gigabits per second with aggregate bandwidth of 3.66 terabits per second.

11:13

Xilinx large FPGAs are rich in added hard IP blocks, which include Memory,

PLLs, DSP, PCIe generation one, two, and three transceivers,

100G Ethernet Interfaces, and even 12 bit ADCs in some cases.



Help us translate!

0:00

In this video,

we will continue our survey of modern programmable logic devices where CPLDs and

smaller FPGAs from Altera, including the MAX 5, the MAX 10, and the Cyclone 5.

The goal in programmable logic device selection is to pick the best fit part for

our requirements.

We will use the programmable logic device selection criteria we established earlier

to evaluate these devices as listed here.

0:26

Here's a portion of the Altera Max V CPLD Family Device handbook.

The Altera Max V has re-programmable flash configuration and

user memory, although the routing switches are based on SRAM.

On power-up the device transfers the configuration memory in flash to the S ram

in about half a millisecond.

Note that the logic available is up to 2,210 logic elements,

more logic than the other CPLD's we have considered.

Speed is limited to 304 megahertz on global clock buffers which is about

par with other CPLD's.

1:01

Maximum static power drives between 0.09 and

2 milliamps depending on the part size.

So these are low power parts.

Dynamic power's not specified.

We use the power play analyzer tool to determine it.

1:17

This device has up to 271 IO pins, an 8:1 ratio of logic cells to IO.

There are nine supported I/O standards.

Data retention's not specified.

Programming cycles' endurance is somewhat minimal.

There is deterministic timing, 7 nanoseconds pin-to-pin delay.

1:37

Design security is enhanced by the integration of the configuration memory on

a single chip.

1:43

This is a picture of the Max V logic element.

It looks more like an MPGA logic element than a CPLD.

It's the heart of this LE.

It's a four input and a flip-flop.

This is because the Max V was designed as a crossover device between a CPLD and

a MPGA.

In reality, it's more like an MPGA than an CPLD.

2:04

This next picture shows the overall layout of the MAX V device which is basically

a sea of logic array block or labs connected by row and column routing.

Each lab contains ten logic elements.

Contrast the Max V floor plan with this floor plan for the Max10.

It looks more sophisticated, which it is.

And better yet, it's in color.

The MAX 10 is a more recent part and

consistent with the trend includes more hard IP blocks, like the PLLs and the ADC.

This is a mixed signal part with both analog and digital functions on the chip.

2:41

Here is a logic element diagram for the MAX 10.

It's almost identical to the MAX 5 logic element with 4 input lop and

a flip flop at the heart and some carry change and mock signal selection.

Even though the max family has been a cpld family Altera finally

dropped all pretense with the max ten and does call it an fpga.

Here is a portion of the altera max 10 fpga family device handbook.

The Altera Max 10 has reprogrammable flash configuration and user memory,

although the routing switches are based on SRAM.

On power up, the device transfers the configuration memory in flash to the SRAM

in about half a millisecond.

Note there are up to 50,000 logic elements, a good size for a small FPGA.

3:29

Speed is limited to 450 megahertz on global.

Very fast for a small FPGA.

Power is not specified.

Use the power play analyzer tool to determine it.

Five watts is the limit for this part.

3:44

This device is up to 500 IO pins, a ten to one ratio of logic cells to IO.

There are 31 supported IO standards.

Notice there are migration paths between pin compatible parts with different logic

amounts.

This is a very beneficial arrangement,

especially when requirements change during a project,

as no board layout is required even if the amount of logic used increases.

4:09

A number of hard IP blocks have been added including block memory.

Multipliers, PLLs, ADCs, and external memory interface.

4:20

Data retention is 20 years with ten thousand programming cycles endurance

which is good.

Designed security is enhanced by the integration of the configuration memory on

a single chip.

4:32

Next, let's look at the product table for the Cyclone V Small FPGA.

The Cyclone V has reprogrammable SRAM configuration and routing.

So it needs an external nonvolatile configuration memory.

On power up,

the device transfers the configuration information to the internal SRAM.

4:50

Notice there are up to 300,000 logic elements, a considerable amount for

a small FPGA.

4:57

Speed is limited to 550 megahertz on global clock buffers.

Very good for a small FPGA.

Power is not specified.

Use the power play analyzer tool to determine it.

5:09

This device has up to 480 I/O pins, a 600 to one ratio of logic cells to I/O.

There are 34 supported I/O standards.

5:19

A number of hard IP blocks have been added including block memory, multipliers,

PLLs, DSP blocks, Hi-speed transceivers and external memory interfaces.

5:32

This shows the layout of the overall Cyclone Five, with the logic cells,

ram blocks, blocks, PLL's, transceiver and memory interfaces.

The basic logic element for the Cyclone Five is the Adaptive Logic Module or ALM.

5:48

It consists of an 8-input adaptive LUT, two Full Adders,

and four foot-plot registers.

This register-rich logic element allows more design-packing capability than

previous generations.

The LUT can also be configured as a 32 by 2 dual-port S-RAM.

The ALM can become a three input adder by combining the full adders with let

arithmetic.

6:12

This is a picture of the ALM in the normal mode.

This is the same ALM as previously shown.

It's just another view of it as it operates in a particular mode.

6:22

Recall the four bit comparator.

How many comparator bits can be implemented in a in a max 10 case there

are only 4 inputs so a two bit comparator can be created.

Larger comparators require that the lots be cascaded, although the logic is

efficiently used there is an added delay relative to the cpld implementation.

In the Cyclone v case.

The six independent input will handle three bits of comparator, so

wider comparators can be made with less delay.

How many full adders can be made in a logic cell?

For the MAX 10 each log can create one full bit adder because of

the addition of the so one LE equals one bit adder.

However from a previous video, we used three Cyclone ALMs to implement

a four bit adder, so each ALM creates about 1.33 adders.

7:16

In this video we have learned, Altera offers the MAX V CPLD and

MAX 10 and Cyclone V FPGA families for smaller logic designs.

7:27

The MAX V and MAX 10 are single chip solutions with more I/O

combined with reasonable logic density and efficient 4-input LUT logic cell.

7:36

The MAX 10 adds analog signal processing via an on-chip ADC.

The Cyclone V is a good entry level FPGA with good speed and

logic density combined with a considerable amount of hard IP blocks.

Including Block memory, PLLs, Multipliers and DSP blocks,

High Speed Transceivers and External Memory Interfaces.

Interactive Transcript



Help us translate!

0:00

In this video we will continue our survey of modern programmable logic

devices with large FPGAs from Altera, including the Arria V,

the Stratix V, the Arria 10 and the Stratix 10.

The goal on Programmable Logic Device Selection is to pick the best fit part for

our requirements.

We'll use the Programmable Logic Device Selection Criteria we established earlier

to evaluate these devices as listed here.

0:28

To start, let's look at the product table flor the Arria V mid range FPGA.

The Altera REF5 has reprogrammable SRAM configuration and routing, so

it needs an external non-volatile configuration memory.

On PowerUp the device transfers the configuration information to

the internal SRAM.

Notice there are up to 500,000 logic elements, about double that of a Cyclone5.

0:55

Speed is limited to 625 megahertz on a global clock buffers.

Power is not specified.

Use the power play analyzer tool to determine it.

This device is up to 704 IO pins.

A 715 to 1 ratio of logic cells to IO.

1:13

A number of hard IP blocks have been added including block memory DSP blocks,

high speed transceivers is 6.6 gigabits per second standard.

With transceiver parts up to 12.5 gigabits per second and

an external memory interface up to DDR three at 1,600 megabits per second.

1:34

Here is the picture of the RDA5 layout.

With an array of logic blocks interspersed with memory and DSP blocks.

And the transceivers and hard DDR memory interfaces on the outside.

This is a diagram of RDF5LM which looks just like the cyclone five ALM.

Made of two, six input luts driving four flip flop registers.

Once the FPGA designer develops a logic cell architecture they like,

they tend to repeat it.

2:02

Now consider the Large FPGA.

2:06

The Altera Stratix V has reprogrammable SRAM configuration and routing, so

it needs the external nonvolatile configuration memory.

On power up,

the device transfers the configuration information to the internal SRAM.

Notice there are up to 950,000 logic elements, about double that of an REF5.

2:25

Speed is limited to 717 megahertz on the global clock buffers.

Powers not specified, we use the power play analyzer tool to determine it.

This device has up to 840 IO pins, And an 1100 to one ratio of logic cells to IO.

2:43

A number of hard IP blocks have been added,

including high speed transceivers up to 28.05 gigbits per second in the GT part.

Block memory, multipliers to 27, 27 precision.

The SP blocks and

external memory interfaces to DDR3 at 1600 megabits per second.

3:06

Here is a picture of the stratics five layout

with an array of logic blocks interspersed with memory and ESP blocks.

And the transceivers on the left and right sides, and

hard DDR memory interfaces on the top and bottom of the device.

3:21

This is a diagram of the Stratix V ALM which looks just like the Cyclone5 or

Arria V ALM made of two six input bots driving four foot plot registers.

You know how this one works already thanks to Alturas' lack of imagination.

3:37

Actually we know their imagination is very good.

But, they know a good design when they see one and so they repeat it.

3:44

Now consider Arria 10 large FPGAs,

3:47

the Altera Arria 10 has reprogrammable SRAM configuration and routing.

So it needs the external non-volatile configuration memory.

Power up the device transfers, the configuration information,

to the internal S ramp.

4:02

Notice there are up to over 1 million logic elements,

about double that of an Arria V.

4:08

Speed is limited to 644 MHz on the global clock buffers.

Not much faster than an Arria V.

4:15

Power is not specified.

We use the power play analyzer tool to determine it.

4:20

This device has up to 840 I/O pins and

1100 to 1 ratio of logic cells to I/O.

A number of hard IP blocks have been added, including high speed

transceivers up to 28.3 gigabits per second, bock memory,

multipliers, DSP blocks, 10 gigabit Ethernet interfaces and

external memory interface with DDR4 up to 2,666 megabits per second.

This is a diagram of the Arria 10 ALM, which is the same as the Cyclone 5 ALM.

4:55

Made out of an eight input adaptive LUT, usually configured as two six-input LUTs.

Driving four flip flop registers.

5:04

Lastly, let's look at the Stratix 10 large FPGA.

5:08

The Altera Stratix 10 has reprogrammable SRAM configuration in routing.

So it needs an external non-volatile configuration memory.

On power up the device transfers the configuration information to

the internal SRAM.

5:22

Notice there are up to over 5.5 million logic elements,

five times that of an Arria 10.

The speed is limited to 1100 MHz on global clock buffers.

The fastest FPGA in existence at this time.

Power is not specified.

Use the power play analyzer tool to determine it.

The device has up to 1640 I/O pins,

a 3300 to 1 ratio of logic cells to I/O.

A number of hard IT blocks have been added,

including high speed transceivers up to 30 gigabits per second,

block memory, multipliers, DSP blocks, 10 gigabit Ethernet interfaces and

external memory interfaces with DDR4 up to 2,666 mega bits per second.

This part is a beast.

Imagine, for a moment, what you can do with something this powerful.

So Altera's HyperFlex architecture has the HyperFlex advantage.

The key innovations that contribute to the HyperFlex advantage are registers

everywhere.

The registers everywhere in the interconnect routing called

Hyper-Registers are distinct from the conventional registers.

They're contained within the adapted logic modules.

A Hyper-Register is associated with each individual routing segment in the device.

Enhanced core clocking.

The programmable clock trees synthesis allows system designers to

create localized clock trees.

Reducing skew and timing uncertainty to obtain maximum core clocking performance

this capability is a key feature that allows the HyperFlex Architecture

to reach two times the performance.

Hyper-Aware Design Flow.

The Hyper-Aware Design Flow includes three new improvements,

a Fast Forward Compile tool, a Hyper-Retimer step, and

enhanced synthesis and place-and-route algorithms that use the Hyper-Registers.

7:20

Here's a picture of a HyperFlex Architecture with registers in orange

at every routing node.

This is what makes the HyperFlex Architecture different from conventional

architectures.

7:32

For more about the HyperFlex Architecture, please see this HyperFlex video at

www.altera.com/support.

/training/videos/hyperflex-architecture-o-

verview-video.tablet.html.

Recall the four bit comparator example.

How many comparator bits can be implemented in a lot?

In this Stratix case, the six independent lot.

Will handle three bits of comparators, so

wider comparators can be made with less delay.

8:07

How many full adders can be made in a logic cell?

For the Stratix 10 the ALM is very similar to the Cyclone 5 ALM, and

from a previous video we used three Cyclone 5 ALMs to implement a 5 bit adder.

So each ALM creates about 1.33 adders.

In this video, we have learned Altera offers the Arria V,

Stratix V, Arria 10 and Stratix 10, FPGAs for large designs.

8:36

Arria V and Stratix V are large devices with up to 1 million logic elements and

integration of many hard IP blocks

to create very powerful parts with great processing power.

8:48

The Arria 10 increases the processing power further, with 28 Gbps serial

transceivers and 2666 Mbps DDR4 DRAM interfaces.

The Stratix 10 is the largest and fastest FPGA currently in production,

with over 5.5 million logic elements and core clock speed of 1100 MHz.

9:12

Altera's Hyperflex Architecture is a revolutionary change that will increase

FPGA performance further, doubling performance at equivalent power levels.

Interactive Transcript



Help us translate!

0:00

In this video we will continue our survey of modern programmable logic devices.

This time with FPGAs from micro semi including The Igloo, The Igloo 2, and

the Accelerator.

But before we begin looking at the parts

some background in FPGA process technology and interconnection is helpful.

0:18

The goal of programmable logic device selection Is to pick the best fit part for

our requirements really is the programmable logic device selection

criteria we established earlier to evaluate these devices.

Micro semi has both FLASH based and anti-fuse base FPGAs and there

are performance differences based on the inter connectors we can see by the chart.

Anti-fuse parts are OTP or one-time programmable,

while FLASH parts can be reprogrammed many times.

FLASH parts don't have high-speed performance, but are very good for

low-power applications.

Anti-fuse parts are very rugged, and

have been used in the most extreme of conditions.

If we take a closer look at the technology.

We can better understand how these performance differences arise.

FSRAM cells can be programmed to, either close, or open a switch,

between routing paths on the FPGA.

Similarly, in FLASH FPGAs the routing switch is controlled

by a FLASH cell program to a 1 or a 0.

In anti fuse parts, the connection between routes is permanently fixed

by melting an interconnection in place during programming.

This connection cannot be reversed.

FLASH cells can be programmed once and

will remain this way permanently until reprogrammed as they are non volatile.

FSRAM cells must be programmed to power up every time as they are volatile and

lose their information when power is off.

1:48

There are many other ramifications to the interconnect type in addition to

volatility and reprogrammability, and we will look at some of them next.

1:58

If we look at our SRAM cell more closely,

It typically is made with six transistors in the circuit shown on the left.

This circuit has a number of pathways between power and ground,

which will have some finite current flowing through them,

even though during operation the cell is in a static state.

This leakage current is significant.

It can lead to power consumption on the order of many watts in larger SRAM FTDAs.

The FLASH cell has fewer pathways and 1000x lower leakage current,

with a very low static power consumption on the order of miliwatts.

Microsemi's FLASH process also allows the part to be placed in a suspended state.

Which they call FLASH freeze which reduces the power further into the microwatt

range.

Because of this low power capability Microsemi call the first parts like this

Igloo as they don't generate any heat from power loss.

The FLASH based LPGAs from Microsemi have a number of inherent advantages.

They flow directly from the technology including true FLASH-based technology.

They are reprogrammable and nonvolatile.

No extra memory is required to create the inner connections.

Live at power-up.

No start up delay.

3:14

Integration provides lower total system cost.

Addition of other IP blocks to create SOC devices that replace

multiple ICs in designs.

Low power across the board.

Every part is lower power, and

some have additional very low power FLASH freeze operating modes.

3:33

Best Design Security, with no external program memory,

reverse engineering the device program file is more difficult.

3:41

Superior reliability.

Flash cells are immune to radiation effects and

can more easily be radiation hardened.

3:49

Here is a summary of Microsemi IGLOO nano f-p-g-a family.

As they are flash based, they are reprogrammable and non-volatile.

Which means they are ready at power-up and need no external memory,

a single-chip solution.

These are smaller-density parts with only up to 6,000 flip-flop cells.

Speed is limited to 250 megahertz on global clock buffers,

slow compared to other FPGAs but still usable.

The most interesting aspect of these devices is low power consumption

on the order of microwatts and flash freeze mode.

4:25

This device has up to 77 I/O pins and 80 to 1 ratio

logic cells to I/O more like a CPLD in that respect.

A few hard IP blocks have been added, including block memory,

FlashROM bits, and PLLs.

4:43

Here's a diagram of the Microsemi IGLOO nano FPGA

showing the sea of versatile logic elements.

RAM blocks across the top, IO blocks around the outside.

Also showing is the AES decryption

which can be used to protect the reading of the programmable contents.

The user flash RAM, flash freeze control.

It charge prompts to enable in circuit programming of the part.

The Microsemi IGLOO nano uses VersaTiles as the main logic element.

This is a finer grain logic element than what we see from other FPGA vendors.

Which can lead to a better utilization of the logic,

but may also increase routing requirements.

There is always a trade off between architectures.

Here the Versatile can be configured either as any 3-input combinatorial

logic or a de-flip-flop, or a de-flip-flop with enable.

This is a much simpler logic element than others we have considered.

5:40

When you use this combination of logic, the versatile can implement any three

input functions including all the ones shown here.

It can be an orgate, and an angate, an xorgate, a mox, etc.

Here is a summary of the Microsemi IGLOO2 fpag family made out of 65

nanometer process.

As they are flash based, they are reprogrammable and

non volatile, which means they are ready at power up and

need no external memory, a single chip solution.

6:10

These are median density parts with up to 150 K logic elements.

6:16

Speed is limited to 400 megahertz and

global clock buffers, adequate compared to other FPGAs.

An interesting aspect of these devices is the low power consumption.

Less than 11 miliwatts even on the largest part in the FLASH freeze mode.

6:30

This device has up to 574 IO pins A 250 to one ratio of logic cells to I/O.

More I/O intensive than other FPGA's of this size.

6:42

One characteristic that distinguishes this device

is that it's chock full of hard IP blocks relative to its predecessor.

6:49

Added IP includes DSP Math Blocks,

DMA Embedded nonvolatile memory or eNVM.

Three different types of RAM.

DDR DR controllers and at the 16 lanes of five gigabit per

second SERDES transceivers and PCIe controllers.

7:11

With this part the layout of the device has become very complex.

So we first look at the block diagram.

It consist of five major sections.

7:22

The high speed memory subsystem which includes 667 megabit per second

DDR controllers.

7:29

The FPGA Fabric with up to 150K logic elements.

The transceiver which include PCIE and XAUI interfaces.

The system controller with design security features and the GPIO blocks.

7:44

The IGLOO2 has been engineered not only to provide a low power mid range FPGA,

but also to have excellent design and data security and reliability as listed here.

Design security features include program data encryption, tamper detection and

zeroization.

8:02

Data security features include a non-deterministic random bit generator or

NRBG and physically unclonable function or PUF like the magic dragon.

8:12

The FEJ fabric is single event upset immune and

the memory includes Single Error Correct Double Error Detect protection.

The IGLOO2 logic element can be used as a combinational logic

element CLE and/or Sequential Logic Element SLE.

8:30

Each logic element consists of four input [INAUDIBLE]

a dedicated carry chain based on the carry look ahead technique.

A separate flip flop which can be used independently from the lut.

The foreign can be configured to implement any foreign put combinational function or

to implement arithmetic function

where the lot output is Xor with the carry input that generate the sum output.

8:55

Here is a summary of the Microsemi Accelator FPGA Family.

As there anti fuse base they are non-volatile single chip solution that

cannot be reprogrammed.

You only get one chance to program these right,

which is not a problem in production but can hamper development.

These are smaller density parts with up to 21,000 flip-flop cells.

Speed is limited to 870 megahertz on global clock buffers,

very fast compared to other FPGA's.

9:29

Power consumption is fairly low, less than 50 milliwatts static power for

the small parts.

And less than 300 milliwatts for the large parts,

although not near as low as the flash parts.

9:41

This device has up to 684 IO pins, a 30 to 1 ratio of logic cells to IO.

So this is an IO rich part.

9:51

A few hard IP blocks have been added,

including up to 292 kilobits of block memory.

And up to 8 PLLs, here is the diagram of the Microsemi Accelerator FPGA

showing the layout of the device.

It consist of a of super clusters, each made of four combinational cells and

two register cells with routing transmitters and receivers.

Several columns of block rams and IO blocks on the outside edges.

10:20

There are two types of Accelerator Logic elements.

The register cell, or R-Cell, and

the combinatorial cell, or C-Cell, depicted here.

The C-Cell can implement more than 4,000 combinatorial functions of

up to five inputs.

10:35

Here's a summary of the Microsemi RTAX FPGA family.

As they are antifuse based,

they are a non-volatile single-chip solution that cannot be reprogrammed.

You only get one chance to program these right,

which is not a problem in production, but can hamper development.

10:53

These are smaller density parts with only up to 21,000 flip flop cells.

10:59

Speeds limited to 870 megahertz in global clock buffers,

very fast compared to other FPGAs.

Power consumption's fairly low, less than 50 milliwatts static power for

the small parts.

And less than 300 milliwatts for the large parts.

Although not near as low as the flash parts.

This device has up to 684 IO pins, a 30 to 1 ratio of logic cells to IO.

So this is an IO-rich part.

11:26

A few hard IP blocks have been added,

including up to 292 kilobits of block memory, and up to 8 PLLs.

11:34

The RTAX layout and logic elements are the same as the accelerator family.

The accelerator family can be used in development to model the RTAX parts,

which are much more expensive.

And this is typically done to save the cost of these OTP devices.

Recall the four-bit comparator?

How many comparative bits can be implemented in an IGLOO 2?

In the IGLOO 2 case, the four independent input lots will handle two bits of

comparator, and will take three lots to make this four-bit comparator.

In the IGLOO, it will take 5 Versatiles.

12:10

How many full adders can be made in a logic cell?

For the micro semi IGLOO, each bit of adder requires 2 Versatiles where

the tiles in the picture are the and/or arrays in the 3 input highlighted in red.

The 4 bit adder will then require 8 Versatiles as shown.

The IGLOO-2 FOR input architecture will also require eight logic elements,

eight lots in this case.

Other FOR input architectures require only four lots, and

six-input ALM architectures require only three ALMs.

12:44

In this video, we have learned MIcrosemi offers both FLASH and Antifuse FPGAs.

Each type has different capabilities and limitations.

The current Microsemi Flash FGP offering, the IGLOO and

the IGLOO2, are instant on, single chip solutions that are reprogrammable,

with very good low power performance and high reliability and security.

13:09

Microsemi Antifuse FPGAs are designed for rugged environments and high reliability,

including the Accelerator family and the RTAX radiation tolerant family.

13:20

The Microsemi IGLOO2 has a wealth of hard IP cores, including memory controllers,

high-speed transceivers, RAMS, DSP blocks, and many security enhancements.

13:32

If security or reliability or

low power are design requirements, Microsemi FPGAs are worth consideration.



Help us translate!

0:00

In this video we'll continue our survey of modern programmable logic devices.

This time with FPGAs and CPLDs from Lattice,

including the ECP5, the ECP three,

the MACHXO3, the MACHXO2,

and iCE 40, proceeding from bigger to smaller devices this time.

The goal of programmable logic device selection is

to pick the best fit part for our requirements.

We'll use the programmable logic device selection criteria we established earlier,

to evaluate these devices.

Lattice offers both small CPLDs and mid-range FPGA parts,

available at low cost and low power consumption,

sometimes in very small packages.

Typically, applications include portable consumer and mobile devices.

Here is a summary of the last ECP5 FPGA family,

made on a 40 nanometer process.

As they're SRAM based,

they're reprogrammable and volatile,

and therefore require an external memory to hold configuration data.

These parts are optimized for cost and low power with moderate density.

These are medium density parts with up to 85 K logic elements.

Speed is limited to 400 megahertz in global clock buffers,

adequate compared to other FPGAs.

Power consumption is fairly low,

about 250 milliwatts, even on the largest part.

This device is up to 365 I/O pins.

A 230 to 1 ratio of logic cells to I/O,

more I/O intensive than other FPGAs of this size.

This device includes several hard IP blocks.

Added IP includes DSP math blocks, RAM blocks,

DDR DRAM memory support,

and up to four lanes of five gigabit per second SERDES transceivers.

Each ECP5 device contains an array of

logic blocks surrounded by programmable I/O cells or PIC.

Interspersed between the rows of logic blocks are rows of embedded block RAM or EBR,

and rows of Digital Signal Processing slices.

In the ECP5 the basic logic element is the slice.

Each slice contains two LUT4s feeding two registers.

In distributed SRAM mode,

slice zero through Slice two are configured as distributed memory,

and slice three is used as Logic or ROM.

The ECP5 sysDSP Slice is very versatile,

and supports many functions that include the following,

full double data rate support for higher operation frequency,

a throughput of up to 370 megabits per second.

Dual-multiplier architecture, this lowers

accumulator overhead to half and the latency to half,

compared to a single multiplier architectures;

fully cascadable DSP across slices,

support for symmetrical, asymmetrical, and non-symmetrical filter;

a multiply one 18 by 36,

or two 18 by 18,

or four 9 by 9 Multiplies per Slice;

you can multiply 36 by 36 by cascading across two sysDSP slices.

A Multiply Accumulate which supports one 18 by 36 multiplier result accumulation,

or two 18 by 18 multiplier result accumulation.

Here's a summary of the Lattice ECP three FPGA family,

made on a 65 nanometer process,

so it will cost more than an equivalent ECP5.

Like the ECP5 they're SRAM based,

so they're reprogrammable and volatile,

and therefore require an external memory to hold configuration data.

These are medium density parts with up to 150 K logic elements,

larger than the later ECP5.

Speed is limited to 500 megahertz on global clock buffers,

adequate compared to other FPGAs.

Power consumption is moderate,

about 450 milliwatts, even on the largest part.

This device is up to 586 I/O pins.

A 250 to 1 ratio of logic cells to I/O,

more I/O intensive than other FPGAs of this size.

This device includes several hard IP blocks.

Added IP includes DSP math blocks, RAM blocks,

DDR DRAM memory support,

and up to 16 lanes of 3.2 gigabits per second SERDES transceivers.

Each Lattice ECP three device contains an array of

logic blocks surrounded by programmable logic cells,

interspersed between the rows of logic blocks or rows of

embedded Block RAM or EBR and rows of digital signal processing slices.

In ECP three the basic logic element is the slice.

Slice zero through Slice two contain two LUT4s feeding two registers,

whereas Slice three contains two LUT4s only.

Slice zero through Slice two can be configured as distributed memory.

The Lattice ECP three sysDSP Slice supports many functions that include the following,

multiply one 18 by 36,

two 18 by 18,

or four 9 by 9 Multiplies per slice;

you can multiply 36 by 36 by cascading across to sysDSP slices;

a Multiply Accumulate up to 18 by

36 Multipliers feeding an Accumulator that can have up to 54-bit resolution.

Here's a summary of the Lattice MACHX02 CPLD family,

made on a 65 nanometer process.

They are SRAM based and therefore reprogrammable and volatile.

However, they have non-volatile configuration memory storage,

which loads the SRAM cells on power up,

which means they need no external memory and are a single chip solution.

These are small density parts,

with up to 7 K logic elements.

Generally competing with CPLDs although they have an FPGA like architecture.

The XO in the product name stands for crossover,

as these parts are intended to crossover from CPLDs to FPGAs.

Speed is limited to 380 megahertz in global clock buffers,

adequate compared to other CPLDs.

Static power consumption is very low,

about 200 microwatts, even on the largest part.

This device is up to 334 I/O pins.

A 20 to 1 ratio of logic cells to I/O,

a very rich I/O part like other CPLDs.

One of the best aspects of these parts comes from packaging,

with parts sizes as small as 2.5 millimeter by 2.5 millimeter,

a tenth of an inch on the side.

One interesting characteristic of this device is the amount of

hard IP blocks available for a programmable part of this small size.

Added IP includes RAM blocks, user flash memory,

both I2C and SPI serial ports,

and DDR DRAM memory support.

The MACHX02 family architecture contains an array of

logic blocks surrounded by programmable I/O or PIO,

and non-volatile configuration memory blocks.

The larger logic density devices of in this family

have PLL's and blocks of Embedded Block RAM or EBR's.

The Embedded Function Block includes the serial port hard IP.

The MACHXO2 Logic Element is a slice with two LUT4's and two flip-flops.

The register in the slice can be configured for

positive or negative edge triggered or level sensitive clocks.

All slices have 15 inputs from routing and one from the carry-chain,

from the adjacent slice or PFU.

There are seven outputs,

six for routing and one to carry-chains to the adjacent PFU.

It is very similar to the ECP3 slice.

Here's a summary of the lattice MACHXO3 CPLD family,

made on the 65 nanometer process.

They are SRAM based and therefore volatile,

however they have non-volatile configuration memory storage

which loads the SRAM cells on power up,

which means they need no external memory and are a single chip solution.

In some cases the non-volatile memory is flash,

that is reprogrammable, in others it is

a lower cost memory that is two times programmable.

The part numbers that end with F are the flash parts.

These are small density parts with up to

9K logic elements more than a MACHXO2 but generally competing with CPLDs,

although they have an FPGA like architecture.

The XO in the product name stands for crossover as

these parts are intended to crossover from CPLDs to FPGAs.

Speed is limited to 388 megahertz on

global clock buffers adequate compared to other CPLDs.

Power consumption is low,

about 20 milliwatts even on the largest part.

This device is up to 384 I/O pins,

a 25 to 1 ratio of logic cells to I/O,

a very rich I/O part like other CPLDs.

One of the best aspects of these parts comes from packaging,

with part sizes as small as 2.5 by 2.5 millimeters,

a tenth of an inch on the side.

One interesting characteristic of this device is the amount of

hard IP blocks available for a programmable part of the small size.

Added IP includes RAM Blocks,

MIPI D-PHY for video interfacing,

both I-squared-C and SPI serial ports,

and DDR DRAM memory support.

The MACHXO3L/LF family architecture contains an array of logic blocks

surrounded by a programmable I/O or PIO and non-volatile configuration memory blocks.

The larger logic density devices in this family have PLLs and Embedded Block RAM, EBR's.

The embedded function block includes the serial port,

and the MIPI video port hard IP.

The MACHXO3 Logic Element is a slice with

two LUT4's and two flip-flops identical to the slice of the MACHXO2.

Here's a summary of the Lattice ICE40 Ultra FPGA family,

made on a 40 nanometer low power process.

They are SRAM based and therefore volatile,

however they have non-volatile configuration memory storage

which loads the SRAM cells on power up,

which means they need no external memory and are single chip solution.

Loaded in the configuration from the NVCM can take tens of milliseconds.

These are small density parts with up to 3K logic elements,

generally competing with CPLDs although they have an FPGA architecture.

Speed is limited to 185 megahertz on global clock buffers slow,

compared to other devices,

but this is to be expected and apart tuned for low power consumption.

As you might expect with a name ICE,

power consumption is very low,

about 95 microwatts static power and 11 milliwatts dynamic power,

even on the largest part,

and even lower on the smaller parts.

This device is up to 39 I/O pins,

a 90 to 1 ratio of logic cells to I/O,

it's an I/O rich part.

One of the best aspects of these parts comes from the packaging,

with parts sizes as small as 2 by 2 millimeters or a tenth of an inch on a side.

One interesting characteristic of this device is the abundance of

hard IP blocks available for programmable parts of the small size.

Added IP blocks include RAM Blocks,

DSP blocks, both I2C and SPI serial ports,

on-chip oscillators, 24 milliamp LED drivers,

an IR LED drive,

and PWM module IP.

The ICE40 Ultra family architecture contains an array of

programmable logic blocks or PLBs, two oscillator generators,

two user configurable I2C controllers,

two user configurable SPI controllers,

DSP blocks, LED drivers and Embedded Block RAM or EBR surrounded by programmable I/O.

The basic logic cell of the ICE40 is a LUT4 and

a D flip-flop with each programmable logic block consisting of eight logic cells.

So recall the 4 bit comparator,

how many comparator bits can be implemented in

the typical lattice logic element which is based on a LUT4?

The four input LUT will handle two bits of comparator and it will take

three LUTs to make this four bit comparator.

How many full adders can be made in a logic cell for Lattice MACHXO2,

each bit of adder requires two LUTs to generate both the sum and the carry out,

so eight LUTs will be used in a four bit adder.

In this video we have learned Lattice specializes in

low cost high value small to medium programmable logic parts,

including the ICE40, the MACHXO2,

the MACHXO3, the ECP3,

and the ECP5 families.

The MACHXO2 and MACHXO3 families are

single chip solutions with on-chip nonvolatile configuration memory storage,

but routing controlled by SRAM cells that must be loaded on power up.

These devices feature low power,

very small size down to 2.5 by 2.5 millimeters and several hard IP blocks.

The ICE40 family includes an abundance of hard IP functions for such a small part,

and very low power consumption.

Lattice devices all have logic elements based on the four input LUT and a register,

adequate but somewhat less capable than other FPGA offerings.