2.2 Memory organization

2.2.1 Introduction

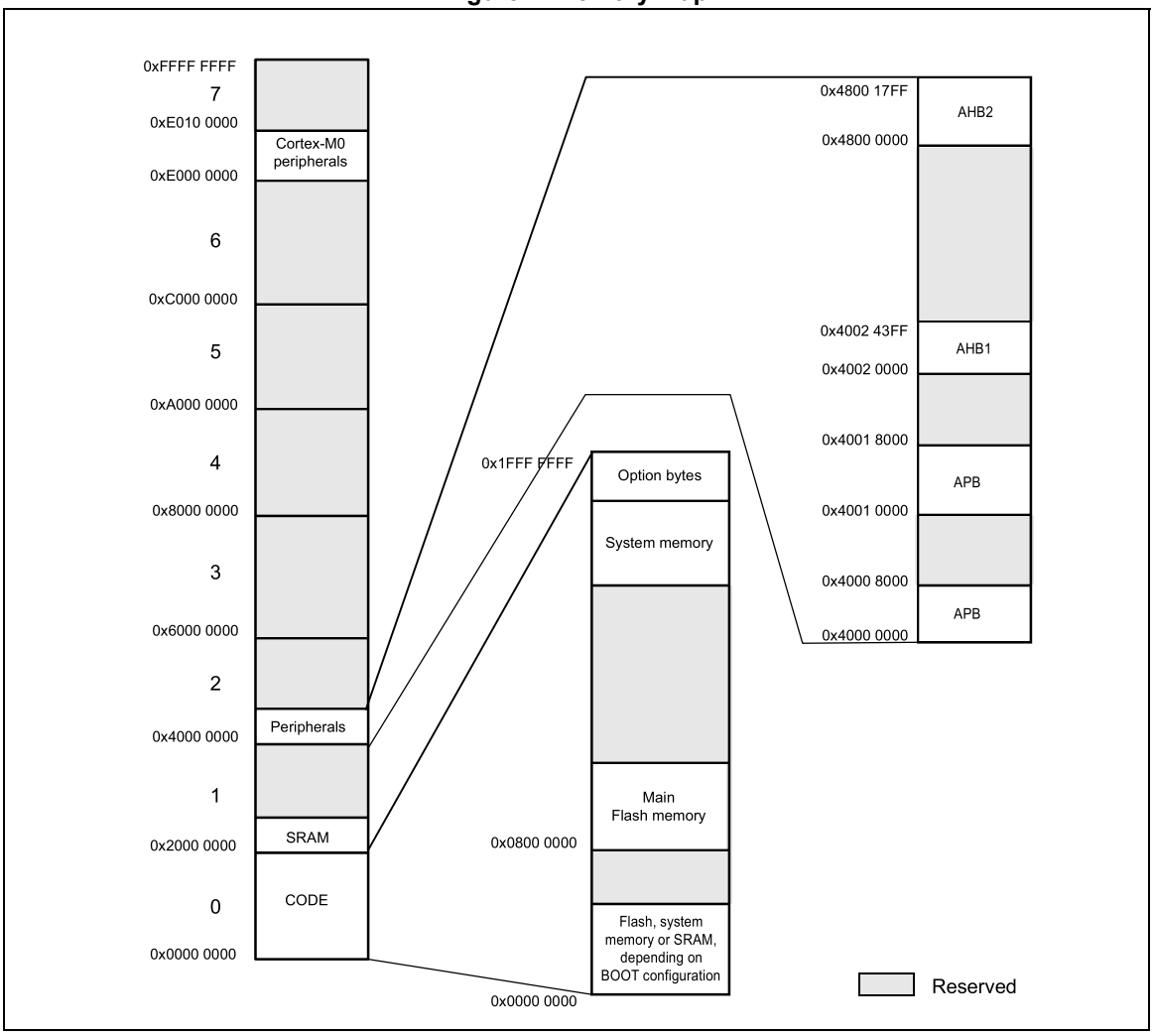
Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

The addressable memory space is divided into eight main blocks, of 512 Mbytes each.

2.2.2 Memory map and register boundary addresses

Figure 2. Memory map



All the memory map areas not allocated to on-chip memories and peripherals are considered “Reserved”. For the detailed mapping of available memory and register areas, refer to the following table, which gives the boundary addresses of the available peripherals.

Table 1. STM32F0xx peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral	Peripheral register map
-	0xE000 0000 - 0xE00F FFFF	1MB	Cortex®-M0 internal peripherals	-
-	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved	-

Table 1. STM32F0xx peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral	Peripheral register map
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF	*Section 8.4.12 on page 164*
	0x4800 1000 - 0x4800 13FF	1KB	GPIOE	*Section 8.4.12 on page 164*
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD	*Section 8.4.12 on page 164*
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC	*Section 8.4.12 on page 164*
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB	*Section 8.4.12 on page 164*
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA	*Section 8.4.12 on page 164*
-	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved	-
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC	*Section 16.6.11 on page 326*
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved	-
	0x4002 3000 - 0x4002 33FF	1 KB	CRC	*Section 12.5.6 on page 232*
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved	-
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH interface	*Section 3.5.9 on page 75*
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved	-
	0x4002 1000 - 0x4002 13FF	1 KB	RCC	*Section 6.4.15 on page 136*
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved	-
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2	*Section 10.6.8 on page 212*
	0x4002 0000 - 0x4002 03FF	1 KB	DMA	*Section 10.6.8 on page 212*
-	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved	-

Table 1. STM32F0xx peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral	Peripheral register map
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved	-
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU	*Section 32.9.6 on page 934*
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved	-
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17	*Section 20.6.17 on page 558*
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16	*Section 20.6.17 on page 558*
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15	*Section 20.5.19 on page 541*
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved	-
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1	*Section 27.8.12 on page 765*
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved	-
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1	*Section 28.9.10 on page 824*
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1	*Section 17.4.21 on page 402*
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved	-
	0x4001 2400 - 0x4001 27FF	1 KB	ADC	*Section 13.12 on page 274*
	0x4001 2000 - 0x4001 23FF	1 KB	Reserved	-
	0x4001 1C00 -0x4001 1FFF	1 KB	USART8	*Section 27.8.12 on page 765*
	0x4001 1800 - 0x4001 1BFF	1 KB	USART7	*Section 27.8.12 on page 765*
	0x4001 1400 - 0x4001 17FF	1 KB	USART6	*Section 27.8.12 on page 765*
	0x4001 0800 - 0x4001 13FF	3 KB	Reserved	-
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI	*Section 11.3.7 on page 225*
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG	*Section 9.1.38 on page 185*
			COMP	*Section 15.5.2 on page 308*
-	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved	-

Table 1. STM32F0xx peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral	Peripheral register map
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved	-
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC	*Section 31.7.7 on page 919*
	0x4000 7400 - 0x4000 77FF	1 KB	DAC	*Section 14.10.15 on page 299*
	0x4000 7000 - 0x4000 73FF	1 KB	PWR	*Section 5.4.3 on page 94*
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS	*Section 7.7.5 on page 147*
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved	-
	0x4000 6400 - 0x4000 67FF	1 KB	CAN	*Section 29.9.5 on page 864*
	0x4000 6000 - 0x4000 63FF	1 KB	USB/CAN SRAM	*Section 30.6.3 on page 900*
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB	*Section 30.6.3 on page 900*
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2	*Section 26.7.12 on page 698*
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1	*Section 26.7.12 on page 698*
	0x4000 5000 - 0x4000 53FF	1 KB	USART5	*Section 27.8.12 on page 765*
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4	*Section 27.8.12 on page 765*
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3	*Section 27.8.12 on page 765*
	0x4000 4400 - 0x4000 47FF	1 KB	USART2	*Section 27.8.12 on page 765*
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved	-
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2	*Section 28.9.10 on page 824*
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved	-
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG	*Section 23.4.6 on page 582*
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG	*Section 24.5.4 on page 588*
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC	*Section 25.7.18 on page 628*
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved	-
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14	*Section 19.4.13 on page 490*
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved	-
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7	*Section 21.4.9 on page 572*
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6	*Section 21.4.9 on page 572*
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved	-
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3	*Section 18.4.19 on page 469*
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2	*Section 18.4.19 on page 469*

Table 2. STM32F0xx memory boundary addresses

Device	Boundary address	Size	Memory Area	Register description
STM32F03x	0x2000 1000 - 0x3FFF FFFF	~512 MB	Reserved	-
	0x2000 0000 - 0x2000 0FFF	4 KB	SRAM	*Section 2.3 on page 52*
	0x1FFF FC00 - 0x1FFF FFFF	1 KB	Reserved	-
	0x1FFF F800 - 0x1FFF FBFF	1 KB	Option bytes	*Section 4 on page 76*
	0x1FFF EC00 - 0x1FFF F7FF	3 KB	System memory	-
	0x0800 8000 - 0x1FFF EBFF	~384 MB	Reserved	-
	0x0800 0000 - 0x0800 7FFF	32 KB	Main flash memory	*Section 3 on page 56*
	0x0000 8000 - 0x07FF FFFF	~128 MB	Reserved	-
	0x0000 0000 - 0x0000 7FFF	32 KB	Main flash memory, system memory or SRAM depending on BOOT configuration	-
STM32F04x	0x2000 1800 - 0x3FFF FFFF	~512 MB	Reserved	-
	0x2000 0000 - 0x2000 17FF	6 KB	SRAM	*Section 2.3 on page 52*
	0x1FFF FC00 - 0x1FFF FFFF	1 KB	Reserved	-
	0x1FFF F800 - 0x1FFF FBFF	1 KB	Option bytes	*Section 4 on page 76*
	0x1FFF C400 - 0x1FFF F7FF	13 KB	System memory	-
	0x0801 8000- 0x1FFF C7FF	~384 MB	Reserved	-
	0x0800 0000 - 0x0801 7FFF	32 KB	Main flash memory	*Section 3 on page 56*
	0x0001 8000 - 0x07FF FFFF	~128 MB	Reserved	-
	0x0000 0000 - 0x0000 7FFF	32 KB	Main flash memory, system memory or SRAM depending on BOOT configuration	-
STM32F05x	0x2000 2000 - 0x3FFF FFFF	~512 MB	Reserved	-
	0x2000 0000 - 0x2000 1FFF	8 KB	SRAM	*Section 2.3 on page 52*
	0x1FFF FC00 - 0x1FFF FFFF	1 KB	Reserved	-
	0x1FFF F800 - 0x1FFF FBFF	1 KB	Option bytes	*Section 4 on page 76*
	0x1FFF EC00 - 0x1FFF F7FF	3 KB	System memory	-
	0x0801 0000 - 0x1FFF EBFF	~384 MB	Reserved	-
	0x0800 0000 - 0x0800 FFFF	64 KB	Main flash memory	*Section 3 on page 56*
	0x0001 0000 - 0x07FF FFFF	~128 MB	Reserved	-
	0x0000 0000 - 0x0000 FFFF	64 KB	Main flash memory, system memory or SRAM depending on BOOT configuration	-