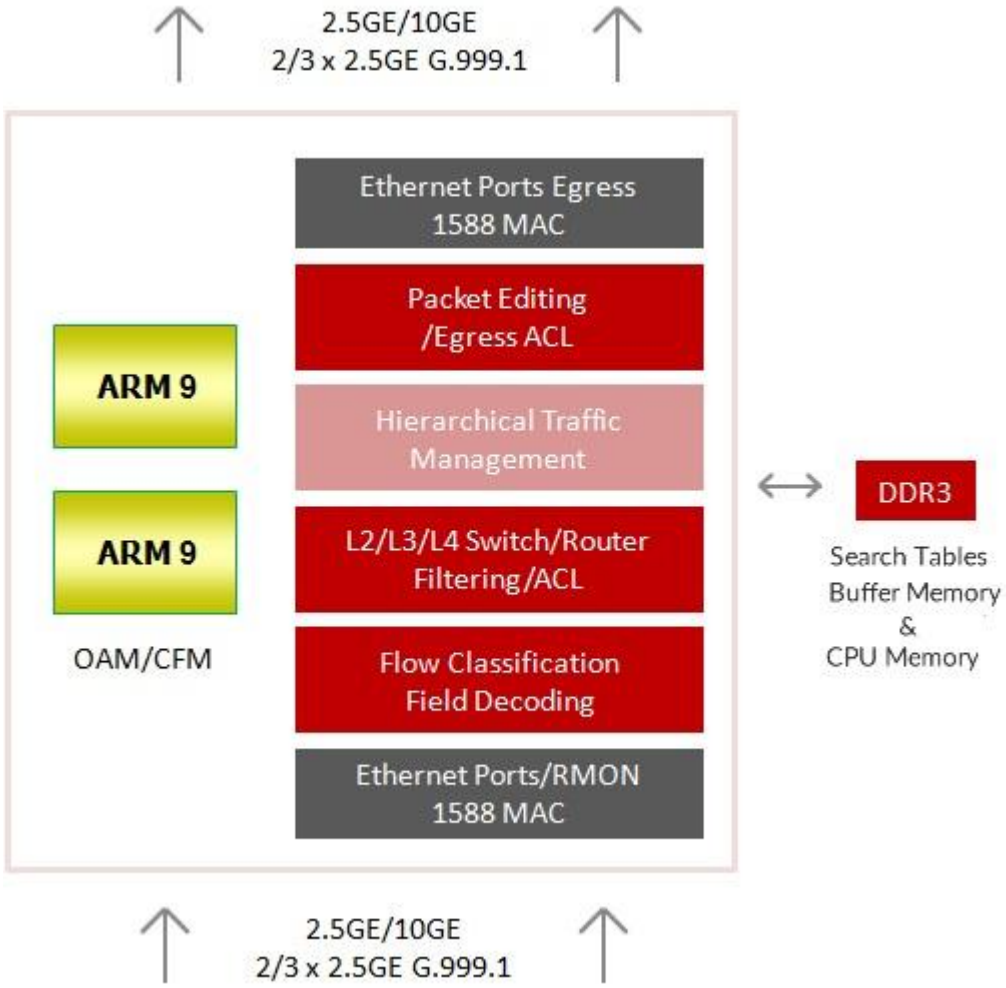
ENET38xxZ/99 Product Family Overview



ENET38xxZ/99 is a family of G.fast solution optimized fabric flow processors (FFP), supporting compliance Carrier Ethernet Switch, OAM/CFM, BBF WT-301, G.999.1 ch Ethernet and EFM bonding implemented on Xilinx 's Zynq7015/30, integrating Dual core ARM cortex 9 CPU, and Programmable Logic. . ENET38xxZ/99 is specially optimized for FTTdp G.fast market supporting 16 to 24 G.fast modems with a scale up version based on ENET48xxZ/99 to support up to 48x G.fast modems, through support for G.999.1 over 10GE interfaces.

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Features

- Flexible interface support that can be customized to any port / interface configuration
- Family of G.fast solution from 5Gbps with 2.5G N/I, 20 Gbps with 10G N/I and 40Gbps supporting 48 G.fast modems and 2 x 10GE N/I
- Integrate dual ARM dual core Cortex 9 powerful CPU
- Enhance flexibility, configurability , and programmability including field upgradeability
- Carrier Ethernet Switching
- OAM/CFM – 802.1ag/ Y.17131 *
- EFM bonding to support up to 8 G.fast
- G.999.1 Interface each support 8 to 16 G. fast modems
- MEF compliance advanced Traffic Manager including support for flow policing, and shaping per virtual port/ G.fast modem
- 1588v2 clock recovery and 1588 end-to-end transparent clock on high end platform
- QoS including WFQ,WRR, WRED and Strict Priority
- Supports 8,16, 24 or 48 G. fast modems
- Programmable Protocol interworking
- Extended buffer space through DDR3
- Low power consumption: less than 3W @ 5Gbps (best for reverse power feeding)

Description

ENET38xxZ/99 multiservice flow processors and traffic manager solutions are specially developed for Metro Access market. Functionality, throughput, and standard compliance of ENET38xxZ/99 are optimized for Carrier Ethernet Access, , Evolve Packet Core, and DPU G.fast market with low power consumption, and include support for G.999.1 protocol support and integrated EFM bonding for better link utilizations.

ENET38xxZ/99 is a part of ENET38xxZ family of multiservice fabric flow processors (FFP), integrating packet processing, protocol interworking, traffic management, G.999.1, Ethernet and Layer 2/3/4 switch. The family also includes a high- end version based on ENET48xxZ/99 to support two 10GE ports and 48 G. fast ports through 3 x 10G G.999.1 ports. The ENET38xxZ/99 FFPs was integrated on Zynq 7015 /30 equipped with powerful dual core ARM ecosystem.

The design of ENET38xxZ/99 is based on a specially efficient architecture resulting in 80% size reduction, enabling an extremely cost-effective implementation based on low cost FPGAs. Ethernity's ENET38xxZ/99 retain the flexibility and programmability of FPGAs, while providing a solution that is cost and power competitive with ASICs. Protocol interworking in ENET solutions include software support for packet editing, which provide ability to receive packets in any format and change a protocol per virtual output port to any other protocol, hence it supports, Q-in-Q, MAC-in-MAC, MPLS-TP, PPPoE, L2TP (*) or any type of L2 protocol (features set can vary from version to version)

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Detailed Features

Classification and Filtering

- Wirespeed packet classification based on first 128 bytes in packet
- Configurable functional actions: filtering, trapping, mirroring, Packet editing (create/modify/delete), QoS remarking
- Control filtering and forwarding
- Rate dependent filters (e.g., limit rate of ingress IGMPv3 packets)
- Configurable control of MAC address learning per port/VLAN
- Configurable packet type rate limitation, e.g., rate of IGMPv3 and OAM packets

Switching

- L2 PBE switching compliant with IEEE 802.1ad
- Configurable Per flow Learning and forwarding profile
- 256 active Bridge Multicast groups
- 4K MAC table
- Switching based on inner MAC and combination of Network Tags and/or outer MAC and combination of Network Tags
- L2 multicast
- Configurable forwarding key and learning key per flow
- Control packets classifier for both user and network L2 control protocol packets
- Flexible forward decision per port per protocol with the ability to forward transparently, to CPU or discard
- Support include ARP, DHCP, IGMPv2, IGMPv3 and other based on flexible configuration options

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Traffic Management

- Support of Jumbo frames up to 9KB
- Hierarchical MEF 10 Metering – on port/service/flow level - any combination of them can be mapped to a specific meter
- Scheduler: Hierarchical, three level scheduler per MEF10
- 8 , 16 or 32 virtual ports queues, each with 8 priority queues, per physical G.999.1 GbE Interface
- Queue manager
    - Total of 512, or 1K Queues
    - Unlimited MC Burst support
    - Configurable Buffer size
- Shaper per queue and each hierarchy – packet, or byte level
- Configurable MTU per priority queues or per cluster

Packet Editing

- Bit- and Byte-level editing of first 128 bytes including QoS remarking, byte counts, sequence ID and DSCP, FCS calculation
- Header modification up to 48 bytes (push/pop/modify) for VLAN
- L2 and L3 loop backs including swap of MAC SA and DA, Swap of IP

OAM (*)

- Hardware support for CFM compliant with 802.1ag
- Support for four ME levels in compliance with TR-101 and TR-156
- Rate limitation and filtering of OAM messages to prevent network attacks
- L2/L3/L4 control packets classifier for both user and network L2 control protocol packets per flow
- Integrated packet generator and analyzer to support OAM packet generation and analysis per Y.1731**,** including per flow BERT
- Hardware processing for L2, L3 Loop backs (swap L2 SA/DA, swap L3 SA/DA)
- Hardware Fast protecting switching within micro seconds

Multicast

- IGMP V2 and V3 compliance, together with MLDv2
- IGMP packet snooping to processor in the U/S direction
- Forwarding and multicast classification based on Source IP and Destination IP

EFM Bonding

- EFM Bonding support over G.fast (configurable 2,4,8)
- Support 8 priority queues over bonded line
- Inherent protection per EFM bonding standard

Synchronization over Packet (*)

- 1588 end-to-end Transparent Clock 1588v2
- Slave mode clock recovery

DDR SDRAM Interface

- External 32-bit DDR3-SDRAM 533 MHz interface

CPU Interface

- Integrated dual core Cortex A9 ARM (up to 800Mhz each)

Interface Options

- 2.5GE -SGMII Network I/F
- 10GE XFI network I/F(*)
- G.999.1 channelized Ethernet interface
    - 16 virtual ports per G.999.1 I/F
    - 2 x 2.5G – G.999.1
    - Optional 4 x 3.5G-G.999.1 (*)
- DDR3

Ordering options

ENET3850/99 – 2.5GbE Uplink – Switch controller supporting 16 G.fast modems

* ENET4200Z/99 – 10GbE Uplink - Switch controller support 24 G.fast modems, 10G GbE Network I/F, together with OAM/CFM

* ENET4840Z/99 – 2 x 10GbE Uplink - Switch controller support 48 G.fast modems, 10G GbE Network I/F, together with OAM/CFM, Hierarchical ACL and PTP

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