Complexity Challenges of G.FAST

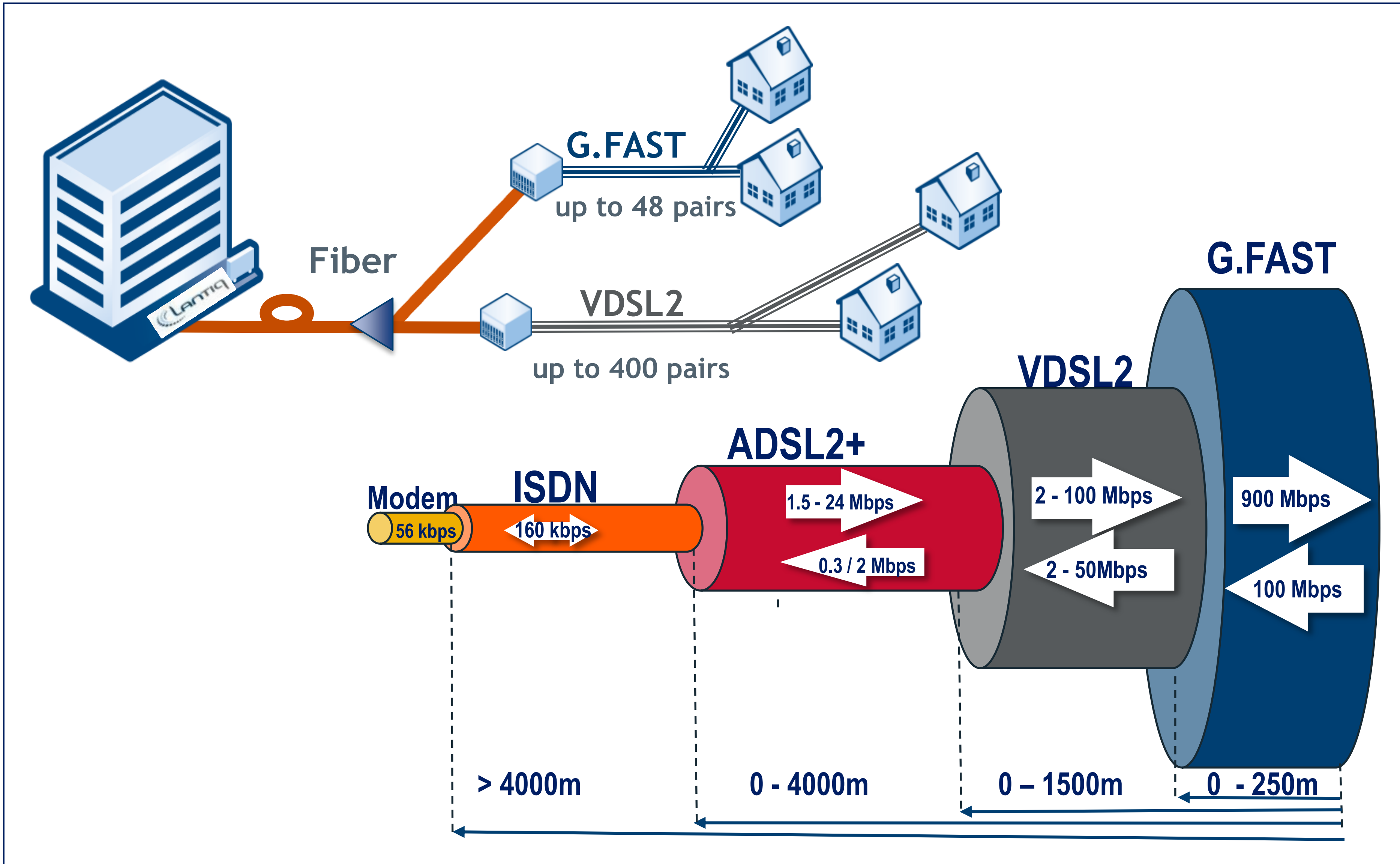
G.FAST Summit, Paris, May 20 – 22, 2014

Rudi Frenzel

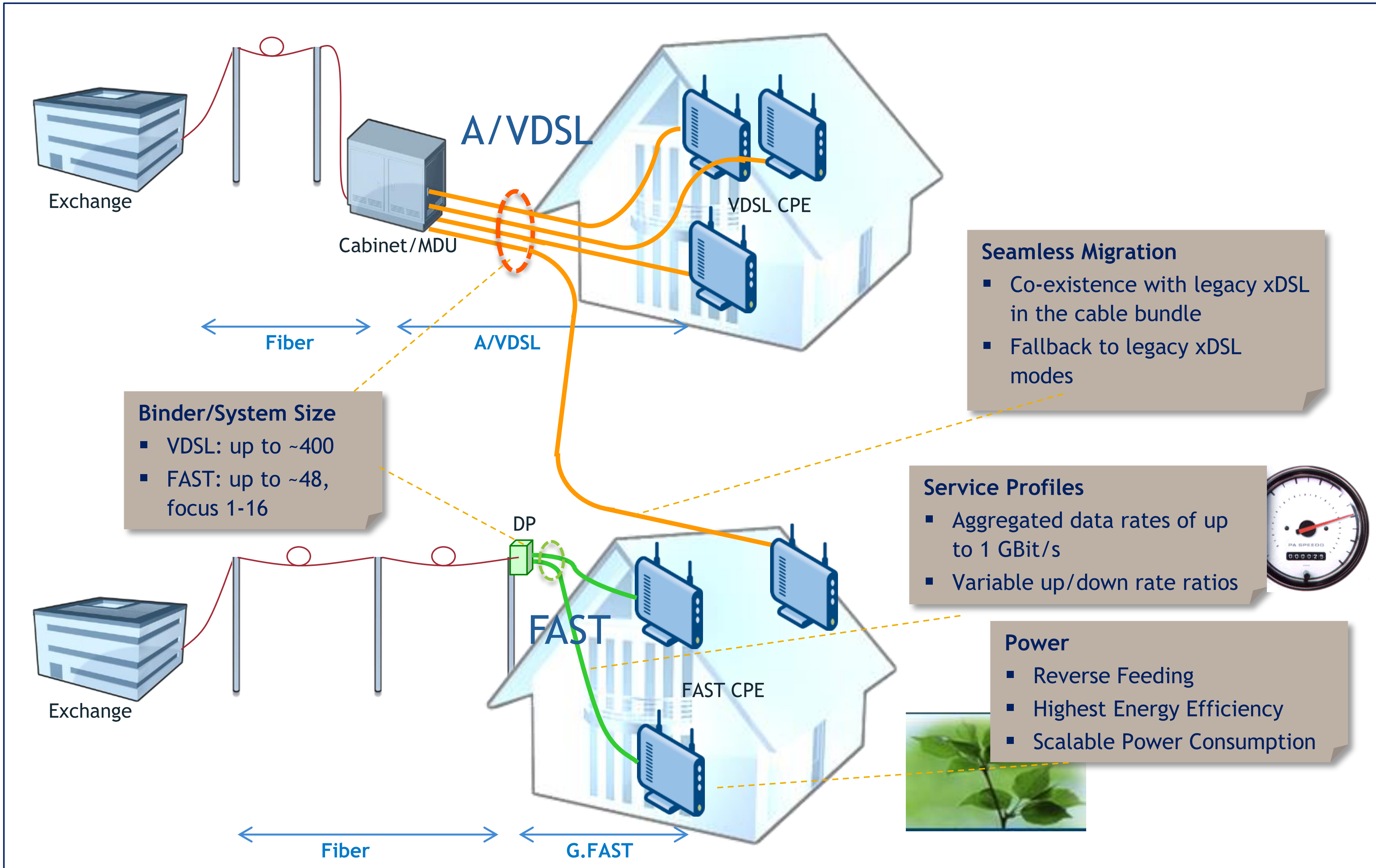
Complexity Challenges of G.FAST

- The G.FAST Application
- The wideband Twisted Pair Channel
- The G.FAST Standard
- Silicon Technology

The Access Evolution towards G.FAST



Application Driven Requirements



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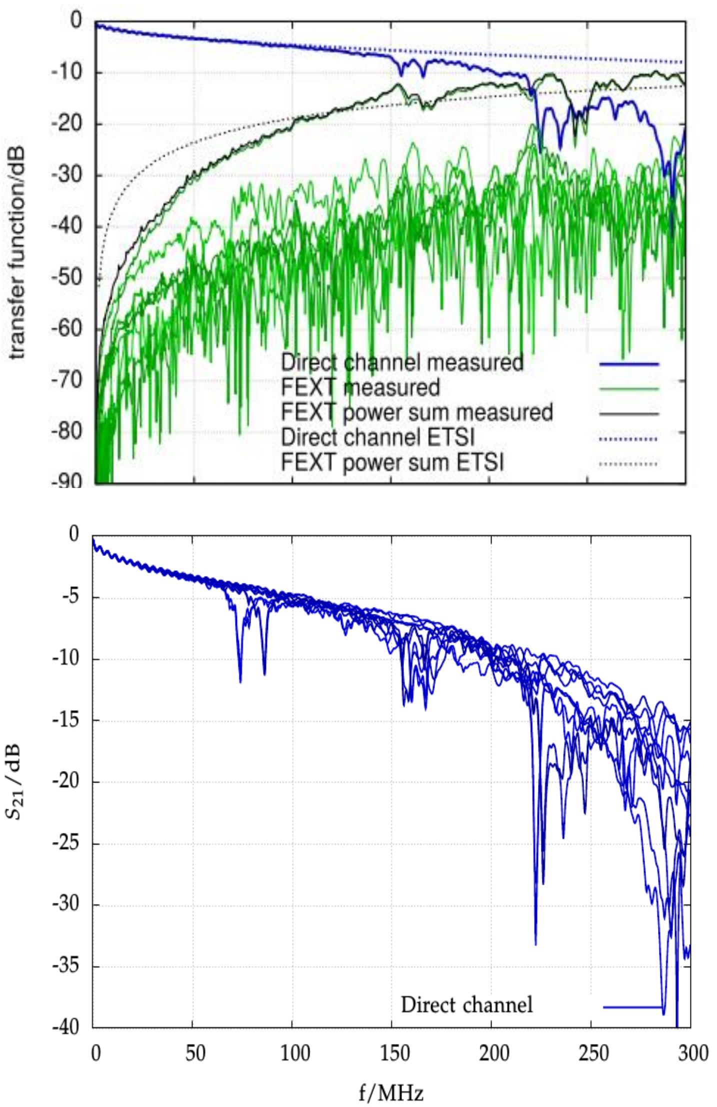
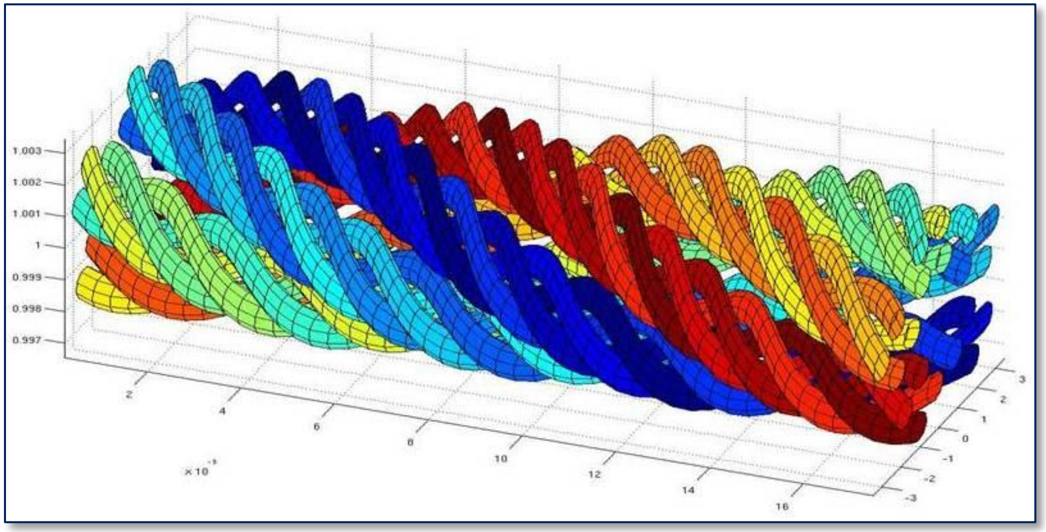
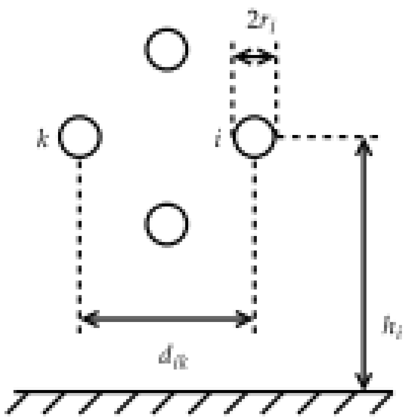
The Twisted Pair Channel above 30MHz



- The twisted pair characteristics are well known up to 30MHz from legacy xDSL2 applications
- Recently, a lot of activities are ongoing getting cable measurements for frequencies up to 200-300MHz to support accurate G.FAST performance prediction
- Obviously, a straight extrapolation of legacy *two-port-models* into the G.FAST band would not reflect critical direct path and xtalk path behavior

The Twisted Pair Channel above 30MHz

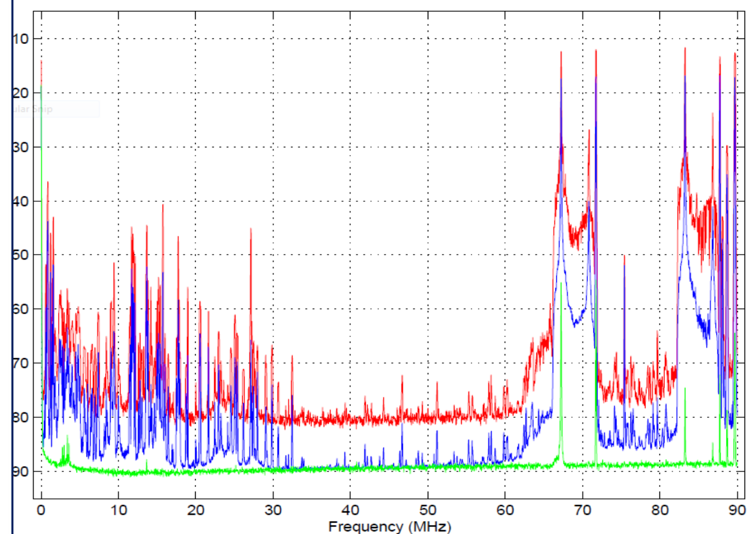




- Based on cable measurements up to 200-300MHz more accurate cable models are under development which cover the entire G.FAST bandwidth
- In order to reflect the in cable xtalk including all modes appropriate models need to include the MIMO behavior of the channel
- More details on a geometry based model approach can be found in “Strobel et al., Wideband Modeling of Twisted-Pair Cables for MIMO Applications”, Globecomm 2013.

Alien and Background Noise

- A lot of activities are ongoing to get a comprehensive view on noise sources within the G.FAST frequency band
- Region specific RF services, HAM radio, TV stations as well as FM broadcast are sources of strong RFI disturbers
- Impulse disturber in home environment
- Several reports on measurements indicate that the background / line AWGN falls below -140dBm/Hz at higher frequencies



- 67.25 MHz (Video)/70.83 MHz (Color)/71.75 MHz (Audio): TV Channel 4
- 83.25 MHz (Video)/86.83 MHz (Color)/87.75 MHz (Audio): TV Channel 6
- 88-108 MHz: Broadcast FM stations

- Source: Spectral Occupancy at VHF: Implications for Frequency –Agile Cognitive Radios. Steven W. Ellingson, IEEE 2005

Challenges from the Wideband Twisted Pair Channel

Physics	VDSL	G.FAST	Complexity
Direct path characteristics	Follows well legacy two port model	MIMO system	"MIMO Processing" algorithms, e.g. PSD control
Xtalk	Well below direct path energy	Close to direct path energy for higher frequencies	Precoder: DSP algorithms and control e.g. non-linear precoding
Common Mode xtalk	NEXT between VDSL ports.	NEXT: VDSL to G.FAST G.FAST to VDSL	Common mode management versus cost and performance
Impulse disturber	Typ. 150Mbps at 10ms SHINE	Typ. 1Gbps at 10ms SHINE	RTX queue memory
Background noise and RFI	-140dBm/Hz, HAM band, AM radio	< -140dBm/Hz, HAM, AM / FM radio, TV stations	Receive dynamics, receiver sensitivity

- The same physical media impose significantly different challenges to the G.FAST compared to VDSL2 due to the extended bandwidth range

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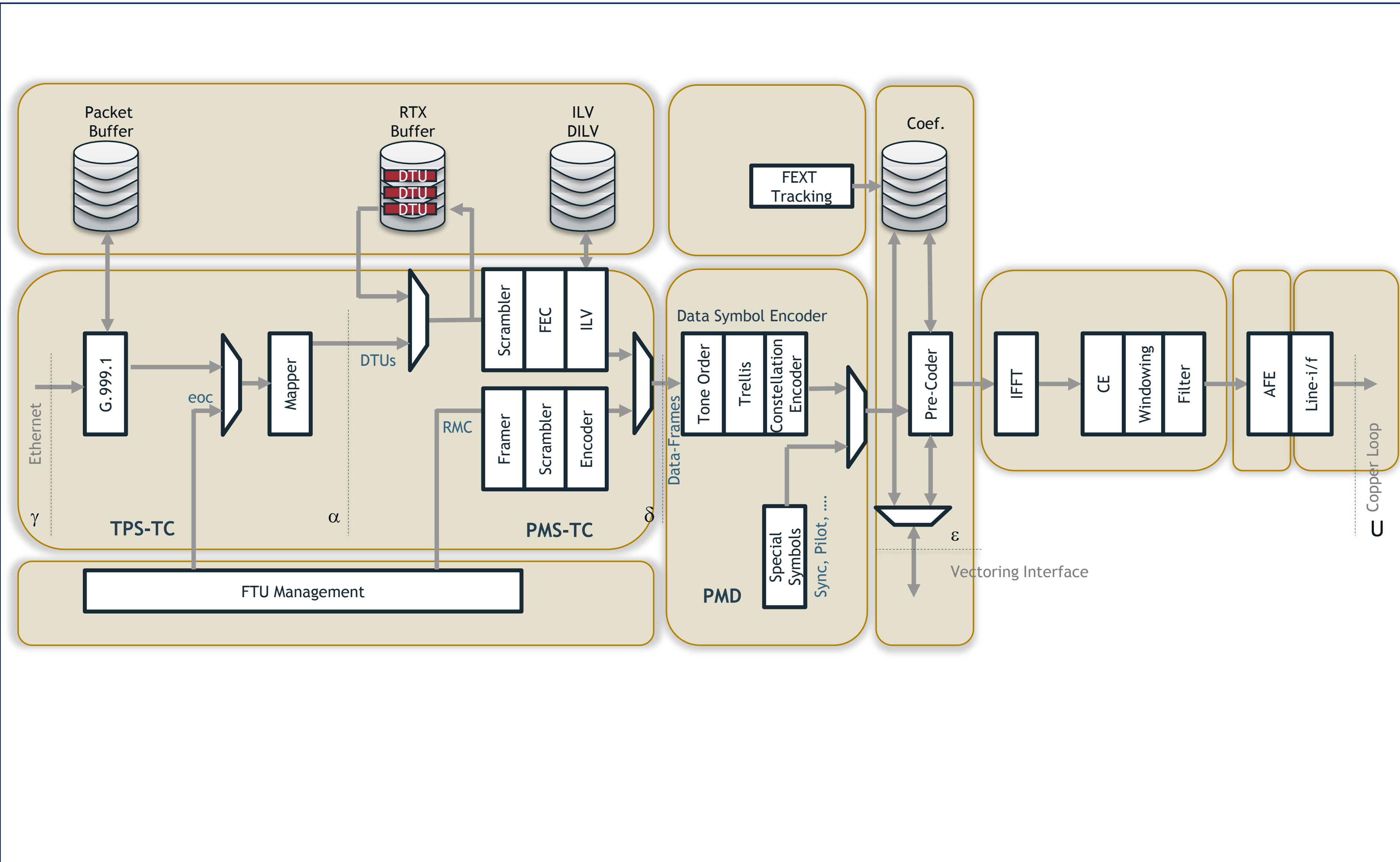
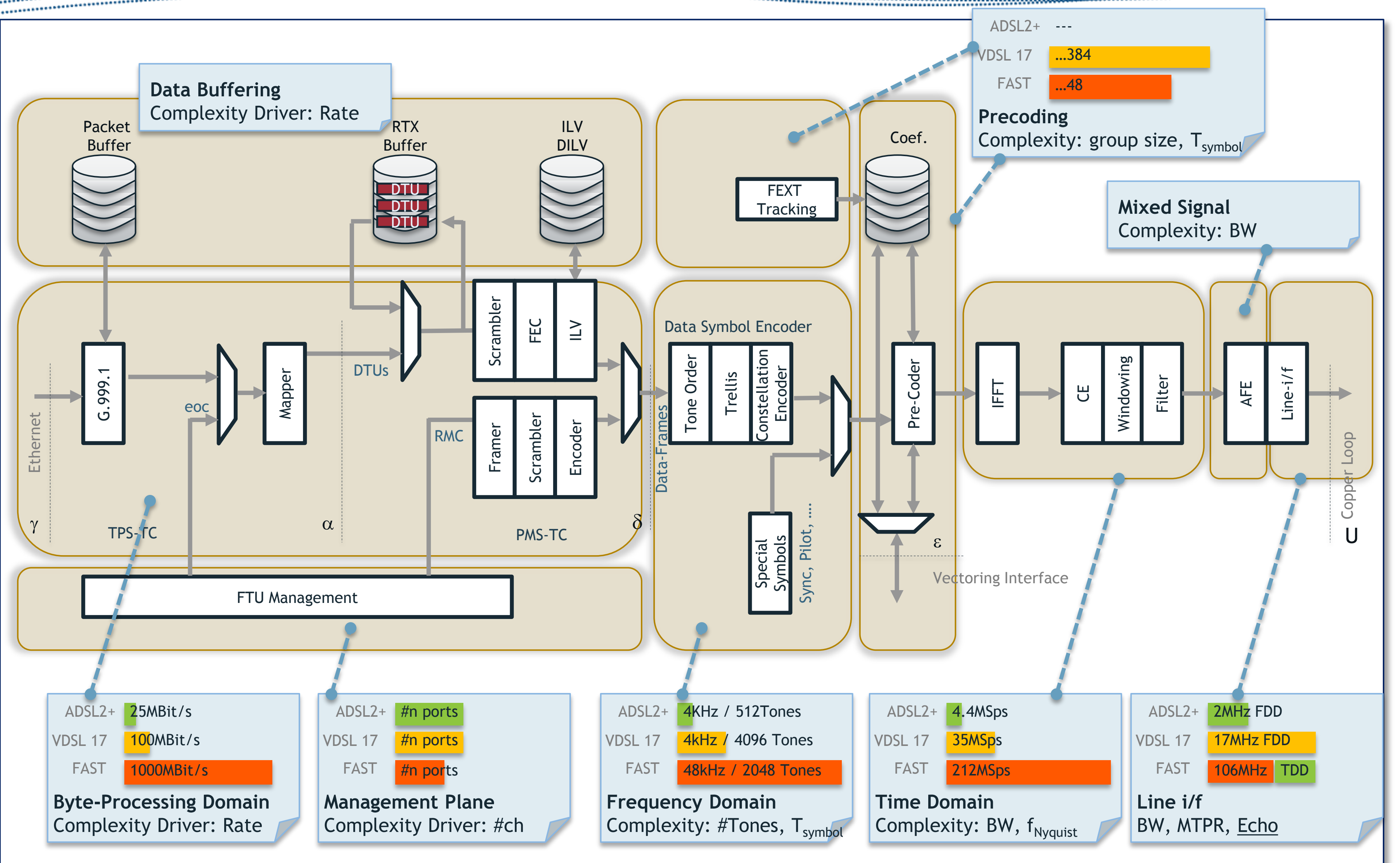
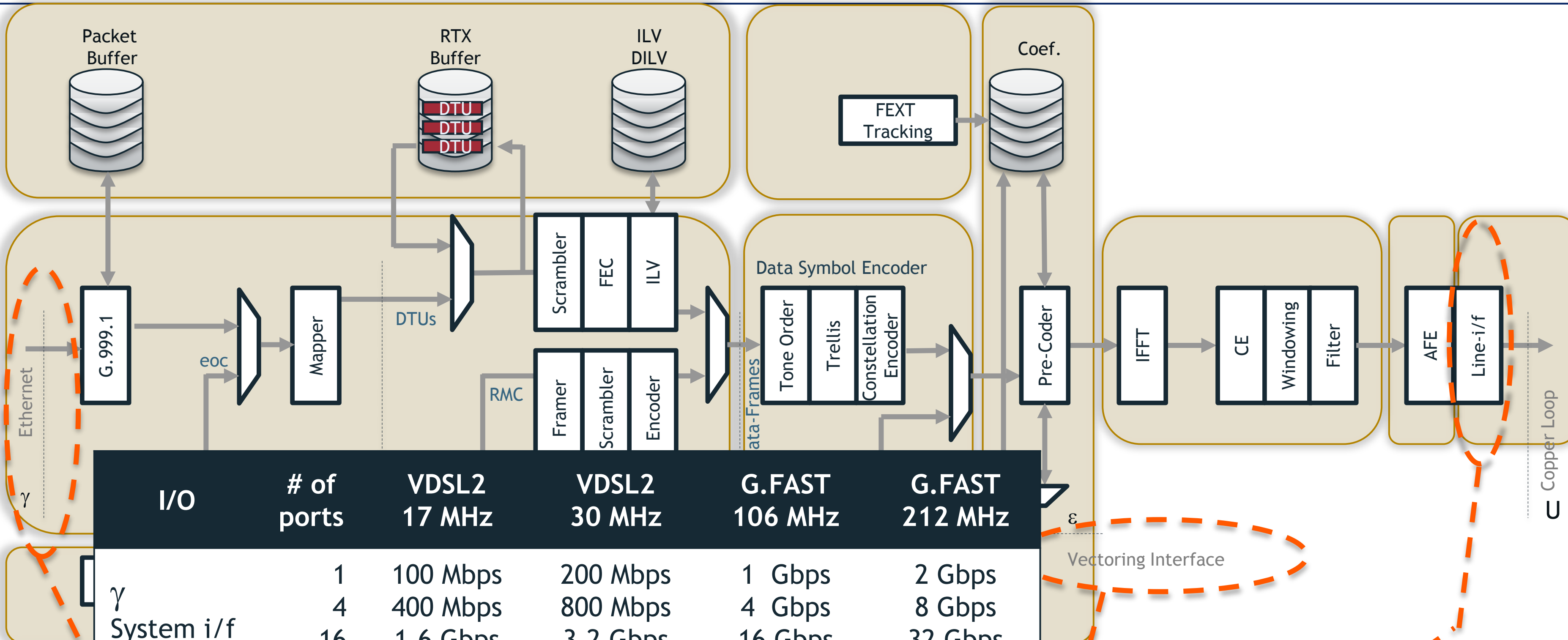
Generic Block Diagram of G.FAST Transmitter



Generic Block Diagram of G.FAST Transmitter



Total Interface Bandwidth - VDSL2 vs G.FAST



I/O	# of ports	VDSL2 17 MHz	VDSL2 30 MHz	G.FAST 106 MHz	G.FAST 212 MHz
γ System i/f	1 4 16	100 Mbps 400 Mbps 1.6 Gbps	200 Mbps 800 Mbps 3.2 Gbps	1 Gbps 4 Gbps 16 Gbps	2 Gbps 8 Gbps 32 Gbps
ε Vectoring Precoder	1 4 16	n/a 1 Gbps 4.2 Gbps	n/a 1.8 Gbps 7.1 Gbps	n/a 6.3 Gbps 25.4 Gbps	3.1 Gbps 12.6 Gbps 50.3 Gbps
D AFE i/f	1 4 16	0.56 Gbps 2.3 Gbps 9 Gbps	1.1 Gbps 4.5 Gbps 18 Gbps	3.3 Gbps 13 Gbps 54 Gbps	6.6 Gbps 26 Gbps 108 Gbps
TOTAL I/O	N=4	<4 Gbps	<8 Gbps	24 Gbps	48 Gbps

High Interface Bandwidth means
- High Package Complexity (#I/Os, routing, size)
- Power Consumption Increase
- Limited Scalability
- Additional System Cost

G.FAST Requirements and affected Areas of Complexity

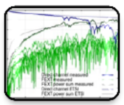
G.FAST Technology

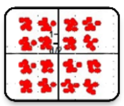

Power

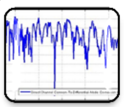

Service Profiles


System Size


Seamless Migration


MIMO Channel


Line and Alien Noise


Impulse Noise, Retx

30→106→212MHz

Key Complexity Areas

Packet Processing MIPS, Memory

Mixed Signal Performance

System Design, PCB, PSU

Algorithms

Signal Processing MIPS, Memory

Chipset Interfaces

G.FAST Requirements and affected Areas of Complexity

G.FAST Technology

- Power
- Service Profiles
- System Size
- Seamless Migration
- MIMO Channel
- Line and Alien Noise
- Impulse Noise, Retx
- 30➔106➔212MHz

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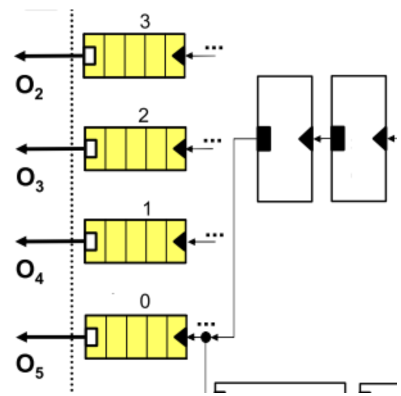

G.FAST Requirements and affected Areas of Complexity

G.FAST Technology


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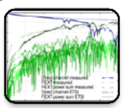
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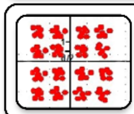
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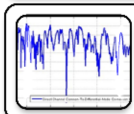
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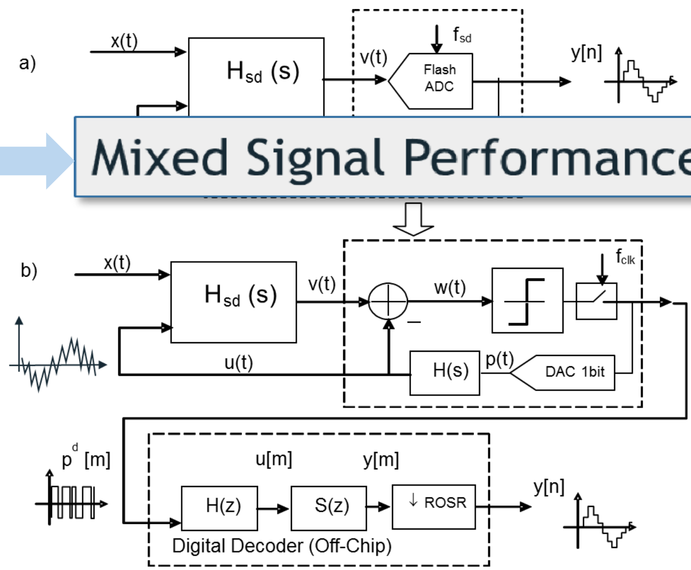

Mixed Signal Performance

G.FAST Requirements and affected Areas of Complexity

G.FAST Technology


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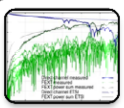
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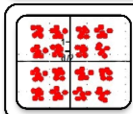
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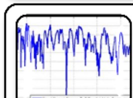
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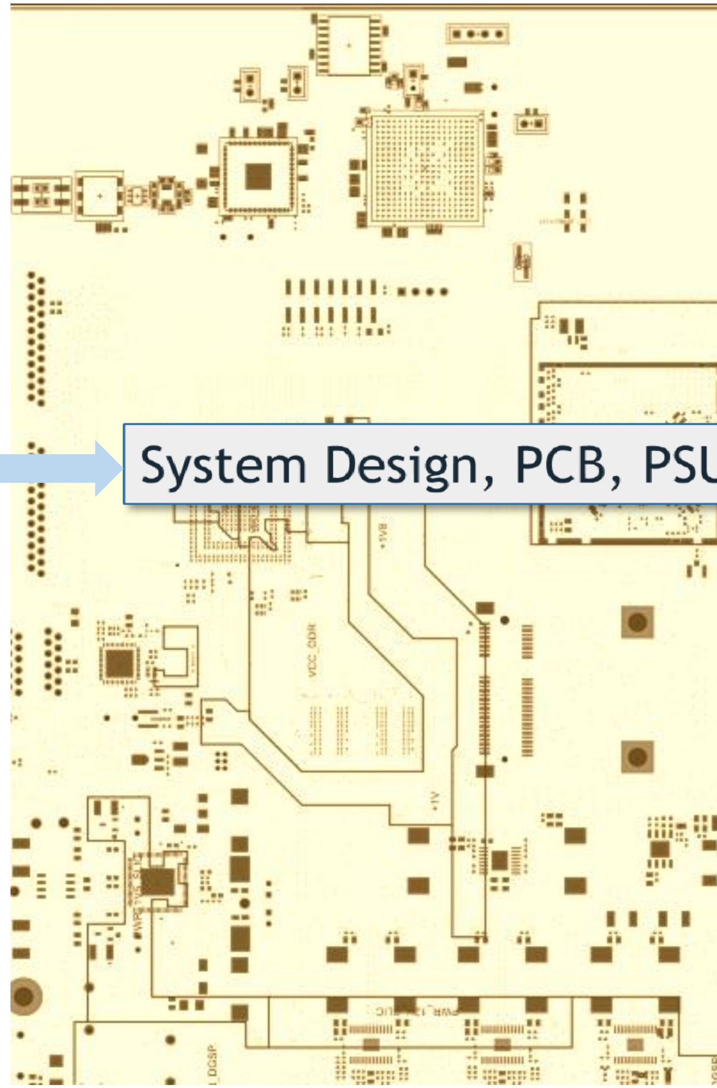

System Design, PCB, PSU

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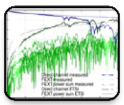
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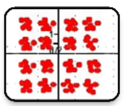
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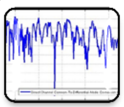
Impulse Noise, Retx


30➔106➔212MHz

Key Complexity Areas

Algorithms

```
    if (n != nold) {
        en=n;
        oldg=gammln(en+1.0
        nold=n;
    } if (p != pold) {
        pold=p;
    }
    sq=sqrt(2.0*am*pc);
    do {
        do {
            angle=PI*ran1(
            y=tan(angle);
            em=sq*y+am;
        } while (em < 0.0
        em=floor(em);
        t=1.2*sq*(1.0+y*y)
            -gammln(en-em+
    } while (ran1(idum) >
    bnl=em;
  }
  if (p != pp) bnl=n-bnl;
  return bnl;
}
```

```
int j;
long k;
static long iy=0;
static long iv[NTAB];
float temp;

if (*idum <= 0 || !iy) {
    if (-(*idum) < 1) *idum=1;
    else *idum = -(*idum);
        if (*idum < 0) *idum += IM;
        if (j < NTAB) iv[j] = *idum;
    }
    iy=iv[0];
}
k=(*idum)/IQ;
*idum=IA*(*idum-k*IQ)-IR*k;
if (*idum < 0) *idum += IM;
j=iy/NDIV;
iy=iv[j];
iv[j] = *idum;
if ((temp=AM*iy) > RNMX) return RNMX;
else return temp;
```

G.FAST Requirements and affected Areas of Complexity

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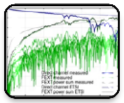
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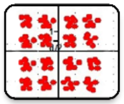
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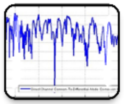
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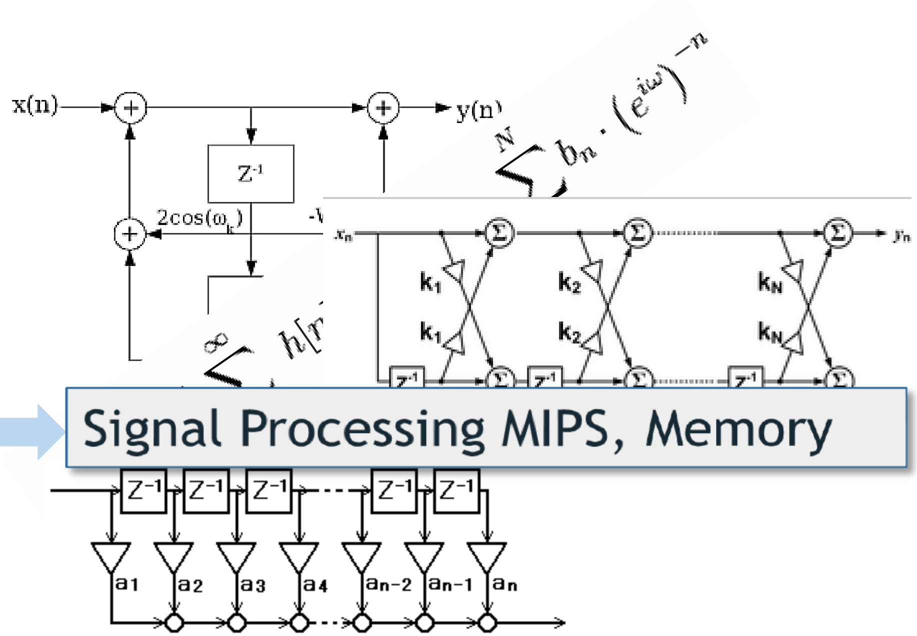

G.FAST Requirements and affected Areas of Complexity

G.FAST Technology

Key Complexity Areas

 Power

 Service Profiles

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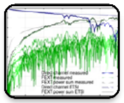
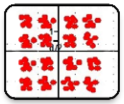
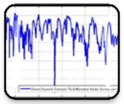
 MIMO Channel

 Line and Alien Noise

 Impulse Noise, Retx

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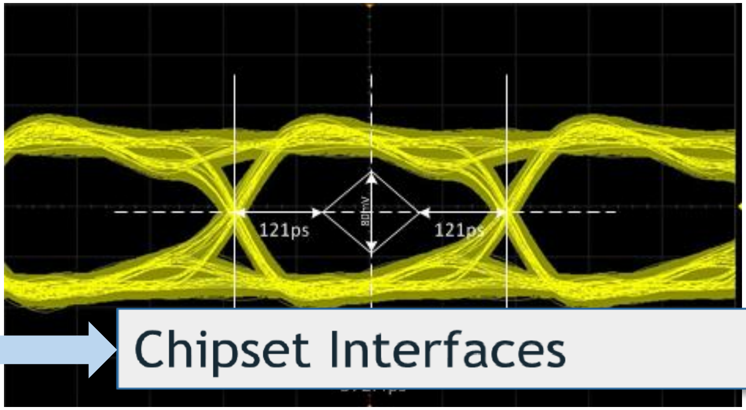

Chipset Interfaces

G.FAST Requirements and affected Areas of Complexity

Parameters	ADSL2+	VDSL2, 17M	VDSL2 30M	Fast, 106a	Fast, 212a
Max. ATP downstream (dBm)	20,4 dBm	14,5 dBm	14,5 dBm	4 dBm	tbd
Max. ATP upstream (dBm)	12,5 dBm	14,5 dBm	14,5 dBm	4 dBm	tbd
Max aggragate data rates	25 Mbps	150 Mbps	250 Mbps	~1000Mbps	tbd
TP channel - loop lengths	> 4km	0 - 1.5km MIMO	0 - 500 m MIMO	0-250 m strong MIMO	tbd strong MIMO
Xtalk cancellation	n/a	Vectoring acc. ITU-T - G.993.5	Vectoring acc. ITU-T - G.993.5	Vectoring part of G.9701	Vectoring part of G.9701
Vectoring Group Sizes	n/a	up to 400	32/64 (MDU ?)	up to 48	tbd
Precoder type	n/a	linear	linear	linear	tbd (non-linear)
Max bandwidth	2,2 MHz	17,6 MHz	30 MHz	106 MHz	(212 MHz)
Number of carrier (total)	512	4096	3478 (4096)	2048	4096
Symbol rate (mandatory)	4,0588 kHz	4 kHz	8 kHz	48 kHz	48 kHz
Duplexing	FDD	FDD	FDD	TDD	TDD
QAM max constellation size	15 bit	15 bit	15 bit	12 bit	12 bit

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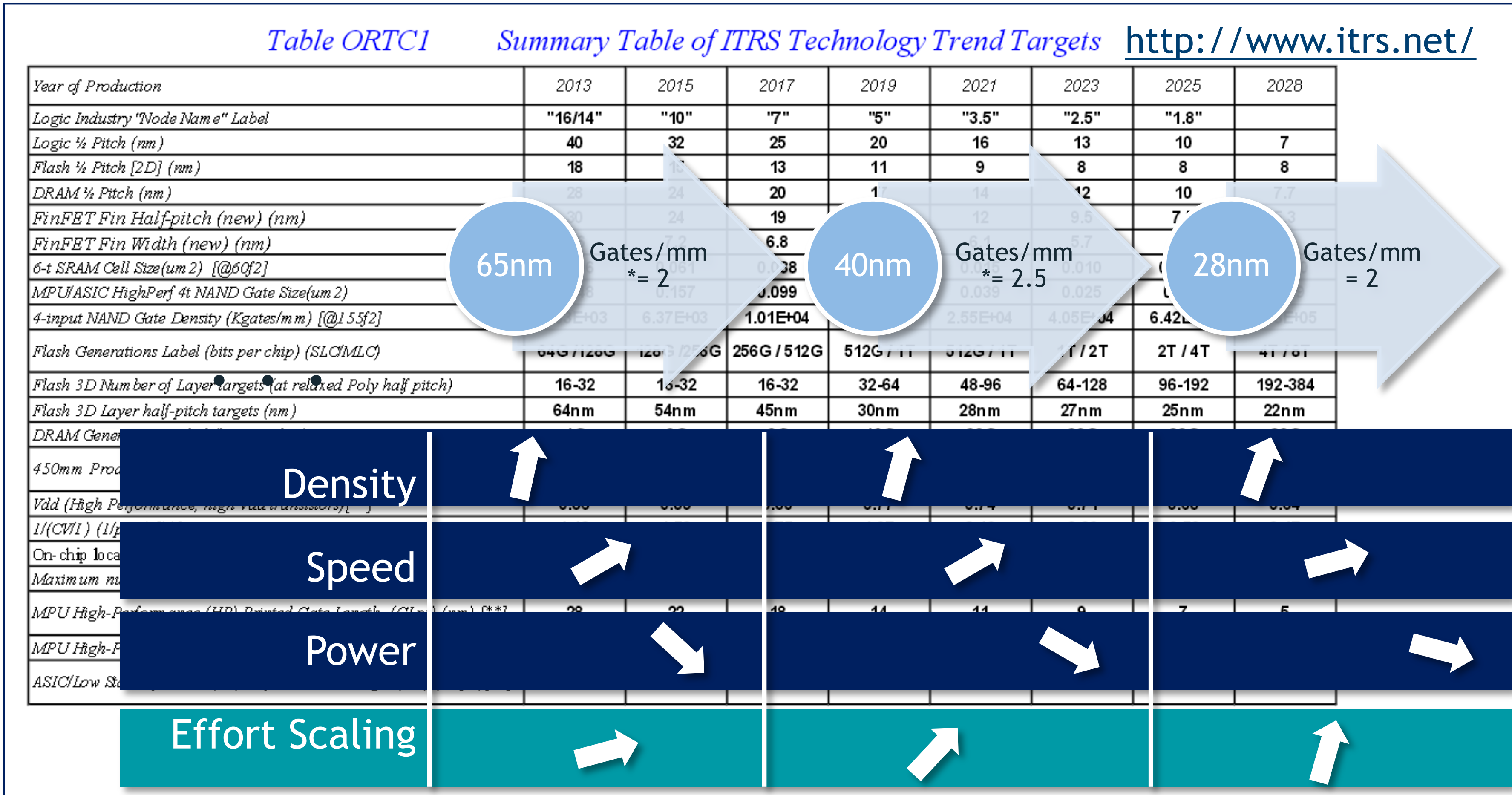
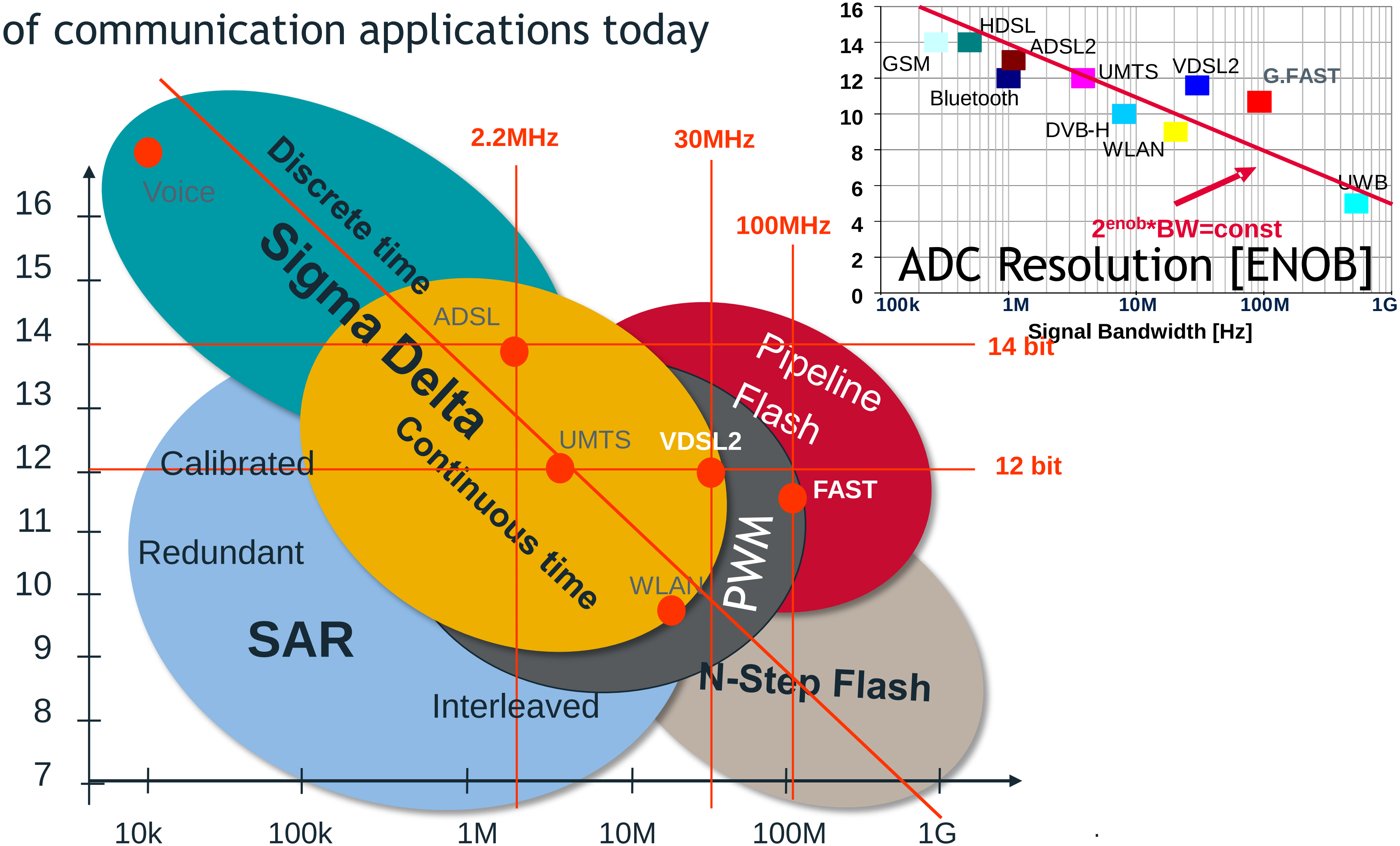
Silicon Technology Solution to G.FAST



- Moore's Law provides the solution to cope with the G.FAST challenges – at least for the *digital* part of it
- What about AMS ?

The Bandwidth Challenge

Sigma delta ADC's cover most
of communication applications today



Sigma Delta ADCs Reach Pipeline Domain

- Figure of Merit

$$FoM = \frac{Power}{(2 \cdot f_{BW} \cdot 2^{ENOB})} \quad [\frac{J}{step}]$$

- CT SD incl. AAF out performs pipeline converters

	Pipeline ADC incl. Prefilter	Sigma delta ADC incl. prefilter
Area	2.4mm2	1.2mm2
Power	217mW	100mW
Bandwidth	30MHz	30MHz
ENOB	11.1	11.3
Clock	105MHz	600MHz
FOM incl. Filter	1.65	0.65

AFE Experiences

- Analog blocks don’t scale well with technology nodes in general
- However, technology innovation enables architectural changes
  - Utilization of speed and logic
  - Innovation on converter types
- Example: Sigma Delta & PWM ADC‘s cover almost complete range of communication
  - Sufficient ENOB for target application
  - Superior in chip size and power compared to pipeline converters

Key Take - Aways

- The G.FAST application drives complexity on chip level as well as on system level significantly compared to legacy xDSL. The key factors are:

  Data rates – Bandwidth – Channel Characteristics above 30MHz

- On chip-set level the complexity increases for
  - Packet Processing - MIPS, Memory
  - Algorithms and Digital Signal Processing - MIPS, Memory, Architectures
  - Chipset Interfaces (data rates & power) and Mixed Signal Performance

- The CMOS technology scaling provides the means to cope with the complexities of G.FAST *today* by
  - Density, speed and power improvements for digital logic and memories
  - Enabler for innovations on architectures and circuit design for the analog / mixed signal field

Lantiq | Connecting the Dots