

Known Limitations

There is a known issue (CCR [#01644165](#)) during LEC checking, workaround is described in the user guide.

Summary of updates to 4.0.2/3 releases that are included in 4.1 release.

Setup/General

- This release is mandatory for sign off of any design in 7nm node.
- Most tool versions have been updated.

Synthesis

- a) Default synthesis scripts use Genus native format. (CUI)
- b) Added support for memory wrappers.
- c) Uses MMMC file for library read in
- d) Supports metrics

Jasper AFL

- a) Added basic DfT checks
- b) Updated afl_setup.tcl for new tool versions.

DFT, ATPG and ATPG simulations

- a) Modus 16.20 tool is now default ATPG tool.
- b) Encounter Test is being phased out, still supported in legacy mode.
- c) Several options included to run_atpg.csh command script.
- d) Option to separate at-speed from stuck-at test mode, driven by IPS requirements.
- e) Option to define timing relations between scan signals to counteract insertion delays on scan signals.
- f) Xcelium 16.11 is now default simulator for ATPG patterns, Incisive supported in legacy mode.
- g) Compilation and sdf annotation divided in two different scripts.
- h) Simulation reports split per corners.
- i) Simulation debug option.

LEC

- a) 2-stage flow is mandatory, 1 stage flow phased out.
- b) 2.0 1801 format supported

CLP

- a) 16.2 commands supported
- b) 1801 2.0 supported

Innovus

- a) Scripts use Common_UI mode
- b) Shares same MMMC file as Genus
- c) Enhanced multithreading

Jiras

Key	Summary	Components
SISFLOW-495	Add \$TMAX_ROOT in http://lvsvn:20000/svn/ip_factory/tags/ipf_scripts_phase4.0.2/scripts/setup/setup_dirs.tcl	DFT
SISFLOW-532	Incorrect specification of the in2reg path group	SYNTHESIS
SISFLOW-509	ATPG run time error	Compile check, DFT
SISFLOW-428	Review AFL DFT Checks	Jasper AFL
SISFLOW-534	Commands for cpf are unusable with innovus 16.20	PNR
SISFLOW-545	DFT : RDF flow not working if the RTL_SCAN_IN=SCAN_IN	DFT
SISFLOW-538	Remove -linedebug from irun commands	DFT Architecture & Methodology
SISFLOW-535	Review digital checklist items related to DFT activity tracking and completion	DFT
SISFLOW-300	SIS Release Flow JIRA fields	DR0-DR3, GA Checklists
SISFLOW-456	Doc 4.0.2 updates	User Guide Documentation
SISFLOW-531	Updates for xcelium	DFT, User Guide Documentation
SISFLOW-440	update tech_lib_setup.tcl for ATPGLIB to pickup verilog not mentor views	DFT
SISFLOW-487	DFT : Inclusion of option inlcudenetnames=yes to write vectors	DFT
SISFLOW-476	sgdc overwritten in case of fatal error	SPYGLASS
SISFLOW-465	Add ability in ATPG scripts to support control of switching variables	DFT
SISFLOW-501	request to change back attribute use_scan_seqs_for_non_dft to false	SYNTHESIS

SISFLOW-482	tech_lib_setup for TSMC28HPC_9T: wrong CLK BUFFERS/CLK INVERTERS list	SETUP
SISFLOW-502	Please update setup_project_template.csh for openLava genus Issue	SETUP
SISFLOW-537	run_phys.csh -synth genus stop workin because it cannot find file	LEC Equivalence Checking
SISFLOW-519	Conformal LEC do file does not function if GENUS version 16.x used	LEC Equivalence Checking
Key	Summary	Components
SISFLOW-170	Each checklist question should have a unique and identified owner	DR0-DR3, GA Checklists
SISFLOW-451	DFT checks in DR2/3	DR0-DR3, GA Checklists
SISFLOW-454	check ATPG script for compatibility with Modus	DFT
SISFLOW-472	TESTMODES text in setup_project_template.csh incorrect	SETUP
SISFLOW-491	compilation script does not support +define	Compile check
SISFLOW-498	syn_opt --physical breaks DfT	SYNTHESIS
SISFLOW-533	Change DR0 questions regarding top-level I/O to architecture level only	DR0-DR3, GA Checklists
SISFLOW-493	rc_flow.tcl make the "Attributes to prevent non-alphanumeric characters" a non-default option	SYNTHESIS
SISFLOW-530	Please improve some of the questions in the verification section of the DR1 checklist	DR0-DR3, GA Checklists
SISFLOW-441	UNIQUIFY step needs to take into account preserved modules.	SYNTHESIS
SISFLOW-524	UNIQUIFY MODULES can fail	SYNTHESIS
SISFLOW-435	RDF does not support synthesis of pure combinational block.	SETUP, SYNTHESIS
SISFLOW-489	[Innovus] change timing_apply_default primary_input_assertion parameter to false	PNR
SISFLOW-516	[TUI-666] message reported in the flow	SYNTHESIS
SISFLOW-520	Abort the scripts if there are errors in constraint file	SYNTHESIS
SISFLOW-447	RDF creates two gate level netlists, <>.v & <>.vg	SYNTHESIS
SISFLOW-521	Check timing intent	SYNTHESIS
SISFLOW-510	Innnous tool does not automatically place IOs	PNR
SISFLOW-527	Synthesis crashes on set_analysis_view for multi-mode design	SYNTHESIS
SISFLOW-529	Driver for a test pin is an internal node	DFT

Key	Summary	Components
SISFLOW-526	Update cdc.do to remove the text for report skip instances	CDC
SISFLOW-417	Support simulations with black boxes	DFT
SISFLOW-484	Request for user defined ncsim arguments	DFT
SISFLOW-523	issue in expand.pl resulting in incorrect expanded.f	SETUP
SISFLOW-522	issue in filelist setup.csh resulting in incorrect rdf4.0.1 expanded.f	SETUP
SISFLOW-504	Introduce timing parameters for Modus for the better simulation control	DFT Architecture & Methodology
SISFLOW-503	Update documentation fro CCD 16.2 when tool is available	CDC, SDC
SISFLOW-406	Improve clock domain handling for at-speed atpg	DFT
SISFLOW-514	Create clear separation for designs that require dedicated at-speed test modes	DFT Architecture & Methodology
SISFLOW-518	CCD Tool Crash due to -mcc option in single SDC mode	SDC
SISFLOW-480	Need checker for scan abstract and RTL pin compatibility	RTLDesignFlow checklist
SISFLOW-511	CCD SDC report files	CDC
SISFLOW-513	Request for lint ruleset update in CCD/Superlint vs. Spyglass	LINT
SISFLOW-470	CoE Recommendation for Analog-Digital isolations	DFT Architecture & Methodology
SISFLOW-461	Update AFL DFT rules and associated scripts	Jasper AFL
SISFLOW-507	Update AFL to jasper 2016.09	LINT
SISFLOW-508	The advised version of Jasper has problems to re-apply waivers after exporting them and re-running the tool	Jasper AFL
SISFLOW-473	CCD creates its own clock groups, having only 2 clocks in 1 clock group even when there are more than 2 clocks in a clock group.	SDC
SISFLOW-500	A set of waivers that live alongside the async FIFO	Jasper AFL
SISFLOW-478	update sdc templates to correct use of -nocase with -regexp switch	SETUP, STA
Key	Summary	Components
SISFLOW-479	script bug if HARD_MACRO_INSTANCE_NAME is defined	PNR
SISFLOW-464	The sync flops are getting changed to non-sync flops	SYNTHESIS
SISFLOW-494	typo in et_flow_ips.tcl	DFT

<u>SISFLOW-460</u>	<u>problem with read_dft_abstract for multiple instances of the same basename</u>	<u>DFT</u>
<u>SISFLOW-469</u>	<u>Preserve is not working properly</u>	<u>SYNTHESIS</u>
<u>SISFLOW-481</u>	<u>date stamp checking in PNR part of run_phys.cssh causes overnight runs to fail</u>	<u>PNR</u>
<u>SISFLOW-488</u>	<u>update EDI libs in tech_lib_setup.tcl from NLDM to ECSM</u>	<u>SETUP</u>
<u>SISFLOW-376</u>	<u>Enable faster ATPG by adding hosts=lst</u>	<u>DFT</u>
<u>SISFLOW-485</u>	<u>Convert ET scripts to Modus</u>	<u>DFT Architecture & Methodology</u>
<u>SISFLOW-443</u>	<u>RDF UserGuide Updates</u>	<u>User Guide Documentation</u>
<u>SISFLOW-474</u>	<u>Please add extra question in DR1 checklist under project management</u>	<u>DR0-DR3, GA Checklists</u>
<u>SISFLOW-466</u>	<u>additional commands in rc_flow.tcl to help LEC</u>	<u>LEC Equivalence Checking, SYNTHESIS</u>
<u>SISFLOW-468</u>	<u>Conformal CCD tool crashing because variable used out of scope.</u>	<u>CDC, SETUP</u>
<u>SISFLOW-467</u>	<u>CDC script issue for handling multiple design modes</u>	<u>CDC</u>
<u>SISFLOW-450</u>	<u>DR1 : 2.08</u>	<u>DR0-DR3, GA Checklists</u>
<u>SISFLOW-458</u>	<u>DFT : HIGHZ instruction support in BSCAN</u>	<u>DFT</u>
<u>SISFLOW-429</u>	<u>add switches into RC for PPA reporting</u>	<u>PNR</u>
<u>SISFLOW-455</u>	<u>Enhance DFT simulation scripts to support parallel runs</u>	<u>DFT</u>
<u>SISFLOW-453</u>	<u>CCD multi mode SDC checks broken</u>	<u>SDC</u>
<u>SISFLOW-449</u>	<u>Consider adding a checklist item to DR2 to ask designer if they have carefully read re-use block documentation</u>	<u>RTLDesignFlow checklist</u>
<u>SISFLOW-515</u>	<u>Change order of syn_opt to pre scan</u>	<u>SYNTHESIS</u>
<u>SISFLOW-372</u>	<u>Add DC scripts to RTL Design Flow and to Stork</u>	<u>SYNTHESIS</u>
<u>SISFLOW-544</u>	<u>AFL Lint - reachable FSM states reported as unreachable?</u>	<u>Jasper AFL</u>
<u>SISFLOW-471</u>	<u>support prefixes to auto inserted scan I/O names</u>	<u>DFT</u>
<u>SISFLOW-193</u>	<u>Update scripts for -cfg switch</u>	<u>SETUP</u>
<u>SISFLOW-222</u>	<u>Tidy up indentation</u>	<u>SETUP</u>

<u>SISFLOW-346</u>	<u>Consider use of -advanced switch with check_dft_rules during synthesis</u>	<u>DFT, SYNTHESIS</u>
<u>SISFLOW-452</u>	<u>Minor editorial correction in filelist_setup.csh file</u>	<u>SETUP</u>
<u>SISFLOW-351</u>	<u>The default for this attribute should be true set_attr hdl_auto_async_set_reset</u>	<u>SYNTHESIS</u>
<u>SISFLOW-512</u>	<u>Enhance Genus area reporting with Flops per module-instance count</u>	<u>SYNTHESIS</u>
<u>SISFLOW-426</u>	<u>Linehold generation for ATS in RDF</u>	<u>DFT</u>
<u>SISFLOW-420</u>	<u>Add RC/Genus warnings when CTL is not loaded for IPS project</u>	<u>DFT</u>
<u>SISFLOW-496</u>	<u>Generating reports after AFL run</u>	<u>Jasper AFL</u>
<u>SISFLOW-486</u>	<u>Reuse question clarification in DR1/2 checklist - how to raise DRU JIRA</u>	<u>DR0-DR3, GA Checklists</u>