Si4460/61/63/64 RF ICs Layout Design Guide

1. Introduction

The purpose of this application note is to help users design PCBs for the next generation EZRadioPRO™ RF ICs, i.e. the Si4460/61/63/64 devices (henceforth referred to as EZRadioPRO™ RF ICs) using good design practices that allow for good RF performance. The matching principles described in detail in "AN627: Si4460/61 Low-Power PA Matching" and in "AN648: Si4463/64 TX Matching".

The RF performance and the critical maximum peak voltage on the output pin strongly depend on the PCB layout as well as the design of the matching networks. For optimal performance, Silicon Labs recommends the use of the PCB layout design hints described in the following sections.

2. Design Recommendations when Using Si4460/61/63/64 RF ICs

- Extensive testing has been completed using reference designs provided by Silicon Labs. It is recommended that designers use the reference designs "as-is" since they minimize detuning effects caused by parasitics or generated by poor component placement and PCB routing.
- The compact RF part of the designs is highlighted by a silkscreen frame, and it is strongly recommended to use the same framed RF layout in order to avoid any possibility of detuning effects. Figure 1 shows the framed compact RF part of the designs.

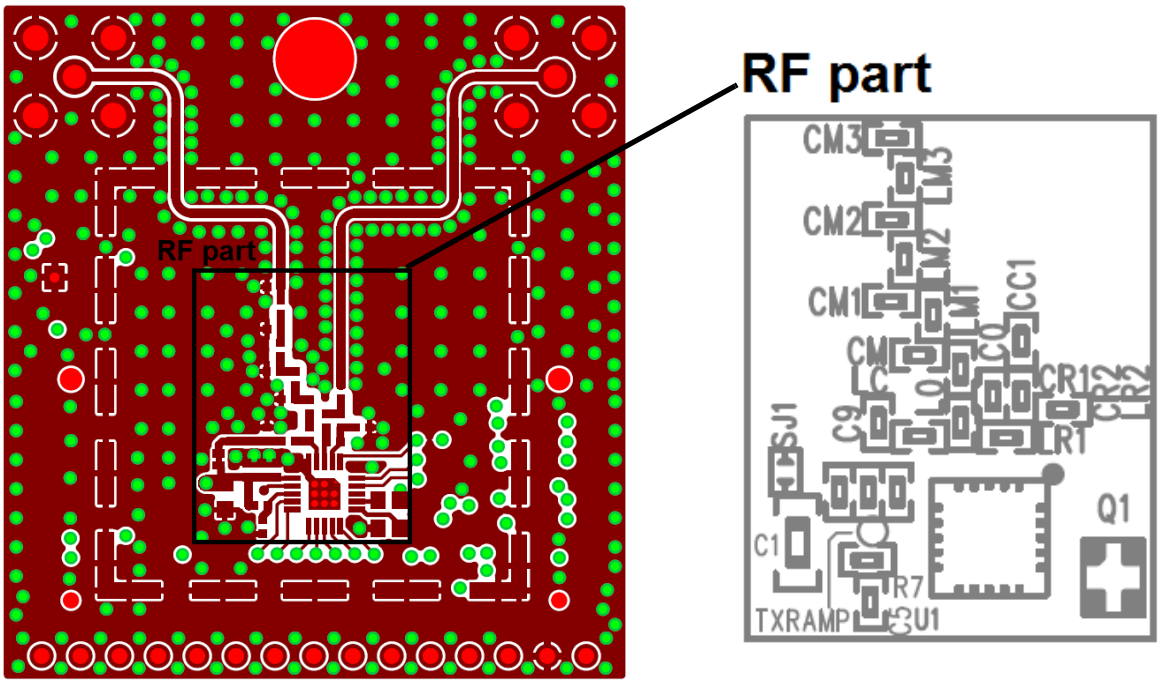


Figure 1. Compact RF Part of the Designs Highlighted on Top Silkscreen

- When layouts cannot be followed as shown by the reference designs (due to PCB size and shape limitations), the layout design rules described in the following sections are recommended.

Copyright © 2012 by Silicon Laboratories

2.1. Matching Network Types and Layout Topologies for the Si4460/61/63/64 RF ICs

The Si4460/61/63/64 devices can use the following TX matching networks:

- Class E (CLE)
- Switched Current (SWC)
- Square-Wave (SQW)

The basic types of board layout configurations are as follows:

- Split TX/RX
- Direct Tie
- Switched TX/RX
- Diversity

In the Split TX/RX type, the TX and RX paths are separated, and individual SMA connectors are provided for each path. This type of Pico Board is best suited to demonstrations of the output power and sensitivity of the EZRadioPRO™ RF ICs.

In the Direct Tie type, the TX and RX paths are connected together directly, without any additional RF switch.

In the Switched TX/RX type, the boards contain a single antenna and a single-pole double-throw (SPDT) RF switch to select between the TX and RX paths.

In the Diversity type, there are two antennas, both of which can be connected either to the TX or the RX path by a double-pole double-throw (DPDT) RF switch.

3. Guidelines for Layout Design When Using the Si4460/61/63/64 RF ICs in Pico Board Form

The typical power regime of the Si4461 is in the +13 to +16 dBm range, while the Si4460 is primarily devoted to the +10…+13dBm applications. For these devices, the preferred matching types for the 315 to 950 MHz frequency range are the CLE and the SWC. The operating principles of these types and the reference designs with element values are given in “AN627: Si4460/61 Low-Power PA Matching”.

For the versions of RF Pico Boards using the Si4463/64 RF ICs (i.e., +20 dBm PA) with CLE and SWC type Split TX/RX and Direct Tie type matchings, general layout guidelines similar to those of the Si4460/61 RF ICs (i.e., +10...+16 dBm PA) can be applied. However, some small additional amount of filtering might be necessary depending on the harmonic restrictions of the relevant EMC regulation. The layout issues of the SQW type matching will be discussed in this section as well. This type of matching can be used effectively when the required output power is high and the operating frequency is low (e.g. 169 MHz). The operating principles of these types and the reference designs with element values are given in “AN648: Si4463/64 TX Matching”.

It is not surprising that the increased TX output power of the Si4463/64 chips is accompanied by a corresponding increase in the absolute level of harmonic signals. Since most regulatory standards (e.g. FCC, ETSI, ARIB etc.) require the harmonic signals to be attenuated below some ***absolute*** power level (in watts or dBm), the amount of low-pass filtering required is generally greater on an RF Pico Board using an Si4463/64 chip. Thus the RF Pico Board layout for the Si4463/64 RF IC may contain a few more components in the L-C low pass filter.

Furthermore, in the case of SQW type matching, it is necessary to pay closer attention to the shape and amplitude of the voltage waveform at the TX output pin of the device due to the increase in output power. Silicon Labs recommends the addition of a harmonic termination circuit (formed by the LH, CH, and RH components) placed in parallel shunt-to-GND configuration at the input of the low-pass filter. This harmonic termination circuit helps to maintain the desired voltage waveform at the TX output pin by providing a good impedance termination at very high harmonic frequencies. Please refer to “AN648: Si4463/64 TX Matching” for further details on this subject.

Some general rules of thumb for designing RF-related layouts for good RF performance are:

- Use as much continuous ground plane metalization as possible.
- Avoid the separation of the ground plane metalization.
- Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
- Use a series of GND vias (a so called “via curtain”) along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10^{th} harmonic. This is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.
- Avoid using long and/or thin transmission lines to connect the components. Otherwise, due to its distributed parasitic inductance some detuning effects can occur.
- Try to avoid placing the nearby inductors in the same orientation to reduce the coupling between them. Use tapered line between transmission lines with different width (i.e. different impedance) to reduce internal reflections.
- Avoid using loops and long wires to obviate its resonances.
- Always ensure good V_{DD} filtering by using some bypass capacitors (especially at the range of the operating frequency).

3.1. Class E Split TX/RX Type Matching Network Layout Based on the 4463-PCE20B915 Pico Board (Separate TX and RX Paths, with Two Antennas)

Examples shown in this section are mainly based on the layout of the 4463-PCE20B915 Pico Boards. These boards contain two separate antennas for the TX and RX paths. This type of Pico Board is best suited for demonstrating the best possible conducted output power and sensitivity of the EZRadioPRO™ RF ICs. For this purpose, the layouts of the TX and RX paths are separated and isolated as much as possible to minimize the coupling effects between them. This type of Pico Board is recommended for laboratory use and not for range tests since the presence of two closely-spaced antennas may cause “shadowing” when receiving a radiated signal.

The main layout design concepts are reviewed through this layout to demonstrate the basic principles. However, for an actual application, the layouts of the Pico Boards with single antenna (or with antenna diversity) should be used as references.

In this section, a four-layer design (based on the layout of the 4463-PCE20B915 Pico Boards) and a two-layer design (based on the layout of the 4438-PCE20B490 Pico Boards) are shown.

The layout design recommendations for the TX only and RX only Pico Boards are also fully covered in this section without directly touch these cases.

The schematic of the CLE Split TX/RX type matching network for the Si446x RevB1 is shown in Figure 2.

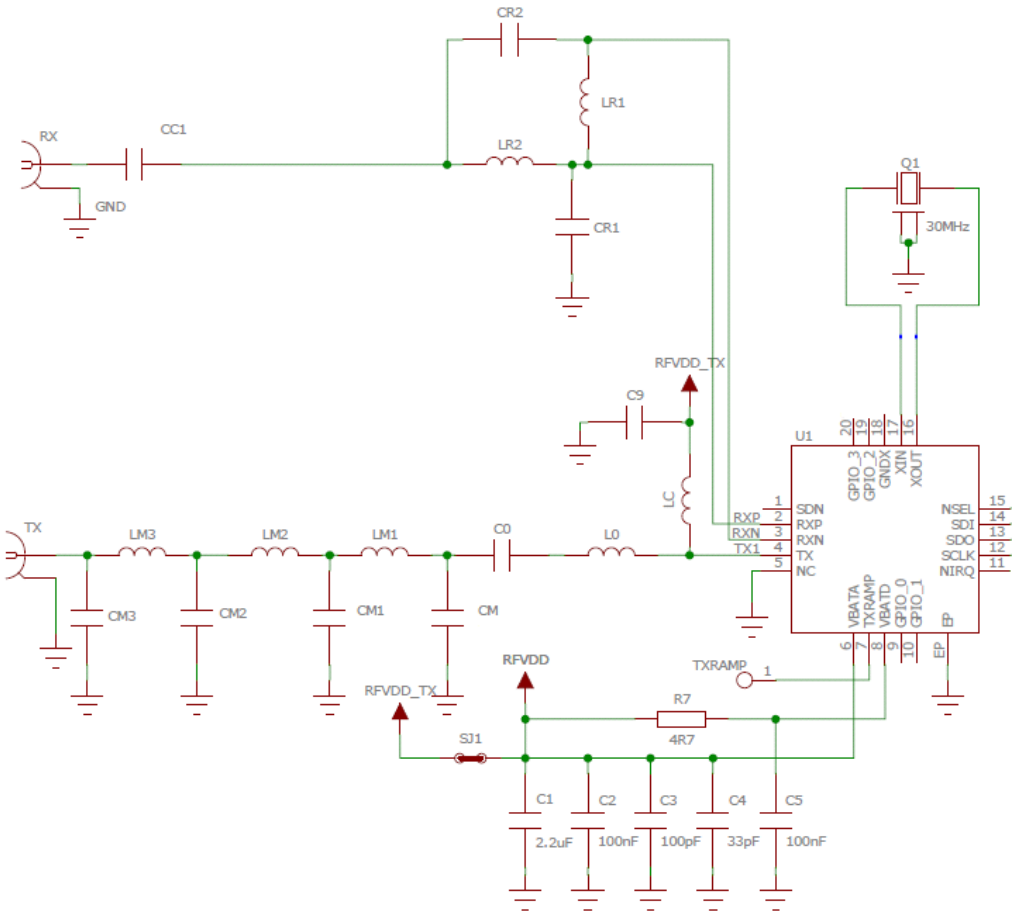


Figure 2. Schematic of the CLE Split TX/RX Type Matching Network for the Si446x RevB1*

***Note:** Component values should be chosen based on frequency band.

The layout structure of the CLE Split TX/RX type matching network is shown in Figure 3.

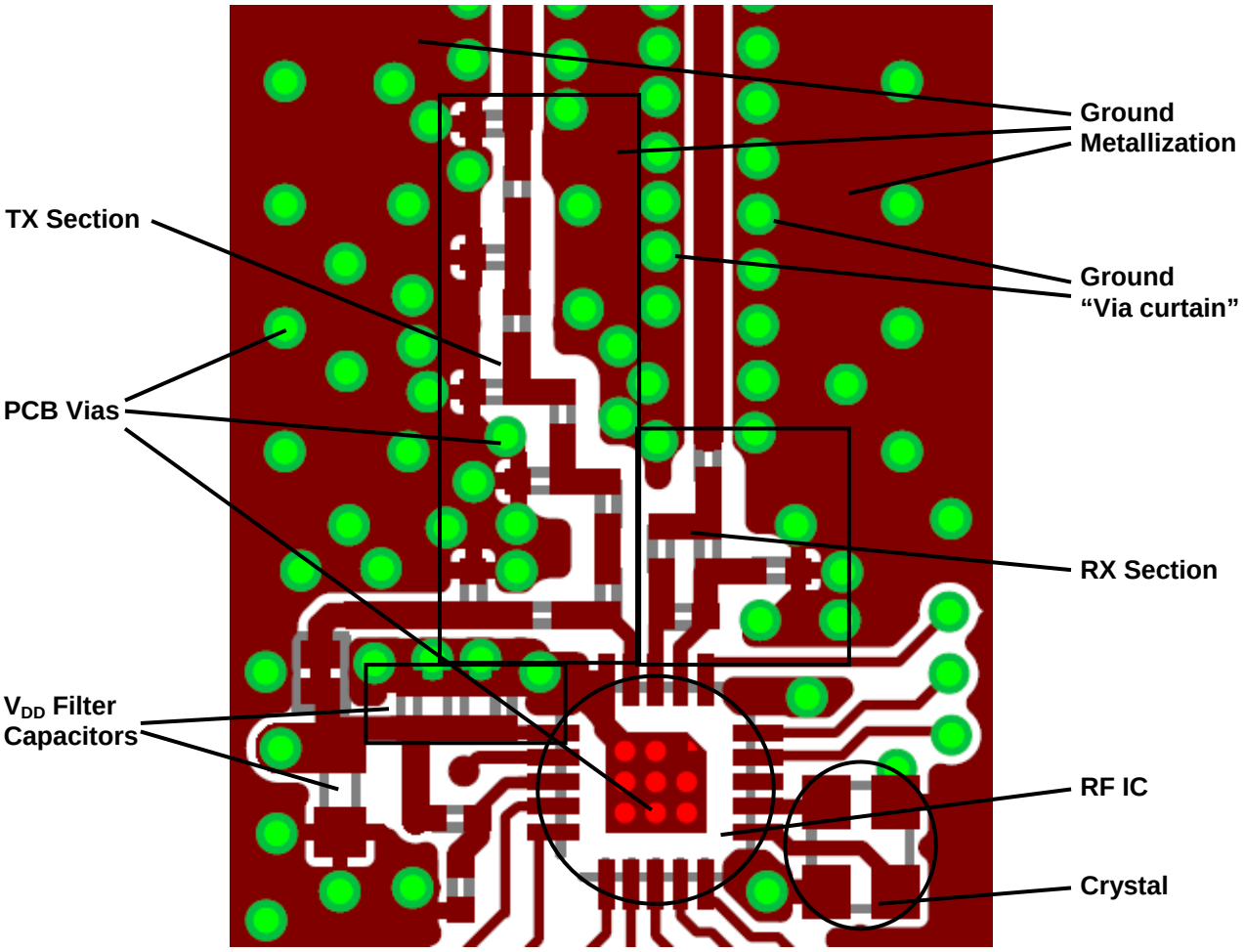


Figure 3. Schematic of the CLE Split TX/RX Type Matching Network for the Si446x RevB1

3.1.1. Layout Design Guidelines

- The L0 inductor should be placed as close to the TX pin of the RF IC as possible (even if this means the RX is further away) in order to reduce the series parasitic inductance which increase the voltage peak at the internal drain pin.
- The TX and RX sections should be separated as much as possible on the top layer to reduce coupling. If the available space allows, flow the GND metal between them and use many vias.
- The neighboring matching network components should be placed as close to each other as possible in order to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Improve the grounding effect in the thermal straps used with capacitors. In addition, thicken the trace near the GND pin of these capacitors. This will minimize series parasitic inductance between the ground pour and the GND pins. Additional vias placed close to the GND pin of capacitors (thus connecting it to the bottom layer GND plane) will further help reduce these effects.

Figure 4 demonstrates the positioning and orientation of the LC and LR components, the separating GND metal between the TX and RX sections, and thermal strapping on the shunt capacitors on the 4463-PCE20B915 Pico Boards.

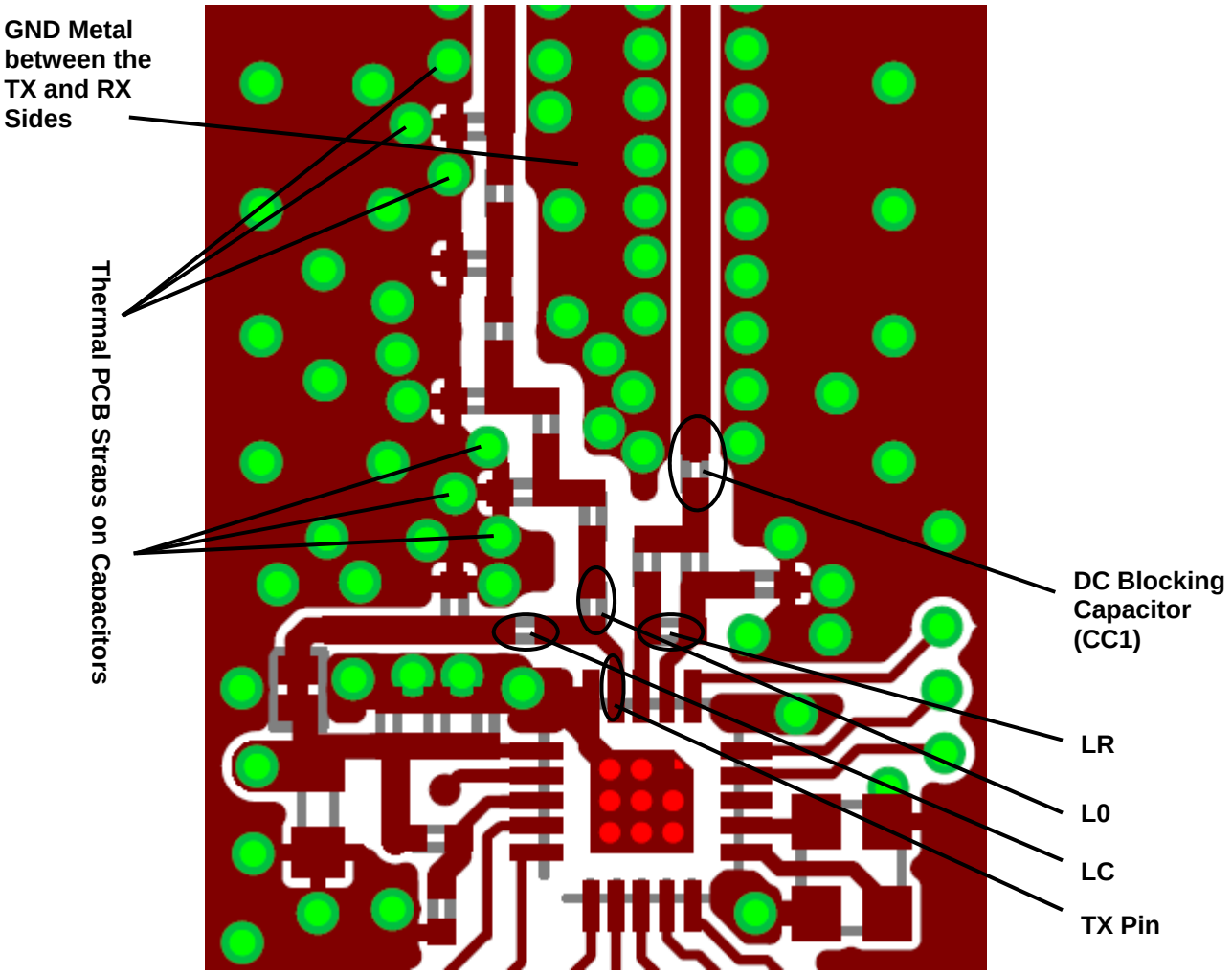


Figure 4. Component Orientation, Placement, and GND Metalization

- The smaller V_{DD} bypass capacitors (C1 and C2) should be kept as close to the V_{DD} pin as possible.
- The exposed pad footprint for the paddle of the RF IC should use as many vias as possible to ensure good grounding and heat sink capability. In the reference designs there are 9 vias, each with 12 mil diameter. The paddle ground should also be connected to the top layer GND metal, if possible, to further improve RF grounding; this may be accomplished with diagonal trace connections through the corners of the RFIC footprint.
- The crystal should be placed as close to the RFIC as possible to ensure that wire parasitic capacitances are kept as low as possible; this will reduce any frequency offsets.
- Use at least 0.5 mm separation between traces/pads to the adjacent GND pour in the areas of the matching networks. This will minimize the parasitic capacitance and reduce the detuning effects.
- If space allows, the nearby inductors of the TX path should be kept perpendicular to each other to reduce coupling between stages of the low pass-filter and match. This will help to improve filter attenuation at higher harmonic frequencies.
- If space allows, the parallel inductor in the RX path (LR) should be perpendicular to the nearby inductors in the TX path as this will reduce TX-to-RX coupling.

Figure 5 demonstrates the grounding of the RFIC, the crystal and V_{DD} filter capacitor positions, and the isolating ground metal between the V_{DD} trace and the crystal on the 4463-PCE20B915 Pico Boards.

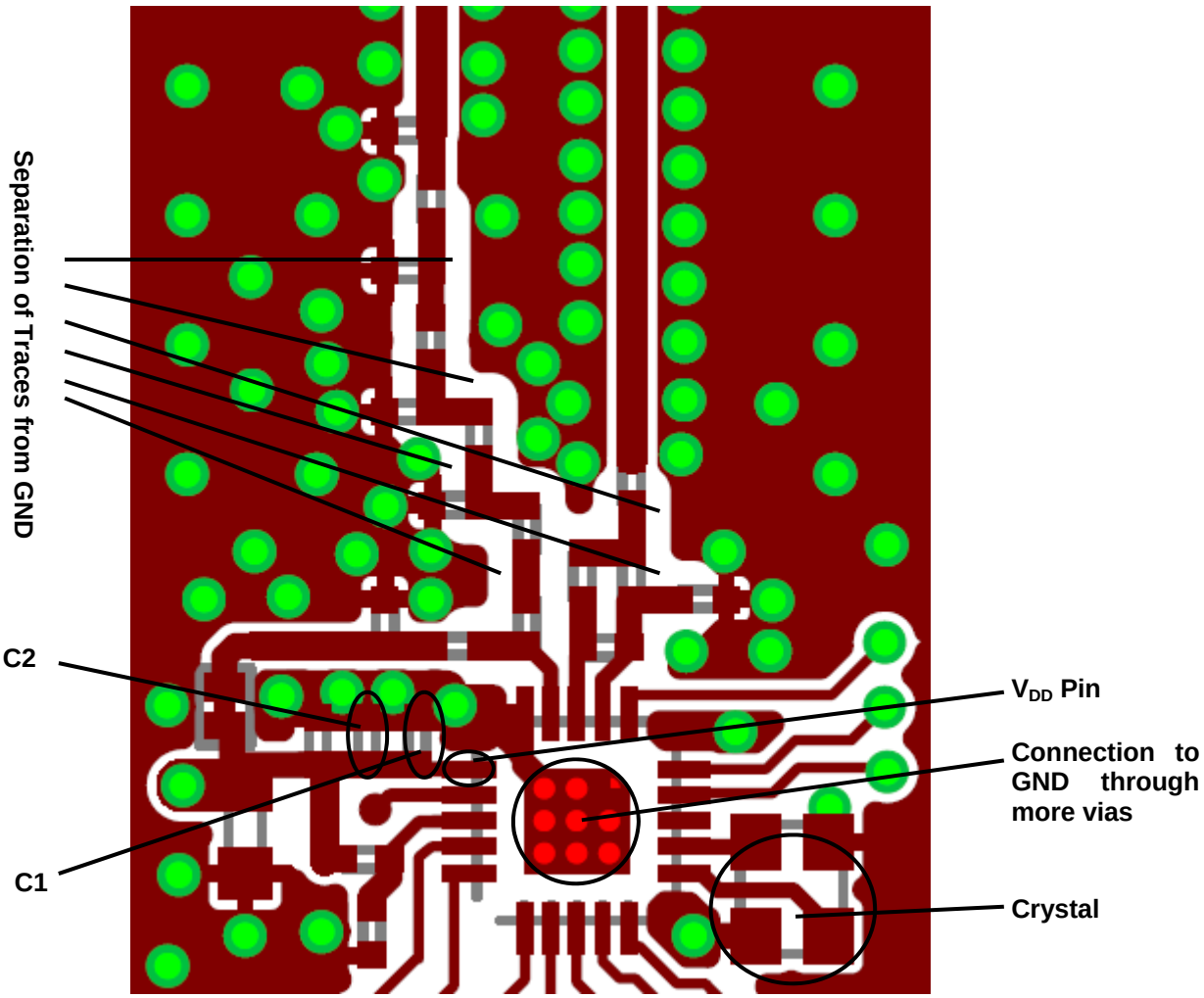


Figure 5. RFIC GND Vias and GND Metalization

- To achieve good RF ground on the layout, it is recommended to add large, continuous GND metalization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VDD filtering and also provides a good ground plane for a monopole antenna. Gaps should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible.
- The area under the matching network (on the bottom layer) should be filled with ground metal as it will help reduce/remove radiation emissions. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the TX LPF/Match and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear unhindered pathway through the GND plane to the back of the RFIC.
- Use as many parallel grounding vias at the GND metal edges (especially at the edge of the PCB and along the Vdd trace) as possible in order to reduce their harmonic radiation caused by the fringing field.
- If necessary shielding cap can be used to shield the harmonic radiations of the PCB; in that case, the shielding cap should cover all of the RF-related components. The shielding cap is usually required for the +20 dBm 915 MHz Si4463 designs due to the strict harmonic radiation limits of the FCC.

Figures 6 and 7 demonstrate the GND metal filled sections in a two-layer design on the entire 4438-PCE20B490 Pico Board PCB. The top and bottom layers are shown, respectively.

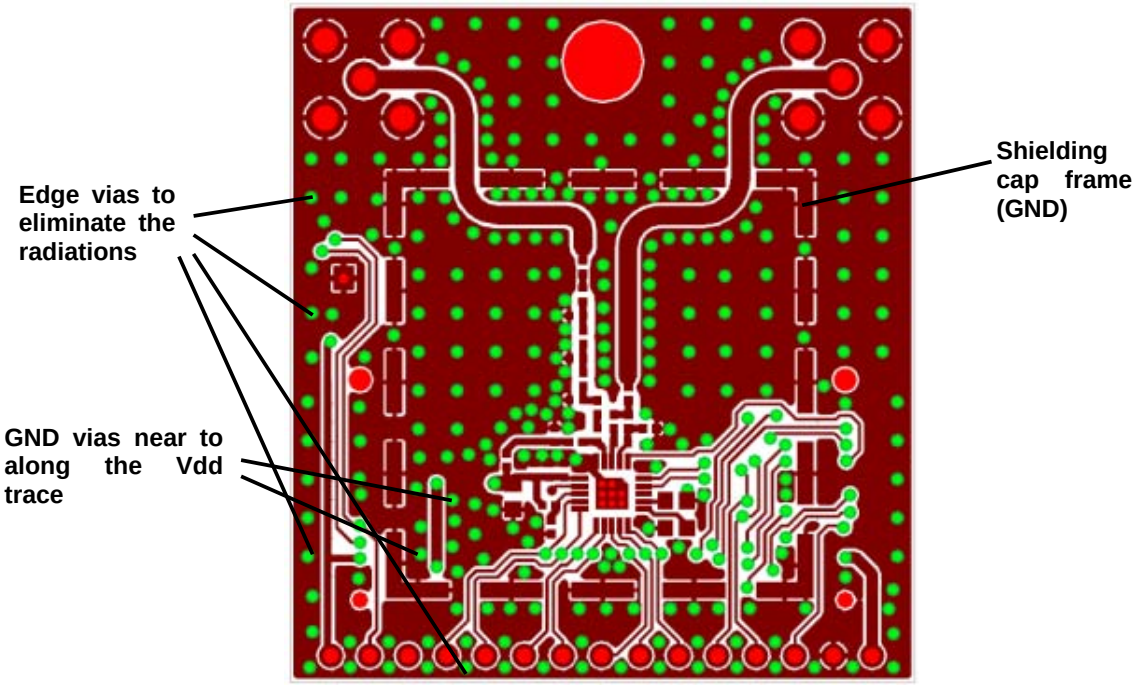


Figure 6. Ground Poured Sections with PCB Vias around the Matching Network (Top Layer)

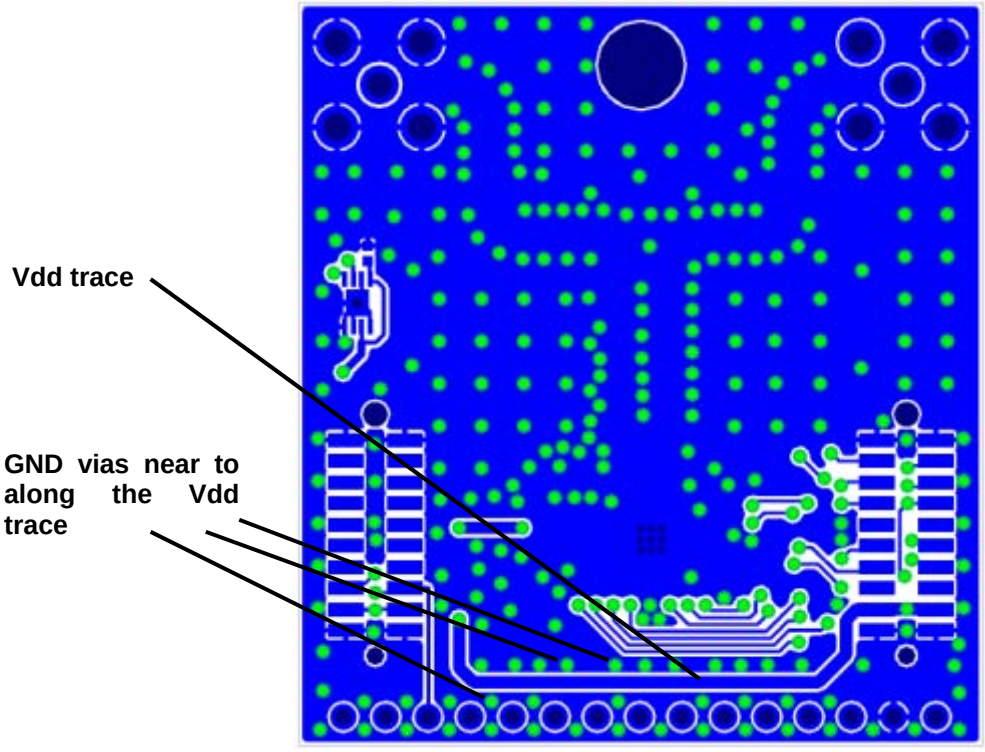


Figure 7. Ground Poured Sections with PCB Vias (Bottom Layer)

Use 50 Ω grounded coplanar lines where possible for connecting the SMA connector(s) to the matching network and/or the RF switch to reduce sensitivity to PCB thickness variation. This will also reduce radiation and coupling effects. The interconnections between the elements are not considered as transmission lines since their lengths are much lower than the wavelength and thus their impedance is not critical. As a result, their recommended width is the smallest possible (i.e. equal to the width of the pad of the applied components). In this way, the parasitic capacitances to the ground can be minimized. In the case of the 4438-PCE20B490 type Pico Board, the only route where 50 Ω coplanar transmission line is used is between the output of the matching networks and the SMA connectors. Examples for the trace dimensions are shown in Table 1.

Use many vias near the coplanar lines in order to reduce as much radiation as possible.

Figure 8 demonstrates the 50 Ω grounded coplanar line of the TX side on the 4438-PCE20B490 Pico Boards.

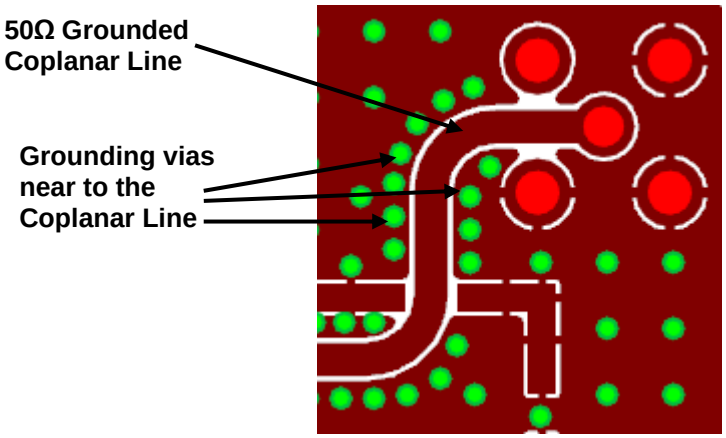


Figure 8. 50 Ω Grounded Coplanar Line on 1.5 mm Thick Substrate

Table 1. Parameters for 50 Ω Grounded Coplanar Lines

f	119−960 MHz	
T	0.018−0.035 mm	
Er	4.6	
H	1.5 mm	0.26 mm*
G	0.25 mm	0.64 mm
W	1.26 mm	0.45 mm
***Note:** In case of the 4 layer PCBs, the thickness between the top and the next inner layer should be taken into account.		

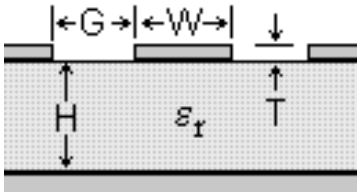


Figure 9. Grounded Coplanar Line Parameters

To achieve better suppression of harmonic radiation, a four-layer design can be applied.

- In a four-layer design, all of the wires/traces should be placed in one of the inner layers, and the whole top and bottom layers should contain as much continuous GND metalization as possible.
- In a four-layer design, the optimal width of the coplanar line will be changed, see Table 1.

Figures 10, 11, 12 and 13 demonstrate the GND metal-filled sections in a four-layer design on the entire 4463-PCE20B915 Pico Board PCB. The top, inner 2, inner 3, and bottom layers are shown, respectively.

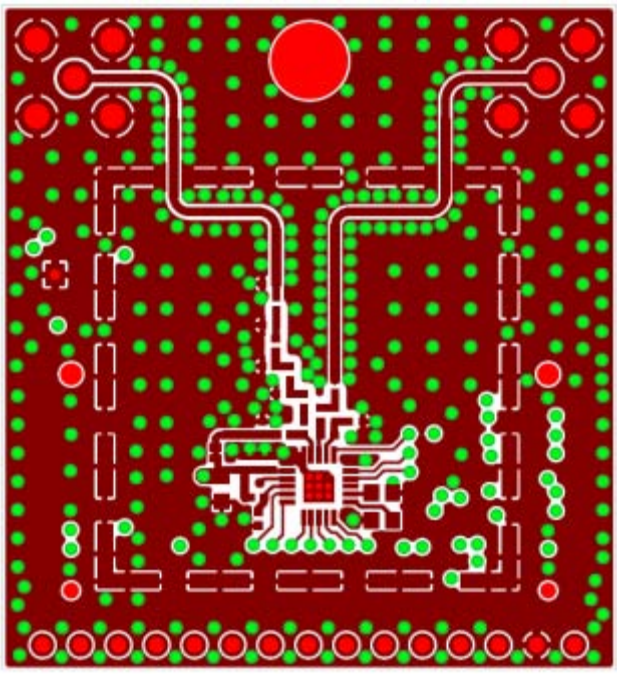


Figure 10. Ground Poured Sections with PCB Vias around the Matching Network (Top Layer)

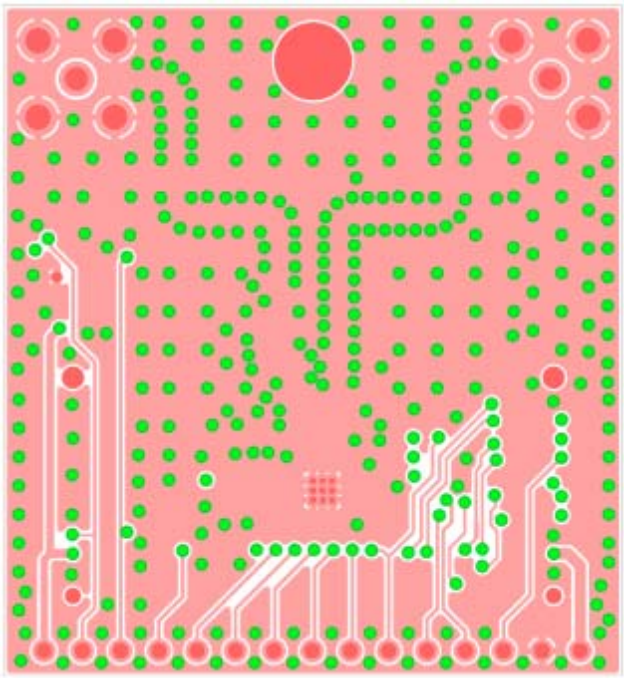


Figure 11. Ground Poured Sections with PCB Vias (Inner2 Layer)

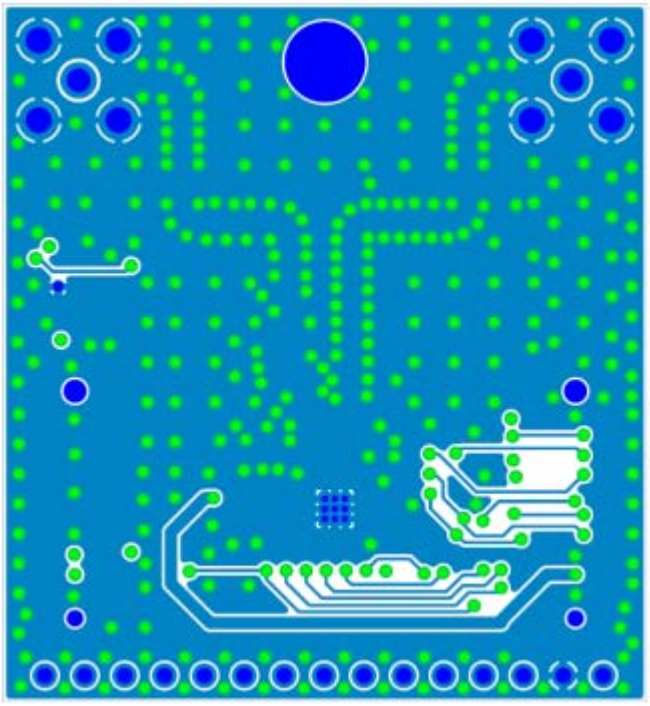


Figure 12. Ground Poured Sections with PCB Vias (Inner3 Layer)

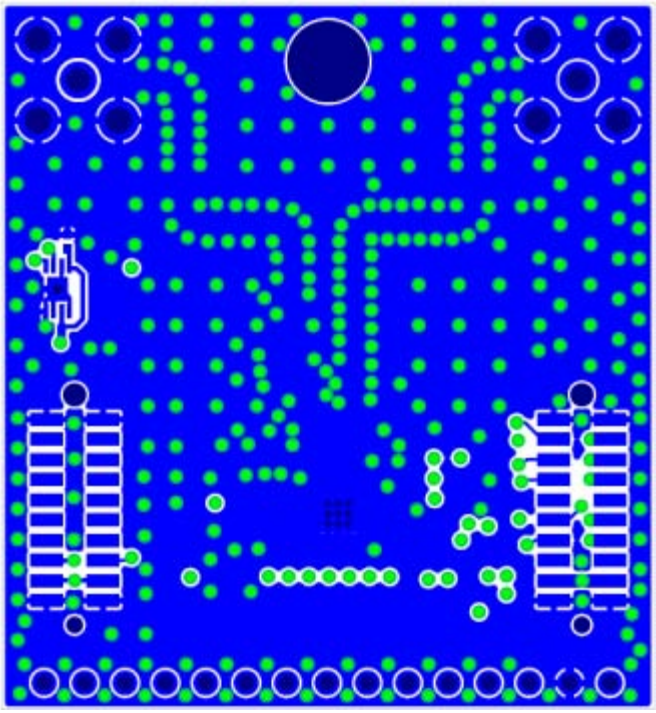


Figure 13. Ground Poured Sections with PCB Vias (Bottom Layer)

3.2. Class E Direct Tie Type Matching Network Layout Based on the 4460-PCE10D434 Pico Board (Single Antenna without RF Switch)

For reference, layout examples shown in this section are based on the layout of the 4460-PCE10D434 RF Pico Boards. These boards contain one antenna, and the TX and RX paths are connected directly together, without the use of an RF switch.

The schematic of the CLE Direct Tie type matching network for the Si446x RevB1 is shown in Figure 14.

During TX mode operation the built-in LNA protection circuit turns on (see “AN627: Si4460/61 Low-Power PA Matching” for more details). In this case, the dc path from the output of the matching network to the GND is not blocked through the RX side, so a dc blocking capacitor (CC1) is necessary.

In case of the Direct Tie type matching, the coupling between the RX and TX sides is not critical since no harmonic leakage through the coupled RX path occurs because both of them are filtered after the common connection point.

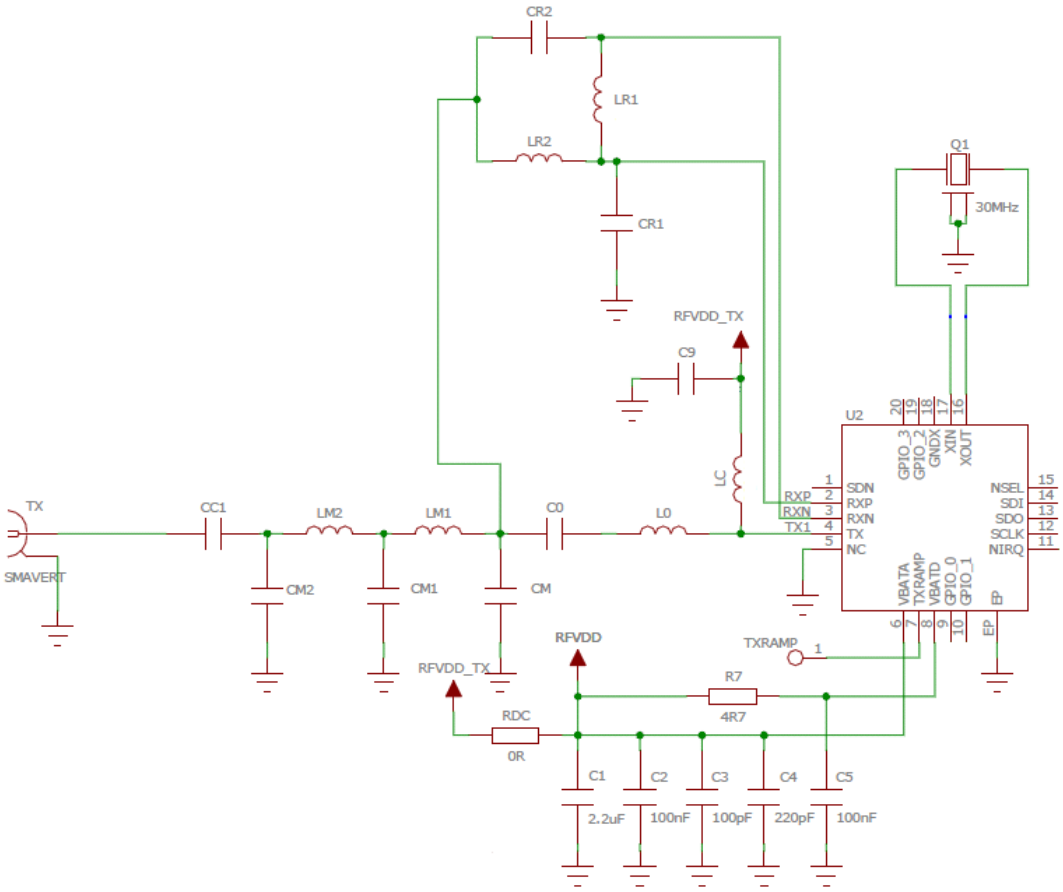


Figure 14. Schematic of the CLE Direct Tie Type Matching Network for the Si446x RevB1*

***Note:** Component values should be chosen based on frequency band.

3.2.1. Layout Design Guidelines

The principles in this case are the same as in the case of the Class-E Split TX/RX type matching, except for the following issues:

- The trace parasitics are critical in case of the connection of LR2, so the shortest traces possible should be used for connecting LR2 to the TX side.
- Since the RX-TX coupling is not critical, there is no separating GND metal between the two sides.

Figure 15 demonstrates the positioning and orientation of components and ground pour flooding on the 4460-PCE10D434 RF Pico Boards.

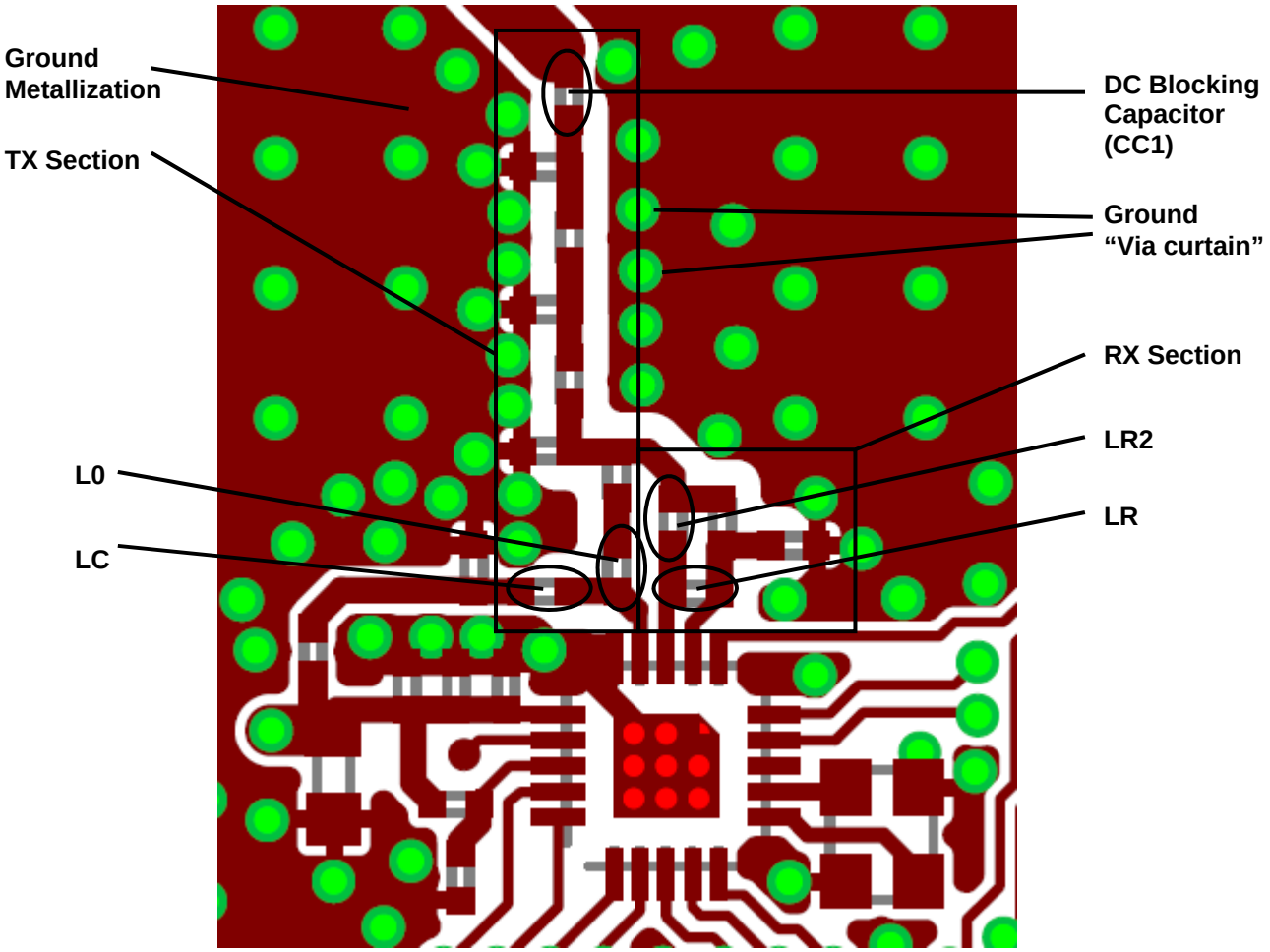


Figure 15. Layout of the Si446x RevB1 CLE Direct Tie Type Matching; Component Orientation, Placement and GND Metalization

3.3. Class E Switched Type Matching Network Layout Based on the 4463-PCE20C915 Pico Board (Single Antenna with RF Switch)

For reference, examples shown in this section are based on the layout of the 4463-PCE20C915 RF Pico Boards. These boards contain a single antenna and an RF switch to select between the TX and RX paths. The schematic of the Switch type matching network for the Si446x RevB1 is shown in Figure 16.

The unavoidable nonlinearity of the RF switch will itself generate some harmonic energy as the desired signal frequency passes through it. It is recommended to place some of the low-pass filter circuitry after the RF switch to attenuate these additional harmonic components. Thus, the matching topology for the Single Antenna with RF Switch board configuration is comprised of two small low-pass filter sections with the RF switch embedded between them.

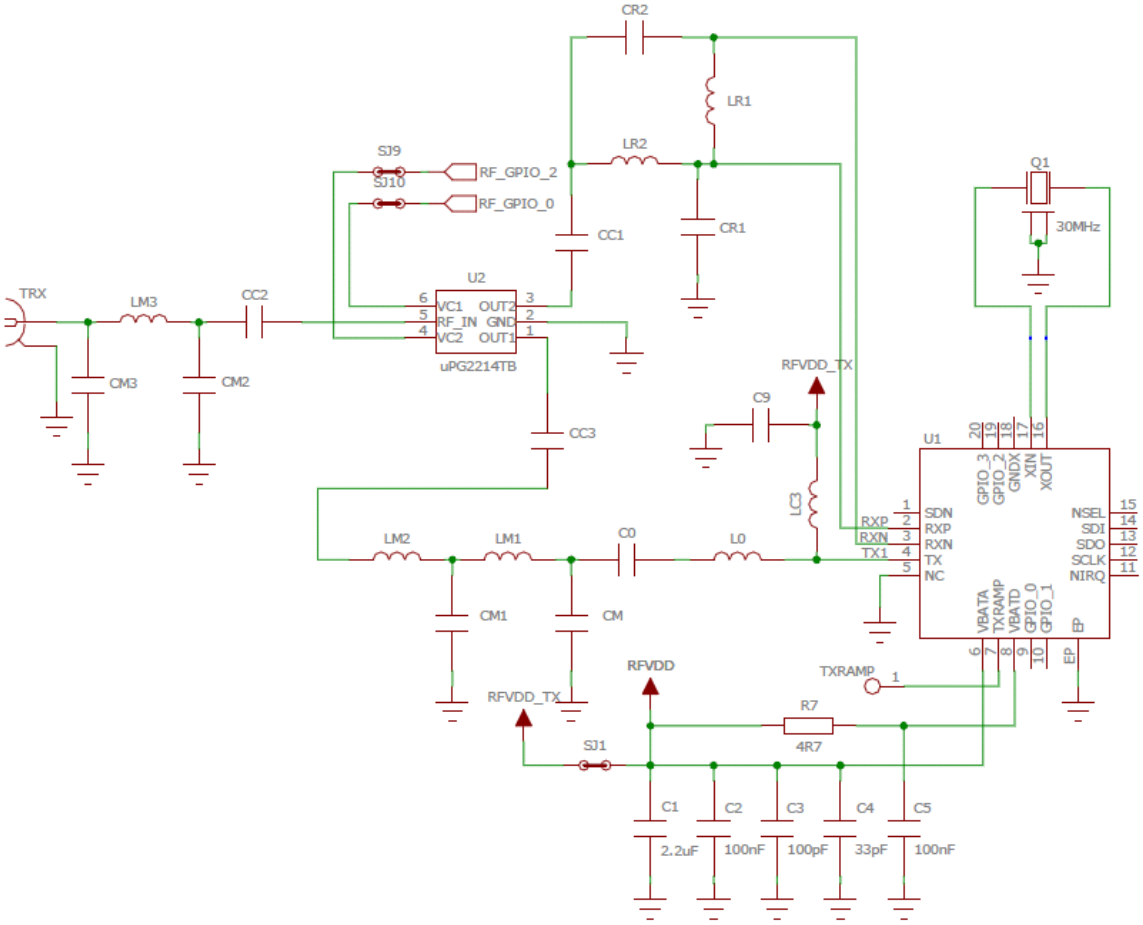


Figure 16. Schematic of the CLE Switch TX/RX type matching network for the Si446x RevB1*

***Note:** Component values should be chosen based on frequency band.

3.3.1. Layout Design Guidelines

- When using a TX/RX switch or a switch to select antennas in an antenna diversity implementation, a series capacitor may be required on all ports (e.g., TX, RX, Antenna) of the switch to block the dc patch between the switch and the ground. Refer to the exact requirements and specifications of the switch used in the application.
- RF switches may themselves behave in a slightly nonlinear fashion, resulting in some regeneration of harmonic energy, regardless of the cleanliness of the input signal to the switch. Thus, it may be necessary to move a portion of the TX low-pass filter to after the RF switch (i.e., just prior to the antenna) in order to further attenuate these regenerated harmonic signals.
- If the RX side matching network is relatively far from the RF switch, then the connecting trace should be a 50 Ω grounded coplanar line.
- The area between the RX and TX sides should be filled with GND metal to increase the isolation (just as in case of the Split type design).

Figure 17 demonstrates the positioning and orientation of components, ground flooding, and thermal strapping on the 4463-PCE20C915 RF Pico Board.

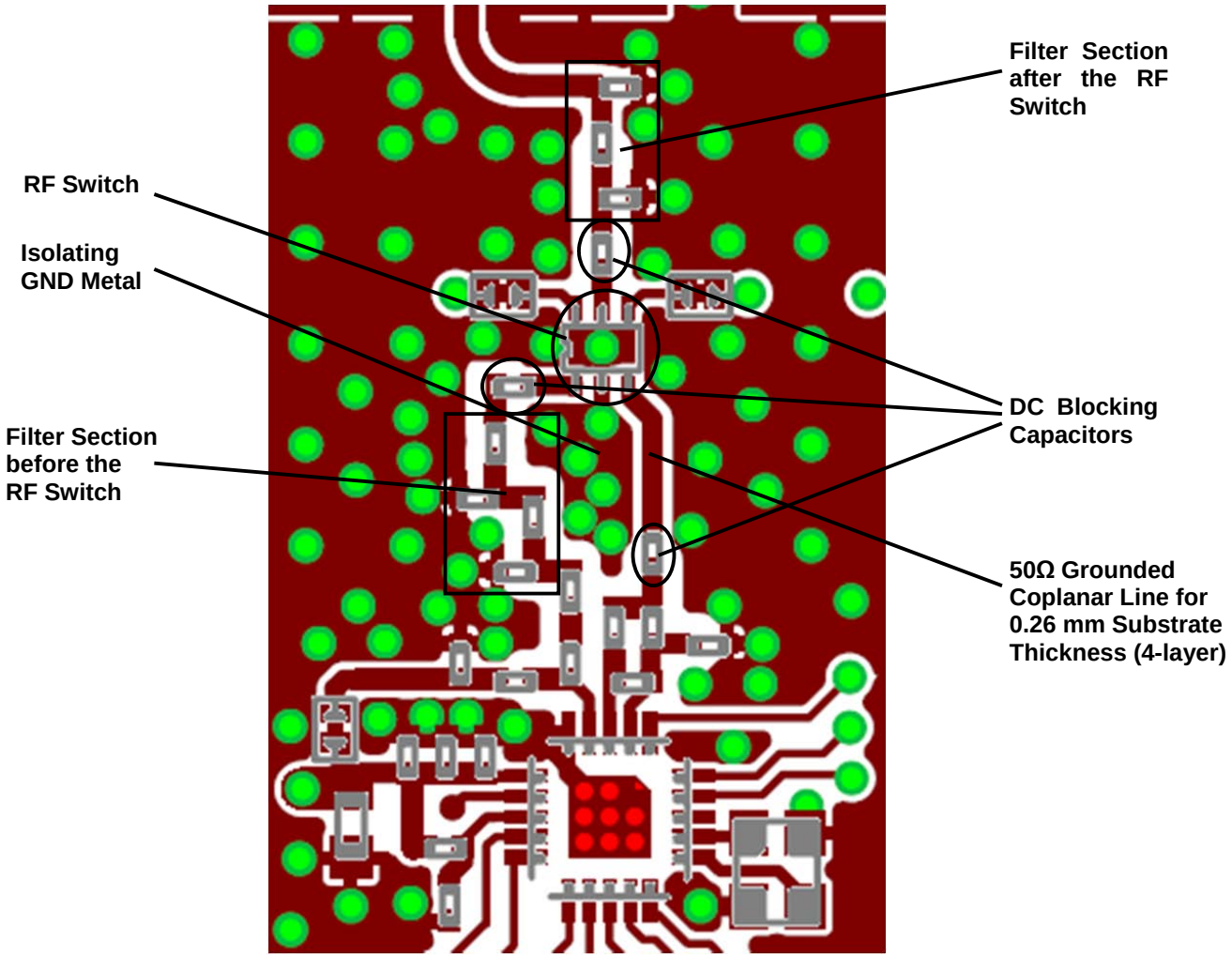


Figure 17. Layout of the Si446x RevB1 CLE Switch Type Matching; Component Orientation, Placement and GND Metalization

3.4. Square-Wave Direct Tie Type Matching Network Layout Based on the 4463-PSQ20D169 Pico Board (Single Antenna without RF Switch)

For reference, layout examples shown in this section are based on the layout of the 4463-PSQ20D169 RF Pico Boards. These boards contain one antenna, and the TX and RX paths are connected directly together without the use of an RF switch.

The schematic of the SQW Direct Tie type matching network for the Si446x RevB1 is shown in Figure 18.

During TX mode operation, the built-in LNA protection circuit turns on (see “AN648: Si4463/64 TX Matching” for more details). In this case, the dc path from the output of the matching network to the GND is not blocked through the RX side, so a dc blocking capacitor (CC1) is necessary.

In the case of Direct Tie type matching, the coupling between the RX and TX sides is not critical since no harmonic leakage through the coupled RX path occurs since both of them are filtered after the common connection point.

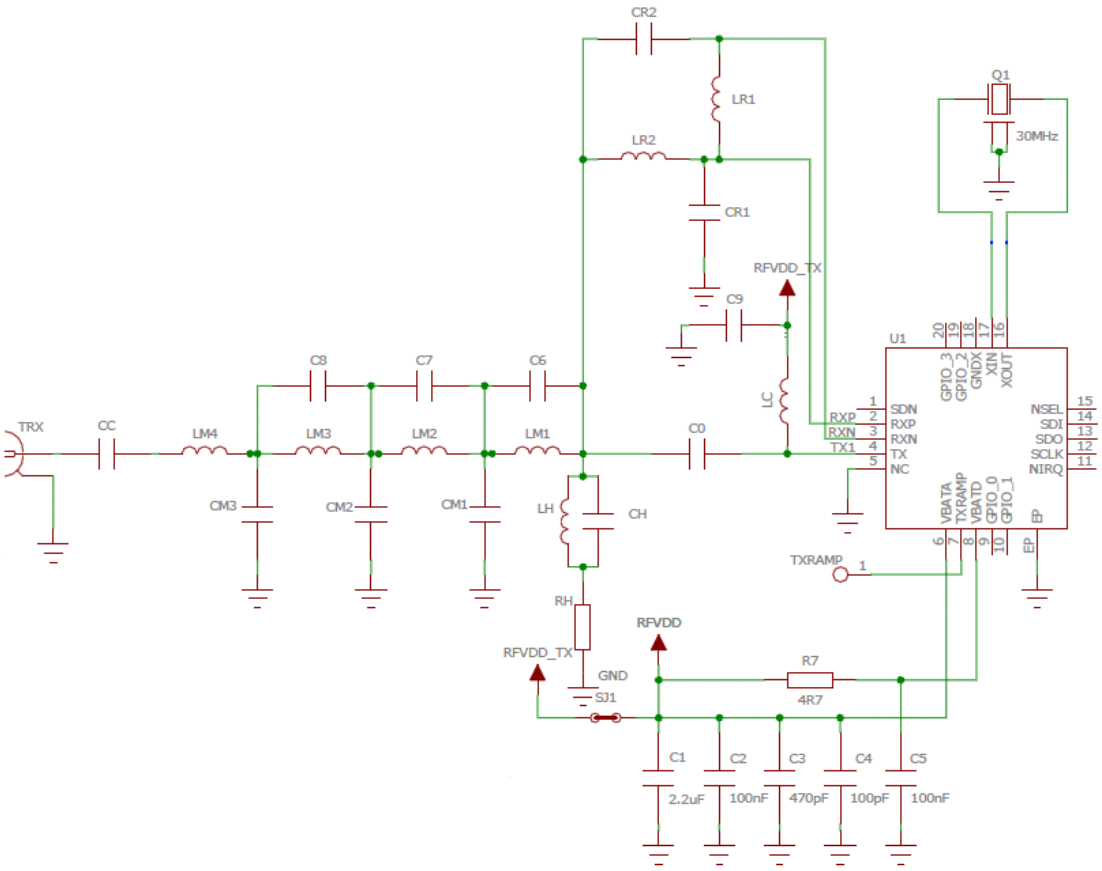


Figure 18. Schematic of the Square-Wave Direct Tie Type Matching Network for the Si446x RevB1*

***Note:** Component values should be chosen based on frequency band.

3.4.1. Layout Design Guidelines

Figure 19 demonstrates the positioning and orientation of components and ground pour flooding on the 4463-PSQ20D169 RF Pico Board.

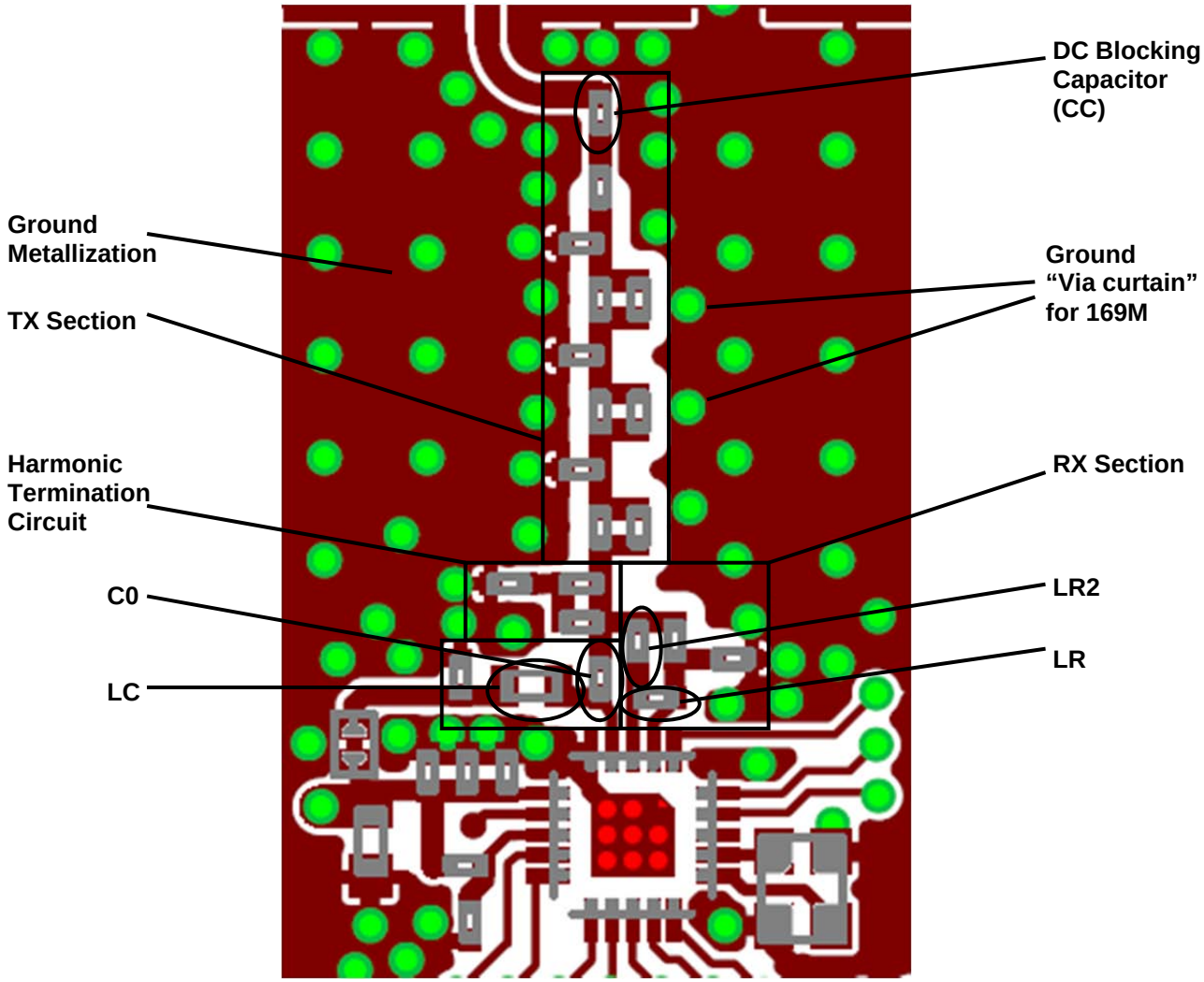


Figure 19. Layout of the Si446x RevB1 SQW Direct Tie Type Matching; Component Orientation, Placement and GND Metalization

3.5. Further Design Recommendations when using additional RF components

In this section, cases with additional components used in their designs, such as FET, FEM, SAW filter, TCXO, and LDO, are described. In general, the extra components' data sheet includes the special layout design recommendations what should be taken into consideration in the layout design.

3.5.1. Layout Design Recommendations when Using external FEM and LDO

For reference, layout examples shown in this section are based on the layout of the 4463-PCE30E915R RF Pico Boards. These boards contain a single antenna, and the TX and RX paths are connected to the external FEM. The external FEM will itself generate some harmonic energy as the desired signal frequency passes through it. It is recommended to place some of the low-pass filter circuitry after the FEM to attenuate these additional harmonic components. Thus, the matching topology for the Single Antenna with FEM board configuration is comprised of two small low-pass filter sections with the FEM embedded between them.

The schematic of the 4463-PCE30E915R RF Pico Boards' matching network is shown in Figure 20.

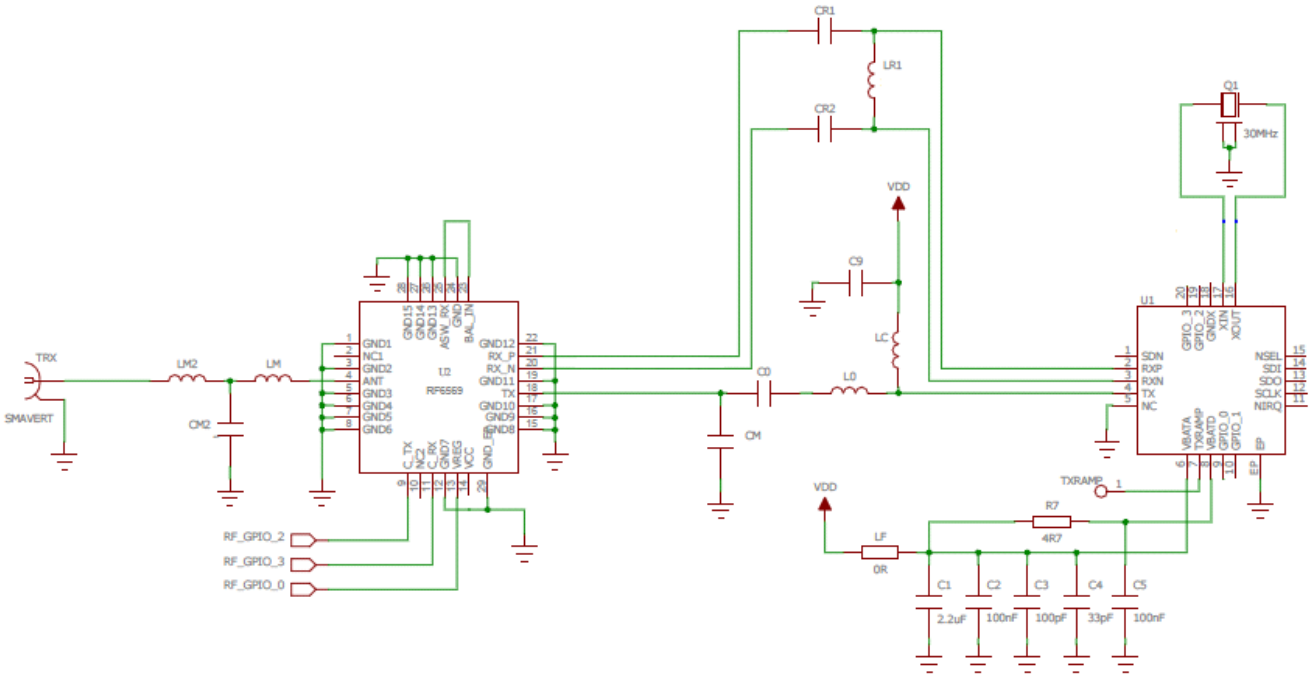


Figure 20. Schematic of the 4463-PCE30E915R RF Pico Boards' Matching Network

The element values of the matching circuit depend on the FEM (see in its data sheet) and on the RFIC as well. If the FEM is matched to 50 Ω, the matching networks found in AN627 or AN648 can be used. The component values should be chosen based on frequency band.

3.5.1.1. Layout Design Guidelines

- FEMs may themselves behave in a nonlinear fashion, resulting in some regeneration of harmonic energy regardless of the cleanliness of the input signal to the FEM. Thus, it may be necessary to move a portion of the TX low-pass filter to after the FEM (i.e., just prior to the antenna) in order to further attenuate these re-generated harmonic signals, but refer to the exact requirements and specifications of the FEM used in the application.
- Due to the higher current consumption, the Vdd trace should be widened compared to cases in which FEM does not appear.
- Place the Vdd trace on an inner layer if possible and avoid putting it close to the edge of the PCB in order to eliminate the possibilities of its harmonic radiation.
- Ensure the best possible RF ground for the FEM.
- If an RF shielding cap is also used, it is recommended to shield all of the RF-related components, including the LDO, in order to eliminate as much of the Vdd trace radiation as possible.
- In a 4 (or more)-layer design, all of the wires/traces should be placed in one of the inner layers, and the entire top and bottom layers should contain as large and continuous GND metalization as possible in order to reduce the traces' radiations.

Figures 21, 22, 23, and 24 demonstrate the positioning and orientation of components, the Vdd trace, and ground pour flooding in a four-layer design on the entire 4463-PCE30E915R RF Pico Board. The top, inner 2, inner 3, and bottom layers are shown, respectively.

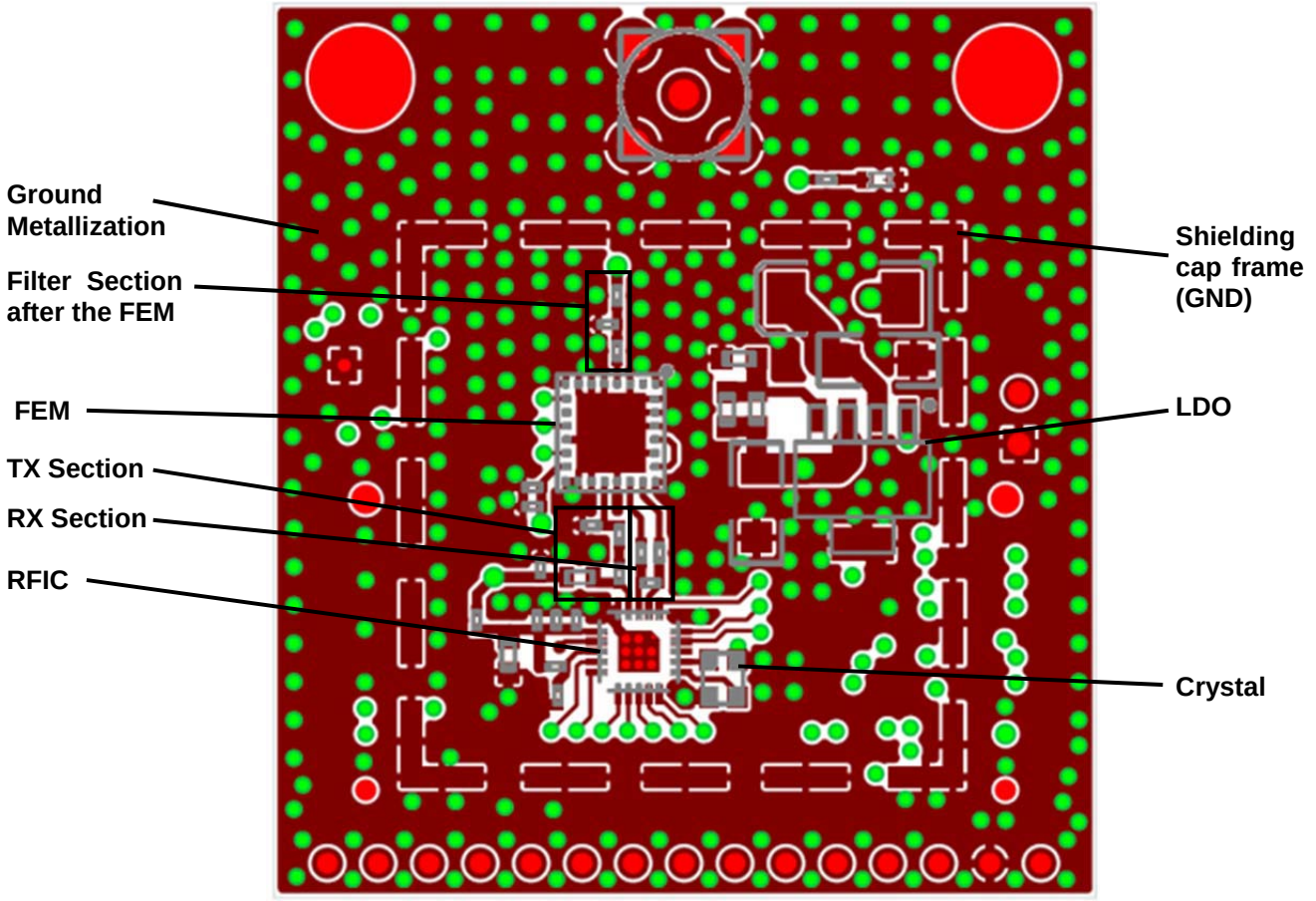


Figure 21. 4463-PCE30E915R RF Pico Board (Top Layer)

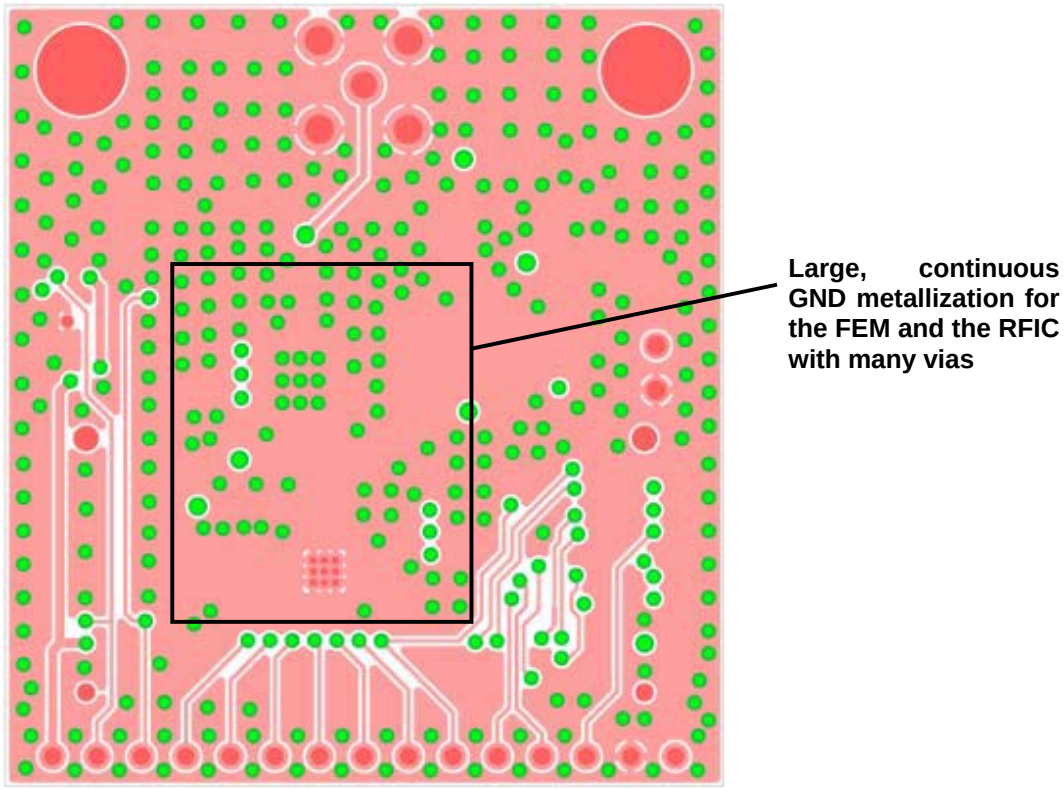


Figure 22. 4463-PCE30E915R RF Pico Board (Inner2 Layer)

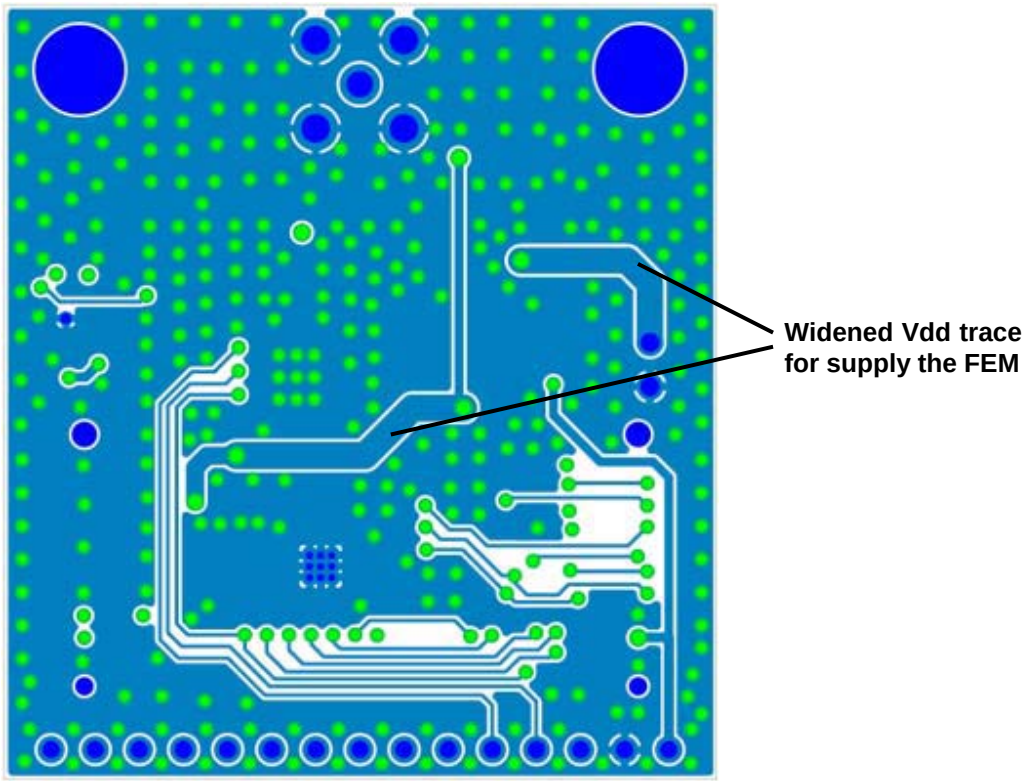


Figure 23. 4463-PCE30E915R RF Pico Board (Inner3 Layer)

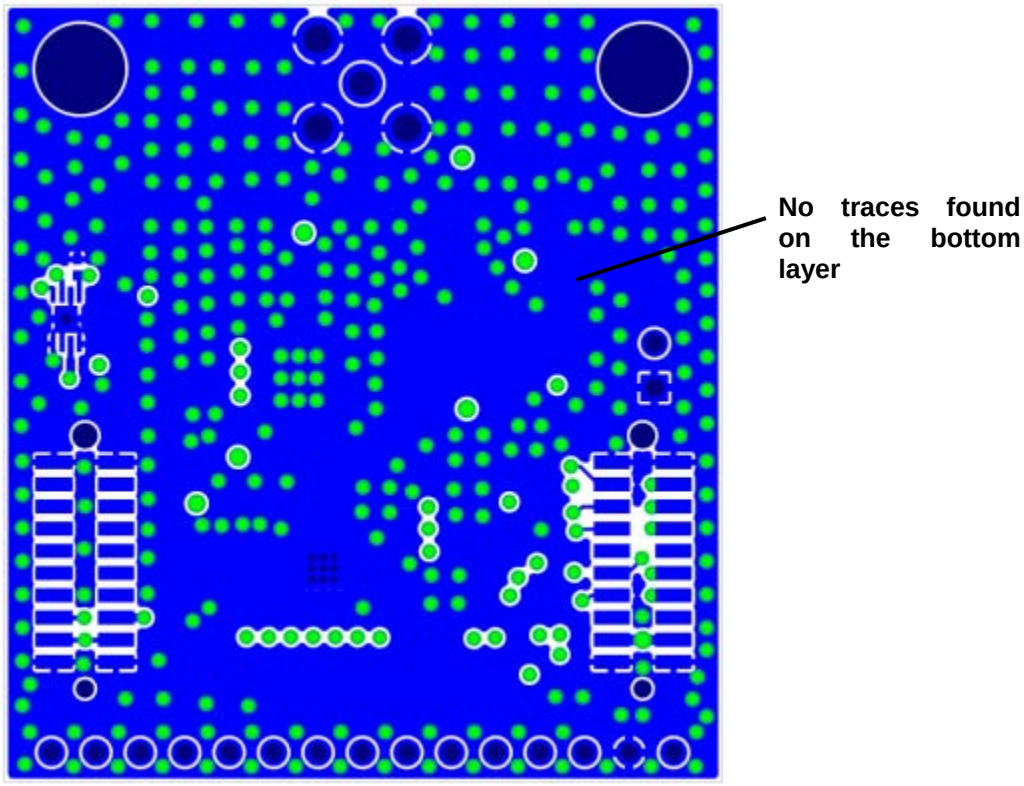


Figure 24. 4463-PCE30E915R RF Pico Board (Bottom Layer)

3.5.2. Layout Design Recommendations when Using SAW filter and TCXO

For reference, layout examples shown in this section are based on the layout of the 4463-PCE20C868SE RF Pico Boards. These boards contain one single antenna and an RF switch to select between the TX and RX paths. In this design, a TCXO is used instead of a standard crystal, and, in the RX path, a SAW filter is also applied. The schematic of the 4463-PCE20C868SE RF Pico Boards' matching network is shown in Figure 25.

The RF switch will itself generate some harmonic energy as the desired signal frequency passes through it. It is recommended to place some of the low-pass filter circuitry after the RF switch to attenuate these additional harmonic components. Thus, the matching topology for the Single Antenna with RF Switch board configuration is comprised of two small low-pass filter sections with the RF switch embedded between them.

In most cases, it is also necessary to put a two-element matching network at the input and at the output of the SAW filter in order to match the SAW filter to 50 Ω. These required matching element values are found in the data sheet of the SAW filter used.

In general, the TCXOs need some filtering capacitors (details are found in the TCXO's data sheet), and, *in the high output power cases* (+20 dBm or higher), it is recommended to use additional filtering sections in order to achieve larger suppression at the reference spurs. These additional filter sections contain a grounding capacitor to the XOUT (RFIC pin 16) and an RC filter from the TCXO output to the input of XIN (RFIC pin 17). It only makes sense when the goal is to comply with the ETSI Category 1 EMC regulation within acceptable margins. The component values should be chosen based on frequency band.

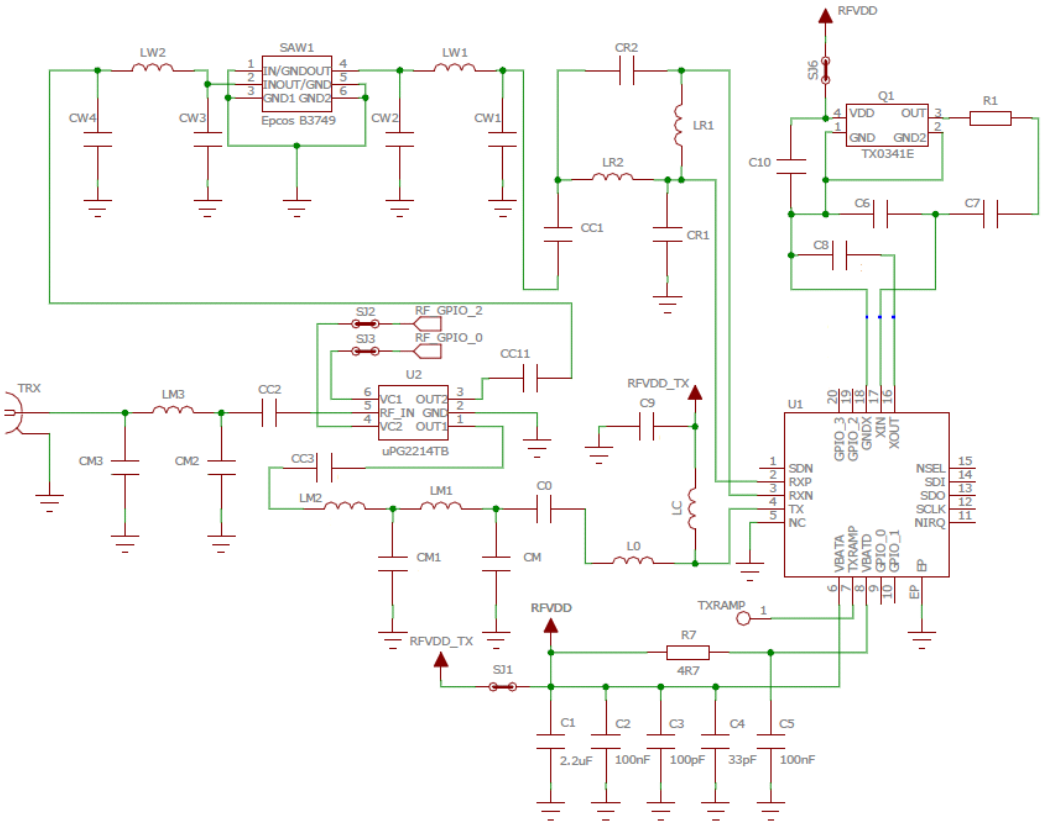


Figure 25. Schematic of the 4463-PCE20C868SE RF Pico Board Matching Network

3.5.2.1. Layout Design Guidelines

The principles in this case are the same as those of the Class-E Switched Type matching with the following additional issues:

- **Regarding the SAW filter** to achieve good ultimate rejection, a low crosstalk is necessary. For that, the coupling through the grounding (i.e. the so called “grounding loops”) should be minimized between the input and the output of the SAW filter; that is why it is NOT recommended to connect the GND pins of the SAW filter directly to each other on the same layer. Details are found in the data sheet of the SAW filter being used.
- In 4 (or more)-layer designs, where the distance between the layers is lower than 0.7 mm, it is also recommended to keep out the GND metalization on the next layer under the area of the SAW filter in order to minimize the grounding loops between the input and the output of the SAW filter.
- **Regarding the TCXO** to achieve better suppression (only in high-output power cases) at the reference spurs, the above mentioned filtering sections should be added to the design.
- It is recommended to separate the TCXO’s ground from the entire ground plane of the PCB and connect it to GNDX (pin 18 of the RFIC) in order to increase the suppression at the reference spurs as well.
- All of the TCXO's filtering capacitors should be connected to the GNDX in order to increase suppression at the reference spurs as well.

Figures 26, 27, 28, and 29 demonstrate the positioning and orientation of components, the ground pour flooding, the TCXO’s and SAW’s layout in a four-layer design on the entire 4463-PCE20C868SE RF Pico Board. The top, inner 2, inner 3, and bottom layers are shown, respectively.

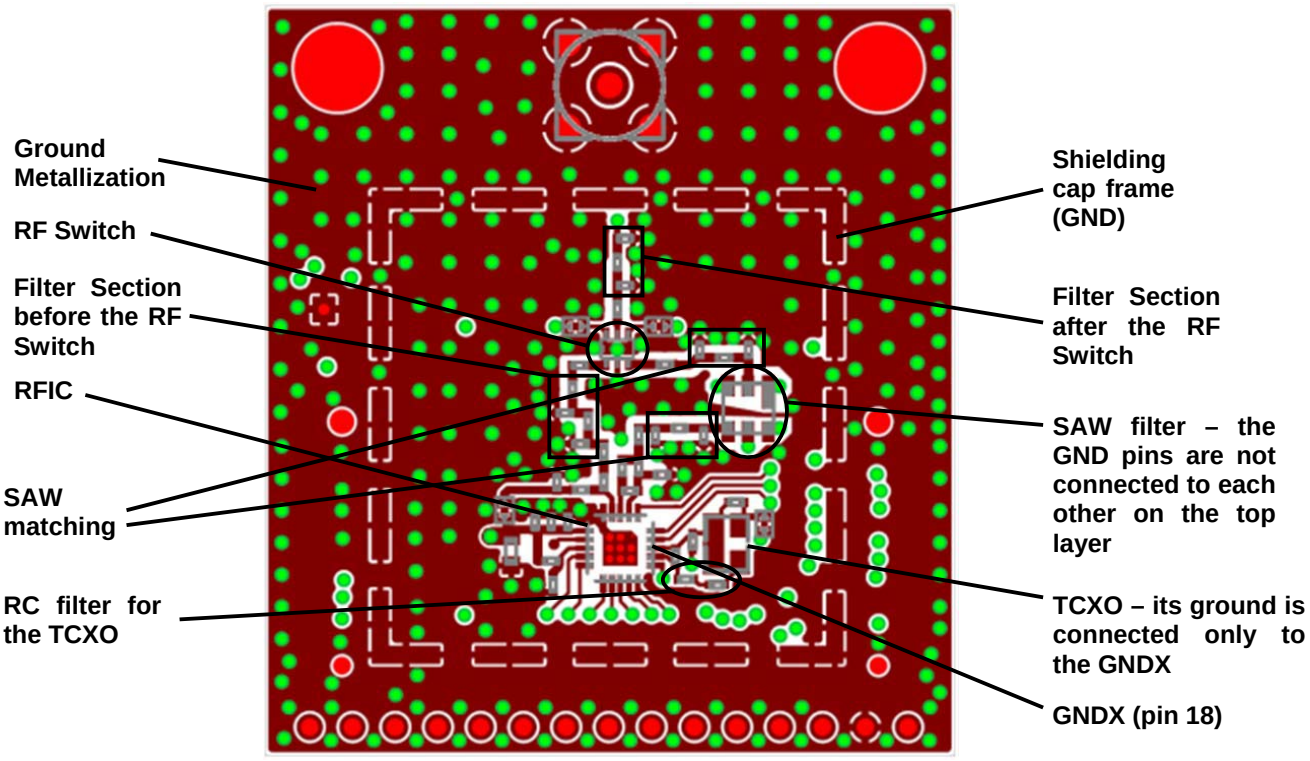


Figure 26. 4463-PCE20C868SE RF Pico Board (Top Layer)

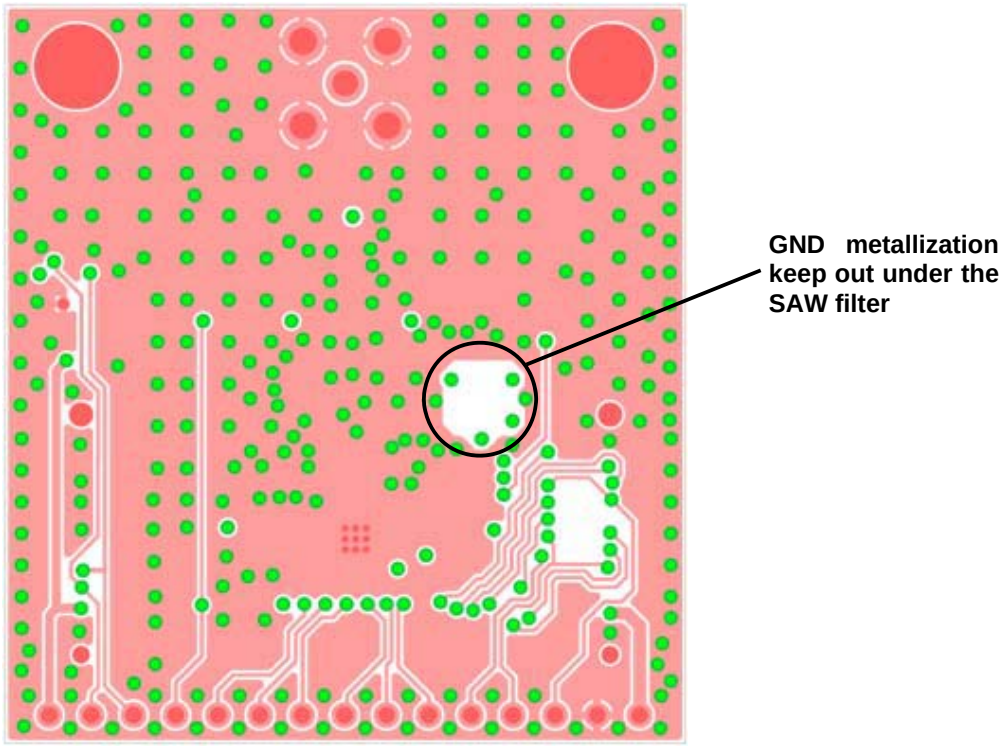


Figure 27. 4463-PCE20C868SE RF Pico Board (Inner2 Layer)

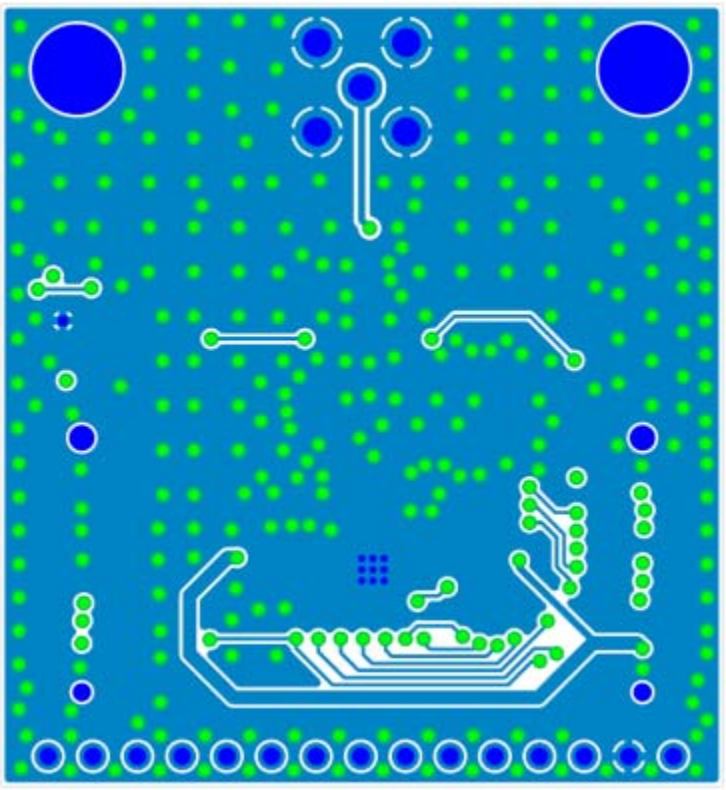


Figure 28. 4463-PCE20C868SE RF Pico Board (Inner3 Layer)

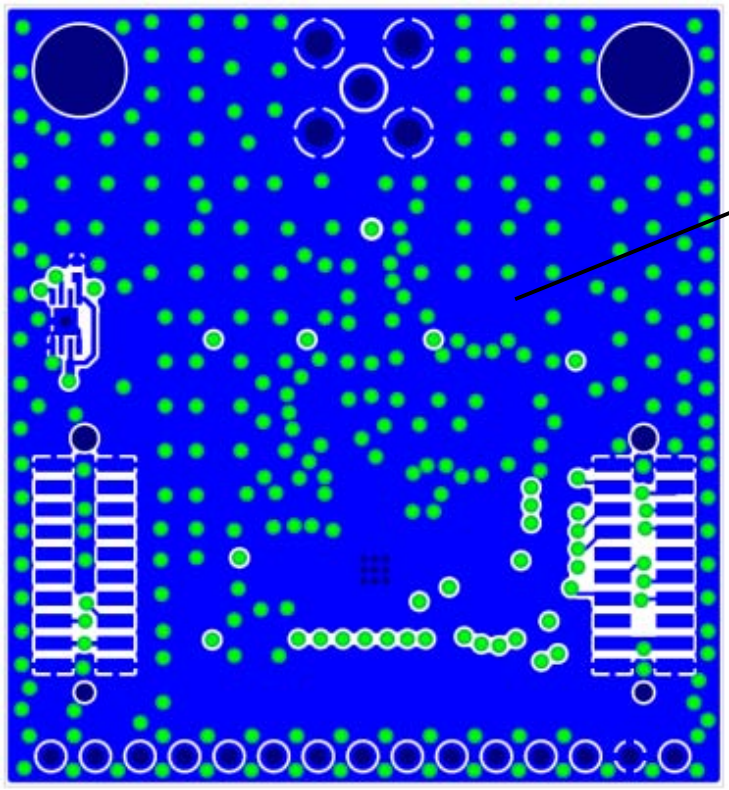


Figure 29. 4463-PCE20C868SE RF Pico Board (Bottom Layer)

4. Guidelines for Layout Design When Using the Si4460/61/63/64 RF ICs in Test Card Form

Due to the fact that the layout design recommendations are mostly concentrated on the close area of the matching network, in the case of using Test Cards, the layout design principles are the same as in the case of using Pico Boards, as described in the previous sections.

The Si4460/61/63/64 devices can use the same type of TX (and RX) matching networks in both cases, and the basic types of board layout configurations are also the same.

Due to these facts, the same operational properties can be achieved when using Test Cards or Pico Boards.

Figures 30 and Figure 31 demonstrate the layout design of the Test Cards and show the top and bottom layers, respectively.

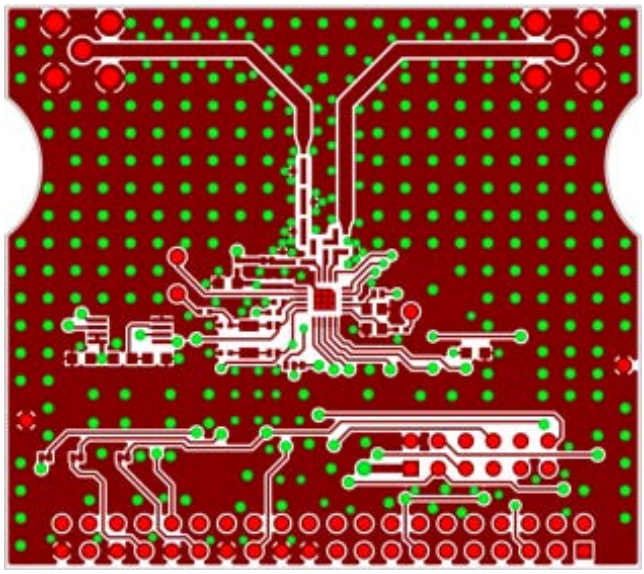


Figure 30. 446x-TCExxBxxx RF Test Card PCB (Top Layer)

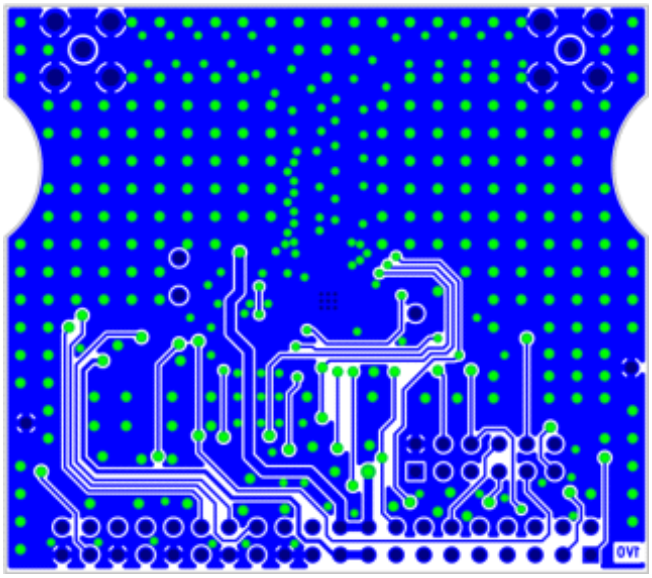
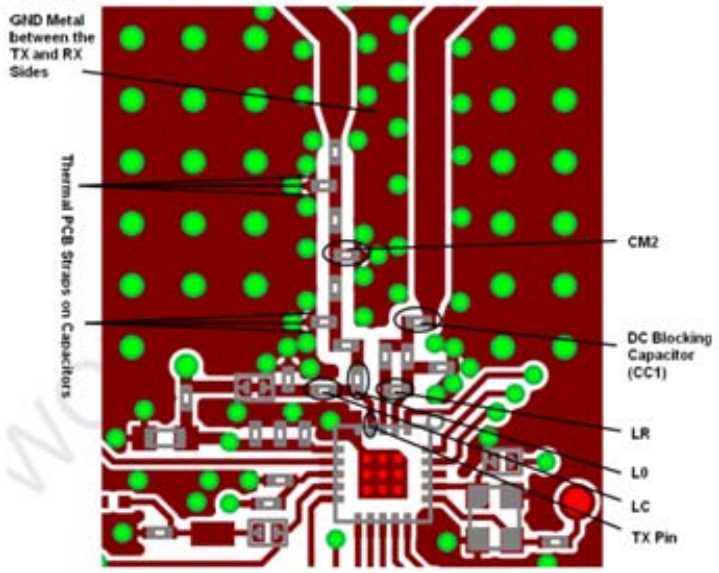
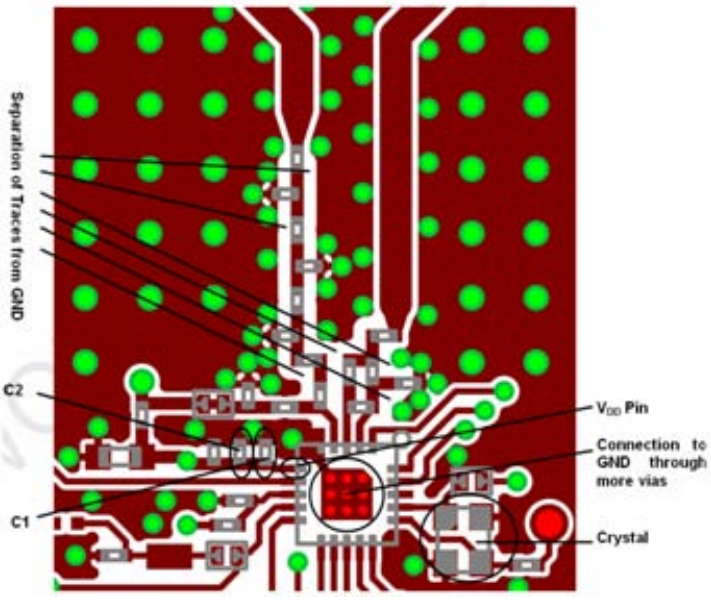
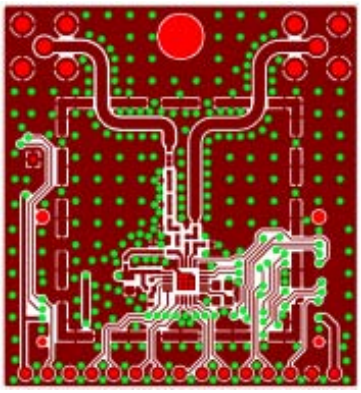
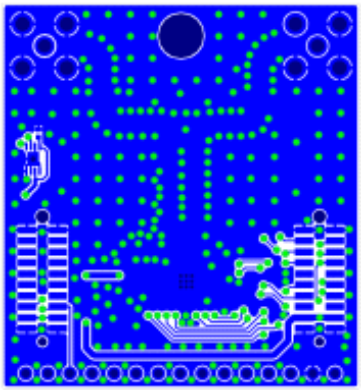
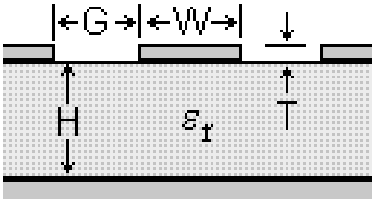
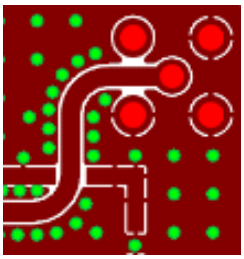


Figure 31. 446x-TCExxBxxx RF Test Card PCB (Bottom Layer)

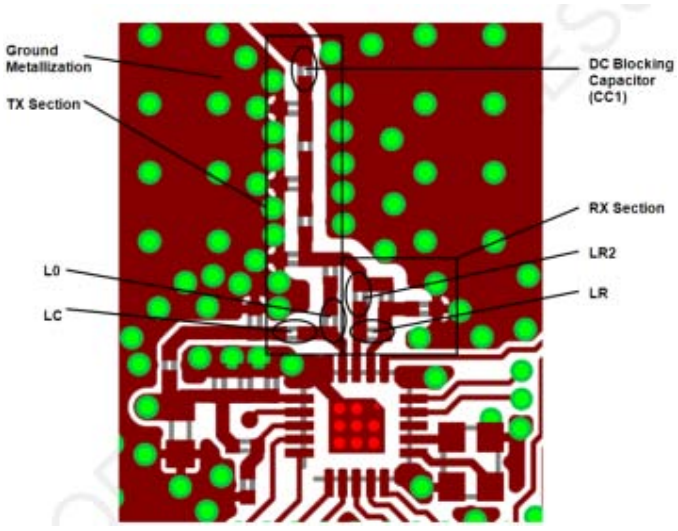
5. Checklist

5.1. Main Layout Design Principles

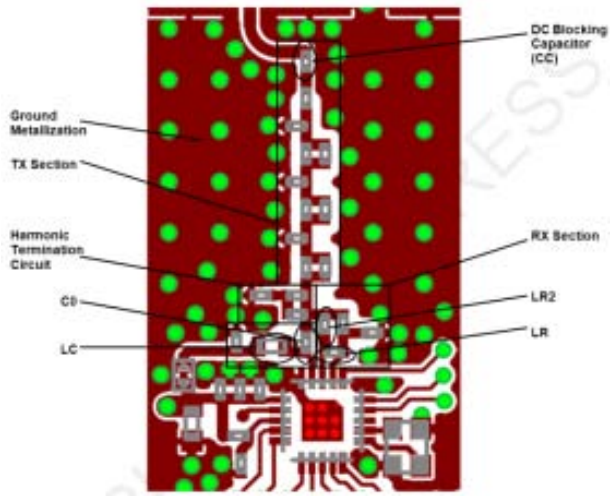
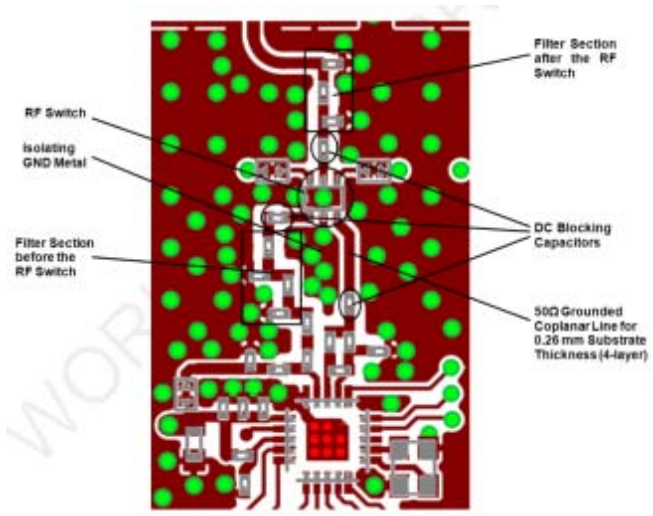
1.	☐	Is the choke inductor (LC) as close to the TX pin as possible?	
2.	☐	Is the RX parallel inductor (LR) perpendicular to the choke inductor (LC) in the TX path? (except for the Direct Tie type matching)	
3.	☐	Are the TX and RX separated by a ground metal on the top layer? (except for the Direct Tie type matching?)	
4.	☐	Are the neighboring matching network components as close to each other as possible?	
5.	☐	Are there more thermal straps used with the capacitors?	
6.	☐	Are the TX path inductors perpendicular to each other?	
7.	☐	Is there at least 0.5 mm separation in the matching between the traces/pads and the GND metal?	
8.	☐	Are the smallest value V_{DD} filter capacitors kept closer to the V_{DD} pin of the RF IC?	
9.	☐	Does the exposed pad footprint use more vias?	
10.	☐	Is the crystal as close to the RF IC as possible?	
11.	☐	Does ground metal exist between the crystal and the V_{DD} feed?	

12.	☐	Was large, continuous GND metalization added to at least the RF sections?	 
13.	☐	Was the area on the bottom layer under the matching network filled with GND metal, and was wiring and routing avoided in this region?	
14.	☐	Are the GND metal edges closed by a “via curtain” where possible, with a via distance less than lambda/10 of the highest (usually 10th) critical harmonic frequency?	
15.	☐	Were 50 Ω grounded coplanar lines used for connecting the matching network, the switch, and/or the SMA connector(s)?	 

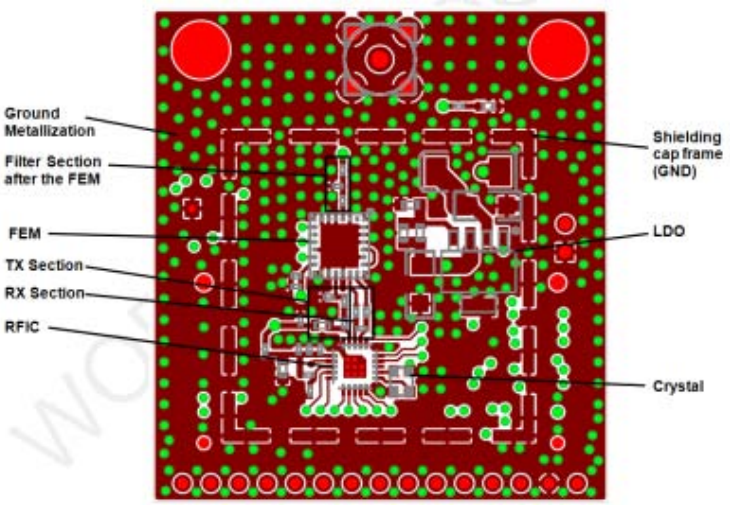
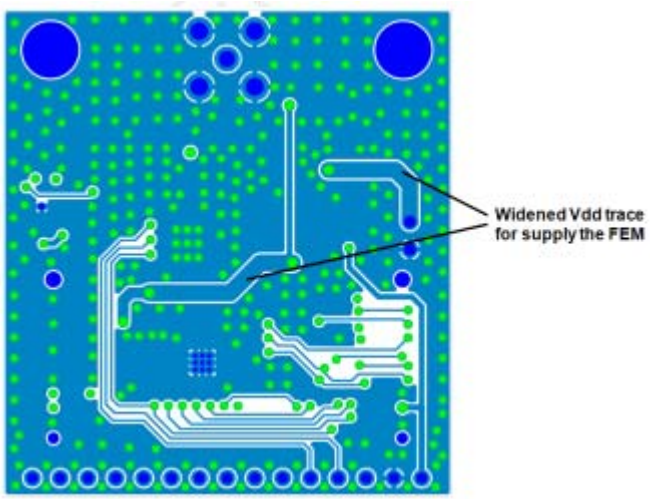
5.2. Additional Concerns for the Direct Tie Type Matching

16.	☐	Is the length of the trace connecting the RX and TX sides minimal?	
17.	☐	Are the traces connecting LR2 as short as possible?	
18.	☐	Is an additional dc blocking capacitor added to the output of the matching network to block the dc path in RX mode?	

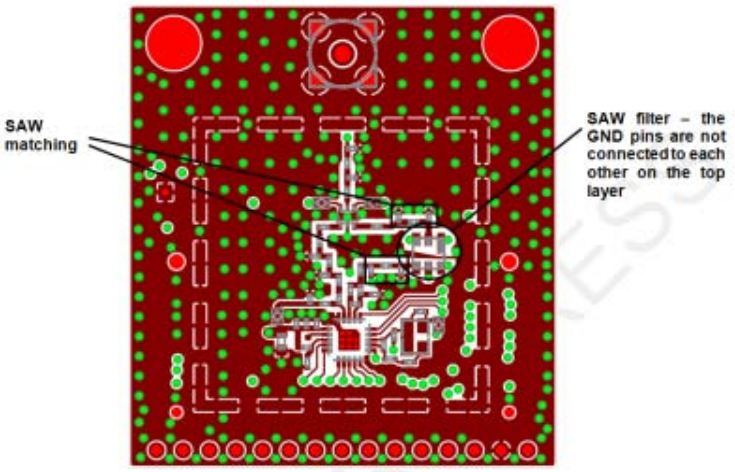
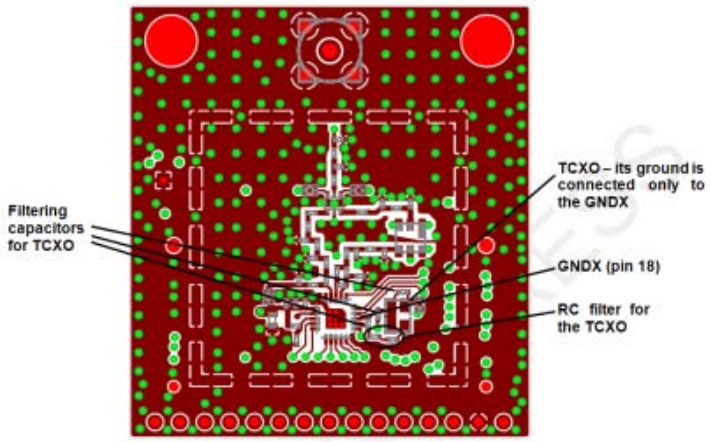
5.3. Additional Concerns for the SQW and the Switch and Diversity Type Matchings

19.	☐	Was the additional harmonic termination circuit added into the TX path in case of SQW matching?	
20.	☐	Were series capacitors added to the TX path to block the dc when a TX/RX switch (or Diversity switch) is used?	
21.	☐	Was a 50 Ω grounded coplanar line used to connect the RX side matching to the RF switch (if they are far from each other)?	
22.	☐	Was the area between the RX and TX sides filled with GND metal?	
23	☐	Are the antennas perpendicular to each other?	
24	☐	Is the distance between the antennas approximately 1/4 wavelength?	

5.4. Additional Concerns for Designs with FEM and LDO

25.	☐	What is in the FEM's data sheet? Is any filter section after the FEM necessary?	
26.	☐	Does the shielding cap cover the LDO's sections as well if it is used?	
27.	☐	Is the Vdd trace widened for supplying the FEM?	
28.	☐	Is there as large and continuous GND metalization for the FEM as possible?	

5.5. Additional Concerns for Designs with SAW Filter and TCXO

29.	☐	What is in the data sheet of the SAW filter? Are additional matching components necessary?	
30.	☐	Is the good ultimate rejection ensured for the SAW? Are the grounding loops minimized between the input and the output of the SAW filter?	
31.	☐	In the **high output power cases** are the additional capacitors and RC filter added for the TCXO?	
32.	☐	In the **high output power cases** are the TCXO's filtering capacitors only connected to the GNDX?	
33	☐	In the **high output power cases** is the TCXO's ground separated from the entire ground plane of the PCB and connected to GNDX?	

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Layout Design Recommendations shown are based on Pico Board form.
- Added general rules for designing a good RF-related layout.
- Added further layout design recommendations for minimizing PCB radiation.
- Added four-layer design examples.
- Added design examples for using FEM, LDO, TCXO, and SAW filter.

Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

Patent Notice
Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.
Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.