PN544

Near field communication (NFC) controller

Rev. 2.1 — 10 December 2008 Objective data sheet
155221 SECURED, STRICTLY CONFIDENTIAL INFORMATION

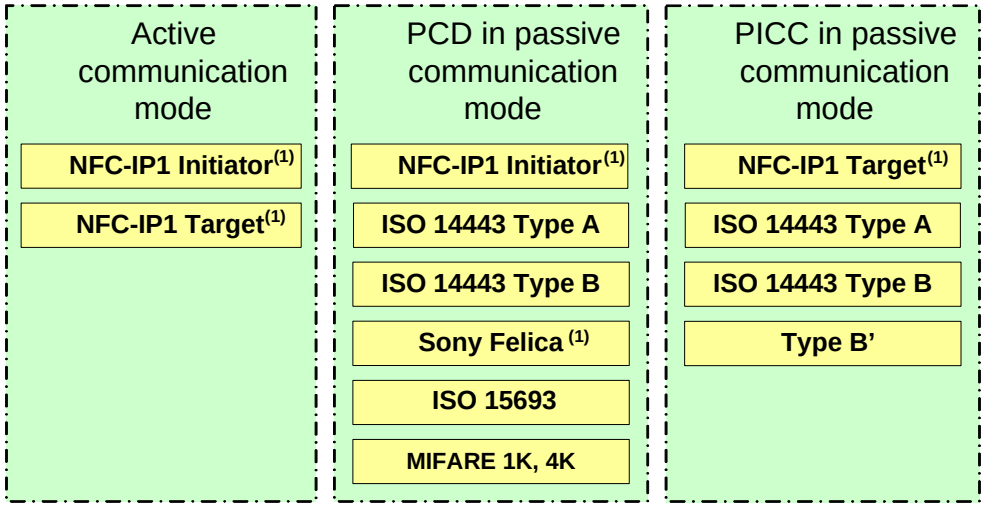
1. Introduction

This objective data sheet describes PN544, NXP's second generation NFC controller. In its objective state, this data sheet requires additional documents for functional chip description and design in. Please refer to the references listed in this document for full list of documentation provided by NXP.

2. General description

The PN544 is full featured NFC controller designed for integration in mobile phones. It is optimized for low power consumption with fully host controllable power states and for low footprint for mobile phone applications.

The PN544 builds a contactless frontend for phone platforms towards contactless applications available on existing infrastructure. Integrated CPU is decoupling the host controller from the timing constraints of RF communication and allowing autonomous operation. With support for both UICC based and separate, phone integrated, secure element it enables the flexibility for application design for different markets.



(1) According to ISO/IEC 18092 (ECMA 340) standard

Fig 1. PN544 transmission modes

Supported transmission modes are listed in Figure 1 "PN544 transmission modes" on page 1. For active and PCD communication modes, host control is required, whereas for the contactless card functionality the PN544 can act autonomously if previously configured by host in such a manner. PICC functionality in passive communication mode can be supported without phone being turned on or even with phone battery removed.[1]

3. Features

- HT80C51MX low power microcontroller core
  - Code memory: 128 KB ROM, 44 KB EEPROM
  - Data memory: 5KB SRAM, 8 KB EEPROM
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated configurable Polling Loop for automatic device discovery
- RF protocols supported
  - Support of ISO/IEC 14443A, ISO/IEC 14443B, FeliCa PCD mode
  - Supports MIFARE reader encryption mechanism (MIFARE 1K/4K)
  - Supports NFC Forum tag (MIFARE Ultralight, Jewel, FeliCa open tag, DESFire)
  - Support of ISO/IEC 15693/ICODE VCD mode
  - Supports of NFC-IP1 protocol
  - Support of ISO/IEC 14443A, ISO/IEC 14443B card emulation
- Supported host interfaces
  - High Speed UART (HSU)
  - SPI
  - I^2C
- Supported secure element interfaces
  - SWP/HCI (Single Wire Protocol) according ETSI/SCP standardization Release 7
  - ISO/IEC 28361 (ECMA 373) NFC-WI interface to connect an external secure IC restricted to 106kb/s. Signal In activation is not implemented.
- Flexible clock supply concept to facilitate PN544 integration
  - Integrated FracNPLL unit to make use of cellular reference clock
  - Internal oscillator for 27.12 MHz crystal connection
- Integrated power management unit
  - Direct connection to a mobile battery (2.3 V to 5.5 V voltage supply range)
  - Power switch for secure companion chips connected over SWP or NFC-WI
  - Support different power-down/standby mode by firmware
  - Powered by the field and Powered by the battery mode when mobile is off supported
- Dedicated IO ports for external device control
- Flexible interrupts using IRQ pin
- Automatic host wake up via host control interface
- Integrated non-volatile memory to store data and executable code for customizing
- Integrated antenna detector for production tests

1. This functionality is strongly dependent on actual implementation and mechanical constraints (e.g. antenna size)

4. Applications

- Mobile phones
- Portable equipment (Personal Digital Assistants, notebooks)
- Consumer devices

5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery Supply Voltage		2.3	-	5.5	V
V_{BAT}	Battery Supply Voltage	RF field generation	2.7	-	5.5	V
PV_{DD}	Pad power supply (supply voltage for host interface)		1.65	1.8	1.95	V
SV_{DD}	Supply voltage for secure chip interface		1.65	1.8	1.95	V
TV_{DD}	Transmitter supply voltage	Configured to 2.7 V, V_{BAT}>3.1V	2.5	2.7	2.9	V
TV_{DD}	Transmitter supply voltage	Configured to 3 V, V_{BAT}>3.4V	2.8	3.0	3.2	V
TV_{DD}	Transmitter supply voltage	Configured to 3.3 V, V_{BAT}>3.7V	3.1	3.3	3.5	V
AV_{DD}, DV_{DD}	Internal Analog, digital supply voltages		1.65	1.8	1.95	V
$SIMV_{CC}$	UICC supply output voltage		1.62	1.8	1.98	V
I_{HPD}	Hard Power Down current consumption	V_{BAT} = 3 V T = 25 °C		5		µA
I_{MON}	Monitor Mode current consumption			10		µA
I_{STBY}	Standby Mode current consumption		30		50	µA
I_{VBAT}	Continuous total current consumption	PCD mode at typical 3 V			170	mA
$I_{SVDD\ max}$	Maximum current in secure element supply				5	mA
$I_{TVDD\ max}$	Maximum current in transmitter path	Case of not correctly tuned antenna or short at transmitter	135	150	165	mA
P_{max}	Maximum power dissipation	Reader (antenna connected) V_{BAT}=5.5V			550	mW
T_{amb}	Operating ambient temperature	JEDEC PCB-0.5	-30		+85	°C

[1] All values listed here are design targets

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5441A2ET [1]	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls; body 4.5 × 4.5 × 0.8 mm	SOT962-1

[1] Refer to "Section 20.4 “Licenses”

7. Marking

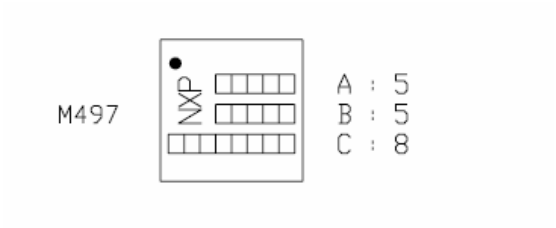


Fig 2. PN544 package marking

Table 3. Marking codes

Type number	Marking code
A	Product name including three digits for string ’544’ and two digits for hardware version
B	Diffusion batch sequence number
C	Manufacturing code including: Diffusion center code Assembly center code ROHS compliancy indicator Manufacturing year and week Mask layout version Product life cycle status code

8. Block diagram

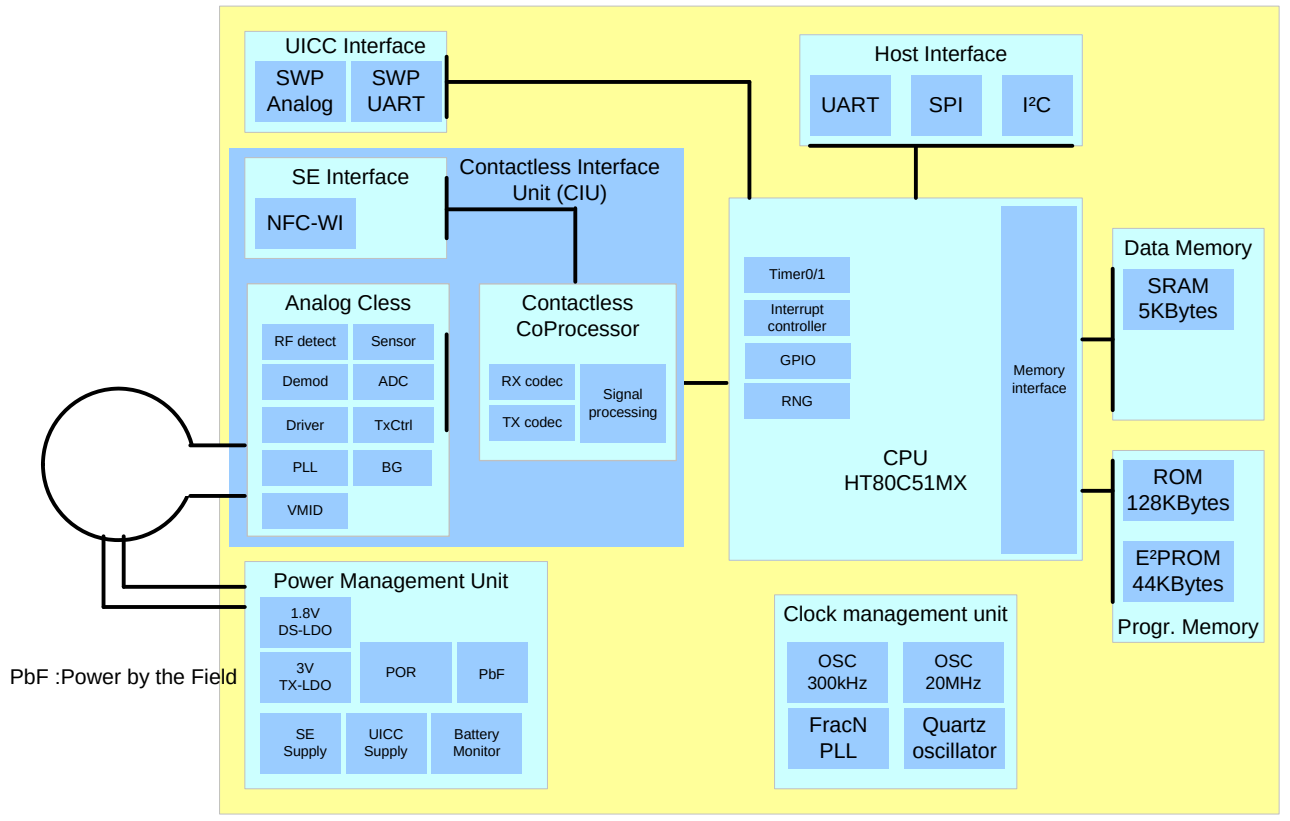


Fig 3. PN544 block diagram

9. Pinning information

9.1 Pinning

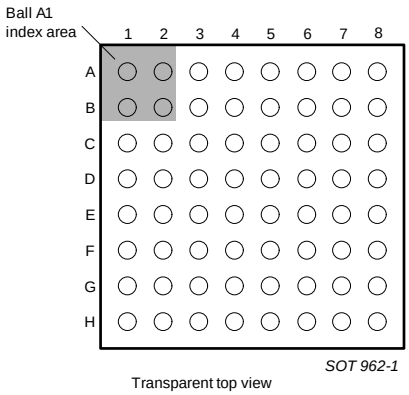


Fig 4. Pinning of PN544 in TFBGA64 (SOT962-1)

Table 4. PN544 Pin description

Symbol	Pin	Type	Ref Voltage	Description
GPIO7	A1	IO	PV_{DD}	General purpose IO / Digital testbus signal
IFSEL0	A2	IO	PV_{DD}	Host interface select input 0
IRQ	A3	O	PV_{DD}	IRQ output
PVDD	A4	Power	n/a	Pad supply voltage input (VI/O)
DVDD	A5	Power	n/a	Digital supply voltage output for decoupling
TMS	A6	I	PV_{DD}	JTAG pin
RFU1	A7	n/a	n/a	Reserved for future use
PMUVCC	A8	Power	n/a	UICC Power in from external PMU
GPIO4	B1	IO	PV_{DD}	General purpose IO / Download mode control
GPIO5	B2	IO	PV_{DD}	General purpose IO / Digital testbus signal
GPIO6	B3	IO	PV_{DD}	General purpose IO / Digital testbus signal
IF1	B4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
PVSS	B5	Ground	n/a	Pad VSS
nOCI	B6	I	PV_{DD}	Selection between OCI and Boundary Scan functionality
VEN	B7	I	V_{BAT}	Enable/disable LDO regulator / Reset
SIMVCC	B8	Power	n/a	Power output to supply the UICC
VDHF	C1	Power	n/a	Monitor rectifier output voltage
GPIO3	C2	O	PV_{DD}	PWR_REQ: power request towards host
GPIO2	C3	O	PV_{DD}	CLK_REQ: clock request towards host
IF2	C4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
TCK	C5	I	PV_{DD}	JTAG pin
NRESET	C6	I	PV_{DD}	Reset input (active low)
SWIO	C7	IO	1.8V - $PMUV_{CC}$	SWP data connection
SVDD	C8	Power	n/a	SE power; fixed to SV_{DD}=1.8V

Table 4. PN544 Pin description *…continued*

Symbol	Pin	Type	Ref Voltage	Description
VCO_VDD	D1	Power	n/a	FracNPLL supply voltage input
DVSS	D2	Ground	n/a	Digital VSS
GPIO1	D3	I	PV_{DD}	CLK_ACK: clock acknowledge from host
IF3	D4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
TDI	D5	I	PV_{DD}	JTAG pin
EXT_SW_CTRL	D6	O	$SIMV_{CC}$	Control output signal for external UICC power switch
SIGOUT	D7	O	SV_{DD}	NFC-WI data output
VBAT	D8	Power	n/a	Battery voltage
XTAL1	E1	I	AV_{DD}	Oscillator or FracNPLL input
AVSS1	E2	Ground	n/a	Analog VSS
GPIO0	E3	I	PV_{DD}	General purpose IO
IF0	E4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
TDO	E5	O	PV_{DD}	JTAG pin
RFU2	E6	n/a	n/a	Reserved for future use
SIGIN	E7	I	SV_{DD}	NFC-WI data input
VEN_MON	E8	I	V_{BAT}	Enable of the battery voltage monitor
XTAL2	F1	O	AV_{DD}	Oscillator output
AVDD_out	F2	Power		Analog supply voltage output for decoupling
AUX3	F3	O	AV_{DD}	Auxiliary Output: this pin delivers analog and digital test signals
IFSEL1	F4	IO	PV_{DD}	Host interface select input 1
IFSEL2	F5	IO	PV_{DD}	Host interface select input 2
VSS	F6	Ground	n/a	VSS
TVDD_OUT	F7	Power	n/a	Antenna driver supply voltage output for decoupling
VBAT2	F8	Power	n/a	Power pin reserved for future use. Shall be connected to V_{BAT} pin
AVDD_in	G1	Power	n/a	Analog supply voltage input after decoupling
AUX1	G2	O	AV_{DD}	Auxiliary Output: this pin delivers analog and digital test signals
AUX4	G3	O	AV_{DD}	Auxiliary Output: this pin delivers analog and digital test signals
VMID	G4	O	AV_{DD}	Voltage receiver reference
PF1	G5	Power	n/a	Powered by the field contact
PF2	G6	Power	n/a	Powered by the field contact
PMU_GND	G7	Ground	n/a	PMU VSS
TVDD	G8	Power	n/a	Antenna driver supply voltage input after decoupling
RFU3	H1	n/a	n/a	Reserved for future use
AUX2	H2	O	AV_{DD}	Auxiliary Output: this pin delivers analog and digital test signals
AVSS2	H3	Ground	n/a	Analog VSS
RX	H4	I	AV_{DD}, AV_{ss}	Receiver input
TVSS1	H5	Ground	n/a	Antenna driver VSS
TX1	H6	O	TV_{DD}, TV_{ss}	Antenna driver
TX2	H7	O	TV_{DD}, TV_{ss}	Antenna driver
TVSS2	H8	Ground	n/a	Antenna driver VSS

9.2 Pin description

In addition to the general pinning list, the pins of PN544 can be divided in groups according to the device they are connected to. Here provided list uses the same structure as functional groups used in Figure 28 “Application schematic” on page 50 and Figure 29 “Application schematic 2” on page 51.

Table 5. Host connection pins

Symbol	Pin	Description
VEN	B7	Enable/disable LDO regulator / Reset / Battery Voltage Monitor
PVDD	A4	Pad supply voltage Input (VI/O)
PMUVCC	A8	UICC power in from mobile PMU
IRQ	A3	IRQ output
NRESET	C6	Reset input (active low)
XTAL1	E1	Oscillator input
IF0	E4	Host interface pin - functionality depends on selected interface
IF1	B4	Host interface pin - functionality depends on selected interface
IF2	C4	Host interface pin - functionality depends on selected interface
IF3	D4	Host interface pin - functionality depends on selected interface

Table 6. UICC connection pins

Symbol	Pin	Description
SIMVCC	B8	Power output to supply the UICC
SWIO	C7	SWP data connection
EXT_SW_CTRL	D6	Control output signal for external UICC power switch

Table 7. SE connection pins via NFC-WI

Symbol	Pin	Description
SVDD	C8	SE power; fixed to SV_{DD}=1.8V
SIGOUT	D7	NFC-WI data output
SIGIN	E7	NFC-WI data input

Table 8. Antenna connection pins

Symbol	Pin	Description
TX1	H6	Antenna driver
TX2	H7	Antenna driver
RX	H4	Receiver input
VMID	G4	Antenna mid voltage
PF1	G5	Powered by the field contact
PF2	G6	Powered by the field contact

Table 9. GPIO pins

Symbol	Pin	Description
GPIO0	E3	General purpose IO
GPIO1	D3	Clock acknowledge
GPIO2	C3	Clock / power request
GPIO3	C2	Power request
GPIO4	B1	General purpose IO / Download mode control
GPIO5	B2	General purpose IO / Digital testbus signal
GPIO6	B3	General purpose IO / Digital testbus signal
GPIO7	A1	General purpose IO / Digital testbus signal

Table 10. Configuration pins

Symbol	Pin	Description
IFSEL0	A2	Host interface select input
IFSEL1	F4	Host interface select input
IFSEL2	F5	Host interface select input

10. Functional description

The PN544 is an NFC transceiver IC designed for mobile phone integration.

It is fully compliant with ETSI/SCP SWP and HCI specifications.
The PN544 provides a HCI interface towards a mobile phone host or any other host on one of PN544's integrated host interfaces and an ETSI SWP and HCI interface towards phone UICC or any other secure element supporting ETSI SWP.

Additionally, it provides NFC-WI interface towards second secure element connected via this interface. Thus, the PN544 can provide full secure element functionality also without UICC present in the system.

It is fully ETSI/SCP HCI compliant with additional command set for NXP specific product features. This IC is fully user controllable by the firmware software interface described in Ref. 7 "PN544 User Manual".

Moreover, the PN544 provides integrated power management unit together with logic adaptable to the phone power state in order to preserve energy supporting powered by the field and powered-down mode.

10.1 Functional / Power states of PN544

PN544's functional states as depicted in Figure 5 "Functional diagram" on page 11 depend on two factors:

- Energy available from the system
- Configuration by host system, both in HW and SW

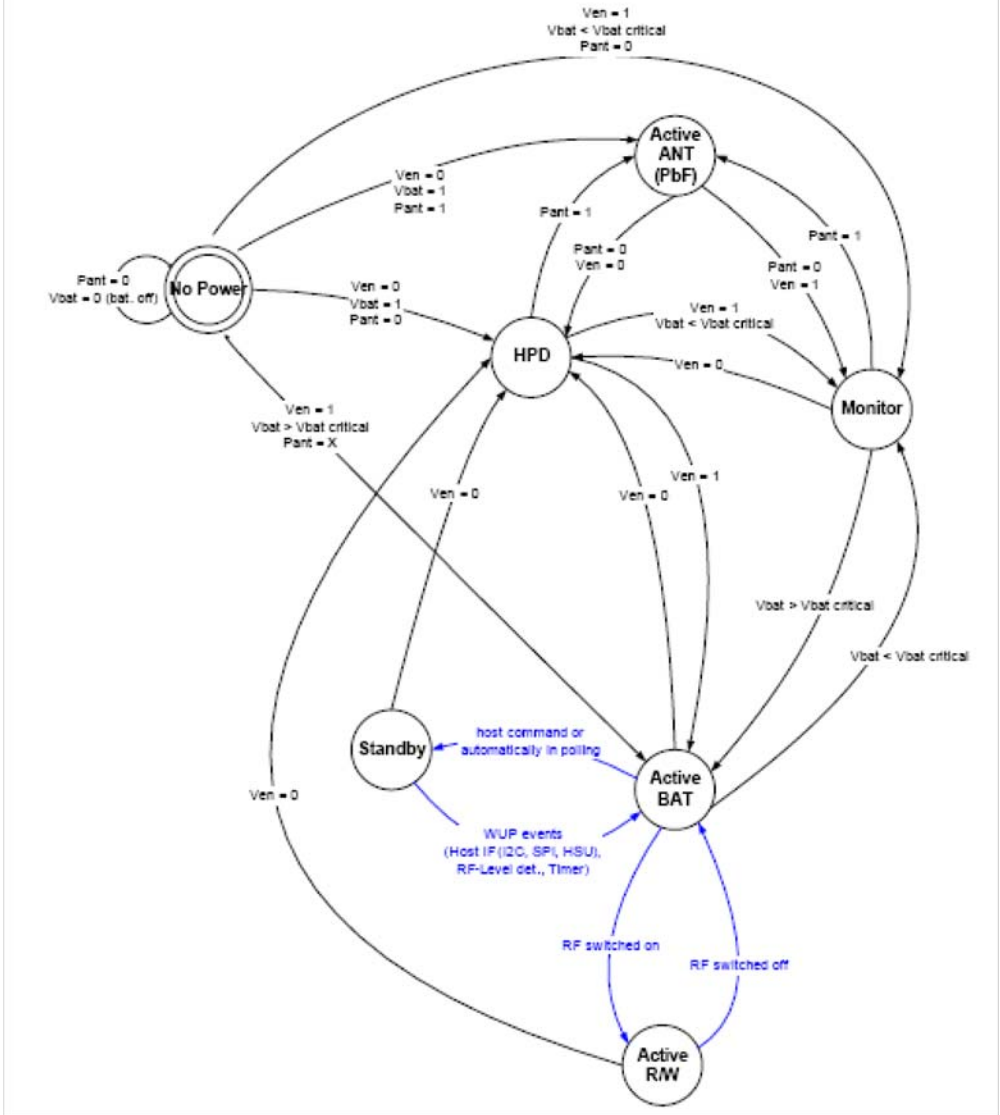


Fig 5. Functional diagram

On application level, PN544 will continuously switch between different states to optimize the current consumption. Please refer to Table 1 "Quick reference data" on page 3 for targeted current consumption in here described states.

The PN544 is designed to allow the host controller full control over its functional states, thus of the power consumption of PN544 based NFC solution and possibility to restrict parts of PN544 functionality.

10.1.1 Standby mode

Standby mode is PN544's default state. PN544 can switch to Standby mode autonomously (if configured by host) or upon dedicated host command to save energy. This state is independent of the PV_{DD} value (meaning whatever the state of the mobile phone baseband; on or off).

In this mode PN544 is not functional as RF frontend and most blocks including CPU are physically detached from power supply. Number of wake-up sources[2] exist to put PN544 into active battery mode:

- Host interface wake-up event (I^2C, SPI, HSU)
- Antenna RF level detector
- Timer event

If wake-up event occurs, PN544 will switch to active battery mode. Any further operation depends on software configuration and/or wake-up source.

Standby mode is available for $V_{BAT} > V_{BAT}$critical and V_{EN}>1.1V.

Table 11. Host pin state in standby mode

Pin name	PV_{DD} biased			PV_{DD} not biased
	I^2C host interface	HSU host interface	SPI host interface	HSU or SPI host interface
GPIO0	Input			InputDis
GPIO1	Input (CLK acknowledge)			InputDis
GPIO2	Output (CLK request)			InputDis
GPIO3	Output (PWR request)			InputDis
GPIO4	Input (Enter download mode)			InputDis
GPIO5	Input			InputDis
GPIO6	Input			InputDis
GPIO7	Input			InputDis
IF0	Input	Output	Input	InputDis
IF1	Input	Input	Input	InputDis
IF2	Open-Drain	[1]	Input	InputDis
IF3	Open-Drain	Output	Output	InputDis
IRQ	Output			InputDis
NRESET	Input			InputDis

[1] The pin state depends of HSU mode

2. All host related wake-up events imply that PV_{DD} is available

10.1.2 Active R/W mode

In this mode, PN544 is acting as reader/writer, searching for or communicating with passive tags or NFC target in the own RF field. Once RF communication has ended, PN544 will switch to active battery mode (i.e. switch RF transmitter off) to save energy.

Active R/W mode shall be used with $2.7V<V_{BAT}<5.5V$, $1.65V<PV_{DD}<1.95V$ and $V_{EN}>1.1V$.

Table 12. Host pin state in Active R/W mode

Pin name	$2.7V<V_{BAT}<5.5V$ $1.65V<PV_{DD}<1.95V$ $V_{EN}>1.1V$.		
	I^2C host interface	**HSU host interface**	**SPI host interface**
GPIO0	Input		
GPIO1	Input (CLK acknowledge)		
GPIO2	Output (CLK request)		
GPIO3	Output (PWR request)		
GPIO4	Input (Enter download mode)		
GPIO5	Input		
GPIO6	Input		
GPIO7	Input		
IF0	Input	Output	Input
IF1	Input	Input	Input
IF2	Open-Drain	[1]	Input
IF3	Open-Drain	Output	Output
IRQ	Output		
NRESET	Input		

[1] The pin state depends of HSU mode

10.1.3 Active battery mode

In active battery mode PN544 is fully powered, but the RF transmitter stage is turned off.

Active battery mode shall be used with V_{BAT}critical<V_{BAT} <5.5V, 1.65V<PV_{DD}<1.95V and V_{EN}>1.1V. If the V_{BAT} monitor is disabled then the mode is guaranteed for 2.3V<V_{BAT}<5.5V.

Table 13. Host pin state in Active battery mode

Pin name	V_{BAT}critical<V_{BAT}<5.5V or 2.3V<V_{BAT}<5.5V if V_{BAT} monitor is disable 1.65V<PV_{DD}<1.95V V_{EN}>1.1V		
	I^2C host interface	**HSU host interface**	**SPI host interface**
GPIO0	Input		
GPIO1	Input (CLK acknowledge)		
GPIO2	Output (CLK request)		
GPIO3	Output (PWR request)		
GPIO4	Input (Enter download mode)		
GPIO5	Input		
GPIO6	Input		
GPIO7	Input		
IF0	Input	Output	Input
IF1	Input	Input	Input
IF2	Open-Drain	[1]	Input
IF3	Open-Drain	Output	Output
IRQ	Output		
NRESET	Input		

[1] The pin state depends of HSU mode

[2] When the V_{BAT} monitor is disable, the pins states cannot be guaranteed when V_{BAT} is below 2.3V

10.1.4 Polling loop

Polling loop is a combination of a dedicated functional and power state of PN544. In polling loop, PN544 will switch between Standby mode (to save energy), Active R/W (to poll for devices in range) or be in active battery mode (either in performing card emulation or in transition between two previous states). Detailed description of polling loop configuration option is given in Ref. 7 “PN544 User Manual”.

10.1.5 Hard power down (HPD) mode

Hard power down mode is entered only by setting V_{EN} to low. As this signal is under host control, PN544 has no influence on entering or exiting this state. By putting V_{EN} < 1.1V, PN544's PMU is physically detached from the battery supply (please refer to Figure 20 "Battery voltage monitor principle" on page 39 for principle schematic).

Table 14. Host pin state in hard power-down mode

Pin name	V_{EN}<1.1V
	All host interfaces All P_{VDD} values [1]
GPIO0	InputDis
GPIO1	InputDis
GPIO2	InputDis
GPIO3	InputDis
GPIO4	InputDis
GPIO5	InputDis
GPIO6	InputDis
GPIO7	InputDis
IF0	InputDis
IF1	InputDis
IF2	InputDis
IF3	InputDis
IRQ	InputDis
NRESET	InputDis

[1] The pin voltage shall still be below PV_{DD} to avoid any extra current consumption

10.1.6 Monitor mode

By V_{EN} > 1.1V and battery supply reaching the monitor threshold (see also Section 10.6.5 “Battery voltage monitor” on page 39) PN544 will autonomously detach internal PMU from battery supply to protect the battery from deep discharge. In monitor mode, PN544 will exit it only if it can be powered from the field or the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 41 “Battery voltage monitor characteristics” on page 53.

Table 15. Host pin state in monitor mode

Pin name	$V_{BAT} < V_{BAT}$critical $V_{EN} > 1.1V$
	All host interfaces All P_{VDD} values [1]
GPIO0	InputDis
GPIO1	InputDis
GPIO2	InputDis
GPIO3	InputDis
GPIO4	InputDis
GPIO5	InputDis
GPIO6	InputDis
GPIO7	InputDis
IF0	InputDis
IF1	InputDis
IF2	InputDis
IF3	InputDis
IRQ	InputDis
NRESET	InputDis

[1] The pin voltage shall still be below PV_{DD} to avoid any extra current consumption

10.1.7 Active antenna mode (Powered-by-field)

Active antenna mode describes the state of PN544 in which the battery supply is not available (either because host has detached PN544 via VEN pin or the battery voltage level has reached the critical level) and RF field provides sufficient energy to power-up PN544.

Table 16. Host pin state in active antenna mode

Pin name	All host interfaces All P_{VDD} values [1]
	$V_{BAT}<V_{BAT}$ critical or $V_{EN}<1.1V$ RF field present
GPIO0	InputDis
GPIO1	InputDis
GPIO2	InputDis - Pull down
GPIO3	InputDis
GPIO4	InputDis - Pull down
GPIO5	InputDis
GPIO6	InputDis
GPIO7	InputDis
IF0	InputDis
IF1	InputDis
IF2	InputDis
IF3	InputDis
IRQ	InputDis - Pull down
NRESET	InputDis

[1] The pin voltage shall still be below PV_{DD} to avoid any extra current consumption

10.2 Microcontroller HT80C51MX

The PN544 is controlled via an embedded HT80C51MX microcontroller core.

The PN544 microcontroller core is an improved version of the ultra low-power 80C51. This microcontroller is an asynchronous core offering following advantages:

- Extremely low power: Zero stand-by power while in sleep mode, both for CPU core and CPU peripherals, but immediately available for full-speed fully-functional operation
- Very low electromagnetic emission (EME)

Its principle features are:

- Clock-less, low-power design
- MMU/MPU interface to interface with Data and Code memory
- Power control module to manage the CPU power consumption
- Interface to configure I/O pads
- Interrupt controller
- Timer 0/1
- Debug interface

10.2.1 PN544 memory management

The memory organization of the PN544 is based on the standard 80C51MX memory model that offers a unified address space for code and data memory.
The integrated Memory Management Unit (MMU) offers improved addressing capabilities in order to address up to 16 MB of physical code/data memory. All types of memories, except the SFRs and the four Register Banks, are accessed via the Memory Management Unit (MMU).

The standard 80C51 memory areas (CODE, DATA, IDATA, etc.) are mapped into 16 MB memory space, therefore the PN544 can operate with the following memory model:

- ROM (128 KB) are used for storing code for execution and fixed data
- RAM (5 KB)
- EEPROM (44 KB Code, 8 KB Data)
  - 8 KB EEPROM module are used for data storage (HCI registries, configuration ...)
  - 44 KB EEPROM are used for code execution only

10.2.2 Timer0/1 description

Timer0/1 comprises two 16-bit timer/counters: Timer0 and Timer1. Both can be configured as either a timer or an event counter.Timer0/1 are general purpose timer/counters.

Timer0/1 have the following functionality:

- Configurable edge or level detection interrupts
- Timer or counter operation
- 4 timer/counter modes

In the Timer function, the register's timer is incremented every timer clock cycle.
In the Counter function, the register is incremented in response to a 1 to 0 transition at its corresponding external input pin.
It is configured to work with following clock frequencies 1kHz/13.56 MHz/27.12 MHz.

This feature is used and reserved for embedded PN544 firmware and can not be used for external application purposes.

10.2.3 Interrupts management

The interrupts are grouped in 3 priority levels shown in Table 17. The interrupts of lower level can be interrupted by the higher levels interrupts.

Table 17. Interrupt sources

Interrupt priority	Interrupt sources
3 (highest)	Internal event like: • Thermal sensor • Current limiter • MMU violation • PV_{DD} presence • PMU_VCC presence
2	RF event and SIGIN activity
1	Host interface and SWP link

For example, if an over current occurs during the treatment of an interrupt due to a host interface, the PN544 will jump to the treatment of the over current.

The management of the interrupts is done by the embedded PN544 firmware and can not be controlled by host.

10.2.4 FW architecture

The PN544 features integrated in firmware are referenced in Ref. 7 "PN544 User Manual"

10.3 Host interfaces

The PN544 supports the following host interfaces:

- HSU Slave Interface, up to 460 800 Baud
- SPI Slave Interface, up to 10 MBaud
- I^2C Slave Interface, up to 3.4 MBaud

Only one host interface can be active at same time as pins are shared for all interfaces[3]. The host interfaces are waken-up in the following way:

- HSU: Wake-up after multiple pulses on RX line
- SPI: Transition of NSS Serial
- I^2C: Wake-up on I^2C address

To enable and ensure data flow control between PN544 and host controller additionally a dedicated interrupt line IRQ is provided.

10.3.1 High Speed UART (HSU) Interface

The high speed UART is a buffered, full or half duplex asynchronous serial interface with multi master support. It provides configurable clock rates.
The different data rates are derived from a single input clock of 27.12 MHz.

10.3.1.1 HSU configuration options

In order to select HSU for host communication, interface selection pins have to be configured as described in Table 18. This information is also provided in the application schematic for quick reference.

Table 18. Pin configuration for HSU interface selection

Pin name	Connection
IFSEL0	Connect to GND
IFSEL1	Connect to GND
IFSEL2	Connect to GND

The HSU interface shares four (4) pins with other host interfaces supported by the PN544. When interface selection pins IFSEL0-2 are configured as described in Table 18, functionality of interface pins IF0-3 changes to one described in Table 19.

Table 19. IF0-3 functionality for HSU interface

Pin name	Functionality
IF0	nc
IF1	RX
IF2	nc
IF3	TX

3. **Remark:** Pin layout would allow simultaneous connection of HSU and I^2C, but this is not supported by PN544.

10.3.2 I²C interface

The I²C interface implements a Slave I²C bus interface with integrated shift register, shift timing generation and Slave address recognition. I²C Standard mode (100 kHz SCLK), Fast mode (400 kHz SCLK) and High speed mode (3.4 MHz SCLK) are supported.

The mains hardware characteristics of the I²C module are:

- Support Slave I²C bus
- Standard, Fast and High speed modes supported
- Wake-up of the PN544 on its own address
- Serial clock synchronization can be used by PN544 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C interface module is optimized for low power, with power consumption of almost zero in sleep mode. It features address decoder for PN544 wake-up functionality.The on-chip I²C logic provides a serial interface that meets the I²C bus specification.

It is recommended to refer the I²C standard for more information.

10.3.2.1 I²C configuration options

In order to select I²C interface for host communication, interface selection pins have to be configured as described in Table 20. This information is also provided in the application schematic for quick reference.

Table 20. Pin configuration for I²C interface selection

Pin name	Connection
IFSEL0	Connect to GND
IFSEL1	Connect to PVDD
IFSEL2	Connect to GND

The I²C interface shares four (4) pins with other host interfaces supported by the PN544. When interface selection pins IFSEL0-2 are configured as described in Table 20, functionality of interface pins IF0-3 changes to one described in Table 21.

Table 21. IF0-3 functionality for I²C interface

Pin name	Functionality
IF0	ADR0: I²C address bit 0 (LSB)
IF1	ADR1: I²C address bit 1
IF2	SDA
IF3	SCL

10.3.2.2 I²C functional description

The I²C interface may operate in any of the following two modes:

- Slave Receiver
- Slave Transmitter

Two types of data transfers are possible on the I²C bus:

- Data transfer from a Master transmitter to a Slave receiver. The first byte transmitted by the Master is the Slave address. Next follows a number of data bytes. The Slave returns an acknowledge bit after each received byte.
- Data transfer from a Slave transmitter to a Master receiver. The first byte (the Slave address) is transmitted by the Master. The Slave then returns an acknowledge bit. Next follows the data bytes transmitted by the Slave to the Master. The Master returns an acknowledge bit after each received byte except the last byte. At the end of the last received byte, a “not acknowledge” is returned.

In a given application, the I²C interface may operate only as a Slave.

In the Slave mode, the I²C interface hardware looks for its own Slave address and the general call address. If one of these addresses is detected, an interrupt is requested.

10.3.3 Serial Peripheral Interface

10.3.3.1 Features

- Synchronous, Serial, Full-Duplex communication, 10 MHz max
- Slave mode
- Programmable clock polarity and phase

10.3.3.2 SPI configuration options

In order to select SPI interface for host communication, interface selection pins have to be configured as described in Table 22.
This information is also provided in the application schematic for quick reference.

Table 22. Pin configuration for SPI interface selection

Pin name	Connection
IFSEL0	CPHA switch: Clock PHAse: defines the sampling edge of MOSI data • CPHA = 1: Data are sampled on MOSI on the odd clock edges of SCK after NSS goes low • CPHA = 0: Data are sampled on MOSI on the even clock edges of SCK after NSS goes low
IFSEL1	CPOL switch: Clock POLarity • IFSEL1 = 0: the clock is idle low, and the first valid edge of SCK will be a rising one. • IFSEL1 = 1: the clock is idle high, and the first valid edge of SCK will be a falling one.
IFSEL2	Connect to PVDD

The SPI interface shares four (4) pins with other host interfaces supported by the PN544. When interface selection pins IFSEL0-2 are configured as described in Table 22, functionality of interface pins IF0-3 changes to one described in Table 23.

Table 23. IF0-3 functionality for SPI interface

Pin name	Functionality
IF0	NSS (Not Slave Select)
IF1	MOSI (Master Out Slave In)
IF2	SCK (Serial Clock)
IF3	MISO (Master In Slave Out)

10.3.3.3 SPI functional description

When a master device transmits data to PN544 (slave device) via the MOSI line, PN544 responds by sending data to the master device via the masters MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal.

PN544 starts logic when receiving a logic low at pin NSS and the clock at input pin SCK. Thus, PN544 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loads the 8 bit shift register. After the 8 bit shift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then PN544 waits for a clock train from the master to shift the data out on the slaves MISO line.

- Master In Slave Out (MISO)

  The MISO line is configured as an input in a master device and as an output in a slave device. It is used to transfer data from the slave to the master, with the most significant bit sent first. The MISO line of a slave device should be placed in the high impedance state if the slave is not selected.

- Master Out Slave In (MOSI)

  The MOSI line is configured as an output in a master device and as an input in a slave device. It is used to transfer data from the master to a slave, with the Most significant bit sent first.

- Serial Clock (SCK)

  The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines. The master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles. Since the master device generates SCK, this line becomes an input on a slave device and an output at the master device.

- Not Slave Select (NSS)

  The slave select input line is used to select a slave device. It has to be low prior to data transactions and must stay low of the duration of the transaction. The NSS line on master side must be tied high.

The timing relationships may be chosen by using IFSEL0 (CPHA) and IFSEL1 (CPLO) pins. Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, in order for the slave device to latch the data.

10.3.4 IOs configuration

This chapter describes the different configurations for the IO pads:

Table 24. IO pins

Symbol	Pin	Description
GPIO0	E3	General purpose IO
GPIO1	D3	Clock acknowledge
GPIO2	C3	Clock / power request
GPIO3	C2	Power request
GPIO4	B1	General purpose IO / Download mode control
GPIO5	B2	General purpose IO / Digital testbus signal
GPIO6	B3	General purpose IO / Digital testbus signal
GPIO7	A1	General purpose IO / Digital testbus signal
IF0	E4	Host interface pin - functionality depends on selected interface
IF1	B4	Host interface pin - functionality depends on selected interface
IF2	C4	Host interface pin - functionality depends on selected interface
IF3	D4	Host interface pin - functionality depends on selected interface

10.3.4.1 Pad configuration description

At least 4 pad configurations are used within the PN544. The pull-up and pull-down configurations offered in the standard pad are not used in the PN544.

Open-Drain

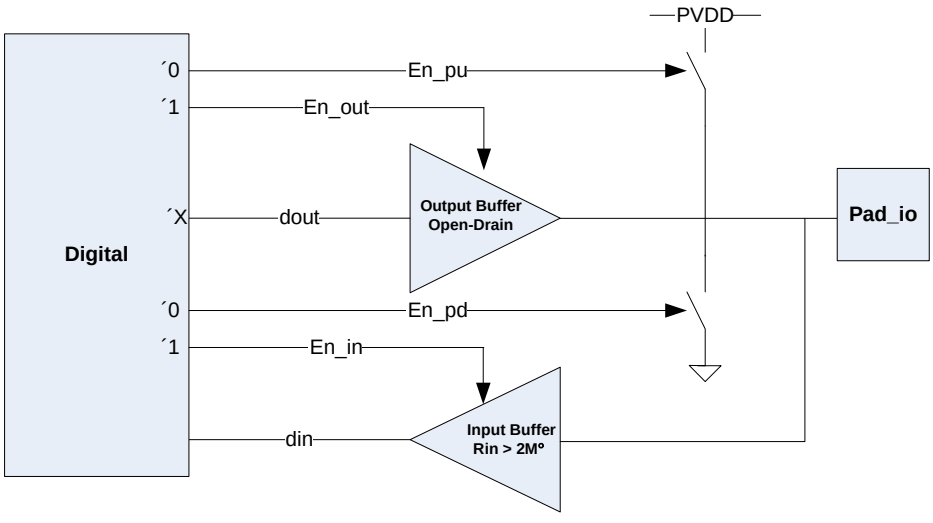


Fig 6. Open-drain

Input

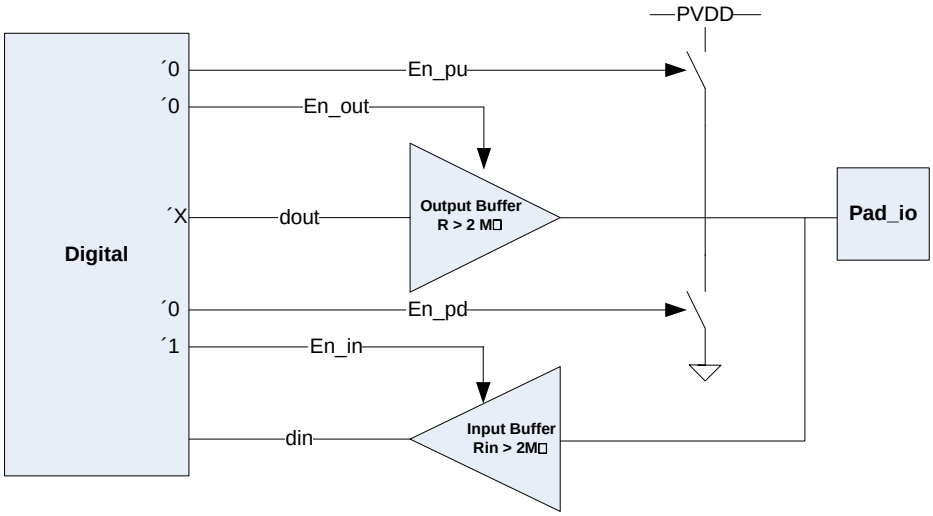


Fig 7. Input

Output

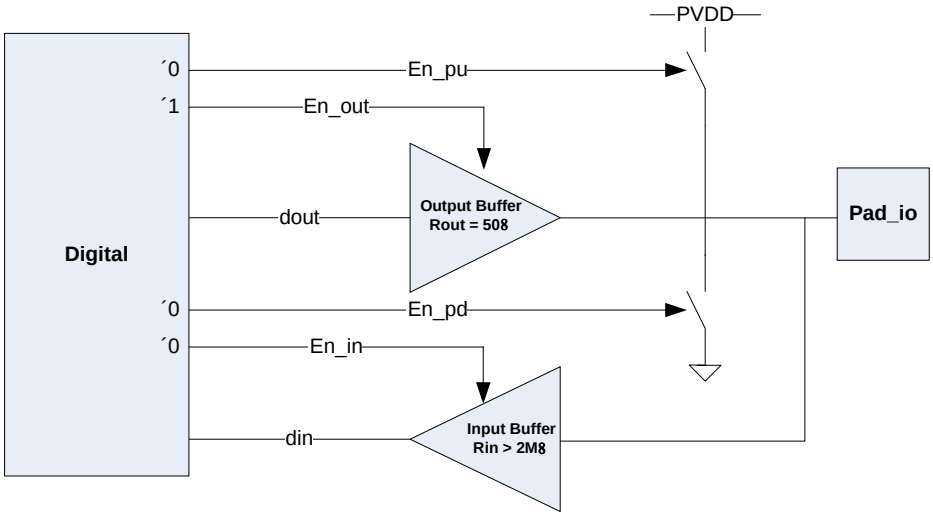


Fig 8. Output

Input Disable

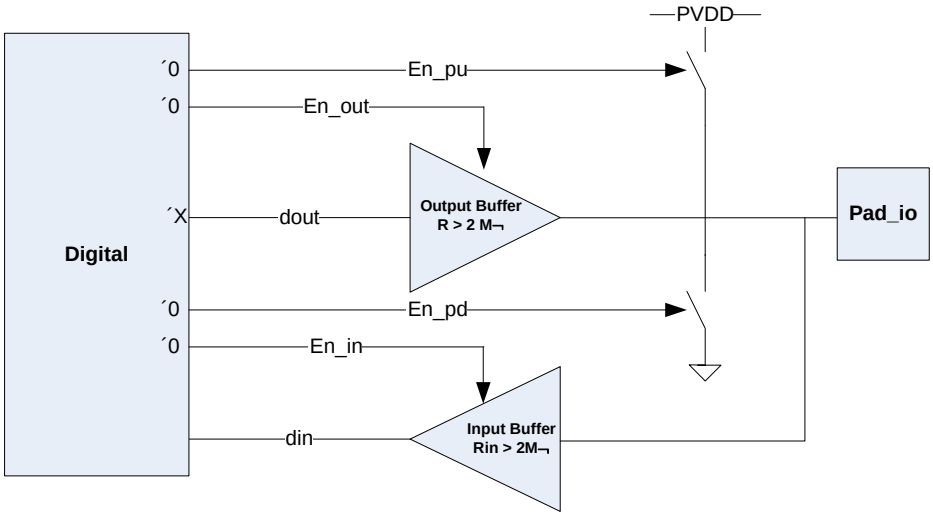


Fig 9. Input Disable (InputDIs)

10.4 Secure element interfaces

The PN544 supports 2 interfaces to be connected to secure element:

- Single Wire Protocol (SWP)
- NFC-WI

10.4.1 SWP interface

The PN544 features ETSI compliant SWP interface towards UICC. The PN544 offers also the possibility to configure SWIO in High Impedance when V_{EN}>1.1V. This could be done via a host command. See Ref. 7 “PN544 User Manual”.

The SWP interface is a bit oriented, point-to-point communication protocol between a UICC and the contactless front end, like the PN544. The PN544 is the master and the UICC is the slave. This interface is based on the transmission of digital information in full duplex mode. The master sends information on the wire in the voltage domain, while the slave sends information back in the current domain.

The PN544 following state machine is implemented in PN544 design:

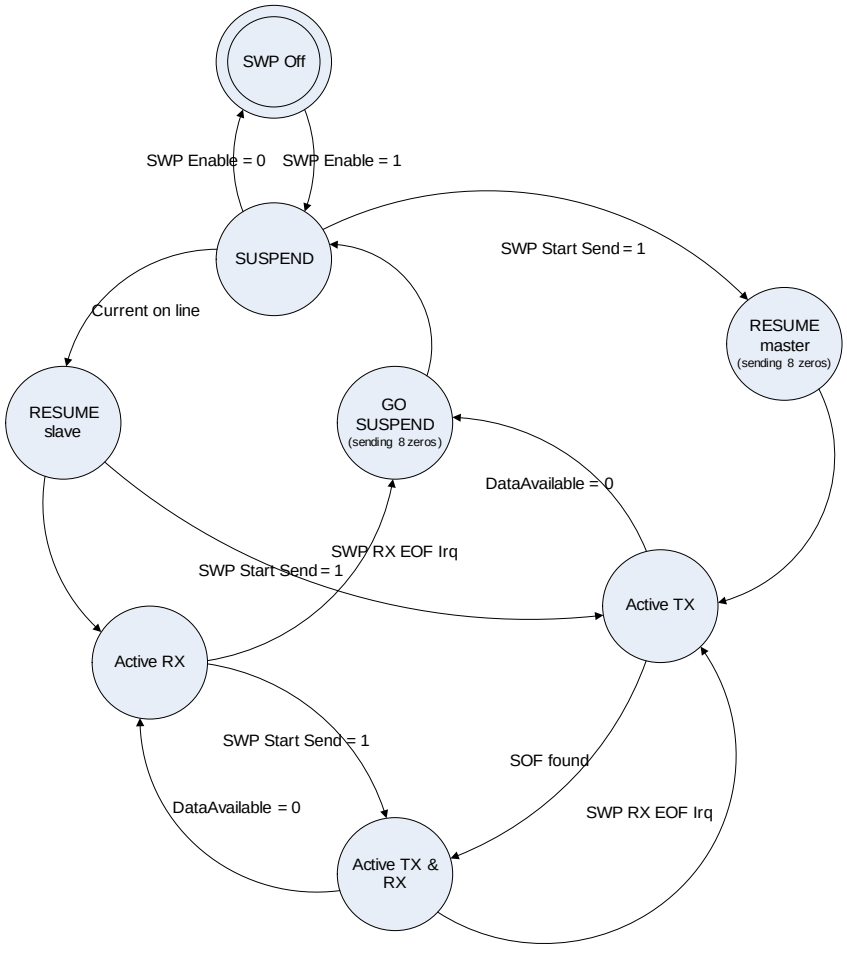


Fig 10. SWP state diagram

PN544 SWP interface implementation features 4 different baud rates:

- 238.1 kbit/s
- 454.5 kbit/s
- 833 kbit/s
- 1.25 Mbit/s (activated by embedded FW if the UICC withstands it, otherwise stays at 833 kbit/s)

The detection threshold on S2 current for the SWP pad is configurable, four values are supported:

- 240 μA
- 260 μA
- 300 μA (default)
- 330 μA

10.4.2 NFC-WI interface support

The NFC-WI provides the possibility to directly connect a secure IC to the PN544 in order to act as a contactless smart card IC via the PN544 at 106kbit/s. The interfacing signals are routed to the pins SIGIN and SIGOUT. SIGIN can receive a digital ISO/IEC 14443A signal sent by the secure IC. The SIGOUT pin can provide a digital signal and a clock to communicate to the secure IC. A secure IC can be provided by NXP Semiconductors.

The following figure outlines the supported communication flows via the PN544 to the secure core IC.

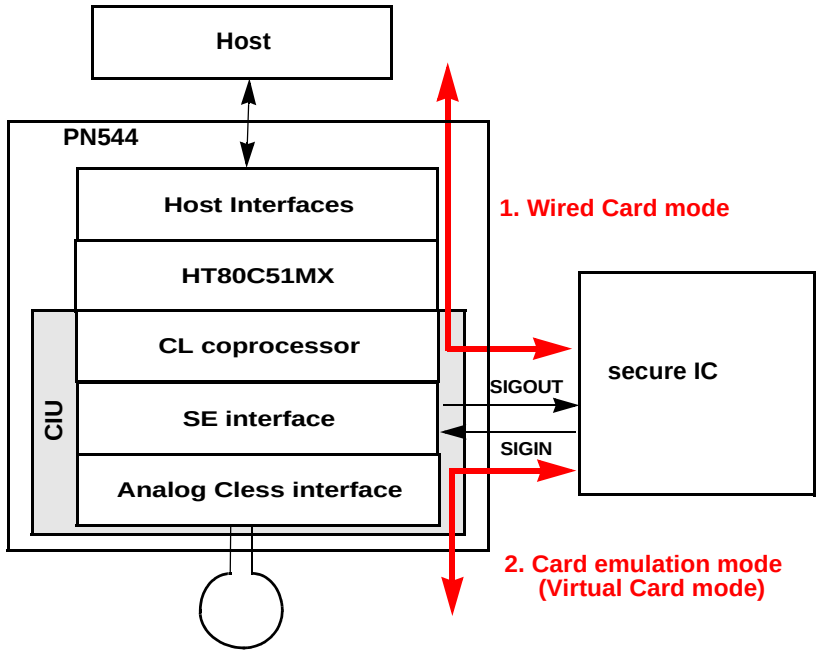


Fig 11. Communication flows supported by the NFC-WI interface

The PN544 generates SV_{DD} to supply the secure IC. The pins SIGIN and SIGOUT are referenced to this supply.

Configured in the Wired Card mode the host controller can directly communicate to the secure IC via SIGIN/SIGOUT. In this mode the PN544 generates the RF clock and performs the communication on the SIGOUT line. To enable the Wired Card mode the clock has to be derived by the internal oscillator or by the FracNPll of the system clock provided by the system.

Configured in Card emulation mode the secure IC can act as contactless smart card IC via the PN544. In this mode the signal on the SIGOUT line is provided by the RF field of the external Reader/Writer. To enable the Virtual Card mode the clock derived by the external RF field has to be used.

The secure IC, e.g. the SmartMX P5CN080, is connected to the PN544 via the pins SIGOUT, SIGIN.

The signal shape for ISO/IEC 14443-A and MIFARE NFC-WI support at SIGOUT is a digital signal at a bit rate of 106 kbit/s between PV_{SS} and SV_{DD}. SIGOUT signal carries the AND combination of the Modified Miller bit coded and the 13.56 MHz carrier. It is either derived from the external RF field signal when in Virtual Card Mode or internally generated when in Wired Card mode.

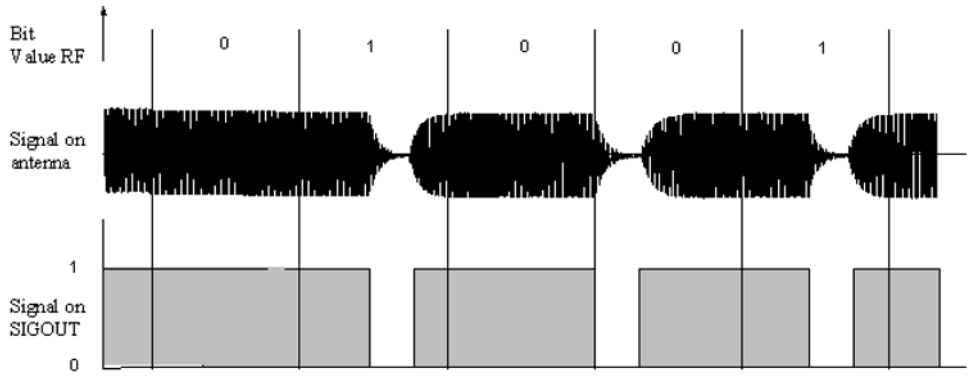


Fig 12. Signal shape for SIGOUT in NFC-WI mode

The signal at SIGIN is a digital Manchester coded signal compliant with ISO/IEC 14443A with a subcarrier frequency of 847.5 kHz generated by the secure IC.

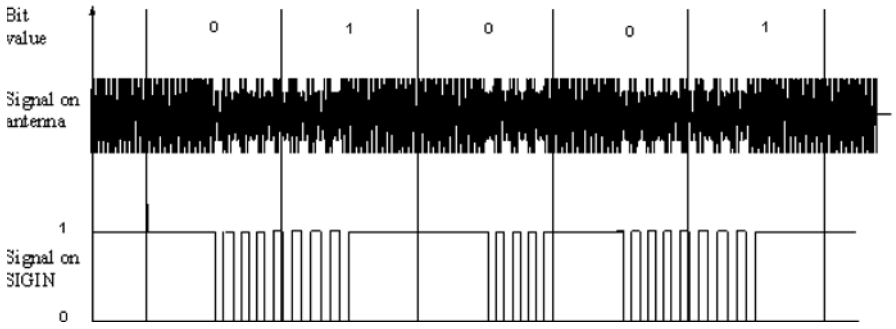


Fig 13. Signal shape for SIGIN in NFC-WI mode

10.5 PN544 clock concept

There are 4 differences clock sources in PN544:

- 27.12 MHz clock coming either/or from:
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated FracNPLL unit
- 13.56 RF clock recovered from RF field
- Low power oscillator 20MHz
- Low power oscillator 333kHz

The Figure 14 describes reference clocks used in PN544.

These sources can be used to clock same blocks depending on functional state of PN544 (Active BAT, Standby, Monitor, Powered by the field...).

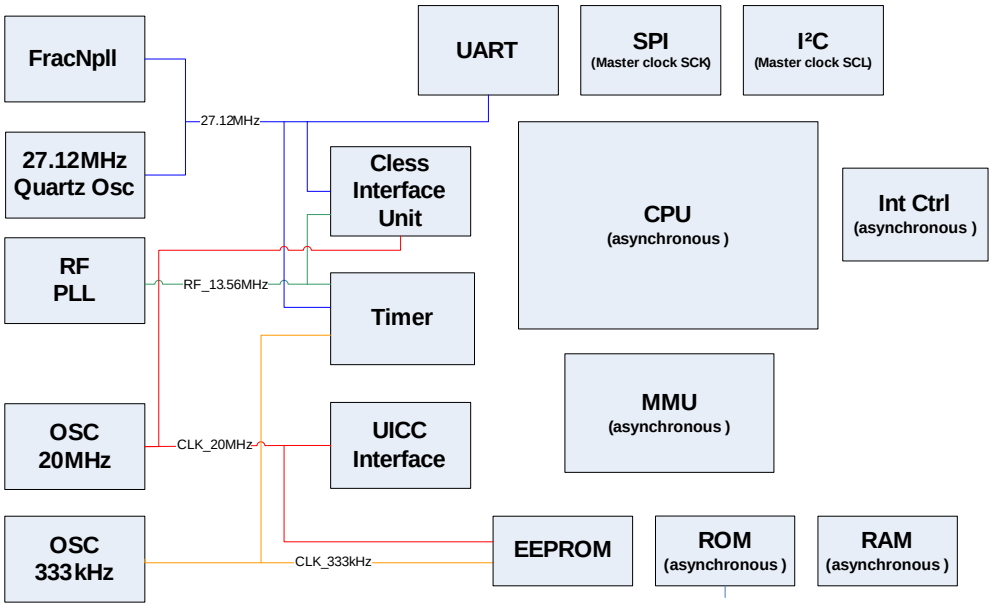


Fig 14. System clock tree

10.5.1 27.12 MHz crystal oscillator

The 27.12 MHz clock applied to the PN544 is the time reference for the RF front-end when PN544 is behaving in reader mode or ISO/IEC 18092 initiator mode.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 15.

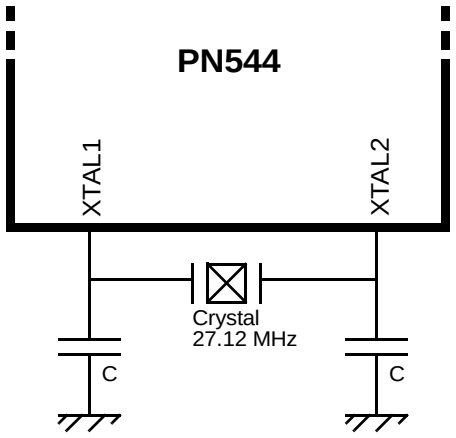


Fig 15. 27.12 MHz crystal oscillator connection

The below table describes the levels of accuracy and stability required on the crystal

Table 25. Crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL}	XTAL frequency		27.107	27.12	27.133	MHz
ESR	Equivalent series resistance			50	100	Ω
C_{LOAD}	Load capacitance			10		pF
P_{XTAL}	Drive level				100	µW

10.5.2 Integrated FracNpll to make use of cellular clock

The FracNpll is designed to generate a low noise 27.12 MHz for an input clock between 10 and 40 MHz.

The 27.12 MHz output of the FracNpll is used as the time reference for the RF front-end when PN544 is behaving in reader mode or ISO/IEC 18092 initiator mode.

Below are characteristics required for Input clock of the FracNpll:

Table 26. Inputs clock requirements of FracNpll

Parameter	Conditions	Min	Typ	Max	Unit
Input frequency		10		40	MHz
Accuracy		-500		500	ppm
Noise floor corner frequency			50		kHz
Noise floor	Offset frequency > 50 kHz			-140	dBc/Hz

Table 26. Inputs clock requirements of FracNpll

Parameter	Conditions	Min	Typ	Max	Unit
peak-peak input voltage		0.2		1.65	V
Duty Cycle		35		65	%
Lock time FracNpll				200	us
Output frequency		27.107	27.12	27.133	MHz
Rise time	20 to 80% of peak-peak input voltage			0.2 × T	s
Falling time	80 to 20% of peak-peak input voltage			0.2 × T	s

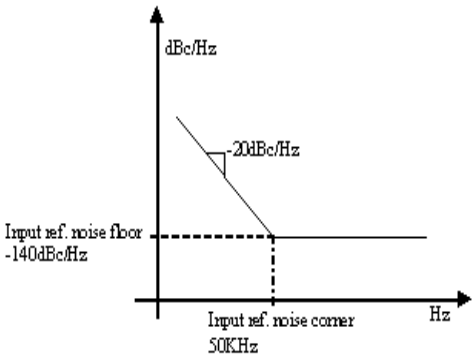


Fig 16. Input reference phase noise characteristics

For configuration of input frequency, please refer to Ref. 7 “PN544 User Manual”.

Please refer to Ref. 7 “PN544 User Manual” and Ref. 9 “PN544 Hardware Design Guide” for detailed description of clock request mechanisms.

10.5.3 Low power 20 MHz oscillator

Low power 20MHz oscillator is used for 3 main purposes:
- Clock SWP block
- Clock Contactless interface sub-block to filter RF spam
- Clock EEPROM memory in READ access

10.5.4 Low power 333 kHz oscillator

A low frequency oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN544 from standby mode.
This allows implementation of low power reader polling loop at application level.
Moreover, this 333 kHz is used as the reference clock for WRITE access to EEPROM memory.

10.6 Supply concept

10.6.1 PN544 supply sources

The PN544 can be supplied from two independent voltage sources: external battery (or similar voltage source) and by the RF field. The functionality used for RF power extraction will be named 'powered by the field' (PbF) in this document. The PbF is an optional feature of PN544 which needs additional external hardware and needs to be enabled via software. If both supply sources are available in the system, PN544 will use both of them concurrently, drawing more current from the stronger one. Simplified working principle is pictured in Figure 17. Both supply sources are connected to PN544's power management unit (PMU), which decides autonomously which one is used to which extent.

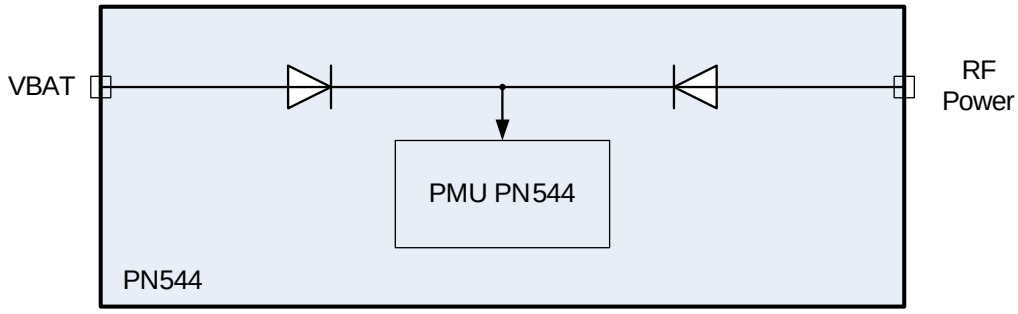


Fig 17. Power sourcing (simplified)

As described in Ref. 9 "PN544 Hardware Design Guide", PN544 monitors battery voltage continuously and will detach PN544 from it once it reaches the specified level. This can occur at any given time. If PbF is not enabled/available, every transaction running at this time will be instantly aborted as battery voltage monitor cuts off PN544 from only available supply. In case PbF is used, PN544 will try to extract total amount of energy needed from the field only, loading it additionally. The completion of transaction cannot be guaranteed under this circumstances as this depends on several factors that can not be influenced by PN544 alone (e.g. antenna design, field strength, transaction content and current state...).

10.6.2 PMU functional description

The Power Management Unit of PN544 generates internal supplies required by PN544 out of VBAT or VDHF inputs supplies:

- AVDD: Analog supply
- DVDD: Digital supply
- VCO_VDD: Analog supply to supply FracNpll
- TVDD: Supply for RF transmitter
- SVDD: Supply of the secure element connected over NFC_WI
- SIMVCC: Supply of the UICC when not directly connected to the mobile PMU

The following functional diagram is describing the main blocks available in PMU:

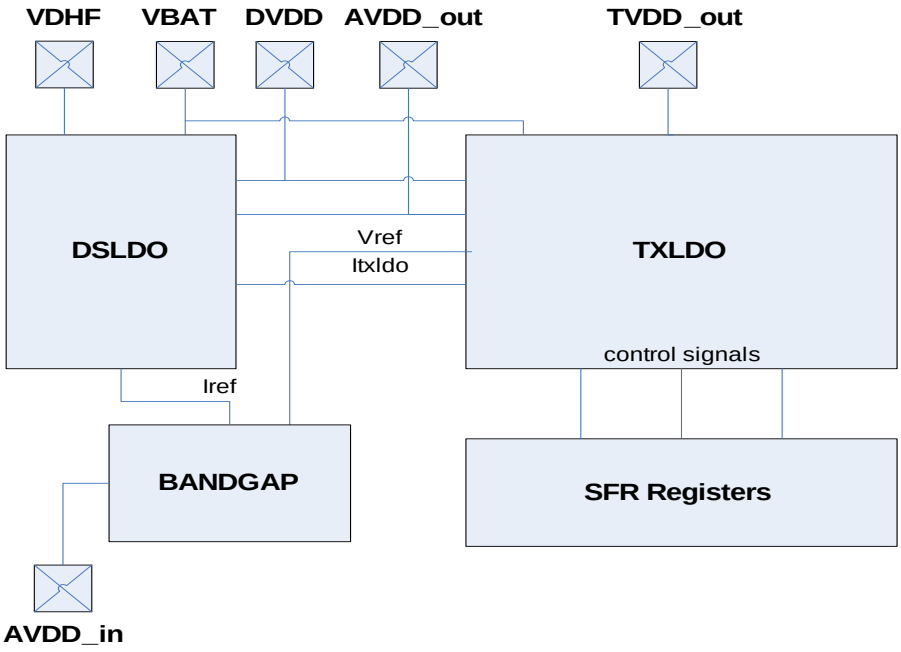


Fig 18. PMU functional diagram

The PN544 PMU design consists on 2main different sub-blocks:

- **DSLDO: Dual supply LDO**

  The Low drop regulator provides different supplies required in the PN544.

  AVDD: Analog supply

  DVDD: Digital supply

  VCO_VDD: Analog supply dedicated to the VCO of the FracNpll

  SVDD: Supply of the secure element

  The inputs of the DSLDO are either VBAT or VDHF.

- **TXLDO**

  This Low drop-out regulator supplies by default TV_{DD} at 3 V. For a battery level above 3 V +Drop-out ~100 mV, the output voltage is stable. When the battery voltage reached ~3.1 V, TV_{DD} follows V_{BAT}.

Those regulators can be disabled. Management of this function is handled by PN544 firmware depending of power states.

10.6.3 Secure element supply

The DS-LDO described above is generating SV_{DD}.

This supply is used to supply secure element connected over NFC-WI.

References of SV_{DD} supply are in Table 1 “Quick reference data” on page 3.

10.6.4 UICC supply

The UICC supply block is in charge to deliver the proper supply for the external UICC and also to provide SWIO data signal.

The following functional diagram is describing the block of UICC interface at phone level:

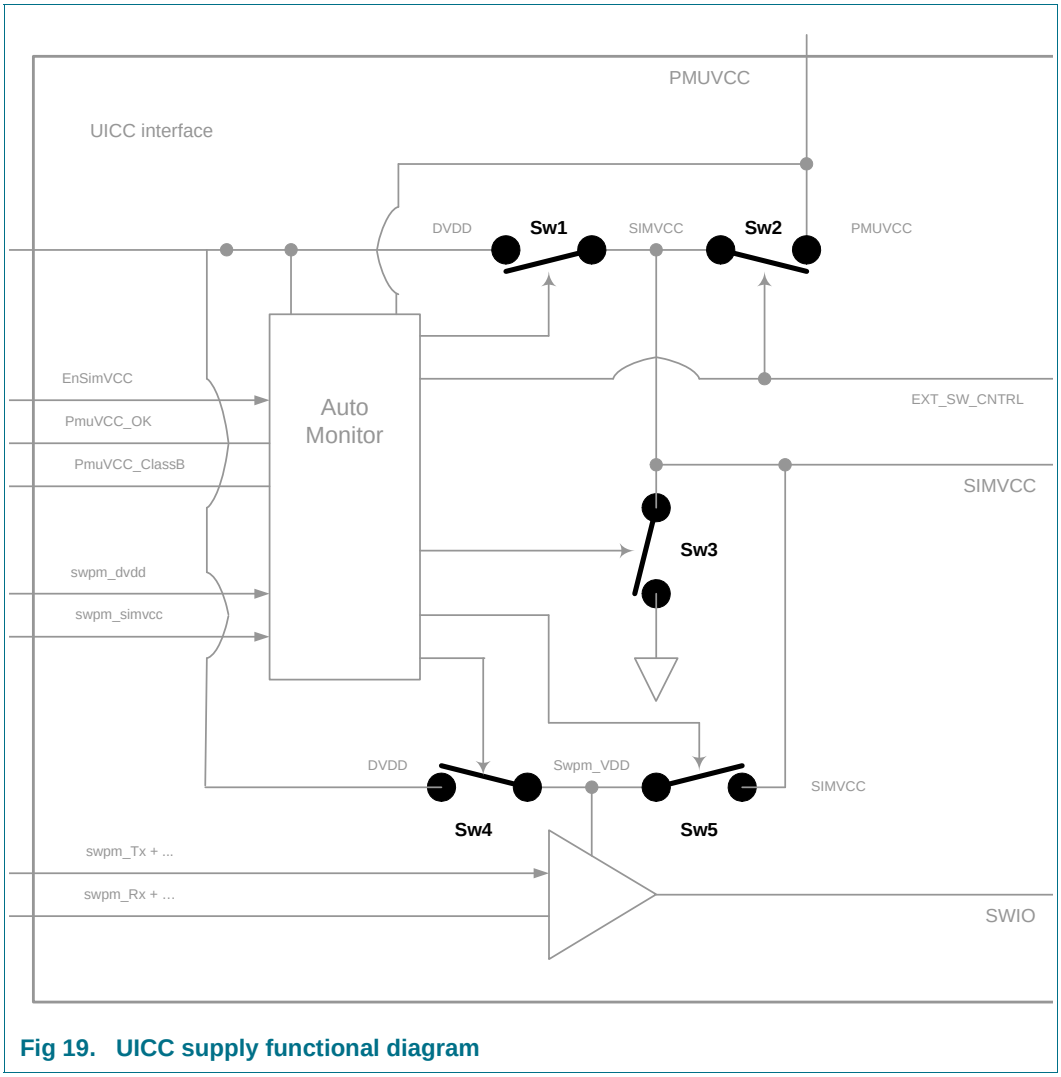


Fig 19. UICC supply functional diagram

At the phone level, a PMU/LDO may be used to generate the UICC supply (VCC) when the phone is active. The voltage can be 1.8 V (class C) or 3 V (class B).

In order to allow contactless transactions in card emulation mode when the battery is too low to allow phone calls but still charged (“powered-down” mode) or in Power-by-the-Field mode (energy extracted from the NFC antenna when the battery is really too low), it is necessary to cut the direct connection between the PMU/LDO output (PMUVCC) and the UICC VCC pin so that the PN544 can also supply the UICC in these specific modes.

Therefore, 2 pins are added on PN544: PMUVCC is connected to the PMU/LDO output while SIMVCC is connected to the UICC VCC pin in order to supply it.

Whatever the mode in which PN544 is, including Hard Power Down (V_{EN} < 1.1V), immediately when $PMUV_{CC}$ rises, $SIMV_{CC}$ will follow $PMUV_{CC}$.

When the phone is OFF (because of a user action or because the battery is too low), the UICC cannot be supplied anymore from the PMU. The PN544 will then supply the UICC thanks to another internal switch which will connect an internal 1.8 V supply to the SIMVCC pin.

The On resistance of the internal switch between PMUVCC and SIMVCC is designed to be below 1.5Ω. If this is too high for a given application, meaning that the voltage drop introduced by the switch is too high to keep the $SIMV_{CC}$ above the ETSI limits, (i.e. 2.7 V in class B and 1.62 V in class C), an external switch can be used to reduce the overall resistance of both switches in parallel. A signal is available on pin EXT_SW_CNTRL to drive the gate of the external switch which has to be made of 2 transistors connected in series in order to cancel the parasitic diodes.

Remark: A possible reference is: FDMA1027P from Fairchild. The switch made with both transistors in series would have then the following max RdsOn: 240 mΩ × 2 = 480 mΩ at VGS = 1.8 V. assuming that the internal switch On resistance is 1500 mΩ, the overall On resistance would be: 363 mΩ.

In order to fulfill the ISO/IEC requirements, an internal switch will also connect $SIMV_{CC}$ to ground when the UICC is not supplied anymore (both internal switches are OFF).

If SWP only is used as an interface to the UICC, it is mandated that the unused pins have a voltage limited to ± 0.4 V with respect to ground. This can be guaranteed by the design of the ISO/IEC 7816 interface on the phone, but only when the battery is charged enough to bias the driver. If not, it is necessary to apply pull-downs on the 3 ISO/IEC 7816 signals (CLK, RST and IO). The PN544 is not capable to permanently apply a pull-down on IO, otherwise the ISO/IEC 7816 interface may be disturbed. A workaround is to drive an external NMOS using the EXT_SW_CTRL pin from the PN544.

The table below describes electrical characteristics of UICC supply as well as SWIO line. The Ron resistors induced by switched are also specified as it has to be taken into account in design application environment.

Table 27. Electrical characteristics of UICC supply and interface

Symbol	Parameter	Conditions	Min.	Nom.	Max.	Unit
$PMUV_{CC}$_Thresh	Threshold on PMUVCC at which $SIMV_{CC}$ is supplied	Ensimvcc = 0	0.3	0.5	0.75	V
ClassB_thresh	Class B detection threshold on PMUVCC		2.2	2.35	2.5	V
$SIMV_{CC}$_DV_{DD}	$SIMV_{CC}$ when supplied by DV_{DD}	I_$SIMV_{CC}$ = 5 mA	1.62		1.98	V
Ron_Sw2_B	Power switch Sw2 RdsOn	$PMUV_{CC}$ = 2.75 V, I_$SIMV_{CC}$ = 50 mA		0.8	1.2	Ω
Ron_Sw2_C	Power switch Sw2 RdsOn	$PMUV_{CC}$ = 1.67 V I_$SIMV_{CC}$ = 30 mA		1	1.5	Ω
Ron_Sw3	Power switch Sw3 RdsOn	DV_{DD} = 1.65 V V_{BAT} = 0 V		600	1000	Ω
Iin_$PMUV_{CC}$_B_0mA	Input current on PMUVCC	$PMUV_{CC}$ = 3 V ± 10% I_$SIMV_{CC}$ = 0 mA		30	45	µA
Iin_$PMUV_{CC}$_C_0mA	Input current on PMUVCC	$PMUV_{CC}$= 1.8V ± 10% I_$SIMV_{CC}$ = 0 mA		20	30	µA
Ich_$SIMV_{CC}$	Charging current on SIMVCC	$SIMV_{CC}$ = 1.0 V $PMUV_{CC}$ = 1.8 V	15	22	30	mA
SWIO_VOH_B	Output High Voltage on SWIO, $PMUV_{CC}$ in class B	I_SWIO = 1 mA I_$SIMV_{CC}$ = 50 mA $PMUV_{CC}$ = 2.75 V	1.4			V
SWIO_VOH_C_ext	Output High Voltage on SWIO, $PMUV_{CC}$ in class C	I_SWIO = 1 mA I_$SIMV_{CC}$ = 30 mA $PMUV_{CC}$ = 1.67 V	0.85 × $SIMV_{CC}$			V
SWIO_VOH_C_int	Output High Voltage on SWIO, $SIMV_{CC}$=DV_{DD}	I_SWIO =1 mA I_$SIMV_{CC}$ = 5 mA $PMUV_{CC}$ = 0 V	0.85 × $SIMV_{CC}$			V
SWIO_VOL	Output low voltage on SWIO	0 µA <I_SWIO < +20 µA			0.3	V
SWIO_IIH_240	Current threshold on SWIO	Target = 240 µA	190	240	290	µA
SWIO_IIH_270	Current threshold on SWIO		220	270	320	µA
SWIO_IIH_300	Current threshold on SWIO		150	300	350	µA
SWIO_IIH_330	Current threshold on SWIO		280	330	380	µA
SWIO_IIH_susp	Current threshold on SWIO	Suspend state	220	270	320	µA

10.6.5 Battery voltage monitor

The PN544 features low power V_{BAT} voltage monitor which protects phone battery from being discharged below critical levels. Refer to Figure 20 for principle schematic.

The battery voltage monitor is enabled via the pin VEN_MON.

The battery voltage monitor consists of ultra low power voltage reference (not depicted), supply switching logic and voltage threshold configuration logic (not depicted). If PN544 is activated by host via VEN pin, the battery voltage monitor is powered and active. When the PN544 monitors battery voltage continuously as long as VEN pin is active and detaches battery supply once the critical level is reached.

If PN544 has been disabled by the host, than the battery voltage monitor is also detached from the battery in order not to consume any power.

In both cases PN544 can be powered by the energy from the field only.

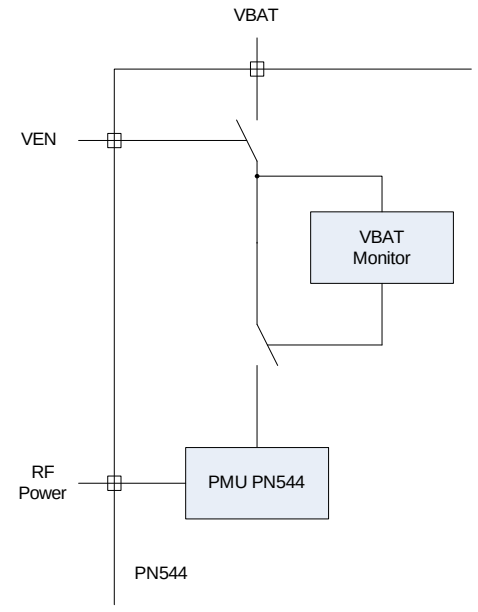


Fig 20. Battery voltage monitor principle

This circuitry is not configurable by application.

The battery voltage monitor threshold value is fixed to 2.6 V.

Table 28. Battery voltage monitor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{THRES}	Threshold voltage	Recommended operating conditions	2.480	2.6	2.720	V
V_{HYST}	Hysteresis voltage	Recommended operating conditions		100		mV

10.7 Contactless interface Unit

The PN544 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Note: All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

10.7.1 Reader/Writer modes

Generally 4 Reader/Writer modes are supported:

- PCD reader/writer for ISO/IEC 14443A/MIFARE
- PCD reader/writer for FeliCa cards
- PCD reader/writer for ISO/IEC 14443B
- VCD reader/writer for ISO/IEC 15693/ICODE.

10.7.1.1 ISO/IEC 14443-A/MIFARE PCD mode

The ISO/IEC 14443-A/MIFARE PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443-A specification.The following diagram describes the communication on a physical level, the communication table describes the physical parameters (the numbers take the antenna effect on modulation depth for higher datarates).

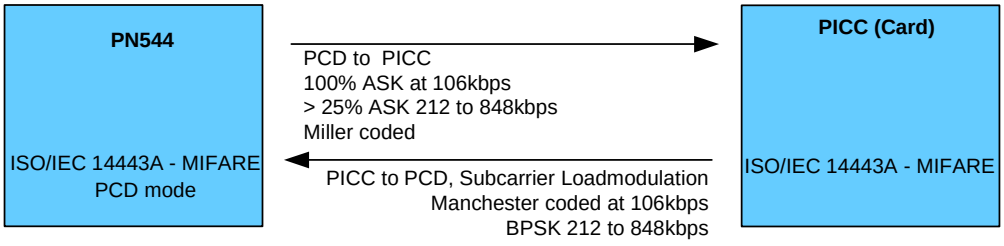


Fig 21. ISO/IEC 14443A/MIFARE Reader/Writer mode communication diagram

Table 29. Communication overview for ISO/IEC 14443A/MIFARE reader/writer

Communication direction		**ISO/IEC 14443A MIFARE**	**ISO/IEC 14443A higher transfer speeds**		
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
PN544 → **PICC** (send data from the PN544 to a card)	Modulation on reader side	100% ASK	>25% ASK	>25% ASK	>25% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PICC → **PN544** (receive data from a card)	Modulation on card side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	Manchester coding	BPSK	BPSK	BPSK

The contactless CoProcessor and the on-chip CPU of the PN544 handle the complete ISO/IEC 14443-A/MIFARE RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.2 FeliCa PCD mode

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The following diagram describes the communication on a physical level, the communication overview describes the physical parameters.

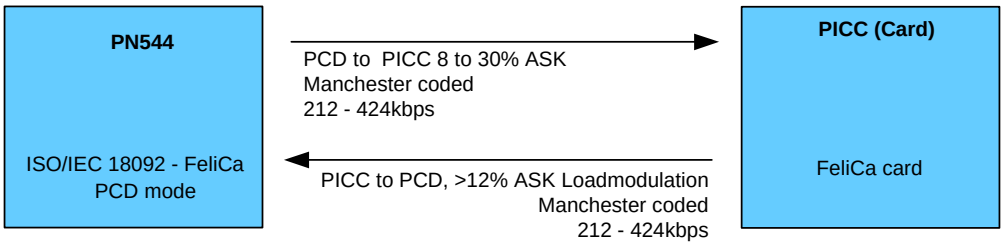


Fig 22. FeliCa reader/writer communication diagram

Table 30. Communication overview for FeliCa reader/writer

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
PN544 → PICC	Modulation on reader side	8 - 30% ASK	8 - 30% ASK
	Bit coding	Manchester Coding	Manchester Coding
	Bit length	(64/13.56) µs	(32/13.56) µs
PICC → PN544	Loadmodulation on card side	>12% ASK	>12% ASK
	Bit coding	Manchester coding	Manchester coding

The contactless CoProcessor of PN544 and the on-chip CPU handle the FeliCa protocol. Nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.3 ISO/IEC 14443B PCD mode

The ISO/IEC 14443-B PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443-B specification.The following diagram describes the communication on a physical level, the communication table describes the physical parameters.

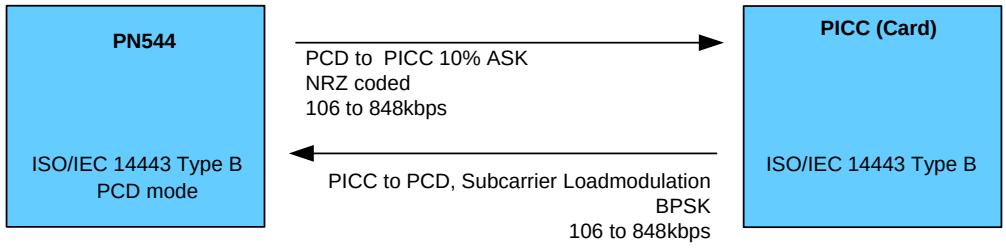


Fig 23. ISO/IEC 14443B reader/writer communication diagram

Table 31. Communication overview for ISO/IEC 14443B reader/writer

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds		
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
PN544 → PICC	Modulation on PN544 side	8-14% ASK	8-14% ASK	8-14% ASK	8-14% ASK
	Bit coding	NRZ	NRZ	NRZ	NRZ
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PICC → PN544	Modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	BPSK	BPSK	BPSK	BPSK

The contactless CoProcessor and the on-chip CPU of the PN544 handle the complete ISO/IEC 14443-B RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.4 ISO/IEC 15693 VCD mode

The ISO/IEC 15693 VCD reader/writer mode is the general reader to card communication scheme according to the ISO/IEC 15693 specification. The PN544 will communicate with VICC using only the higher datarates of the VICC (26.48kbit/s with single subcarrier and 26.69kbit/s with dual subcarrier).

The PN544 supports the commands as defined by the ETSI, and on top offers the inventory of the tags (anticollision sequence) on its own.

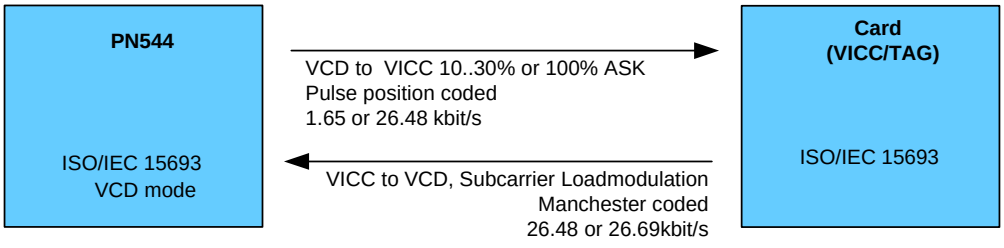


Fig 24. ISO/IEC 15693 VCD mode communication diagram

The following figures shows the communication schemes used. Both TAG to PN544 communication schemes can be used with both PN544 to TAG ones. It gives 4 combinations of communication schemes.

Table 32. Communication overview for ISO/IEC 15693 VCD

Communication direction			
PN544 → VICC	**Transfer speed**	**1.65 kbit/s**	**26.48 kbit/s**
	Modulation on VCD side	10-30% or 100% ASK	10-30% or 100% ASK
	Bit coding	Pulse Position Modulation 1 out of 256 mode	Pulse Position Modulation 1 out of 4 mode
	Bit length	(8192/13.56) µs	(512/13.56) µs
VICC → PN544	**Transfer speed**	**26.48 kbit/s**	**26.69 kbit/s**
	Subcarrier	Single Subcarrier	Dual Subcarrier
	Loadmodulation on VICC side	load modulation amplitude shall be at least 10 mV	
	Bit coding	Manchester coding	

10.7.2 ISO/IEC 18092, ECMA 340 NFCIP-1 operating mode

A NFCIP-1 communication takes place between 2 devices:

- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

The NFCIP-1 communication differentiates between Active and Passive communication modes.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data
- Passive Communication mode means that the Target answers to an Initiator command in a load modulation scheme. The Initiator is active in terms of generating the RF field.

In order to fully support the NFCIP-1 standard the PN544 supports the Active and Passive Communications mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

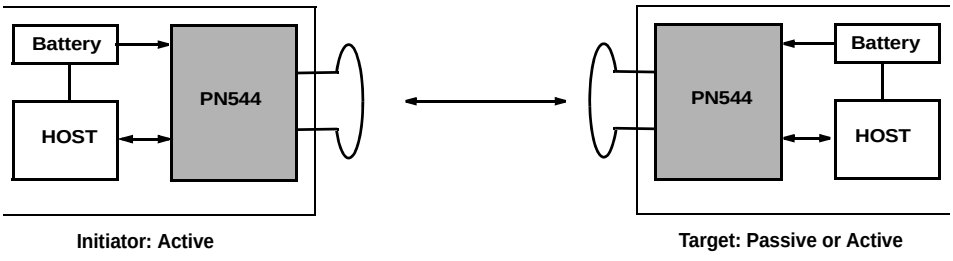


Fig 25. NFCIP-1 mode

The contactless CoProcessor of PN544 and the on-chip CPU handle NFCIP-1 protocol, for all communication modes and data rates, for both Initiator and Target. Nevertheless a dedicated external host has to handle the application layer communication.

10.7.2.1 ACTIVE Communication mode

Active Communication Mode means both the Initiator and the Target are using their own RF field to transmit data.

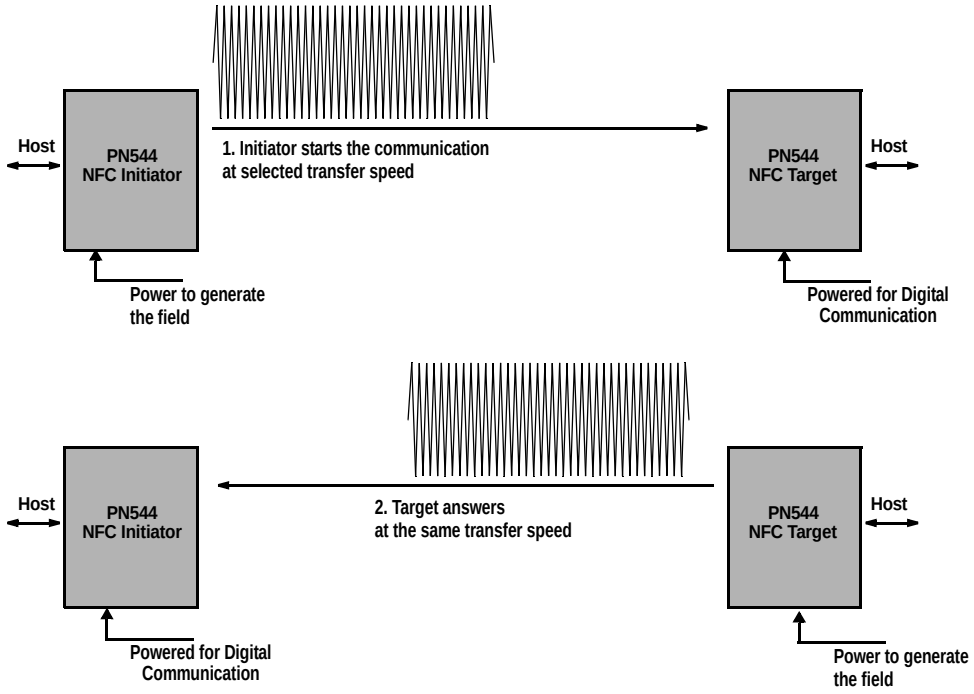


Fig 26. Active NFC mode

The following table gives an overview of the active communication modes:

Table 33. Communication overview for NFC Active Communication mode

Communication scheme		**ISO/IEC 18092, ECMA 340, NFCIP-1**		
Baud rate		**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
Bit length		(128/13.56) μs	(64/13.56) μs	(32/13.56) μs
Initiator to Target	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded
Target to Initiator	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded

10.7.2.2 PASSIVE Communication mode

Passive Communication Mode means that the target answers to an Initiator command in a load modulation scheme.

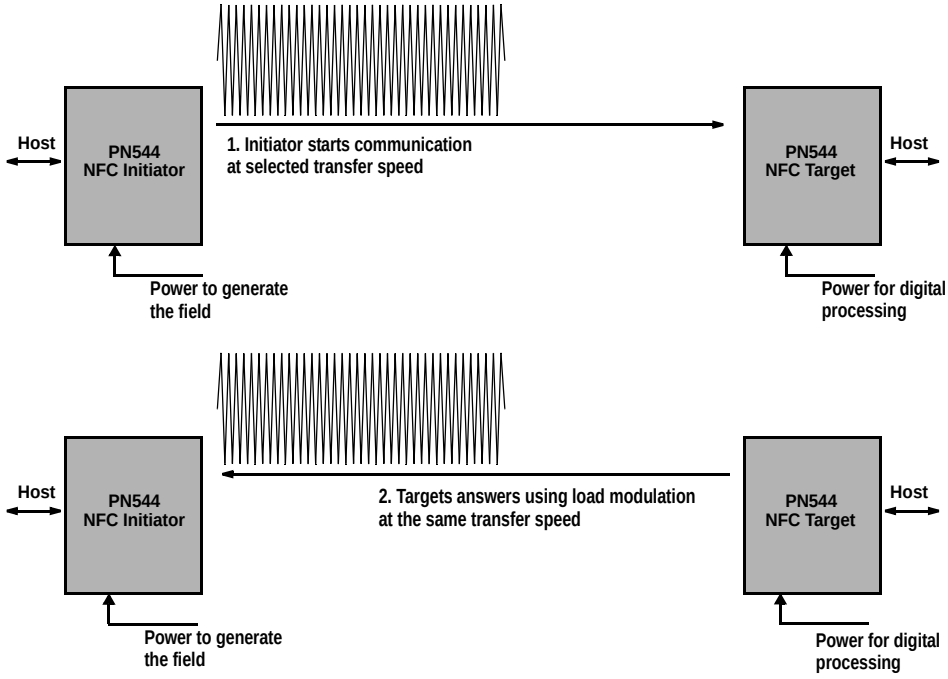


Fig 27. Passive NFC mode

The following table gives an overview of the active communication modes:

Table 34. Communication overview for NFC Passive Communication mode

Communication scheme		**ISO/IEC 18092, ECMA 340, NFCIP-1**		
Baud rate		**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
Bit length		(128/13.56) μs	(64/13.56) μs	(32/13.56) μs
Initiator to Target	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Modified Miller coding	Manchester Coded	Manchester Coded
Target to Initiator	Modulation	Subcarrier load modulation	>12% ASK	>12% ASK
	Subcarrier frequency	13.56 MHz/16	No subcarrier	No subcarrier
	Bit coding	Manchester coding	Manchester coding	Manchester coding

10.7.2.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or ECMA 340.

10.7.2.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the ISO/IEC 18092 or ECMA340 NFCIP-1 standard. However the datalink layer is according to the following policy:

- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction.
- PSL shall be used to change the speed between the target selection and the data transfer, but the speed should not be changed during a data transfer.

10.7.3 Card Operation mode

The PN544 can be addressed as a ISO/IEC 14443 A, MIFARE, ISO/IEC 14443 B or B' cards. This means that the PN544 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A, ISO/IEC 14443B interface description.

MIFARE is supported via NFC-WI or via SWP CLT.

Note: The PN544 does not support a complete card protocol. This has to be handled either by a connected companion secure chip or the host controller.

The following tables describe the physical parameters.

10.7.3.1 ISO/IEC 14443-A / MIFARE Card Operation mode

Table 35. MIFARE Card Operation mode

Communication direction		ISO/IEC 14443A/ MIFARE	ISO/IEC 14443A higher transfer speeds		
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
reader / writer → PN544	Modulation on reader side	100% ASK	> 25% ASK	>25% ASK	>25% ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN544 → reader/ writer	Modulation on PN544 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	Manchester coding	BPSK	BPSK	BPSK

10.7.3.2 ISO/IEC 14443 B and B' Card Operation mode

Table 36. ISO/IEC 14443 B Card Operation mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds		
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
reader / writer → PN544	Modulation on reader side	10% ASK	10% ASK	10% ASK	10% ASK
	Bit coding	NRZ	NRZ	NRZ	NRZ
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN544 → reader/ writer	Modulation on PN544 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	BPSK	BPSK	BPSK	BPSK

11. Application design-in information

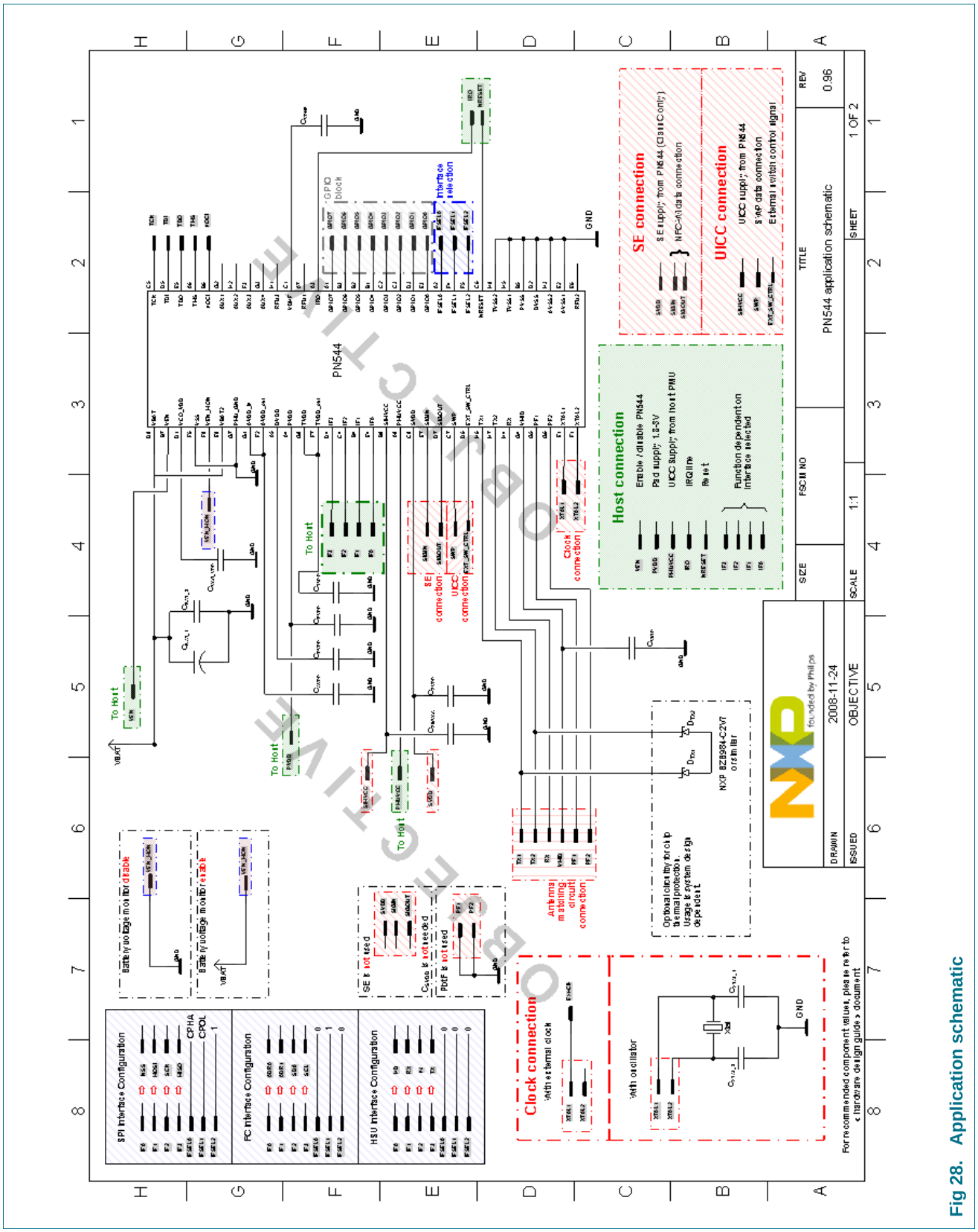


Fig 28. Application schematic

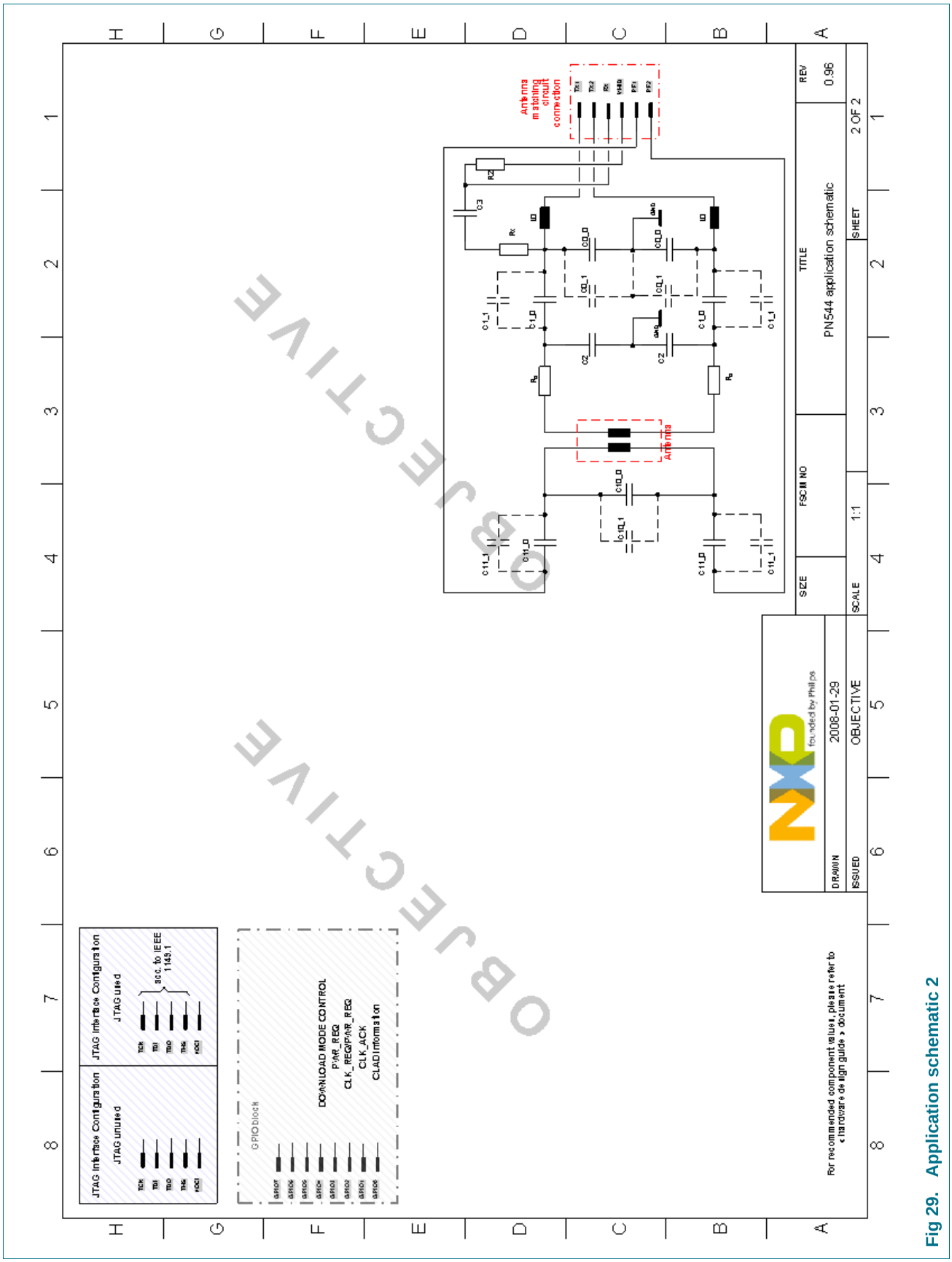


Fig 29. Application schematic 2

12. Limiting values

Table 37. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
PV_{DD}	Pad Supply Voltage			1.65	1.95	V
V_{BAT}	Power Supply Voltage			2.3	5.5	V
P_{tot}	Total power dissipation	Reader mode			<tbd>	mW
I_{TVDD}	Maximum current in TVDD		[1]		100	mA
I_{SVDD}	Maximum current in SVDD switch				30	mA
V_{ESD}	Electrostatic discharge voltage					
V_{ESDH}	ESD Susceptibility (Human Body model)	1500 Ω, 100pF; EIA/JESD22-A114-D			± 1.0	kV
V_{ESDM}	ESD Susceptibility (Human Body model) for RX, TX1, TX2, PF1 and PF2	1500 Ω, 100pF; EIA/JESD22-A114-D			500	V
V_{ESDC}	ESD Susceptibility (Charge Device model)	Field induced model; EIA/JESC22-C101-C			500	V
V_{ESDC}	ESD Susceptibility (Charge Device model) for RX, TX1, TX2, PF1 and PF2	Field induced model; EIA/JESC22-C101-C			300	V
T_{stg}	Storage temperature			-55	150	°C

[1] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

13. Recommended operating conditions

Table 38. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	Ambient Temperature			-30	+25	+85	°C
V_{BAT}	Power Supply Voltage	V_{SS} = 0 V	[1][2]	2.3		5.5	V
PV_{DD}	Supply Voltage for host interface	V_{SS} = 0 V	[1]	1.65	1.8	1.95	V

[1] V_{SS} represents PV_{SS}, DV_{SS}, AV_{SS1}, AV_{SS2}, TV_{SS1}, TV_{SS2}.

[2] Supply voltage of V_{BAT} below 3.6 V can reduce the performance in reader/writer mode (e.g. the achievable operating distance).

14. Thermal characteristics

Table 39. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{thj-a}	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer Jedec PCB-0.5		<tbd>	<tbd>	K/W

15. Characteristics

15.1 Current consumption characteristics

Table 40. Current consumption characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{HPD}	Hard-Power-down current	V_{BAT} = 3 V, V_{EN}= 0 V	[5]		<tbd>	5	µA
I_{SPD}	Standby mode current	V_{BAT} = 3 V	[5]		<tbd>	50	µA
I_{MON}	Monitor mode current	V_{BAT} = 3 V				10	µA
I_{PVDD}	Pad supply current	PV_{DD} = 1.8 V	[2]			<tbd>	mA
I_{SVDD}	Output supply current	sam_switch_en set to 1	[3]			30	mA
I_{TVDD}	Transmitter supply current	Continuous wave, TV_{DD} = 3 V	[1][4]		60	100	mA
I_{PMU_VCC}	PMU_VCC supply current	Class B, no SWP activity	[6]		30	45	µA
I_{PMU_VCC}	PMU_VCC supply current	Class C, no SWP activity	[6]		20	30	µA

[1] I_{TVDD} depends on TV_{DD} and the external circuitry connected to Tx1 and Tx2.

[2] I_{PVDD} is given for maximum host interface speed, all other pins DC biased, outputs loaded with more than 100kΩ

[3] I_{SVDD} depends on the overall load on S_{VDD} pad.

[4] During operation with a typical circuitry the overall current is below 100 mA.

[5] I_{SPD} and I_{HPD} are the total currents over all supplies.

[6] When SWP is activated in class C, the SWIO pin current of 1.1mA peak shall be added. And in both classes the UICC current shall be added if the UICC is connected to SIMVCC. These values are defined in the ETSI 102 221 standard.

15.2 Functional block electrical characteristics

15.2.1 Battery voltage monitor characteristics

Table 41. Battery voltage monitor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{THRES}	Threshold voltage		2.48	2.6	2.72	V
V_{HYST}	Hysteresis voltage			100		mV

15.3 Pin characteristics

15.3.1 XTAL pin characteristics (XTAL1, XAL2)

Table 42. Pin characteristics for 27.12 MHz XTAL Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{inXTAL1}$	XTAL1 Input Capacitance	AV_{DD} = 1.8 V, VDC = 0.65 V, VAC = 0.9 Vpp		2		pF
$V_{IHXTAL1}$	High level input voltage			1.8		V
$V_{OLXTAL1}$	Low level input voltage			0		V
$V_{OHXTAL2}$	High level output voltage			1.1		V
$V_{OLXTAL2}$	Low level output voltage			0.2		V
$C_{inXTAL2}$	XTAL2 Input Capacitance			2		pF

[1] See the Figure 28 “Application schematic” on page 50 for example of appropriate connected components. The layout should ensure minimum distance between the pins and the components

15.3.2 VEN and VEN_MON input pin characteristics

Table 43. VEN input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.1		V_{BAT}	V
V_{IL}	Low level input voltage		0		0.4	V
I_{IH}	High level input current	$V_I = V_{BAT}$			1	µA
I_{IL}	Low level input current	V_I = 0 V	-1			µA
C_{in}	Input capacitance			<tbd>		pF

15.3.3 NRESET input pin characteristics

Table 44. NRESET input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage		0.7 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level input voltage		0		0.3 × PV_{DD}	V
I_{IH}	High level input current	$V_I = PV_{DD}$			1	µA
I_{IL}	Low level input current	V_I = 0 V; Remark: Current due to internal pull-up	-15		-50	µA
C_{in}	Input capacitance			<tbd>		pF

15.3.4 Output pin characteristics for IRQ

Table 45. Output pin characteristics for IRQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	I_{OH} = -100 µA	PV_{DD}-0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL} = -100 µA	0		0.2	V
I_{IH}	High level input current	$V_I = PV_{DD}$ Pad in high Z			1	µA
I_{IL}	Low level input current	V_I = 0 V; Pad in high Z	-1			µA
C_{in}	Output Capacitance				5	pF
C_L	Load Capacitance				20	pF
$t_{rise,fall}$	Rise and fall times	maximum for CLmax = 20 pF slew rate disable slew rate enable		<tbd>	 15 30	ns

15.3.5 Pin characteristics for GPIOs, IF0 and IF1

Table 46. Pin characteristics for GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, IFSEL0, IFSEL1, IFSEL2, IF0, IF1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.7 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.3 × PV_{DD}	V
V_{OH}	High level output voltage	I_{OH} < 100 µA	PV_{DD} -0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL} < 100 µA	0		0.2	V
I_{IH}	High level input current	$V_I = PV_{DD}$; Pad in high Z			1	µA
I_{IL}	Low level input current	V_I = 0 V; Pad in high Z	-1			µA
C_{IN}	Input capacitance				<tbd>	pF
C_{OUT}	Load capacitance				20	pF

15.3.6 Pin characteristics for IF2, IF3

Table 47. Pin characteristics for IF2 and IF3 configured as I²C pads

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.7 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.3 × PV_{DD}	V
V_{OH}	High level output voltage	I_{OH} < 100 µA	PV_{DD} -0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL} < 100 µA	<tbd>		<tbd>	V
I_{IH}	High level input current	V_I = PV_{DD}; Pad in high Z			1	µA
I_{IL}	Low level input current	V_I = 0 V; Pad in high Z	-1			µA
C_{IN}	Input capacitance				10	pF
C_{OUT}	Load capacitance		10		400	pF
TSP	Width of suppressed spikes	Not in HS mode			50	ns

[1] Pins IF2 and IF3 have two pads connected to one package pin. Therefore, the electrical characteristics of those pads differ from other digital pins

Table 48. Pin characteristics for IF2 and IF3 not used as I²C pads

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.7 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.3 × PV_{DD}	V
V_{OH}	High level output voltage	I_{OH} < 100 µA	PV_{DD} -0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL} < 100 µA	0		0.2	V
I_{IH}	High level input current	V_I = PV_{DD}; Pad in high Z			1	mA
I_{IL}	Low level input current	V_I = 0 V; Pad in high Z	-1			mA
C_{IN}	Input capacitance				<tbd>	pF
C_{OUT}	Load capacitance				20	pF

15.3.7 SWIO pin characteristics

Table 49. Electrical characteristics of SWIO

Symbol	Parameter	Conditions	Min.	Nom.	Max.	Unit
V_{OH} class B	Output High Voltage on SWIO, $PMUV_{CC}$ in class B	I_SWIO = 1 mA I_$SIMV_{CC}$ = 50 mA $PMUV_{CC}$ = 2.75 V	1.4			V
V_{OH} class C external	Output High Voltage on SWIO, $PMUV_{CC}$ in class C	I_SWIO = 1 mA I_$SIMV_{CC}$ = 30 mA $PMUV_{CC}$ = 1.67 V	0.85 × $SIMV_{CC}$			V
V_{OH} class C internal	Output High Voltage on SWIO, $SIMV_{CC}$ = DV_{DD}	I_SWIO = 1 mA I_$SIMV_{CC}$ = 5 mA $PMUV_{CC}$ = 0 V	0.85 × $SIMV_{CC}$			V
V_{OL}	Output low voltage on SWIO	0 µA < I_SWIO < +20 µA			0.3	V
I_{IH}_240	Current threshold on SWIO	Target = 240 µA	190	240	290	µA
I_{IH}_270	Current threshold on SWIO		220	270	320	µA
I_{IH}_300	Current threshold on SWIO		150	300	350	µA
I_{IH}_330	Current threshold on SWIO		280	330	380	µA
I_{IH}_susp	Current threshold on SWIO	Suspend state	220	270	320	µA
I_{leak}	Leakage current	High Impedance			<tbd	µA

[1] To allow for overshoot the voltage on SWIO shall remain between -0,3 V and $V_{OH\ max}$ + 0,3 V during dynamic operation

Table 50. S1 waveform timings

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
t_F	Fall time	CLOAD < 50 pF[2]	5 ns	-	0.05 × T	
		T < 5000 ns				
		CLOAD < 50 pF[2]	5	-	250	ns
		T > 5000 ns				
t_R	Rise time	CLOAD < 50 pF[2]	5 ns	-	0.05 × T[1]	
		T < 5000 ns				
		CLOAD < 50 pF[2]	5	-	250[1]	ns
		T > 5000 ns				
T_{H1}	Duration of the state H for coding a logical 1 of S1		0.70 × T	0.75 × T	0.80 × T	
T_{H0}	Duration of the state H for coding a logical 0 of S1		0.20 × T	0.25 × T	0.30 × T	
T	Bit duration[3]	@ 238.1 kbit/s	3.907		4.54	µs
T	Bit duration[3]	@ 454.5 kbit/s	2.047		2.379	µs
T	Bit duration[3]	@ 833 kbit/s	1.117		1.298	µs
T	Bit duration[3]	@ 1.25 Mbit/s	0.744		0.865	µs

[1] Valid for the leading edge and the trailing edge of each bit

[2] Load capacitance is different then specified in ETSI to include capacitance of the connector and routing towards UICC

[3] This is compatible with Extended bit durations as defined in ETSI TS 102 613

15.3.8 Output pin characteristics for EXT_SW_CTRL

Table 51. Output pin characteristics for EXT_SW_CTRL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	I_{OH} < 100 µA	$SIMV_{CC}$ - 0.1		$SIMV_{CC}$	V
V_{OL}	Low level output voltage	I_{OL} < 100 µA	0		0.1	V
C_{out}	Load Capacitance				2	nF

15.3.9 Input pin characteristics for SIGIN

Table 52. Input/output pin characteristics for SIGIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage	1.65 < SV_{DD} < 1.95	1.1		SV_{DD}	V
V_{IL}	Low level Input voltage		0		0.7	V
I_{IH}	High level input current	V_I = SV_{DD}; Pad in high Z;			1	µA
I_{IL}	Low level input current	V_I = 0 V; Pad in high Z;	-1			µA
C_{in}	Input Capacitance			<tbd>		pF

15.3.10 Output pin characteristics for SIGOUT

Table 53. Output pin characteristics for SIGOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	DV_{DD} - 0.1 < SV_{DD} < DV_{DD} I_{OH} < 1 mA	SV_{DD} - 0.4		SV_{DD}	V
V_{OL}	Low level output voltage	DV_{DD} - 0.1 < SV_{DD} < DV_{DD} I_{OL} < 1 mA	0		0.2	V
I_{IH}	High level input current	Pad in high Z V_I = SV_{DD}			1	µA
I_{IL}	Low level input current	Pad in high Z; V_I = 0 V;	-1			µA
C_{in}	Input Capacitance			<tbd>		pF
C_{out}	Load Capacitance				30	pF
$t_{rise,fall}$	Rise and fall times	Between 10% to 90% SV_{DD} level C_{out} = 30 pF			12	ns

15.3.11 Output pin characteristics for AUX1/AUX2/AUX3/AUX4

Table 54. Output pin characteristics for AUX1/AUX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	AV_{DD} = 1.8 V, I_{OH} = -100 µA	AV_{DD} - 0.2		AV_{DD}	V
V_{OL}	Low level output voltage	AV_{DD} = 1.8 V, I_{OL} = 100 µA	0		0.2	V
I_{IH}	High level input current	V_I = DV_{DD}; Pad in High Z			1	µA
I_{IL}	Low level input current	V_I = 0; Pad in High Z	-1			µA
C_{in}	Input Capacitance			<tbd>		pF
C_{out}	Load Capacitance				15	pF

15.3.12 Input pin characteristics for RX

Table 55. Input pin characteristics for RX

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{INRX}	Dynamic Input voltage Range	AV_{DD} = 1.8 V		0		AV_{DD}	V
C_{inrx}	RX Input Capacitance			<tbd>	<tbd>	<tbd>	pF
R_{inrx}	RX Input Series resistance	AV_{DD} = 1.8 V Receiver active, V_{RX} = 1 Vpp, 0.9 V DC offset			<tbd>		Ω
$V_{RX,MinIV,CM}$	Minimum Input voltage for Card Mode	106 kbit/s	[2]		150		mVpp
$V_{RXMod,RM}$	Minimum modulation voltage, Reader Mode	<tbd>(gain settings)	[1]		5		mV

[1] The minimum modulation voltage is valid for reader mode. It corresponds to the baseband signal amplitude after carrier is removed

[2] Minimum Voltage required such that Miller, Type B and FeliCa type commands can be decoded when modulation is according to ISO/IEC specs

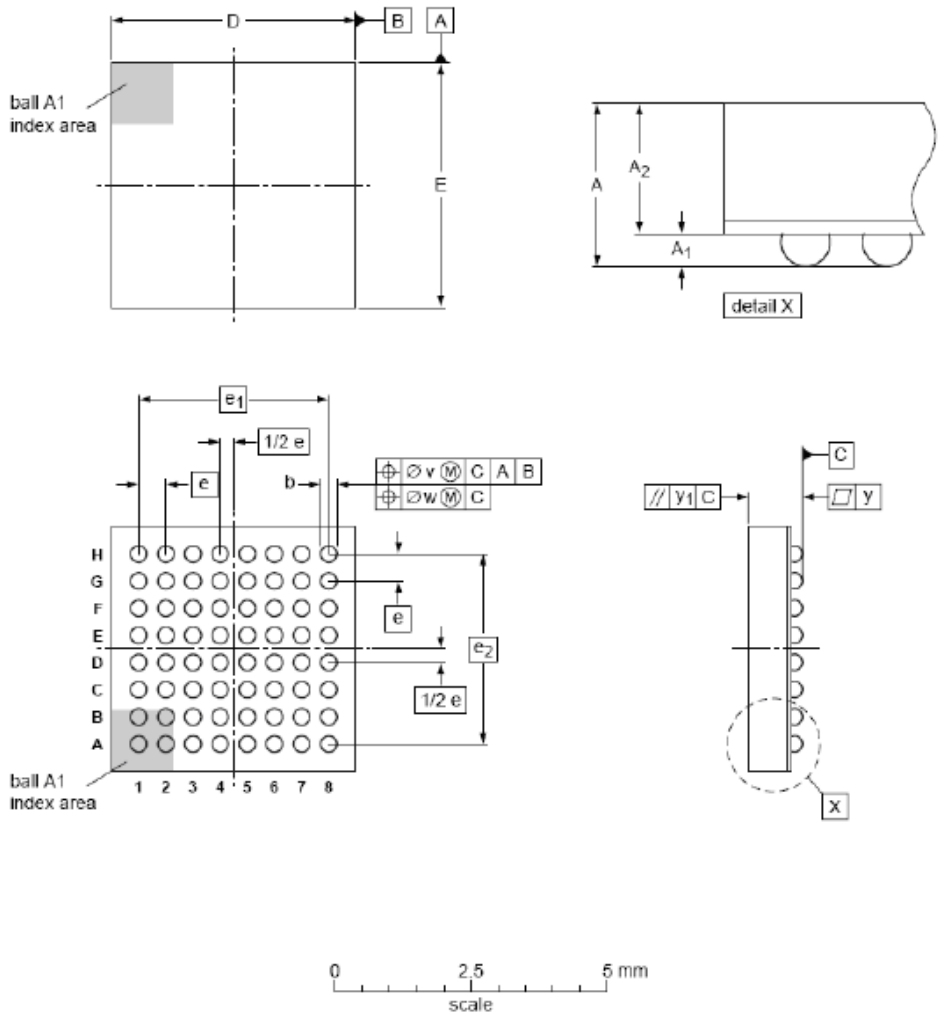
15.3.13 Output pin characteristics for TX1/TX2

Table 56. Output pin characteristics for TX1/TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH, C32, 3 V}$	High level output voltage	TV_{DD} = 3 V and I_{TX} = 30 mA, PMOS fully on	TV_{DD} - 150			mV
$V_{OL, C32, 3 V}$	Low level output voltage	TV_{DD} = 3 V and I_{TX} = 30 mA, NMOS fully on			150	mV

16. Package outline

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls; body 4.5 x 4.5 x 0.8 mm **SOT962-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.1	0.25 0.15	0.85 0.75	0.35 0.25	4.6 4.4	4.6 4.4	0.5	3.5	3.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT962-1	---	---	---			~~06-07-07~~ 06-08-01

Fig 30. Package outline SOT962-1

17. Abbreviations

Table 57. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
Automatic anticollision	Detect and recognize requests from any NFC initiator or reader/writer device, like NFC-Target, ISO/IEC 14443, Type A PICC (identical to NFC -Target) or ISO/IEC 14443, Type B PICC
Automatic device discovery	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and UltraLight PICC, ISO/IEC 15693 VICC
Autonomous tag communication	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and UltraLight PICC, ISO/IEC 15693 VICC
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
Loadmodulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) measured at the card's coil.
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin).
MISO	Master In Slave Out (for SPI interface)
MOSI	Master Out Slave In (for SPI interface)
NFC-WI	Near Field Communication - Wired Interface
NSS	Not Slave Select (for SPI interface)
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO/IEC 14443 specification or MIFARE.
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443 specification or MIFARE.
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification or MIFARE.
PICC emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller.
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443 specification or MIFARE.
Powered by the field mode	A contactless device supports powered-by-the-field mode if it is capable of performing PICC emulation mode transactions while extracting the required power from the electromagnetic RF-field generated by a coupled PCD. Example: contactless plastic smart cards.
SCK	Serial Clock (for SPI interface)
SPI	Serial Peripheral Interface
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).
VCD	Vicinity Coupling Device. Definition for a reader/writer device according to the ISO/IEC 15693 specification.

18. References

[1] **ETSI SWP —** TS 102 613 V7.3.0

[2] **ETSI HCI —** TS 102622 V7.2.0

[3] **ISO/IEC 14443 —** parts 2: 2001 COR 1 2007 (01/11/2007), part 3: 2001 COR 1 2006 (01/09/2006) and part 4: 2nd edition 2008 (15/07/2008)

[4] **ISO/IEC 28361 (NFC-WI) —** 1st edition, 01/10/2007

[5] **I^2C Specification —** I^2C Specification, Version 2.1, January 2000, **http://test.com/**

[6] **SPI —**

[7] **PN544 User Manual —**

[8] **PN544 Application Schematic —**

[9] **PN544 Hardware Design Guide —**

[10] **PN544 Antenna Design Guide —**

[11] **ISO/IEC 18092 (NFC-IP1) —** 1st edition, 01/04/2004

[12] **ISO/IEC15693 —** part 2: 2nd edition (15/12/2006), part 3: 1st edition (01/04/2001)

19. Revision history

Table 58. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
155221	10 December 2008	Objective data sheet		155220
Modifications:	• Figure 3 “PN544 block diagram” on page 5: ESD HBM update • Table 4 “PN544 Pin description” on page 6: renamed PWR_RFU to **VBAT2** • Table 16 “Host pin state in active antenna mode” on page 17: corrected host interfaces of GPIO2, GPIO4 and IRQ: InputDis -> **InputDis - Pull down** • Table 19 “IF0-3 functionality for HSU interface” on page 20: rewording functionality of pin IF0			
155220	23 October 2008	Objective data sheet		155210
155210	14 May 2008	Objective data sheet		
Modifications:	• Initial version			

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20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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