

Power Semiconductor Diodes and Transistors

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A low-power diode, called signal diode, is a *p-n* junction device. A high-power diode, called power diode, is also a *p-n* junction device but with constructional features somewhat different from a signal diode. Likewise, power transistors also differ in construction from signal transistors.

The voltage, current and power ratings of power diodes and transistors are much higher than the corresponding ratings for signal devices. In addition, power devices operate at lower switching speeds whereas signal diodes and transistors operate at higher switching speeds.

Power semiconductor devices are used extensively in power-electronic circuits. Some applications of power diodes include their use as freewheeling diodes, for ac to dc conversion, for recovery of trapped energy etc. Power transistors, used as a switching device in power-electronic circuits, must operate in the saturation region in order that their on-state voltage drop is low. Their applications as switching elements include dc choppers and inverters.

The object of this chapter is to describe power diodes, power transistors and MOS-controlled thyristor (MCT). A thyristor is more important component of power semiconductor devices, it is, therefore, discussed in detail in Chapter 4.

2.1 THE p-n JUNCTION

A *p-n* junction forms the basic building block of all power semiconductor devices. It is, therefore, worthwhile here to review this junction at an introductory level.

A *p-n* junction is formed when *p*-type semiconductor is brought in metallurgical, or physical, contact with *n*-type semiconductor. A *p*-region has greater concentration of holes whereas *n*-region has more electron-concentration. In *p*-region, free holes are called majority carriers and free electrons minority carriers. In *n*-region, free electrons are called majority carriers whereas free holes are called minority carriers.

Doping densities in *p* and *n* type semiconductors may be different. As such, *p*-type material may be designated p^+ , p or p^- ; similarly *n*-type material as n^+ , n^- etc. Rough guidelines for labelling of *p* as p^+ , p^- etc and *n* as n^- , n^+ etc are as under :

(a) If doping (or acceptor) density in *p*-type semiconductor = doping (or donor) density in *n*-type semiconductor, then it is called *p-n* junction. For example, if doping density in both *p* and *n* layers is about 10^{16} cm^{-3} to 10^{17} cm^{-3} , junction is termed *p-n* junction.

(b) If doping density in *p*-region is much greater than that in *n*-region, it is called $p^+ n$ junction. For example, if doping densities are 10^{19} cm^{-3} in *p* layer and 10^{17} cm^{-3} in *n* layer, then it is termed $p^+ n$ junction.

(c) If doping density in *n*-type is less than that given in part (b), the junction is called $p^+ n^-$ junction. For example, if doping densities are 10^{19} cm^{-3} and 10^{13} cm^{-3} for *p* and *n* types respectively, then $p^+ n^-$ junction is formed.

(d) If both *p* and *n*-layers are heavily doped, it is called $p^+ n^+$ junction and if very lightly doped, a $p^- n^-$ junction is formed. For example, if density is 10^{19} cm^{-3} in both *p* and *n* layers, $p^+ n^+$ junction is formed.

In general, p^+ indicates highly doped *p* region, n^- lightly doped *n* region and so on.

2.1.1 Depletion Layer

When physical contact between *p* and *n* regions is made, free electrons in *n* material diffuse across the junction into *p* material, Fig. 2.1 (a). Diffusion of each electron from *n* to *p*, leaves a positive charge behind in the *n*-region near the junction. Similarly, diffusion of each hole from *p* to *n*, leaves a negative charge behind in the *p* region near the junction. As a result of this diffusion, *n* region near the junction becomes positively charged and *p* region in the vicinity of junction becomes negatively charged, Fig. 2.1 (b). These charges establish an electric field across the junction. When this field grows strong enough, it stops further diffusion. Some electrons, as these diffuse from *n* to *p*, recombine with holes in *p*-region and disappear. Similar recombination occurs in *n*-region.

When electric field stops further diffusion, charge carriers (holes and electrons) don't move. As a consequence, opposite charges on each side of the junction produce immobile ions, Fig. 2.1 (b). The region extending into both *p* and *n* semiconductor layers is called *depletion region* or *space-charge region*. The width of depletion region, or *depletion layer*, is of the order of $5 \times 10^{-4} \text{ mm}$. In equilibrium, there is a potential difference of 0.7 V across the depletion region in silicon and 0.3 V across the depletion region in germanium. This potential difference across the depletion layer is called *barrier potential*.

When positive terminal of a battery is connected to *p*-type material and negative terminal to *n*-type material, Fig. 2.1 (c), the *p-n* junction is forward biased. Positive terminal of the battery sucks electrons from *p* material leaving holes there. These holes travel

through *p* material towards the negative charge at *p-n* junction and thus neutralize partly this negative charge. Similarly, negative terminal of the battery injects electrons into *n* layer. These electrons move through *n* material, reach the *p-n* junction thereby neutralizing partly the positive charge. As a result, width of depletion region gets reduced.

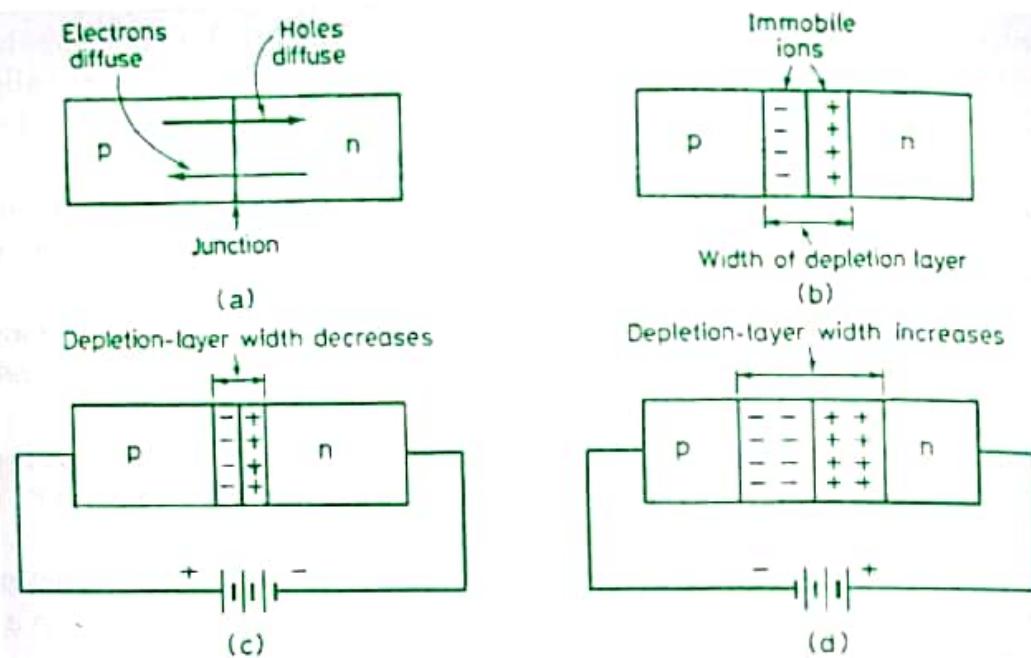


Fig. 2.1. A *p-n* junction showing (a) direction of holes and electrons diffusion (b) depletion region (c) effect of forward biasing and (d) effect of reverse biasing.

In case *p* material is connected to negative terminal of the battery and *n* material to positive terminal of battery, then it can be deduced that width of depletion layer increases, Fig. 2.1 (d).

A rise in junction temperature also decreases width of depletion layer. As the barrier potential depends on width of the depletion layer, the barrier potential decreases with rise in junction temperature.

For power semiconductor devices, it should be kept in mind that (i) a junction with lightly doped layer on its one side requires large breakdown voltage and (ii) a junction with highly doped layers on its both sides requires low breakdown voltage.

2.2 BASIC STRUCTURE OF POWER DIODES

Power diodes differ in structure from signal diodes. A signal diode constitutes a simple *p-n* junction as shown in Fig. 2.1. The intricacies in constructing power diodes arise from the need to make them suitable for high-voltage and high-current applications. Thus, a power diode should be so designed as to handle high forward current and a large reverse breakdown voltage.

The practical realization and the resulting structure of a power diode is shown in Fig. 2.2 (a). It consists of heavily doped *n⁺* substrate*. On this substrate, a lightly doped *n⁻* layer is epitaxially grown. Now a heavily doped *p⁺* layer is diffused into *n⁻* layer to form the anode of power diode, Fig. 2.2 (a). This shows that *n⁻* layer is the basic structural feature not found

* material on which something grows.

in signal diodes. The function of n^- layer is to absorb the depletion layer of the reverse biased $p^+ n^-$ junction J_1 . The breakdown voltage needed in a power diode governs the thickness of n^- layer; greater the breakdown voltage, more the n^- layer thickness. This n^- layer is lightly doped, nearly intrinsic. Because of this reason, n^- layer is sometimes called *i-layer* and the device as *p-i-n* diode or PiN diode.

The drawback of n^- layer is to add significant ohmic resistance to the diode when it is conducting a forward current. This leads to large power dissipation in the diode; so proper cooling arrangements in large diode ratings are essential.

The circuit symbol of a power diode, shown in Fig. 2.2 (b), is the same as that for a signal diode.

The modifications in the context of diode, presented above, makes them appropriate for high-power applications. As diode, or *p-n* junction, is the basic building block of all other power semiconductor devices; same basic modifications should be implemented in all low-power semiconductor devices in order to raise their power-handling capabilities.

2.3 CHARACTERISTICS OF POWER DIODES

As stated before, power diode is a two-terminal, *p-n* semiconductor device. The two terminals of diode are called anode and cathode, Fig. 2.2 (b) and Fig. 2.3 (a). Two important characteristics of power diodes are now described.

2.3.1 Diode i-v Characteristics*

When anode is positive with respect to cathode, diode is said to be *forward biased*. With increase of the source voltage V_s from zero value, initially diode current is zero. From $V_s = 0$ to cut-in voltage, the forward-diode current is very small. *Cut-in voltage* is also known as *threshold voltage* or *turn-on voltage*. Beyond cut-in voltage, the diode current rises rapidly and the diode is said to conduct. For silicon diode, the cut-in voltage is around 0.7 V. When diode conducts, there is a forward voltage drop of the order of 0.8 to 1 V.

For low-power diodes, current in the forward direction increases first exponentially with voltage and then becomes almost linear as shown in Fig. 2.3 (b). For power diodes, the forward current grows almost linearly with voltage, Fig. 2.3 (c). The high magnitude of current in a power diode leads to ohmic drops that hide the exponential part of *i-v* curve. The n^- region, or drift region, forms a considerable drop in the ohmic resistance of power diodes.

When cathode is positive with respect to anode, the diode is said to be *reverse biased*. In the reverse biased condition, a small reverse current called leakage current, of the order of microamperes or milliamperes (for large diodes) flows. The leakage current is almost independent of the magnitude of reverse voltage until this voltage reaches breakdown

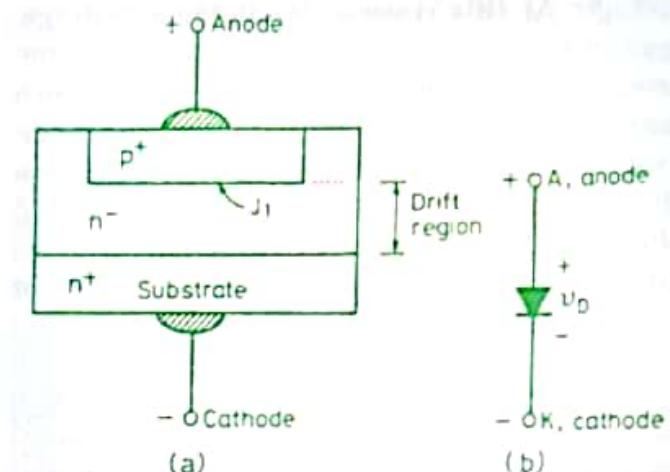


Fig. 2.2. (a) Structural features of power diode and (b) its circuit symbol.

* Some authors write *v-i* characteristics.

voltage. At this reverse breakdown, voltage remains almost constant but reverse current becomes quite high - limited only by the external circuit resistance. A large reverse breakdown voltage, associated with high reverse current, leads to excessive power loss that may destroy the diode. This shows that reverse breakdown of a power diode must be avoided by operating it below the specific peak reverse repetitive voltage V_{RRM} . Fig. 2.3 (c) illustrates the $i-v$ characteristics of power diode and V_{RRM} . For an ideal diode, the $i-v$ characteristics are shown in Fig. 2.3 (d). Here, voltage drop across conducting diode, $v_D = 0$, reverse leakage current = 0, cut-in voltage = 0 and reverse breakdown voltage V_{RRM} is infinite.

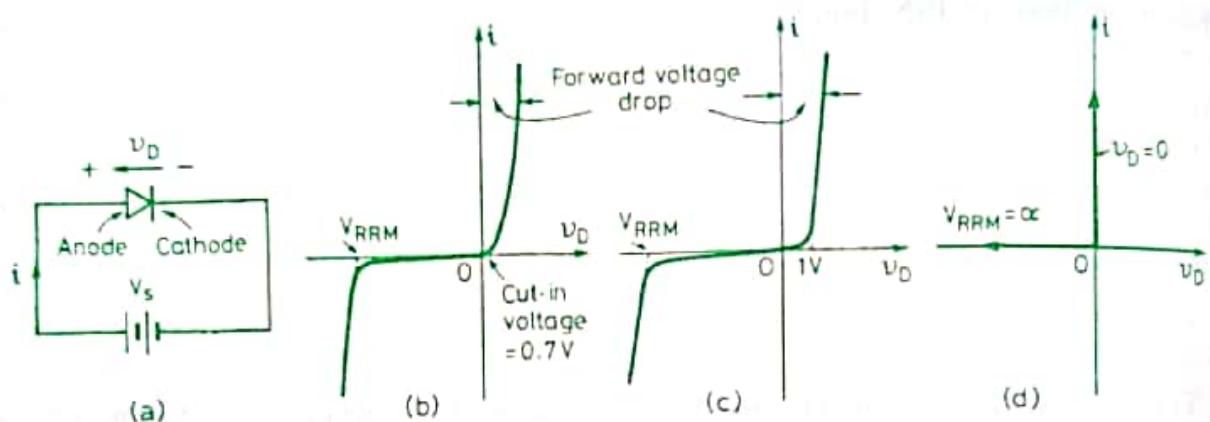


Fig. 2.3. (a) A forward-biased power diode. $i-v$ characteristics of (b) signal diode
(c) power diode and (d) ideal diode.

Diode manufacturers also indicate the value of peak inverse voltage (PIV) of a diode. This is the largest reverse voltage to which a diode may be subjected during its working. PIV is the same as V_{RRM} .

The power diodes are now available with forward current ratings of 1 A to several thousand amperes and with reverse voltage ratings of 50 V to 5000 V or more.

2.3.2 Diode Reverse Recovery Characteristics

After the forward diode current decays to zero, the diode continues to conduct in the reverse direction because of the pressure of stored charges in the depletion region and the semiconductor layers. The reverse current flows for a time called *reverse recovery time* t_{rr} . The diode regains its blocking capability until reverse recovery current decays to zero. The *reverse recovery time* t_{rr} is defined as the time between the instant forward diode current becomes zero and the instant reverse recovery current decays to 25% of its reverse peak value I_{RM} as shown in Fig. 2.4 (a).

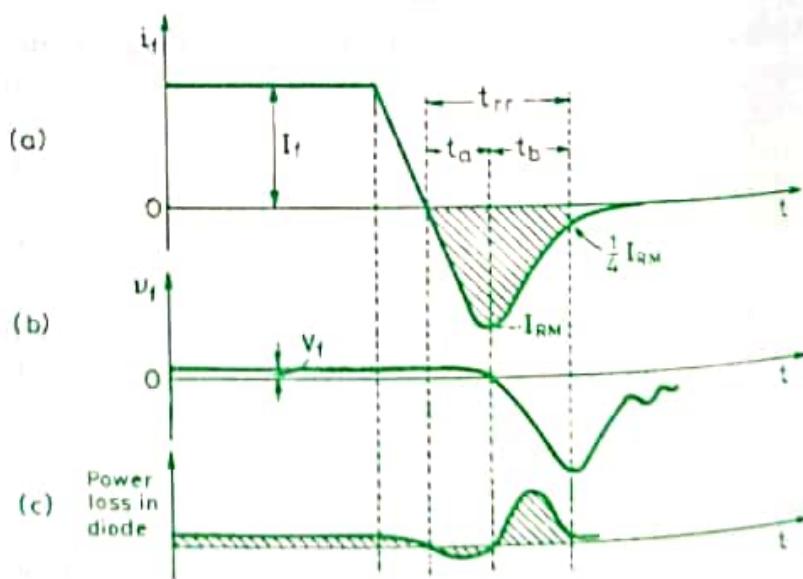


Fig. 2.4. Reverse recovery characteristics (a) variation of forward current i_f , (b) forward voltage drop v_f and (c) power loss in a diode.

The reverse recovery time is composed of two segments of time t_a and t_b , i.e. $t_{rr} = t_a + t_b$. Time t_a is the time between zero crossing of forward current and peak reverse current I_{RM} . During the time t_a , charge stored in depletion layer is removed. Time t_b is measured from the instant of reverse peak value I_{RM} to the instant when $0.25 I_{RM}$ is reached, Fig. 2.4 (a). During t_b , charge from the semiconductor layers is removed. The shaded area in Fig. 2.4 (a) represents the stored charge, or reverse recovery charge, Q_R which must be removed during the reverse recovery time t_{rr} . The ratio t_b/t_a is called the *softness factor* or *S-factor*. This factor is a measure of the voltage transients that occur during the time diode recovers. Its usual value is unity and this indicates low oscillatory reverse recovery process. In case *S-factor* is small, diode has large oscillatory over voltages. A diode with *S-factor* equal to one is called *soft-recovery diode* and a diode with *S-factor* less than one is called *snappy-recovery diode* or *fast-recovery diode*. In Fig. 2.4 (b) is shown the waveform of forward-voltage drop v_f across the diode. The product of v_f and i_f gives the power loss in a diode. Its variation is shown in Fig. 2.4 (c). The average value of $v_f i_f$ gives the total power loss in a diode. Fig. 2.4 (c) reveals that major power loss in a diode occurs during the period t_b .

It is noticed from Fig. 2.4 (a) that peak inverse current I_{RM} can be expressed as

$$I_{RM} = t_a \frac{di}{dt} \quad \dots(2.1)$$

where $\frac{di}{dt}$ is the rate of change of reverse current. The reverse recovery characteristics of Fig. 2.4 (a) can be taken to be triangular. Under this assumption, storage charge Q_R , from Fig. 2.4 (a), is given by

$$Q_R = \frac{1}{2} I_{RM} \cdot t_{rr}$$

or $I_{RM} = \frac{2Q_R}{t_{rr}} \quad \dots(2.2)$

If $t_{rr} \approx t_a$, then from Eq. (2.1),

$$I_{RM} = t_{rr} \cdot \frac{di}{dt} \quad \dots(2.3)$$

From Eqs. (2.2) and (2.3), we get

$$t_{rr} \cdot \frac{di}{dt} = \frac{2Q_R}{t_{rr}}$$

or $t_{rr} = \left[\frac{2Q_R}{(di/dt)} \right]^{1/2} \quad \dots(2.4)$

From Eq. (2.1), with $t_a \approx t_{rr}$, we get

$$I_{RM} = t_{rr} \cdot \frac{di}{dt} = \left[\frac{2Q_R}{(di/dt)} \right]^{1/2} \cdot \frac{di}{dt}$$

$$= \left[2Q_R \left(\frac{di}{dt} \right) \right]^{1/2} \quad \dots(2.5)$$

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[ART. 2.4]

It is seen from Eqs. (2.4) and (2.5) that reverse recovery time t_{rr} and peak inverse current I_{RM} are dependent on storage charge and rate of change of current $\frac{di}{dt}$. The storage charge depends upon the forward diode current I_F . This shows that reverse recovery time and peak inverse current depend on forward field, or diode, current. A power-electronics engineer must know peak reverse current I_{RM} , stored charge Q_R , S-factor, PIV etc. in order to be able to design the circuitry employing power diodes. These parameters are usually specified in the catalogue supplied by the diode manufacturers.

2.4 TYPES OF POWER DIODES

Diodes are classified according to their reverse recovery characteristics. The three types of power diodes are as under :

- (i) General purpose diodes
- (ii) Fast recovery diodes
- (iii) Schottky diodes.

These are now described briefly.

2.4.1 General-purpose Diodes

These diodes have relatively high reverse recovery time, of the order of about 25 μs . Their current ratings vary from 1 A to several thousand amperes and the range of voltage rating is from 50 V to about 5 kV. Applications of power diodes of this type include battery charging, electric traction, electroplating, welding and uninterruptible power supplies (UPS).

2.4.2 Fast-recovery Diodes

The diodes with low reverse recovery time, of about 5 μs or less, are classified as fast-recovery diodes. These are used in choppers, commutation circuits, switched mode power supplies, induction heating etc. Their current ratings vary from about 1 A to several thousand amperes and voltage ratings from 50 V to about 3 kV.

For voltage ratings below about 400 V, the epitaxial process is used for diode fabrication. These diodes have fast recovery time, as low as 50 ns.

For voltage ratings above 400 V, diffusion technique is used for the fabrication of diodes. In order to shorten the reverse-recovery time, platinum or gold doping is carried out. But this doping may increase the forward voltage drop in a diode.

2.4.3 Schottky Diodes

This class of diodes use metal-to-semiconductor junction for rectification purposes instead of $p-n$ junction. The metal is usually aluminium and semiconductor is silicon. Therefore, a Schottky diode has aluminium-silicon junction. The silicon is n -type.

When Schottky diode is forward biased, free electrons in n material move towards the Al- n junction and then travel through the metal (aluminium) to constitute the flow of forward current. Since metal does not have any holes, this forward current is due to the movement of electrons only. As the metal has no holes, there is no storage charge and no reverse recovery time. It can, therefore, be said that rectified current flow in a Schottky diode is by the movement of majority carriers (electrons) only and the turn-off delay caused by recombination is avoided. As such, Schottky diode can switch off much faster than $p-n$ junction diode.

As compared to *p-n* junction diode, a Schottky diode has (*i*) lower cut-in voltage, (*ii*) higher reverse leakage current and (*iii*) higher operating frequency. Their reverse voltage ratings are limited to about 100 V and forward current ratings vary from 1 A to 300 A. Applications of Schottky diode include high-frequency instrumentation and switching power supplies.

The electrical and thermal characteristics of power diodes are similar to those of thyristors which are described in Chapter 4.

2.5 POWER TRANSISTORS

Power diodes are uncontrolled devices. In other words, their turn-on and turn-off characteristics are not under control. Power transistors, however, possess controlled characteristics. These are turned on when a current signal is given to base, or control, terminal. The transistor remains in the on-state so long as control signal is present. When this control signal is removed, a power transistor is turned off.

Power transistors are of four types as under :

- (*i*) Bipolar junction transistors (BJTs)
- (*ii*) Metal-oxide-semiconductor field-effect transistors (MOSFETs)
- (*iii*) Insulated gate bipolar transistors (IGBTs) and
- (*iv*) Static induction transistors (SITs).

These four types are now described one after the other.

2.5.1 Bipolar Junction Transistors

A bipolar transistor is a three-layer, two junction *n-p-n* or *p-n-p* semiconductor device. With one *p*-region sandwiched by two *n*-regions, Fig. 2.5 (a), *n-p-n* transistor is obtained. With two *p*-regions sandwiching one *n*-region, Fig. 2.5 (b), *p-n-p* transistor is obtained. The term 'bipolar' denotes that the current flow in the device is due to the movement of both holes and electrons. A BJT has three terminals named collector (C), emitter (E) and base (B). An emitter is indicated by an arrowhead indicating the direction of emitter current. No arrow is associated with base or collector. Power transistors of *n-p-n* type are easy to manufacture and are cheaper also. Therefore, use of power *n-p-n* transistors is very wide in high-voltage and high-current applications. Hereafter, *n-p-n* transistors would only be considered.

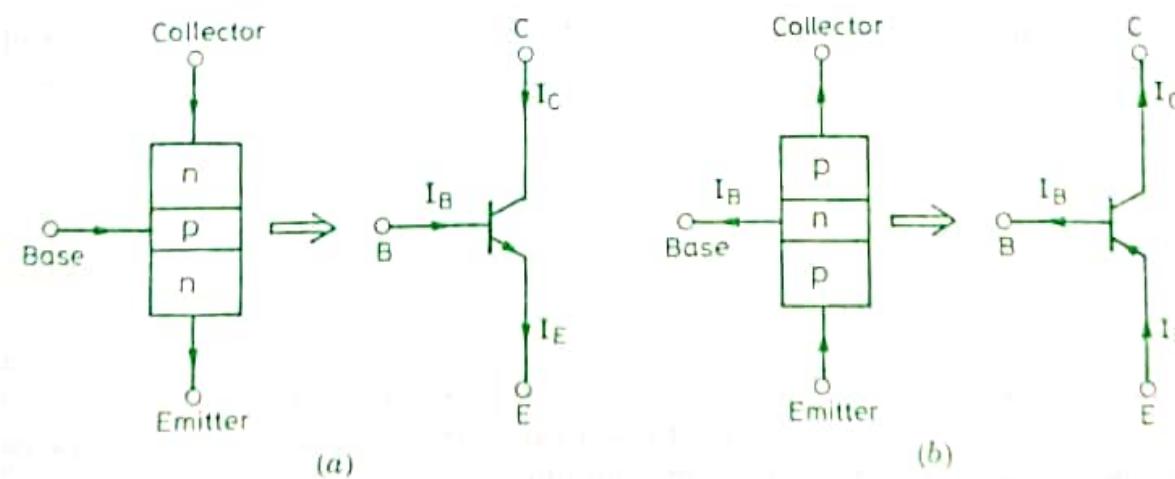


Fig. 2.5. Bipolar junction transistors (a) *n-p-n* type and (b) *p-n-p* type.

2.5.1.1 Steady-state Characteristics. Out of the three possible circuit configurations for a transistor, common-emitter arrangement is more common in switching applications. So, a common emitter *npn* circuit for obtaining its characteristics is considered as shown in Fig. 2.6 (a).

Input characteristics. A graph between base current I_B and base-emitter voltage V_{BE} gives input characteristics. As the base-emitter junction of a transistor is like a diode, I_B versus V_{BE} graph resembles a diode curve. When collector-emitter voltage V_{CE2} is more than V_{CE1} , base current, for the same V_{BE} , decreases as shown in Fig. 2.6 (b).

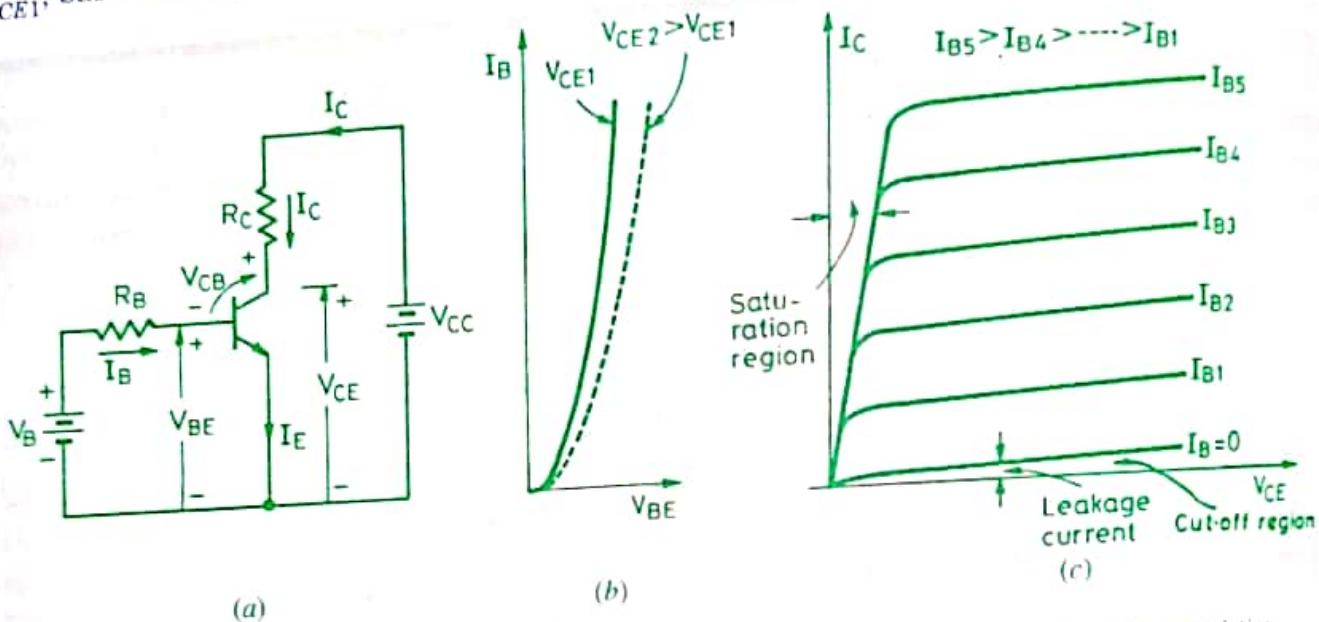


Fig. 2.6. (a) *n-p-n* transistor circuit characteristics, (b) input characteristics and (c) output characteristics.

Output characteristics. A graph between collector current I_c and collector-emitter voltage V_{CE} gives output characteristics of a transistor. For zero base current, i.e. for $I_B = 0$, as V_{CE} is increased, a small leakage (collector) current exists as shown in Fig. 2.6 (c). As the base current is increased from $I_B = 0$ to I_{B1}, I_{B2} etc., collector current also rises as shown in Fig. 2.6 (c).

Fig. 2.7 (a) shows two of the output characteristic curves, 1 for $I_B = 0$ and 2 for $I_B \neq 0$. The initial part of curve 2, characterised by low V_{CE} , is called the saturation region. In this region, the transistor acts like a switch. The flat part of curve 2, indicated by increasing V_{CE} and almost constant I_C , is the active region. In this region, transistor acts like an amplifier. Almost vertically rising curve is the breakdown region which must be avoided at all costs.

For load resistor R_C , Fig. 2.6 (a), the collector current I_C is given by

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

This is the equation of load line. It is shown as line AB in Fig. 2.7 (a). A load line is the locus of all possible operating points. Ideally, when transistor is on, V_{CE} is zero and $I_C = V_{CC}/R_C$. This collector current is shown by point A on the vertical axis. When the transistor is off, or in the cut-off region, V_{CC} appears across collector-emitter terminals and there is no collector current. This value is indicated by point B on the horizontal axis. For the resistive load, the line joining points A and B is the load line.

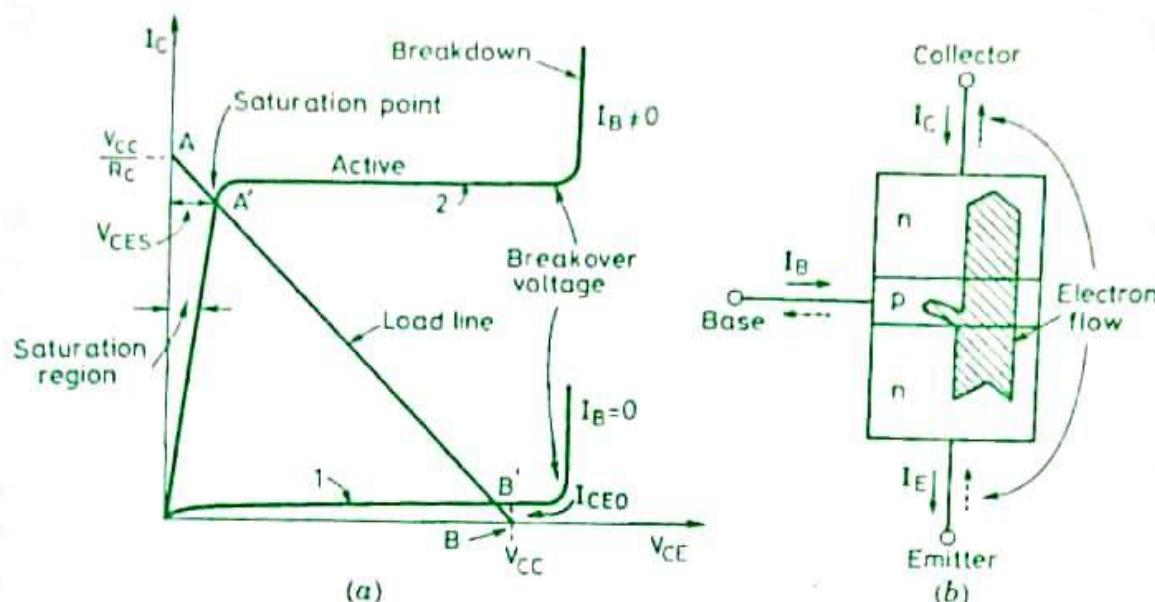


Fig. 2.7. (a) Output characteristics and load line for *npn* transistor and (b) electron flow in an *npn* transistor.

Relation between α and β . Most of the electrons, proportional to I_E , given out by emitter, reach the collector as shown in Fig. 2.7 (b). In other words, collector current I_C , though less than emitter current I_E , is almost equal to I_E . A symbol α is used to indicate how close in value these two currents are. Here α , called *forward current gain*, is defined as

$$\alpha = \frac{I_C}{I_E} \quad \dots(2.6)$$

As $I_C < I_E$, value of α varies from 0.95 to 0.99.

In a transistor, base current is effectively the input current and collector current is the output current. The ratio of collector (output) current I_C to base (input) current I_B is known as the *current gain* β .

$$\therefore \beta = \frac{I_C}{I_B} \quad \dots(2.7)$$

As I_B is much smaller, β is much more than unity ; its value varies from 50 to 300. In another system of analysis, called *h* parameters, h_{FE} is used in place of β .

$$\therefore \beta = h_{FE} = \frac{I_C}{I_B} \quad \dots(2.7)$$

Use of KCL in Fig. 2.6 (a) gives

$$I_E = I_C + I_B \quad \dots(2.8)$$

Remember that emitter current is the largest of the three currents, collector current is almost equal to, but less than, emitter current. Base current has the least value. Dividing both sides of Eq. (2.8) by I_C , we get

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

or

$$\alpha = \frac{\beta}{\beta + 1}$$

and

Transistor Switch. Transistor operation as a switch means that transistor operates either in the saturation region or in the cut-off region and nowhere else on the load line. As an ideal switch, the transistor operates at point A in the saturated state as closed switch with $V_{CE} = 0$ and at point B in the cut-off state as an open switch with $I_C = 0$, Fig. 2.7 (a). In practice, the large base current will cause the transistor to work in the saturation region at point A' with small saturation voltage V_{CES} . Here subscript S is used to denote saturated value. Voltage V_{CES} represents on-state voltage drop of the transistor which is of the order of about 1 V. When the control, or base, signal is reduced to zero, the transistor is turned off and its operation shifts to B' in the cut-off region, Fig. 2.7 (a). A small leakage current I_{CBO} flows in the collector circuit when the transistor is off.

For Fig. 2.6 (a), KVL for the circuit consisting of V_B , R_B and emitter gives

$$V_B - R_B I_B - V_{BE} = 0 \quad \dots(2.11)$$

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

or

$$\text{Also, from Fig. 2.6 (a), } V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$

or

$$= V_{CC} - \frac{\beta R_C}{R_B} (V_B - V_{BE}) \quad \dots(2.12)$$

Also

$$V_{CE} = V_{CB} + V_{BE} \quad \dots(2.13)$$

$$V_{CB} = V_{CE} - V_{BE}$$

or

If V_{CES} is the collector-emitter saturation voltage, then collector current I_{CS} is given by

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C} \quad \dots(2.14)$$

and the corresponding value of minimum base current, that produces saturation, is

$$I_{BS} = \frac{I_{CS}}{\beta} \quad \dots(2.15)$$

If base current is less than I_{BS} , the transistor operates in the active region, i.e. somewhere between the saturation and cut-off points. If base current is more than I_{BS} , V_{CE} is almost zero and collector current from Eq. (2.14) is given by $I_{CS} = V_{CC}/R_C$. This shows that collector current at saturation remains substantially constant even if base current is increased.

With base current more than I_{BS} , hard drive of transistor is obtained. With hard saturation, on-state losses of transistor increase. Normally, the practical circuit is designed for hard-drive of transistor and therefore, base current I_B is greater than I_{BS} given by Eq. (2.15). The ratio of I_B and I_{BS} is defined as the overdrive factor (ODF).

$$\therefore \text{ODF} = \frac{I_B}{I_{BS}} \quad \dots(2.16)$$

ODF may be as high as 4 or 5.

The ratio of I_{CS} to I_B is called *forced current gain* β_f where

$$\beta_f = \frac{I_{CS}}{I_B} < \text{natural current gain } \beta \text{ or } h_{FE} \quad \dots(2.17)$$

The total power loss in the two junctions of a transistor is

$$P_T = V_{BE} I_B + V_{CE} I_C \quad \dots(2.18)$$

Under saturated state, V_{BES} is greater than V_{CES} , this means BEJ is forward biased. Further Eq. (2.13) shows that V_{CB} is negative under saturated conditions, therefore, CBJ is also forward biased. In other words, under saturated conditions, both junctions in a power transistor are forward biased.

Example 2.1. A bipolar transistor shown in Fig. 2.6 (a) has current gain $\beta = 40$. The load resistance $R_C = 10 \Omega$, dc supply voltage $V_{CC} = 130 \text{ V}$ and input voltage to base circuit, $V_B = 10 \text{ V}$. For $V_{CES} = 1.0 \text{ V}$ and $V_{BES} = 1.5 \text{ V}$, calculate :

- (a) the value of R_B for operation in the saturated state,
- (b) the value of R_B for an overdrive factor 5,
- (c) forced-current gain and
- (d) power loss in the transistor for both parts (a) and (b).

Solution. Here, $\beta = 40$, $R_C = 10 \Omega$, $V_{CC} = 130 \text{ V}$, $V_B = 10 \text{ V}$, $V_{CES} = 1.0 \text{ V}$ and $V_{BES} = 1.5 \text{ V}$

(a) From Eq. (2.14), for operation in the saturated state,

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C} = \frac{130 - 1.0}{10} = 12.90 \text{ A}$$

From Eq. (2.15), base current that produces saturation,

$$I_{BS} = \frac{I_{CS}}{\beta} = \frac{12.90}{40} = 0.3225 \text{ A}$$

Value of R_B for $I_{BS} = 0.3225 \text{ A}$ is given by Eq. (2.11) as,

$$R_B = \frac{V_B - V_{BES}}{I_{BS}} = \frac{10 - 1.5}{0.3225} = 26.357 \Omega$$

(b) Base current with overdrive, from Eq. (2.16), is

$$I_B = \text{ODF} \times I_{BS} = 5 \times 0.3225 = 1.6125 \text{ A}$$

$$\therefore R_B = \frac{10 - 1.5}{1.6125} = 5.27 \Omega$$

(c) Forced current gain, from Eq. (2.17), is

$$\beta_f = \frac{I_{CS}}{I_B} = \frac{12.90}{1.6125} = 8,$$

which is less than the natural current gain $\beta = 40$.

(d) Power loss in transistor, from Eq. (2.18), is

$$P_T = V_{BES} I_B + V_{CES} I_{CS}$$

$$\text{For normal base drive, } P_T = 1.5 \times 0.3225 + 1.0 \times 12.9 = 13.384 \text{ W}$$

With overdrive, $P_T = 1.5 \times 1.6125 + 1.0 \times 12.9 = 15.32 \text{ W}$

It is seen from above that power loss with hard drive of transistor is more.

2.5.1.2 BJT Switching Performance. When base current is applied, a transistor does not turn on instantly because of the presence of internal capacitances. Fig. 2.9 shows the various switching waveforms of an *npn* power transistor with resistive load between collector and emitter, Fig. 2.8.

When input voltage v_B to base circuit is made $-V_2$ at t_0 , junction *EB* or *EBJ* is reverse biased, $v_{BE} = -V_2$, the transistor is off, $i_B = i_C = 0$ and $v_{CE} = V_{CC}$. Fig. 2.9. At time t_1 , input voltage v_B is made $+V_1$ and i_B rises to I_{B1} as shown in Fig. 2.9. After t_1 , base-emitter voltage v_{BE} begins to rise gradually from $-V_2$ and collector current i_c begins to rise from zero (actually a small leakage current I_{CEO} exists as shown in Fig. 2.7 (a)) and collector-emitter voltage v_{CE} starts falling from its initial value V_{CC} . After some time delay t_d , called delay time, the collector current rises to $0.1 I_{CS}$, v_{CE} falls from V_{CC} to $0.9 V_{CC}$ and v_{BE} reaches $V_{BES} = 0.7 \text{ V}$. This delay time is required to charge the base-emitter capacitance to $V_{BES} = 0.7 \text{ V}$. Thus, *delay time* t_d is defined as the time during which the collector current rises from zero to $0.1 I_{CS}$ and collector-emitter voltage falls from V_{CC} to $0.9 V_{CC}$.

After delay time t_d , collector current rises from $0.1 I_{CS}$ to $0.9 I_{CS}$ and v_{CE} falls from $0.9 V_{CC}$ to $0.1 V_{CC}$ in time t_r . This time t_r is known as *rise time* which depends upon transistor junction capacitances. *Rise time* t_r is defined as the time during which collector current rises from $0.1 I_{CS}$ to $0.9 V_{CC}$ and collector-emitter voltage falls from $0.9 V_{CC}$ to $0.1 V_{CC}$. This shows that total turn-on time $t_{on} = t_d + t_r$. Value of t_{on} is of the order of 30 to 300 nano seconds. The transistor remains in the on, or saturated, state so long as input voltage stays at V_1 . Fig. 2.9 (a).

In case transistor is to be turned off, then input voltage v_B and input base current i_B are reversed. At time t_2 , input voltage v_B to base circuit is reversed from V_1 to $-V_2$. At the same time, base current changes from I_{B1} to $-I_{B2}$ as shown in Fig. 2.9 (b). Negative base current I_{B2} removes excess carriers from the base. The time t_s required to remove these excess carriers is called *storage time* and only after t_s , base current I_{B2} begins to decrease towards zero. Transistor comes out of saturation only after t_s . *Storage time* t_s is usually defined as the time during which collector current falls from I_{CS} to $0.9 I_{CS}$ and collector-emitter voltage v_{CE} rises from V_{CES} to $0.1 V_{CC}$, Fig. 2.9 (d) and (e). Negative input voltage enhances the process of removal of excess carriers from base and hence reduces the storage time and therefore, the turn-off time.

After t_s , collector current begins to fall and collector-emitter voltage starts building up. Time t_f , called *fall time*, is defined as the time during which collector current drops from $0.9 I_{CS}$ to $0.1 I_{CS}$ and collector-emitter voltage rises from $0.1 V_{CC}$ to $0.9 V_{CC}$, Fig. 2.9 (d) and (e). Sum of storage time and fall time gives the transistor turn-off time t_{off} i.e., $t_{off} = t_s + t_f$. The various waveforms during transistor switching are shown in Fig. 2.9. In this figure, t_n = conduction period of transistor, t_o = off period, $T = 1/f$ is the periodic time and f is the switching frequency.

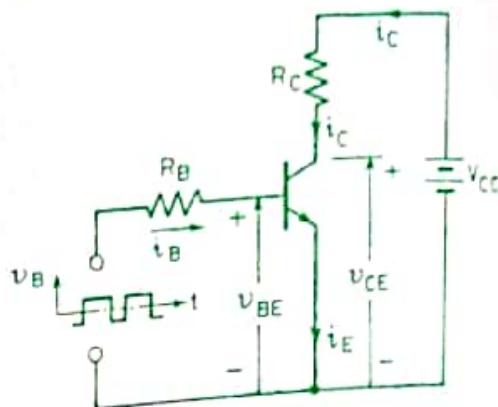


Fig. 2.8. *npn* transistor with resistive load.

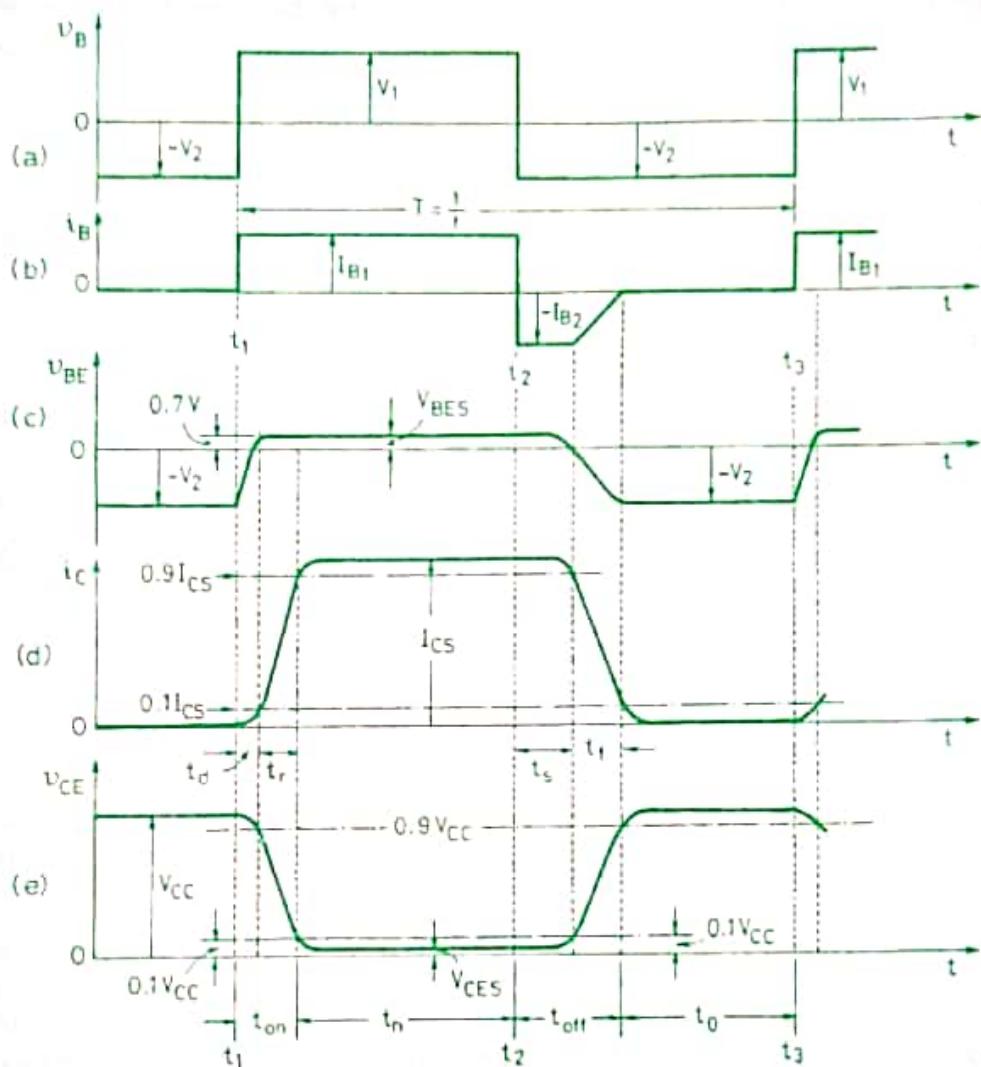


Fig. 2.9. Switching waveforms for *n*p*n* power transistor of Fig. 2.8.

2.5.1.3 Safe Operating Area. The safe operating area (SOA or SOAR) of a power transistor specifies the safe operating limits of collector current I_C versus collector-emitter voltage V_{CE} . For reliable operation of the transistor, the collector current and voltage must always lie within this area. Actually, two types of safe operating areas are specified by the manufacturers, FBSOA and RBSOA.

The forward-base safe operating area (FBSOA) pertains to the transistor operation when base-emitter junction is forward biased to turn-on the transistor. For a power transistor, Fig. 2.10 shows typical FBSOA for its dc as well as single-pulse operation. The scale for I_C and V_{CE} are logarithmic. Boundary *AB* is the maximum limit for dc and continuous current for V_{CE} less than about 80 V. For V_{CE} for more than 80 V, collector current has to be reduced to boundary *BC* so as to limit the junction temperature to safe values. For still higher V_{CE} , current should further be reduced so as to avoid secondary breakdown limit. Boundary *CD* defines this secondary breakdown limit. Boundary *DE* gives the maximum voltage capability for this particular transistor.

For pulsed operation, power transistor can dissipate more peak power so long as average power loss is within safe limits of junction temperature. In Fig. 2.10, 5 ms, 500 μ s etc. indicate pulse widths for which transistor is on. It is seen that FBSOA increases as pulse-width is decreased.

It should be noted that FBSOA curves, as given by the manufacturers, are for a case temperature of 25°C and for dc and single-pulse operation. In order to take into consideration the actual working temperature and repetitive nature of the pulses, these curves must be modified with the help of thermal impedance of the device.

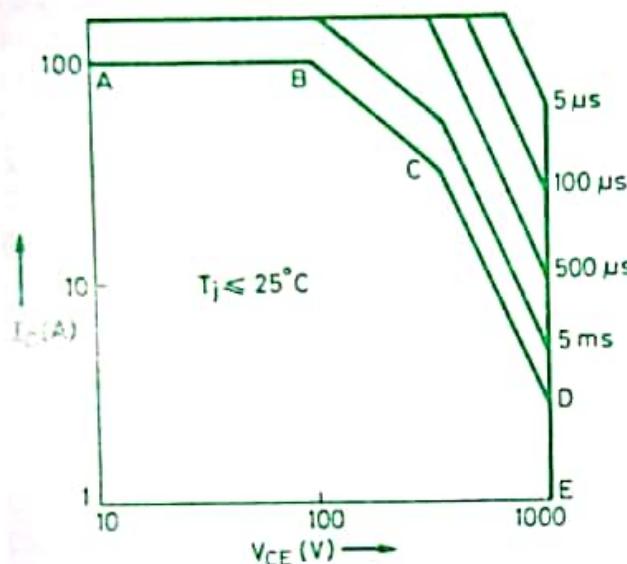


Fig. 2.10. Typical forward biased safe operating area (FBSOA) for a power transistor (logarithmic scale).

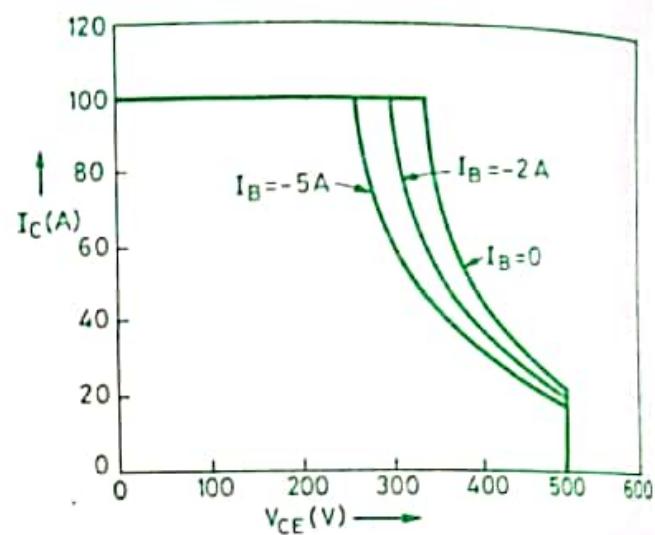


Fig. 2.11. Typical reverse-block safe operating area (RBSOA) for a power transistor.

During turn-off, a transistor is subjected to high current and high voltage with base-emitter junction reverse biased. Safe operating area for transistor during turn-off is specified as reverse blocking safe operating area (RBSOA). This RBSOA is a plot of collector current versus collector-emitter voltage as shown in Fig. 2.11. RBSOA specifies the limits of transistor operation at turn-off when the base current is zero or when the base-emitter junction is reverse biased (*i.e.*, with base current negative). With increased reverse bias, area RBSOA decreases in size as shown in Fig. 2.11.

Example 2.2. For a power transistor, typical switching waveforms are shown in Fig. 2.12 (a). The various parameters of the transistor circuit are as under :

$$V_{CC} = 220\text{ V}, V_{CES} = 2\text{ V}, I_{CS} = 80\text{ A}, t_d = 0.4\text{ } \mu\text{s}, t_r = 1\text{ } \mu\text{s}, t_n = 50\text{ } \mu\text{s}, \\ t_s = 3\text{ } \mu\text{s}, t_f = 2\text{ } \mu\text{s}, t_o = 40\text{ } \mu\text{s}, f = 5\text{ kHz}.$$

Collector to emitter leakage current $I_{CEO} = 2\text{ mA}$.

Determine average power loss due to collector current during t_{on} and t_n . Find also the peak instantaneous power loss due to collector current during turn-on time.

Solution. During delay time, the time limits are $0 \leq t \leq t_d$. Fig. 2.12 (a) shows that in this time, $i_c(t) = I_{CEO}$ and $v_{CE}(t) = V_{CC}$.

\therefore Instantaneous power loss during delay time is

$$P_d(t) = i_c v_{CE} = I_{CEO} V_{CC} = 2 \times 10^{-3} \times 220 = 0.44\text{ W}$$

Average power loss during delay time with $0 \leq t \leq t_d$ is given by

$$P_d = \frac{1}{T} \int_0^{t_d} i_c(t) \cdot v_{CE}(t) dt$$

$$\begin{aligned}
 &= \frac{1}{T} \int_0^{t_d} I_{CEO} \cdot V_{CC} dt = f \cdot I_{CEO} \cdot V_{CC} \cdot t_d \\
 &= 5 \times 10^3 \times 2 \times 10^{-3} \times 220 \times 0.4 \times 10^{-6} = 0.88 \text{ mW}
 \end{aligned}$$

where $f = \frac{1}{T}$ = frequency of transistor switching.

During rise time, $0 \leq t \leq t_r$,

$$i_C(t) = \frac{I_{CS}}{t_r} \cdot t$$

and

$$v_{CE}(t) = \left[V_{CC} - \frac{V_{CC} - V_{CES}}{t_r} \cdot t \right]$$

\therefore Average power loss during rise time is

$$\begin{aligned}
 P_r &= \frac{1}{T} \int_0^{t_r} \frac{I_{CS}}{t_r} \cdot t \left[V_{CC} - \frac{V_{CC} - V_{CES}}{t_r} \cdot t \right] dt \\
 &= f \cdot I_{CS} \cdot t_r \left[\frac{V_{CC}}{2} - \frac{V_{CC} - V_{CES}}{3} \right] \\
 &= 5 \times 10^3 \times 80 \times 1 \times 10^{-6} \left[\frac{220}{2} - \frac{220 - 2}{3} \right] = 14.933 \text{ W}
 \end{aligned}$$

Instantaneous power loss during rise time is

$$P_r(t) = \frac{I_{CS}}{t_r} \cdot t \left\{ V_{CC} - \frac{V_{CC} - V_{CES}}{t_r} \cdot t \right\}$$

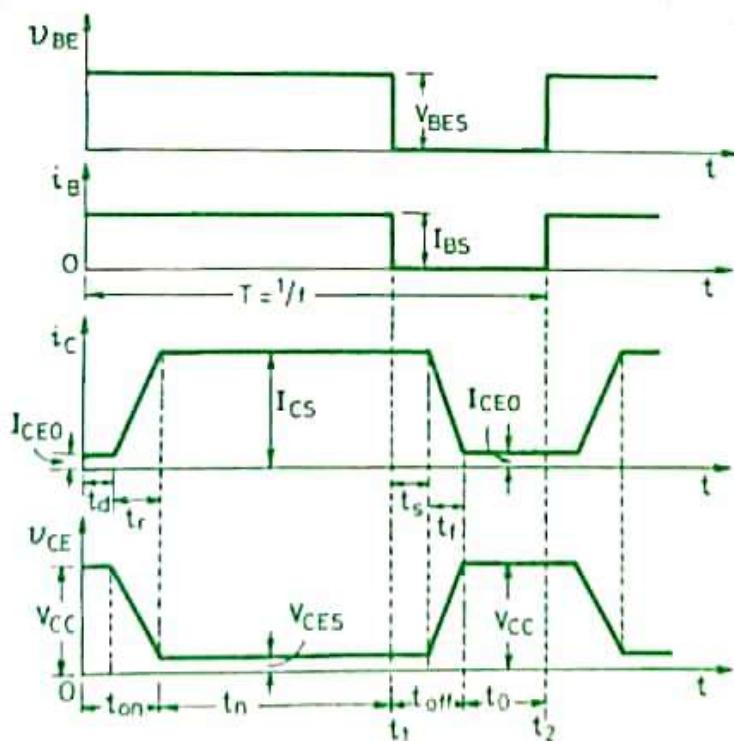


Fig. 2.12.(a) Switching waveforms for Examples 2.2 and 2.3.

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[ART. 2.5]

$$= \frac{I_{CS} \cdot t}{t_r} V_{CC} - \frac{I_{CS} \cdot t^2}{t_r^2} [V_{CC} - V_{CES}] \quad \dots(i)$$

$\frac{dP_r(t)}{dt} = 0$ gives time t_m at which instantaneous power loss during t_r would be maximum. It is seen from Eq. (i) that

$$t_m = \frac{V_{CC} \cdot t_r}{2[V_{CC} - V_{CES}]} = \frac{220 \times 1 \times 10^{-6}}{2[220 - 2]} = 0.5046 \mu s$$

Peak instantaneous power loss P_{rm} during rise time is obtained by substituting the value of $t = t_m$ in Eq. (i).

$$\begin{aligned} P_{rm} &= \frac{I_{CS}}{t_r} \cdot \frac{V_{CC}^2 \cdot t_r}{2[V_{CC} - V_{CES}]} - \frac{I_{CS}}{t_r^2} \frac{(V_{CC} \cdot t_r)^2 [V_{CC} - V_{CES}]}{4[V_{CC} - V_{CES}]^2} \\ &= \frac{I_{CS} \cdot V_{CC}^2}{4[V_{CC} - V_{CES}]} = \frac{80 \times 220^2}{4[220 - 2]} = 4440.4 \text{ W} \end{aligned}$$

Total average power loss during turn-on

$$P_{on} = P_d + P_r = 0.00088 + 14.933 = 14.9339 \text{ W}$$

During conduction time, $0 \leq t \leq t_n$

$$i_C(t) = I_{CS} \quad \text{and} \quad V_{CE}(t) = V_{CES}$$

Instantaneous power loss during t_n is

$$P_n(t) = i_C \cdot v_{CE} = I_{CS} \cdot V_{CES} = 80 \times 2 = 160 \text{ W}$$

Average power loss during conduction period is

$$\begin{aligned} P_n &= \frac{1}{T} \int_0^{t_n} i_C \cdot v_{CE} \cdot dt = f I_{CS} \cdot V_{CES} \cdot t_n \\ &= 5 \times 10^3 \times 80 \times 2 \times 50 \times 10^{-6} = 40 \text{ W.} \end{aligned}$$

Example 2.3. Repeat Example 2.2 for obtaining average power loss during turn-off time and off-period, and also peak instantaneous power loss during fall time due to collector current.

Sketch the instantaneous power loss for period T as a function of time.

Solution. During storage time, $0 \leq t \leq t_s$,

$$i_C(t) = I_{CS} \quad \text{and} \quad v_{CE}(t) = V_{CES}$$

Instantaneous power loss during t_s is

$$\begin{aligned} P_s(t) &= i_C(t) v_{CE}(t) \\ &= I_{CS} \cdot V_{CES} = 80 \times 2 = 160 \text{ W} \end{aligned}$$

Average power loss during t_s is

$$\begin{aligned} P_s &= \frac{1}{T} \int_0^{t_s} I_{CS} \cdot V_{CES} \cdot dt = f \cdot I_{CE} \cdot V_{CES} \cdot t_s \\ &= 5 \times 10^3 \times 80 \times 2 \times 3 \times 10^{-6} = 2.4 \text{ W} \end{aligned}$$

During fall time, $0 \leq t \leq t_f$, $i_C(t) = \left[I_{CS} - \frac{I_{CS} - I_{CEO}}{t_f} \cdot t \right]$

During t_f , I_{CEO} is negligibly small in comparison with I_{CS} .

$$\therefore i_C(t) = I_{CS} \left[1 - \frac{t}{t_f} \right]$$

and

$$v_{CE}(t) = \frac{V_{CC} - V_{CES}}{t_f} \cdot t$$

Average power loss during fall time is

$$\begin{aligned} P_f &= \frac{1}{T} \int_0^{t_f} I_{CS} \left(1 - \frac{t}{t_f} \right) \left[\frac{V_{CC} - V_{CES}}{t_f} \cdot t \right] dt \\ &= f(V_{CC} - V_{CES}) \cdot t_f \left[\frac{I_{CS}}{2} - \frac{I_{CS}}{3} \right] \\ &= f \cdot t_f \cdot \frac{I_{CS}}{6} [V_{CC} - V_{CES}] \\ &= 5 \times 10^3 \times 3 \times 10^{-6} \times 80 \times \frac{1}{6} \times (220 - 2) = 43.6 \text{ W} \end{aligned}$$

Instantaneous power loss during fall time is

$$\begin{aligned} P_f(t) &= I_{CS} \left[1 - \frac{t}{t_f} \right] \left[\frac{V_{CC} - V_{CES}}{t_f} t \right] \\ &= \frac{I_{CS}(V_{CC} - V_{CES}) \cdot t}{t_f} - I_{CS} (V_{CC} - V_{CES}) \frac{t^2}{t_f^2} \end{aligned}$$

$\frac{dP_f(t)}{dt} = 0$ gives time t_m at which instantaneous power loss during t_f would be maximum. Here $t_m = t_f/2$.

\therefore Peak instantaneous power dissipation during t_f is

$$\begin{aligned} P_{fm} &= I_{CS} \left(1 - \frac{1}{2} \right) \left(\frac{V_{CC} - V_{CES}}{2} \right) = \frac{I_{CS} (V_{CC} - V_{CES})}{4} \\ &= \frac{80(220 - 2)}{4} = 4360 \text{ W} \end{aligned}$$

Total average power loss during turn-off process is

$$P_{off} = P_s + P_f = 2.4 + 43.6 = 46 \text{ W}$$

During off-period, $0 \leq t \leq t_0$,

$$i_C(t) = I_{CEO} \text{ and } v_{CE}(t) = V_{CC}$$

Instantaneous power loss during t_0 is

$$P_0(t) = i_C \cdot v_{CE} = I_{CEO} \cdot V_{CC} = 2 \times 10^{-3} \times 220 = 0.44 \text{ W}$$

Average power loss during t_0 is

$$\begin{aligned} P_0 &= \frac{1}{T} \int_0^{t_0} P_0(t) dt = f I_{CEO} \cdot V_{CC} \cdot t_0 \\ &= 5 \times 10^3 \times 2 \times 10^{-3} \times 220 \times 40 \times 10^{-6} = 0.088 \text{ W} \end{aligned}$$

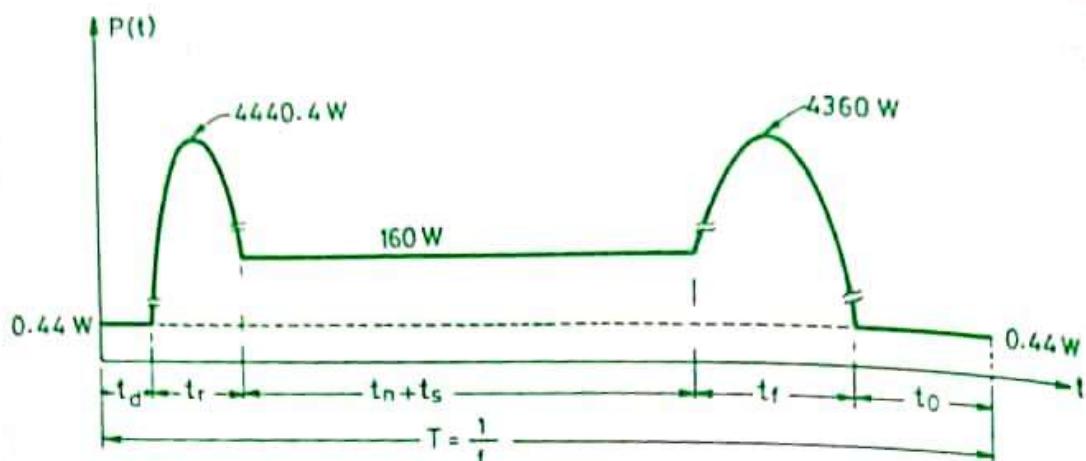
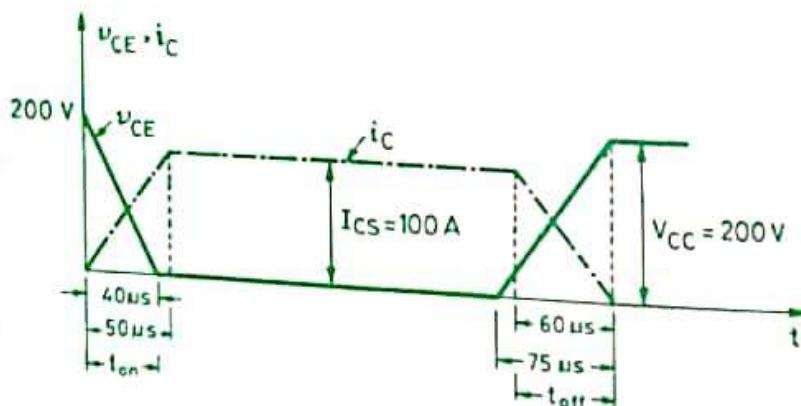


Fig. 2.12. (b) Sketch of instantaneous power loss in a transistor for Examples 2.2 and 2.3.
Total average power loss in power-transistor due to collector current over a period T_{13}

$$P_T = P_{on} + P_n + P_{off} + P_0 = 14.9339 + 40 + 46 + 0.088 = 101.022 \text{ W.}$$

From the data obtained in Examples 2.2 and 2.3, the power loss variation as a function of time, over a period T , is sketched in Fig. 2.12 (b).

Example 2.4. A power transistor has its switching waveforms as shown in Fig. 2.13. If the average power loss in the transistor is limited to 300 W, find the switching frequency at which this transistor can be operated.



Solution. Energy loss during turn-on
Fig. 2.13. Switching waveform for Example 2.4.

$$\begin{aligned}
 &= \int_0^{t_{on}} i_C \cdot v_{CE} dt \\
 &= \int_0^{t_{on}} \left(\frac{I_{CS}}{50} \times 10^6 t \right) \left(V_{CC} - \frac{V_{CC}}{40} \times 10^6 t \right) dt \\
 &= \int_0^{t_{on}} (2 \times 10^6 t) (200 - 5 \times 10^6 t) dt \\
 &= 0.1067 \text{ watt-sec}
 \end{aligned}$$

$$\text{Energy loss during turn-off} = \int_0^{t_{off}} \left(100 - \frac{100}{60} \times 10^6 t \right) \left(\frac{200}{75} \times 10^6 t \right) dt \\ = 0.1603 \text{ watt-sec}$$

Total energy loss in one cycle

$$= 0.1067 + 0.1603 = 0.267 \text{ W-sec}$$

Average power loss in transistor

$$= \text{Switching frequency} \times \text{Energy loss in one cycle}$$

\therefore Allowable switching frequency,

$$f = \frac{300}{0.267} = 1123.6 \text{ Hz.}$$

2.6 POWER MOSFETs

A metal-oxide-semiconductor field-effect transistor (MOSFET) is a recent device developed by combining the areas of field-effect concept and MOS technology.

A power MOSFET has three terminals called drain (D), source (S) and gate (G) in place of the corresponding three terminals collector, emitter and base for BJT. The circuit symbol of power MOSFET is as shown in Fig. 2.14 (a). Here arrow indicates the direction of electron flow. A BJT is a current controlled device whereas a power MOSFET is a voltage-controlled device. As its operation depends upon the flow of majority carriers only, MOSFET is a unipolar device. The control signal, or base current in BJT is much larger than the control signal (or gate current) required in a MOSFET. This is because of the fact that gate circuit impedance in MOSFET is extremely high, of the order of 10^9 ohm. This large impedance permits the MOSFET gate to be driven directly from microelectronic circuits. BJT suffers from second breakdown voltage whereas MOSFET is free from this problem. Power MOSFETs are now finding increasing applications in low-power high frequency converters.

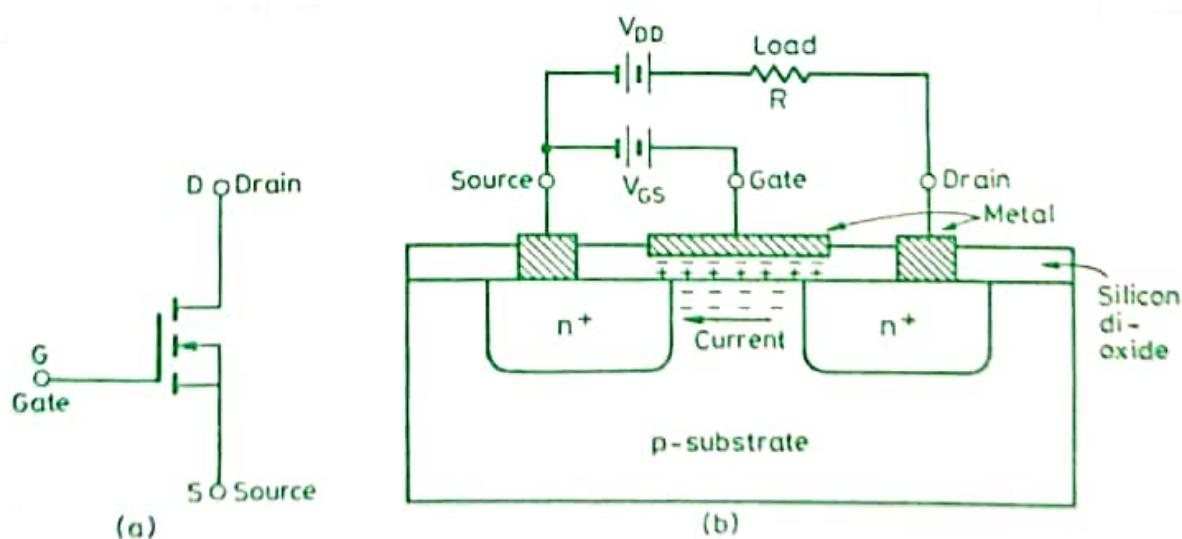


Fig. 2.14. N-channel enhancement power MOSFET (a) circuit symbol and (b) its basic structure.

Power MOSFETs are of two types ; *n*-channel enhancement MOSFET and *p*-channel enhancement MOSFET. Out of these two types, *n*-channel enhancement MOSFET is more common because of higher mobility of electrons. As such, only this type of MOSFET is studied in what follows.

A simplified structure of *n*-channel planar MOSFET of low power rating is shown in Fig. 2.14 (b). On *p*-substrate (or body), two heavily doped *n*⁺ regions are diffused as shown. An insulating layer of silicon dioxide (SiO_2) is grown on the surface. Now this insulating layer is etched in order to embed metallic source and drain terminals. Note that *n*⁺ regions make contact with source and drain terminals as shown. A layer of metal is also deposited on SiO_2 layer so as to form the gate of MOSFET in between source and drain terminals, Fig. 2.14 (b).

When gate circuit is open, junction between *n*⁺ region below drain and *p*-substrate is reverse biased by input voltage V_{DD} . Therefore, no current flows from drain to source and load. When gate is made positive with respect to source, an electric field is established as shown in Fig. 2.14 (b). Eventually, induced negative charges in the *p*-substrate below SiO_2 layer are formed thus causing the *p* layer below gate to become an induced *n* layer. These negative charges, called electrons, form *n*-channel between two *n*⁺ regions and current can flow from drain to source as shown by the arrow. If V_{GS} is made more positive, induced *n*-channel becomes more deep and therefore more current flows from *D* to *S*. This shows that drain current I_D is enhanced by the gradual increase of gate voltage, hence the name enhancement MOSFET.

The main disadvantage of *n*-channel planar MOSFET of Fig. 2.14 (b) is that conducting *n*-channel in between drain and source gives large on-state resistance. This leads to high power dissipation in *n*-channel. This shows that planar MOSFET construction of Fig. 2.14 (b) is feasible only for low-power MOSFETs.

The constructional details of high power MOSFET are illustrated in Fig. 2.15. In this figure is shown a planar vertical diffused metal-oxide-semiconductor (VDMOS) structure for *n*-channel which is quite common for power MOSFETs. On *n*⁺ substrate, high resistivity *n*⁻ layer is epitaxially* grown. The thickness of *n*⁻ layer determines the voltage blocking capability of the device. On the other side of *n*⁺ substrate, a metal layer is deposited to form the drain terminal. Now *p* regions are diffused in the epitaxially grown *n*⁻ layer. Further, *n*⁺ regions are diffused in *p* regions as shown. As before, SiO_2 layer is added, which is then etched so as to fit metallic source and gate terminals. A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

When gate circuit voltage is zero, and V_{DD} is present, *n*⁻ – *p*⁻ junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons form *n*-channel in the *p* regions as shown. So a current from drain to source is established as indicated by arrows. With gate voltage increased, current I_D also increases as expected. Length of *n*-channel can be controlled and therefore on-resistance can be made low if short length is used for the channel.

* A mixture of silicon atoms and pentavalent atoms, deposited on wafer, forms a layer of *n*-type semiconductor on heated surface. This layer is called epitaxial layer.

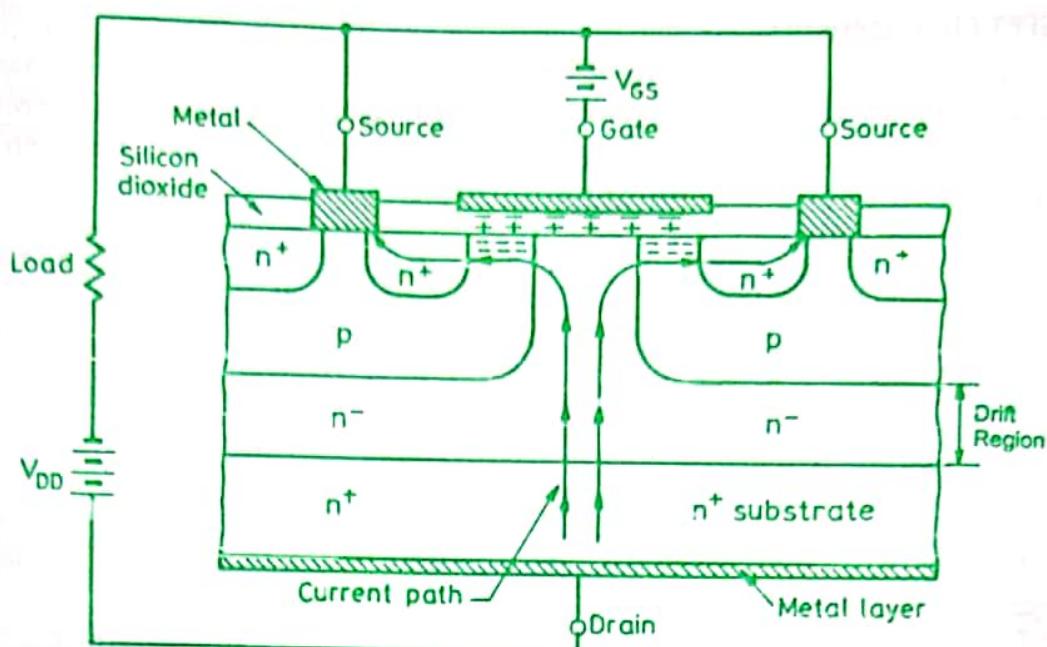


Fig. 2.15. Basic structure of a *n*-channel VDMOS power MOSFET.

An examination of the basic structure of *n*-channel VDMOS power MOSFET (PMOSFET) reveals that a parasitic *npn* bipolar junction transistor exists between the source and drain as shown in Fig. 2.16. The *p* body acts as the base, *n⁺* layer as the emitter (or source) and *n⁻* layer as the collector (or drain) of this BJT. Since source is connected to both base and emitter of parasitic BJT, the source short circuits both base and emitter. As a result, potential difference between base and emitter of the parasitic BJT is zero and therefore, BJT is always in the cut-off state.

Also, vertical travel from source to drain indicates the existence of a parasitic diode as shown on the right in Fig. 2.16. The parasitic diode, with source acting as anode and drain as cathode may be used in half-bridge or full-bridge rectifiers. The parasitic diode also shows that reverse voltage blocking capability of PMOSFET is almost zero. This in-built diode is an advantage in inverter circuits.

In Fig. 2.15, source is negative and drain is positive. Therefore, electrons flow from source to *n⁺* layer, then through *n*-channel of *p* layer and further through *n⁻* and *n⁺* layers to drain. The current must flow opposite to the flow of electrons as indicated in Fig. 2.15. Since the conduction of current is due to the movement of electrons only, PMOSFET is a majority carrier device. Hence, time delays caused by removal or recombination of minority carriers are eliminated during the turn-off process of this device. PMOSFET with a turn-off time of 100 ns are available. Owing to its low turn-off time, PMOSFET can be operated in a frequency range of 1 to 10 MHz.

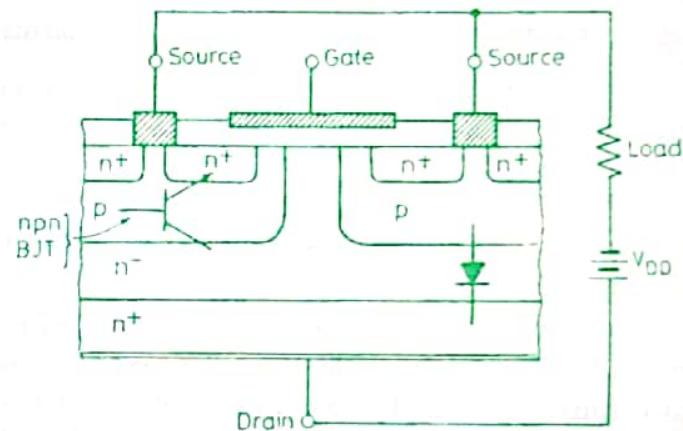


Fig. 2.16. PMOSFET showing parasitic BJT and parasitic diode.

2.6.1 PMOSFET Characteristics

The static characteristics of power MOSFET are now described briefly. The basic circuit diagram for *n*-channel PMOSFET is shown in Fig. 2.17 where voltages and currents are as indicated. The source terminal S is taken as common terminal, as usual, between the input and output of a MOSFET.

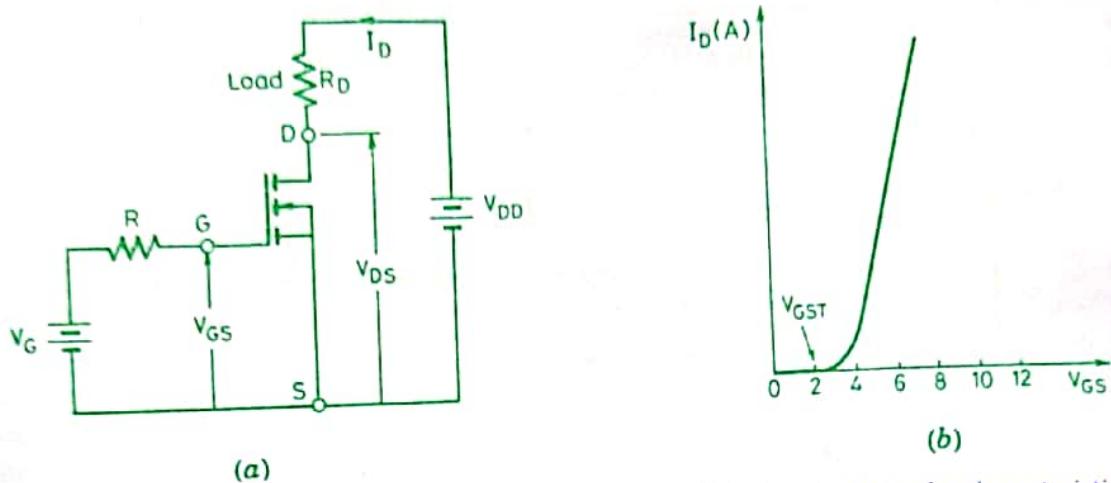


Fig. 2.17. *N*-channel power MOSFET (a) circuit diagram and (b) its typical transfer characteristic.

(a) **Transfer characteristics.** This characteristic shows the variation of drain current I_D as a function of gate-source voltage V_{GS} . Fig. 2.17 (b) shows typical transfer characteristics for *n*-channel PMOSFET. Threshold voltage V_{GST} is an important parameter of MOSFET. V_{GST} is the minimum positive voltage between gate and source to induce *n*-channel. Thus, for threshold voltage below V_{GST} , device is in the off-state. Magnitude of V_{GST} is of the order of 2 to 3 V.

(b) **Output characteristics.** PMOSFET output characteristics, shown in Fig. 2.18 (a), indicate the variation of drain current I_D as a function of drain-source voltage V_{DS} , with gate-source voltage V_{GS} as a parameter. For low values of V_{DS} , the graph between $I_D - V_{DS}$ is almost linear; this indicates a constant value of on-resistance $R_{DS} = V_{DS}/I_D$. For given V_{GS} , if V_{DS} is increased, output characteristic is relatively flat, indicating that drain current is nearly constant. A load line intersects the output characteristics at A and B. Here A indicates fully-on condition and B fully-off state. PMOSFET operates as a switch either at A or at B just like a BJT.

When power MOSFET is driven with large gate-source voltage, MOSFET is turned on, $V_{DS,ON}$ is small. Here, the MOSFET acting as a closed switch, is said to be driven into ohmic region (called saturation region in BJT). When device turns on, PMOSFET traverses $i_D - V_{DS}$ characteristics from cut-off, to active region and then to the ohmic region, Fig. 2.18 (a). When PMOSFET turns off, it takes backward journey from ohmic region to cut-off state.

(c) **Switching characteristics.** The switching characteristics of a power MOSFET are influenced to a large extent by the internal capacitance of the device and the internal impedance of the gate drive circuit. At turn-on, there is an initial delay t_{dn} during which input capacitance charges to gate threshold voltage V_{GST} . Here t_{dn} is called *turn-on delay time*.

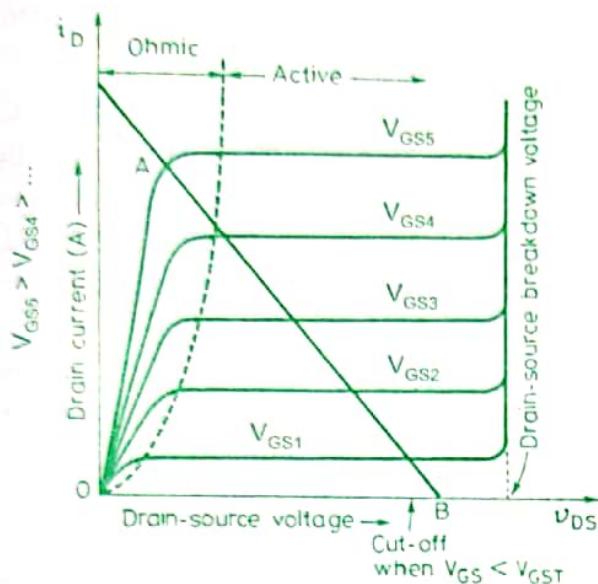


Fig. 2.18. (a) Output characteristics of PMOSFET.

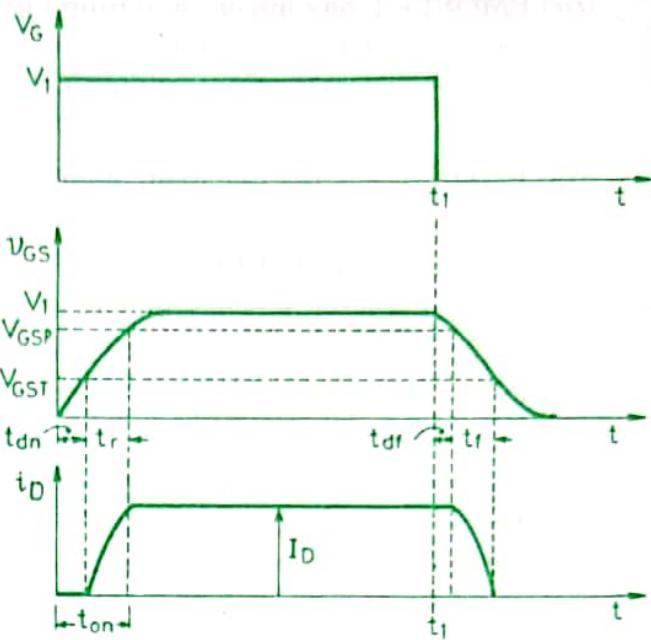


Fig. 2.18. (b) Switching waveforms for PMOSFET.

There is further delay t_r , called *rise time*, during which gate voltage rises to V_{GSP} , a voltage sufficient to drive the MOSFET into on state. During t_r , drain current rises from zero to full-on current I_D . Thus, the total turn-on-time is $t_{on} = t_{dn} + t_r$. The turn-on time can be reduced by using low-impedance gate-drive source.

As MOSFET is a majority carrier device, turn-off process is initiated soon after removal of gate voltage at time t_1 . The turn-off delay time, t_{df} , is the time during which input capacitance discharges from overdrive gate voltage V_1 to V_{GSP} . The *fall time*, t_f , is the time during which input capacitance discharges from V_{GSP} to threshold voltage. During t_f , drain current falls from I_D to zero. So when $V_{GS} \leq V_{GST}$, PMOSFET turn-off is complete. Switching waveforms for a power MOSFET are shown in Fig. 2.18 (b).

2.6.2 PMOSFET Applications

The on-resistance of MOSFET increases with voltage rating ; this makes the device very lossy at high-current applications. Since the on-resistance has positive temperature coefficient, parallel operation of PMOSFETs is relatively easy. The positive temperature coefficient also reduces the second breakdown effect in PMOSFETs.

PMOSFETs find applications in high-frequency switching applications, varying from a few watts to few kW. The device is very popular in switched-mode power supplies and inverters. These are, at present available with 500 V, 140 A ratings.

2.6.3 Comparison of PMOSFET with BJT

The three terminals in a PMOSFET are designated as gate, source and drain. In a BJT, the corresponding three terminals are base, emitter and collector. A PMOSFET has several features different from those of BJT. These are outlined below :

- (i) BJT is a bipolar device whereas PMOSFET is a unipolar device.
- (ii) A PMOSFET has high input impedance (mega ohm) whereas input impedance of BJT is low (a few kilo-ohm).

- (iii) PMOSFET has lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching losses but lower conduction loss. So, at high frequency applications, PMOSFET is the obvious choice. But at lower operating frequencies (less than about 10 to 20 kHz), BJT is superior.
- (iv) PMOSFET is voltage controlled device whereas BJT is current controlled device.
- (v) PMOSFET has positive temperature coefficient for resistance. This makes parallel operation of PMOSFETs easy. If a PMOSFET shares increased current initially, it heats up faster, its resistance rises and this increased resistance causes this current to shift to other devices in parallel. A BJT has negative temperature coefficient, so current sharing resistors are necessary during parallel operation of BJTs.
- (vi) In PMOSFETs, secondary breakdown does not occur, because it has positive temperature coefficient. As BJT has negative temperature coefficient, secondary breakdown does occur. In BJT, with decrease in resistance with rise in temperature, the current increases. This increased current over the same area results in hot spots and breakdown of the BJT.
- (vii) PMOSFETs in higher voltage ratings have more conduction loss.
- (viii) The state of the art PMOSFETs are available with ratings upto 500 V, 140 A whereas BJTs are available with ratings upto 1200 V, 800 A.

2.7 INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

IGBT has been developed by combining into it the best qualities of both BJT and PMOSFET. Thus an IGBT possesses high input impedance like a PMOSFET and has low on-state power loss as in a BJT. Further, IGBT is free from second breakdown problem present in BJT. All these merits have made IGBT very popular amongst power-electronics engineers. IGBT is also known as metal oxide insulated gate transistor (MOSIGT), conductively-modulated field effect transistor (COMFET) or gain-modulated FET (GEMFET). It was also initially called insulated gate transistor (IGT).

2.7.1 Basic Structure

Fig. 2.19 illustrates the basic structure of an IGBT. It is constructed virtually in the same manner as a power MOSFET. There is, however, a major difference in the substrate. The n^- layer substrate at the drain in a PMOSFET is now substituted in the IGBT by a p^+ layer substrate called collector C. Like a power MOSFET, an IGBT has also thousands of basic structure cells connected appropriately on a single chip of silicon.

In IGBT, p^+ substrate is called *injection layer* because it injects holes into n^- layer. The n^- layer is called drift region. As in other semiconductor devices, thickness of n^- layer determines the voltage blocking capability of IGBT. The p layer is called body of IGBT. The n^- layer in between p^+ and p regions serves to accommodate the depletion layer of pn^- junction, i.e. junction J_2 .

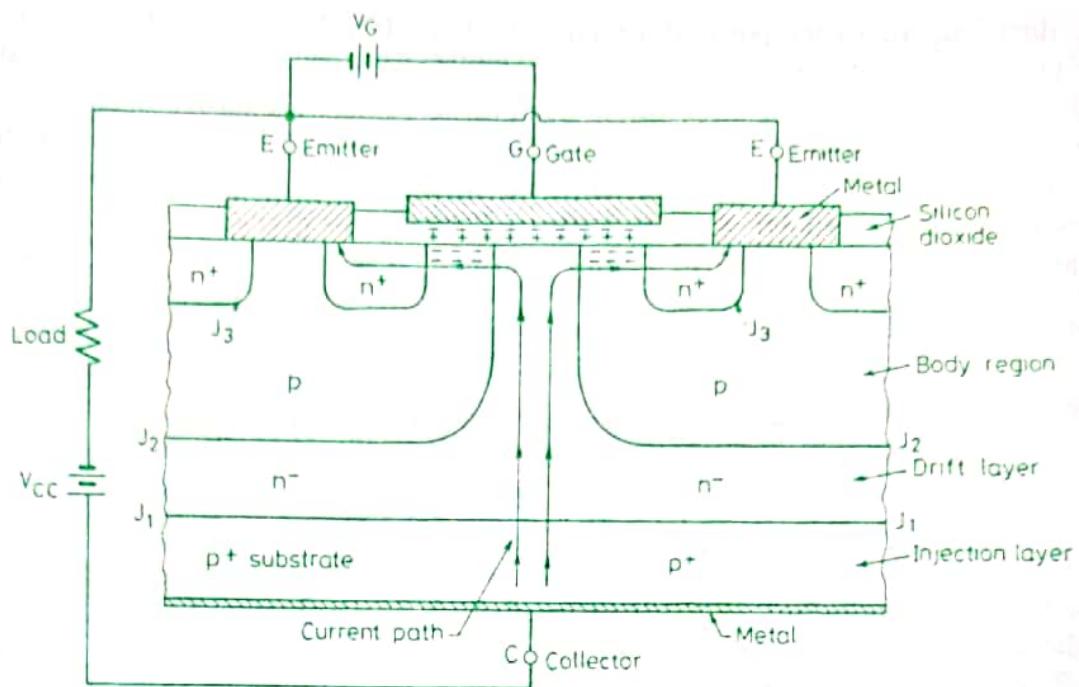


Fig. 2.19. Basic structure of an insulated gate bipolar transistor (IGBT).

2.7.2 Equivalent Circuit

An examination of Fig. 2.19 reveals that if one moves vertically up from collector to emitter, one comes across p^+ , n^- , p layers. Thus, IGBT can be thought of as the combination of MOSFET and p^+n^-p transistor Q_1 as shown in Fig. 2.20 (a). In this figure, R_d is the resistance offered by n^- drift region. From Fig. 2.20 (a), an approximate equivalent circuit, as shown in Fig. 2.20 (b), can be obtained where R_{ch} is the n -channel resistance.

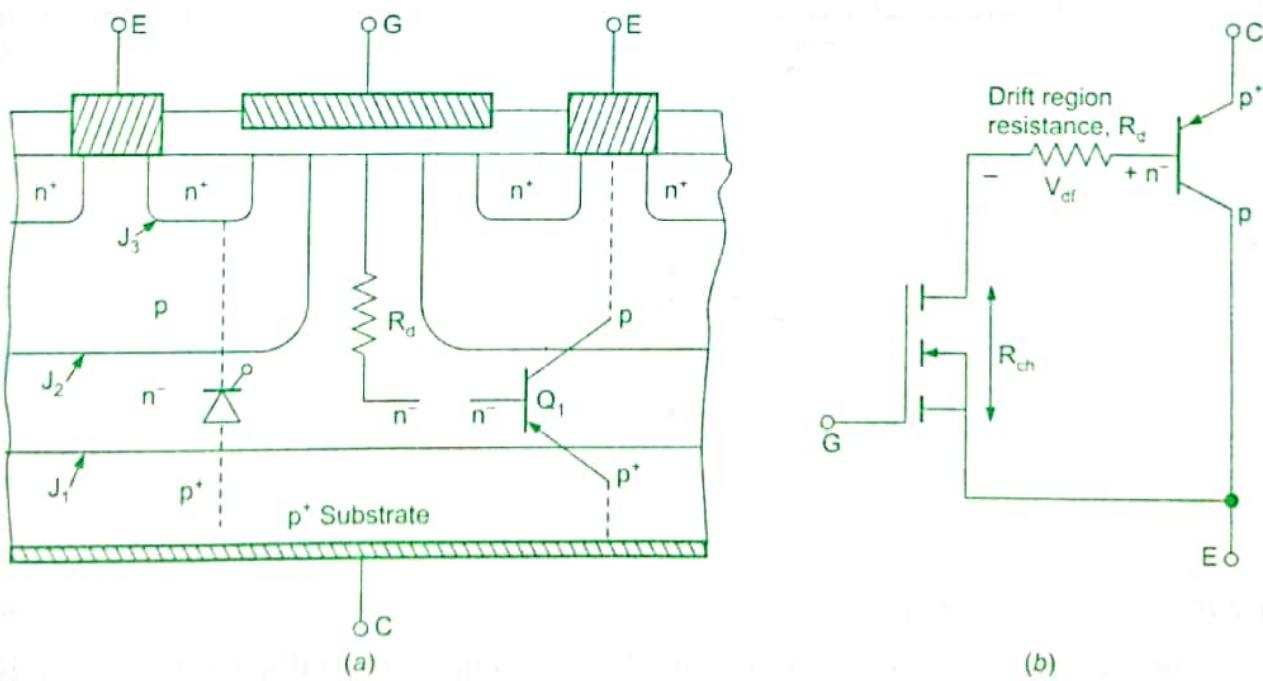


Fig. 2.20. IGBT (a) basic structure showing parasitic transistor Q_1 and R_d (b) approximate equivalent circuit.

For deriving an exact equivalent circuit of an IGBT, refer to Fig. 2.20 (c) where transistor Q_1 is shown as p^+n^-p and R_{by} is the p -body resistance. This figure also shows that another Q_2 is formed by layers n^-p and n^+ . Therefore, IGBT structure is equivalent to two transistors, Q_1 as p^+n^-p and Q_2 as n^-pn^+ . Note that collector p of Q_1 is the same as base of Q_2 . Similarly, Q_1 base n^- is the same as collector of Q_2 . The interconnection between two transistors Q_1 and Q_2 is shown in Fig. 2.20 (d). This figure gives the complete equivalent circuit of an IGBT. Here R_{by} is the resistance offered by p region to the flow of hole current I_h .

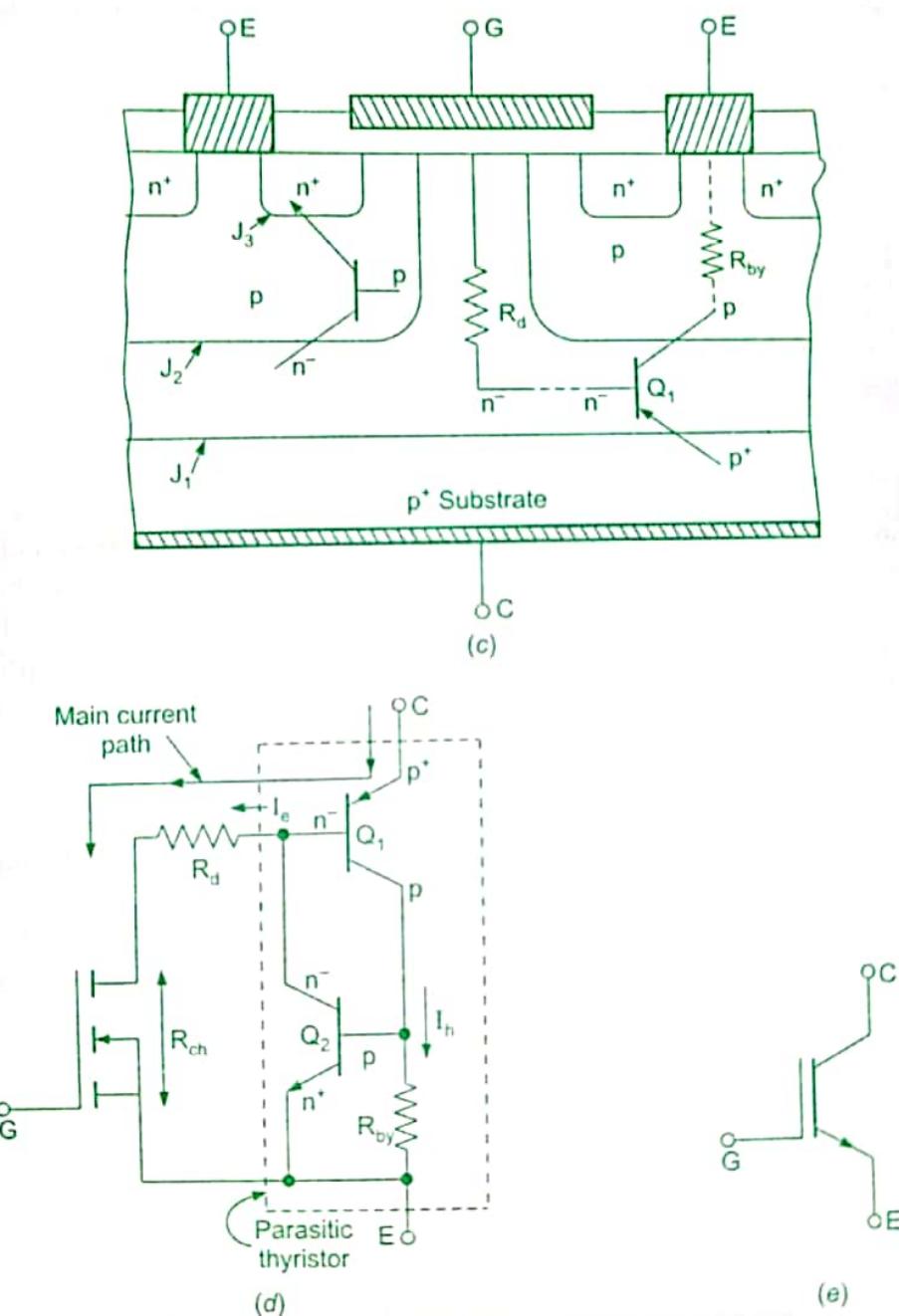


Fig. 2.20. IGBT (c) basic structure showing parasitic transistors (d) exact equivalent circuit and (e) circuit symbol.

The two transistor equivalent circuit shown in Fig. 2.20 (d) illustrates that an IGBT structure has a parasitic thyristor in it. Parasitic thyristor is also shown dotted in Fig. 2.20 (a) and in Fig. 2.20 (d). Fig. 2.20 (e) gives the circuit symbol of an IGBT.

2.7.3 Working

When collector is made positive with respect to emitter, IGBT gets forward biased. With no voltage between gate and emitter, two junctions between n^- region and p region (*i.e.* junction J_2) are reverse biased; so no current flows from collector to emitter, Fig. 2.19.

When gate is made positive with respect to emitter by voltage V_G , with gate-emitter voltage more than the threshold voltage V_{GET} of IGBT, an n -channel or *inversion layer*, is formed in the upper part of p region just beneath the gate, as in PMOSFET, Fig. 2.19. This n -channel short-circuits the n^- region with n^+ emitter regions. Electrons from the n^+ emitter begin to flow to n^- drift region through n -channel. As IGBT is forward biased with collector positive and emitter negative, p^+ collector region injects holes into n^- drift region. In short, n^- drift region is flooded with electrons from p -body region and holes from p^+ collector region. With this, the injection carrier density in n^- drift region increases considerably and as a result, conductivity of n^- region enhances significantly. Therefore, IGBT gets turned on and begins to conduct forward current I_C .

Collector current I_C or emitter current I_E , consists of two current components : (i) hole current I_h due to injected holes flowing from collector, p^+n^-p transistor Q_1 , p -body region resistance R_{by} and emitter Fig. 2.20 (d) and (ii) electronic current I_e due to injected electrons flowing from collector, injection layer p^+ , drift region n^- , n -channel resistance R_{ch} , n^+ and emitter. This means that collector, or load, current $I_C = \text{emitter current } I_E = I_h + I_e$.

Major component of collector current is electronic current I_e , $\therefore I_C \approx I_E$. Main current path for collector, or load, current is through p^+ , n^- , drift resistance R_d and n -channel resistance R_{ch} as shown in Fig. 2.20 (c). Therefore, the voltage drop in IGBT in its on-state is

$$\begin{aligned} V_{CE.on} &= I_C \cdot R_{ch} + I_C \cdot R_d + V_{j1} \\ &= \text{Voltage drop [in } n\text{-channel + across drift in } n^- \text{ region} \\ &\quad + \text{across forward biased } p^+n^- \text{ junction } J_1] \end{aligned}$$

Here V_{j1} is usually 0.7 to 1 V as in a $p-n$ diode. The voltage drop $I_c \cdot R_{ch}$ is due to n -channel resistance, almost the same as in a PMOSFET. The voltage drop $V_{df} = I_c \cdot R_d$ in IGBT is much less than that in PMOSFET. It is due to substantial increase in the conductivity caused by injection of electrons and holes in n^- drift region. The conductivity enhancement is the main reason for low on-state voltage drop in IGBT than it is in PMOSFET.

2.7.4 Latch-up in IGBT

It is seen from Fig. 2.20 (a) and (c) that IGBT structure has two inherent transistors Q_1 and Q_2 , which constitute a parasitic thyristor. When IGBT is on, the hole-current flows through transistor p^+n^-p and p -body resistance R_{by} . If load current I_c is large, hole component of current I_h would also be large. This large current would increase the voltage drop $I_h \cdot R_{by}$ which may forward bias the base p -emitter n^+ junction of transistor Q_2 . As a consequence, parasitic transistor Q_2 gets turned on which further facilitates in the turn-on of parasitic transistor p^+n^-p labelled Q_1 . The parasitic thyristor, consisting of Q_1 and Q_2 , eventually latches on through regenerative action, when sum of their current gains $\alpha_1 + \alpha_2$ reaches unity as in a conventional thyristor (discussed in chapter 4). With parasitic thyristor on, IGBT latches up and after this, collector emitter current is no longer under the control of gate terminal. The only way now to turn-off the latched up IGBT is by forced commutation of current as is done in a conventional thyristor. If this latch up is not aborted quickly, excessive power dissipation may destroy the IGBT. The latch up discussed here occurs when the collector current I_{CE} exceeds a certain critical value. The device manufacturer's always



specify the maximum permissible value of load current I_{CE} that IGBT can handle without latch up.

At present, several modifications in the fabrication techniques are listed in the literature which are used to avoid latch-up in IGBTs. As such, latch-up free IGBTs are available.

2.7.5 IGBT Characteristics

The circuit of Fig. 2.21 (a) shows the various parameters pertaining to IGBT characteristics.

Static I-V or output characteristics of an IGBT (*n*-channel type) show the plot of collector current I_c versus collector-emitter voltage V_{CE} for various values of gate-emitter voltage V_{GE} for various values of gate-emitter voltage V_{GE} etc. These characteristics are shown in Fig. 2.21 (b). In the forward voltages V_{GE1} , V_{GE2} etc. The direction, the shape of the output characteristics is similar to that of BJT. But here the controlling parameter is gate-emitter voltage V_{GE} because IGBT is a voltage-controlled device. When the device is off, junction J_2 blocks forward voltage and in case reverse voltage appears across collector and emitter, junction J_1 blocks it. In Fig. 2.21 (b), V_{RM} is the maximum reverse breakdown voltage.

The transfer characteristic of an IGBT is a plot of collector current I_C versus gate-emitter voltage V_{GE} as shown in Fig. 2.21 (c). This characteristic is identical to that of power MOSFET. When V_{GE} is less than the threshold voltage V_{GET} , IGBT is in the off-state.

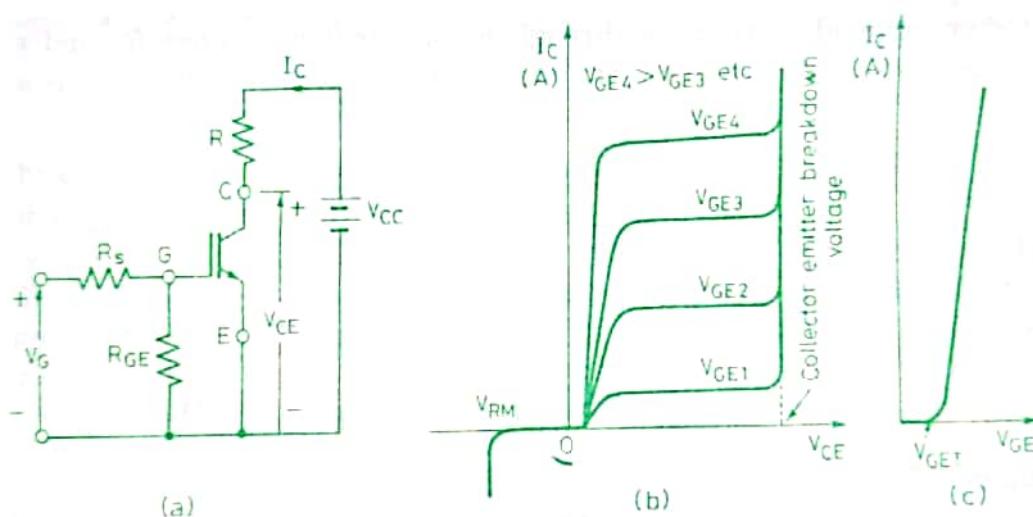
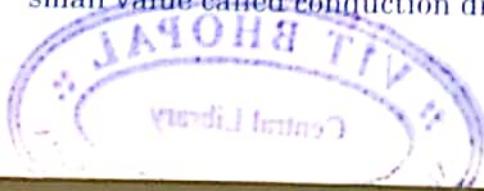


Fig. 2.21. IGBT (a) circuit diagram (b) static I-V characteristics and (c) transfer characteristics.

2.7.6 Switching Characteristics

Switching characteristics of an IGBT during turn-on and turn-off are sketched in Fig. 2.22. The turn-on time is defined as the time between the instants of forward blocking to forward on-state (7). Turn-on time is composed of delay time t_{dn} and rise time t_r , i.e. $t_{on} = t_{dn} + t_r$. The *delay time* is defined as the time for the collector-emitter voltage to fall from V_{CE} to $0.9 V_{CE}$. Here V_{CE} is the initial collector-emitter voltage. Time t_{dn} may also be defined as the time for the collector current to rise from its initial leakage current I_{CE} to $0.1 I_C$. Here I_C is the final value of collector current.

The *rise time* t_r is the time during which collector-emitter voltage falls from $0.9 V_{CE}$ to $0.1 V_{CE}$. It is also defined as the time for the collector current to rise from $0.1 I_C$ to its final value I_C . After time t_{on} , the collector current is I_C and the collector-emitter voltage falls to small value called conduction drop = V_{CES} where subscript *S* denotes saturated value.



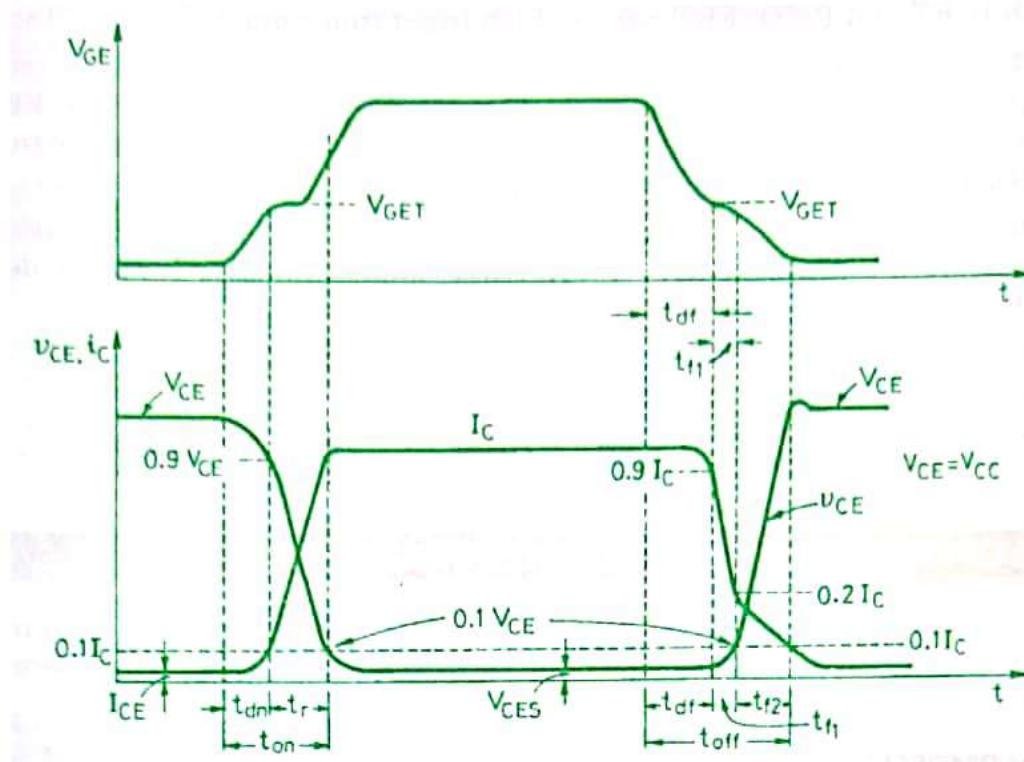


Fig. 2.22. IGBT turn-on and turn-off characteristics.

The turn-off time is somewhat complex. It consists of three intervals : (i) delay time, t_{df} (ii) initial fall time, t_{f1} and (iii) final fall time, t_{f2} ; i.e. $t_{off} = t_{df} + t_{f1} + t_{f2}$. The delay time is the time during which gate voltage falls from V_{GE} to threshold voltage V_{GET} . As V_{GE} falls to V_{GET} during t_{df} , the collector current falls from I_C to $0.9 I_C$. At the end of t_{df} , collector-emitter voltage begins to rise. The first fall time t_{f1} is defined as the time during which collector current falls from 90 to 20% of its initial value I_C , or the time during which collector-emitter voltage rises from V_{CES} to $0.1 V_{CE}$.

The final fall time t_{f2} is the time during which collector current falls from 20 to 10% of I_C , or the time during which collector-emitter voltage rises from $0.1 V_{CE}$ to final value V_{CE} , see Fig. 2.22.

2.7.7 Application of IGBTs

IGBTs are widely used in medium power applications such as dc and ac motor drives, UPS systems, power supplies and drives for solenoids, relays and contactors. Though IGBTs are somewhat more expensive than BJTs, yet they are becoming popular because of lower gate-drive requirements, lower switching losses and smaller snubber circuit requirements. IGBT converters are more efficient with less size as well as cost, as compared to converters based on BJTs. Recently, IGBT inverter induction-motor drives using 15-20 kHz switching frequency are finding favour where audio-noise is objectionable. In most applications, IGBTs will eventually push out BJTs. At present, the state of the art IGBTs of 1200 V, 500 A ratings, 0.25 to 20 μ s turn-off time with operating frequency upto 50 kHz are available.

2.7.8 Comparison of IGBT with MOSFET

The relative merits and demerits of IGBT over PMOSFET are enumerated below :

- In PMOSFET, the three terminals are called gate, source, drain whereas the corresponding terminals for IGBT are gate, emitter and collector.

- (ii) Both IGBT and PMOSFET possess high input impedance.
- (iii) Both are voltage-controlled devices.
- (iv) With rise in temperature, the increase in on-state resistance in PMOSFET is much pronounced than it is in IGBT. So, on-state voltage drop and losses rise rapidly in PMOSFET than in IGBT, with rise in temperature.
- (v) With rise in voltage rating, the increment in on-state voltage drop is more dominant in PMOSFET than it is in IGBT. This means IGBTs can be designed for higher-voltage ratings than PMOSFETs.

In view of the above comparison, (a) PMOSFETs are available upto about 500 V, 140 A ratings whereas state of the art IGBTs have 1200 V, 500 A ratings and (b) operating frequency in PMOSFETs is upto about 1 MHz whereas its value is upto about 50 kHz in IGBTs.

2.8 SAFE OPERATING AREAS FOR PMOSFET AND IGBT

Safe operating area (SOA) of any semiconductor device specifies the maximum value of current and voltage which the device can handle without any harm to it. Here SOAs are considered first for PMOSFET and then for IGBT.

2.8.1 SOA for PMOSFET

For a PMOSFET, SOA specifies limits of drain current I_D and drain-source voltage V_{DS} as shown in Fig. 2.23. For reliable operation of PMOSFET, I_D and V_{DS} must fall within this area. The scale for both I_D and V_{DS} is logarithmic.

Boundary AD is the maximum limit for dc and continuous current for V_{DS} less than about 20 V. For V_{DS} more than 20 V, drain current has to be reduced to boundary DE so that junction temperature does not exceed the maximum rated value T_{Jm} of PMOSFET. Boundary EC gives the maximum voltage capability V_{DSM} for this PMOSFET.

For pulsed operation, PMOSFET can dissipate more peak power so long as average power loss is within safe limits of junction temperature. For pulsed operation, $I_{DM} = OB$ is the maximum limit for drain current. As pulse width decreases from 1 ms to 0.01 ms, the SOA increases as shown in Fig. 2.23. For switched-mode operation, SOA is almost square with $OB = I_{DM}$ and $OC = V_{DSM}$ as the limiting boundaries. It is because for a few microsecond turn-on, the heat energy generated in PMOSFET is too meagre to cause any noticeable rise in junction temperature.

There is no distinction between forward-bias SOA and reverse-bias SOA for a PMOSFET, these are identical.

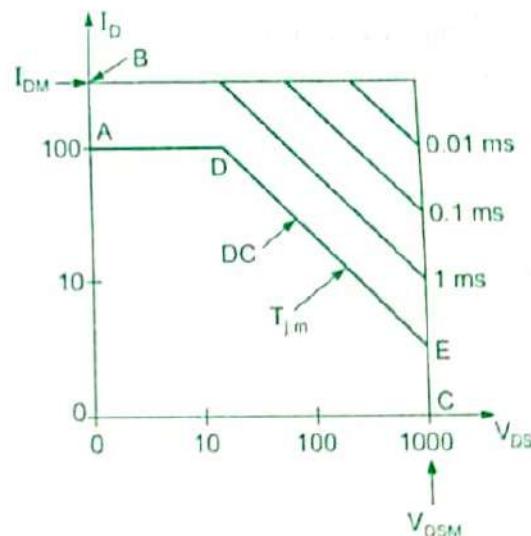


Fig. 2.23. SOA of PMOSFET.

2.8.2 SOA for IGBT

An IGBT has both FBSOA during turn-on and RBSOA during turn-off. The FBSOA (forward-bias safe operating area) is similar to PMOSFET. Scales for both I_C and V_{CE} are logarithmic. Maximum collector current is OA for dc and for voltages upto $V_{CE} = AB$. For $V_{CE} > AB$, I_C decreases. As pulse width of load current reduces, FBSOA gets increased as shown in Fig. 2.24 (a).

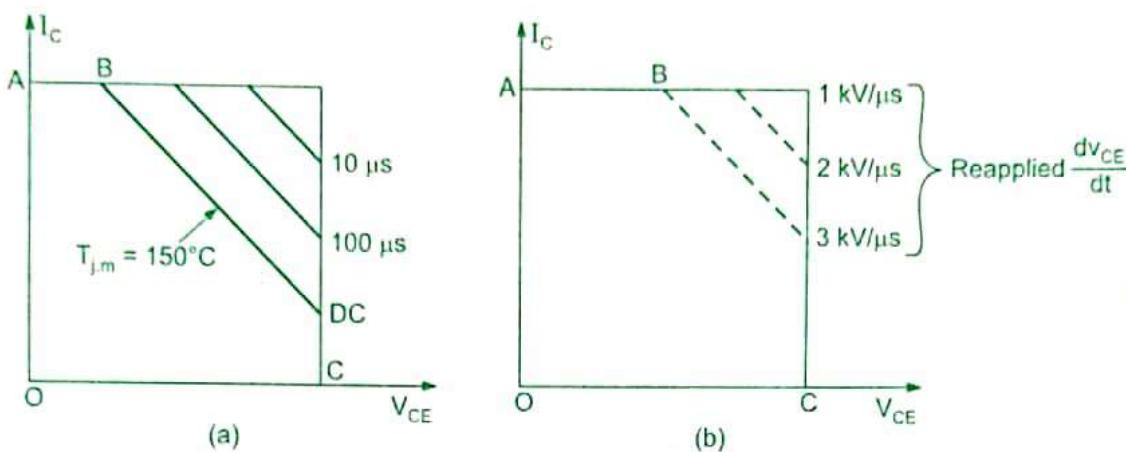


Fig. 2.24. SOA of IGBT (a) FBSOA (b) RBSOA.

The reverse-bias safe-operating area RBSOA is different from FBSOA. At the turn-off of IGBT, if the reapplied $\frac{dv_{CE}}{dt}$ increases, the RBSOA gets reduced as shown in Fig. 2.24 (b).

The large value of reapplied $\frac{dv_{CE}}{dt}$ causes latch-up or turn-on of IGBT just as a thyristor gets turned on by reapplied dv/dt . In an IGBT, if C_{j2} is the junction capacitance of reverse biased junction J_2 , then $C_{j2} \times \frac{dv_{CE}}{dt}$ may act as collector-emitter current. If this value is large, IGBT may get latched up which is undesirable. Therefore, as $\frac{dv_{CE}}{dt}$ increases, the RBSOA becomes smaller so as to avoid latch-up.

OA is the maximum value of I_C upto voltage $V_{CE} = AB$. If $\frac{dv_{CE}}{dt} = 3000 \text{ V}/\mu\text{s}$, I_C must be lowered for V_{CE} greater than AB .

2.9 STATIC INDUCTION TRANSISTOR (SIT)

SIT is a high-power high-frequency semiconductor device. It is the solid-state version of triode vacuum tube. SIT was commercially introduced by Tokin Corporation of Japan in 1987.

Basic structure of SIT is shown in Fig. 2.25 (a) and its symbol in Fig. 2.25 (b). It is basically n^+ n^- n device with a buried grid-like p^+ gate structure. It has short n -channel

structure and p^+ gate electrodes are buried in n^-n epi-layers as shown. The buried gate structure gives lower gate-source channel resistance, lower gate source capacitance and lower thermal resistance.

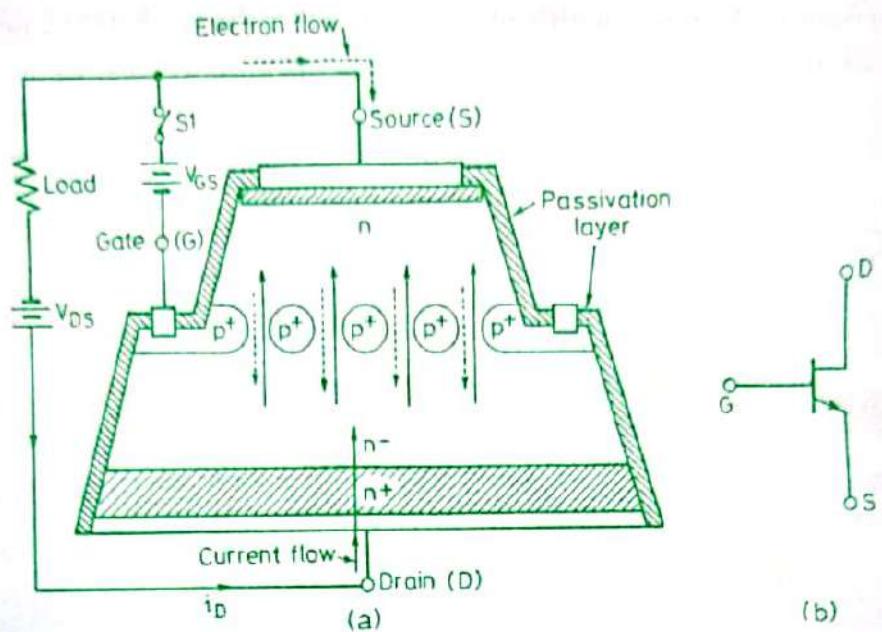


Fig. 2.25. (a) Basic structure of SIT (b) device symbol.

SIT is normally an on device, i.e. if $V_{GS} = 0$ with V_{DS} present, electrons (majority carriers) would flow from source S to n , pass through gaps in between gate p^+ electrodes and would then continue their journey through n^- , n^+ and reach drain as shown in Fig. 2.25 (a). The drain current I_D would flow from D to S as shown. If V_{GS} is negative, $p^+ n$ junctions get reverse biased. As a result, depletion layer is formed around p^+ electrodes and this reduces the current flow from its value when $V_{GS} = 0$, Fig. 2.26 (a). At some higher value of reverse bias voltage V_{GS} , the depletion layer would grow to such an extent as to cut-off the channel completely, Fig. 2.26 (b) and load current i_D would, therefore, be zero.

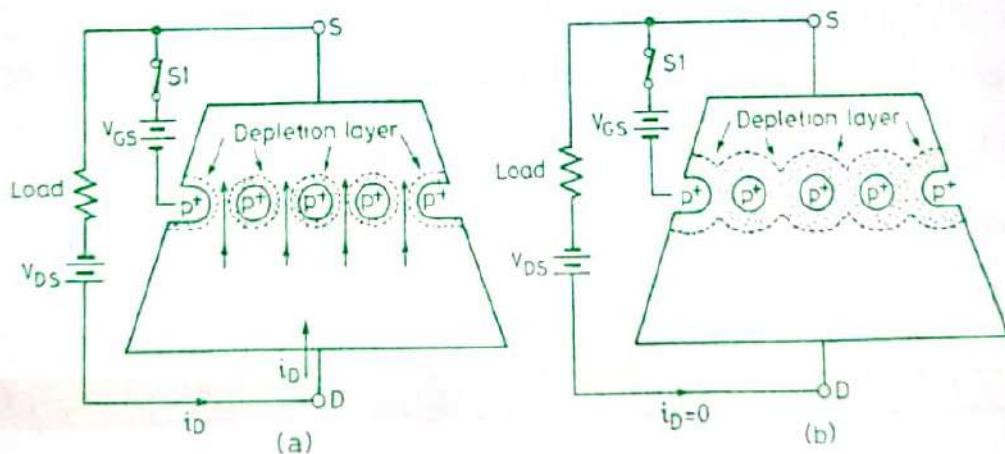


Fig. 2.26. (a) Lower reverse bias, load current i_D reduced due to depletion layer
(b) higher reverse bias, expanded depletion layer stops current flow.

Although, the device conduction drop is lower than that of equivalent series-parallel operation of PMOSFETs, the essentially large drop in SIT makes it unsuitable for general

power-electronic applications. For example, a 1500 V, 180 A SIT has a channel resistance of 0.5Ω giving 90 V conduction drop at 180 A. An equivalent thyristor or GTO drop may be around 2 V [11]. Though conduction drop in SIT is abnormally high, the turn-on and turn-off times of the device are very low. For the SIT cited above, typical t_{on} and t_{off} are around $0.35 \mu\text{s}$. High conduction drop associated with very low turn-on and turn-off times result in low on-off energy losses. Thus, SIT is being used in high-power, high-frequency applications such as AM/FM transmitters, induction heaters, high-voltage low-current power supplies, ultrasonic generators etc. SITs with 1200 V, 300 A rating with t_{on} and t_{off} around 0.25 to $0.35 \mu\text{s}$ and 100 kHz operating frequency are available.

SIT is a majority carrier (electrons only) device, therefore SOA is limited by junction temperature. As channel resistance rises with temperature, parallel operation of SITs is easy.

SIT is normally-on device, normally-off device is under development.

2.10 MOS-CONTROLLED THYRISTOR (MCT)

An MCT is a new device in the field of semiconductor-controlled devices. It is basically a thyristor with two MOSFETs built into the gate structure. One MOSFET is used for turning on the MCT and the other for turning off the device. An MCT is a high-frequency, high-power, low-conduction drop switching device.

An MCT combines into it the features of both conventional four-layer thyristor having regenerative action and MOS-gate structure. However, in MCT, anode is the reference with respect to which all gate signals are applied. In a conventional SCR, cathode is the reference terminal for gate signals.

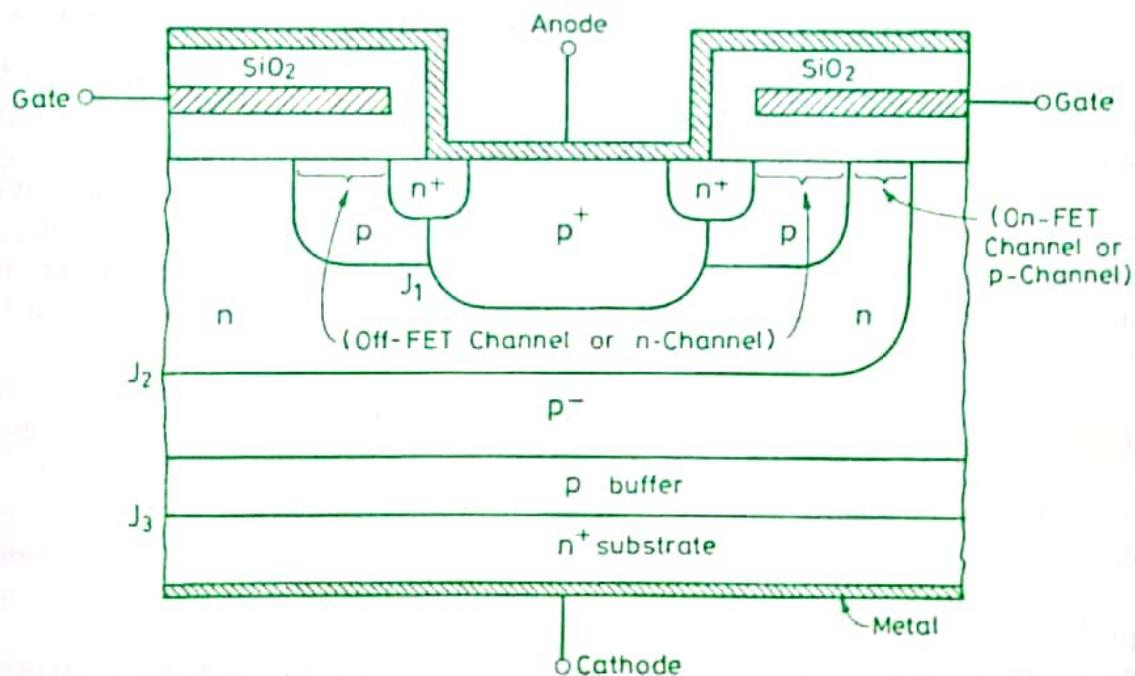


Fig. 2.27. Basic structure of an MCT.

The basic structure of an MCT cell is shown in Fig. 2.27. A practical MCT consists of thousands of these basic cells connected in parallel, just like a PMOSFET [7, 8]. This is done in order to achieve a high-current carrying capacity of the device.

The equivalent circuit of MCT is shown in Fig. 2.28 (a). It consists of one on-FET, one off-FET and two transistors. One on-FET, a *p*-channel MOSFET and the other off-FET, an *n* channel MOSFET, represent MOS-gate structure of MCT. The *nppn* structure of MCT is represented by two transistors *npn* and *pnp* as shown in Fig. 2.28 (a). An arrow towards the gate terminal indicates *n*-channel MOSFET and the arrow away from the gate terminal as the *p*-channel MOSFET. The two transistors in the equivalent circuit indicate that there is regenerative feedback in the MCT just as it is in an ordinary thyristor. Fig. 2.28 (b) gives the circuit symbol of an MCT.

An MCT is turned-on by a negative voltage pulse at the gate with respect to the anode and is turned-off by a positive voltage pulse. Working of MCT can be understood better by referring to the equivalent circuit of Fig. 2.28 (a).

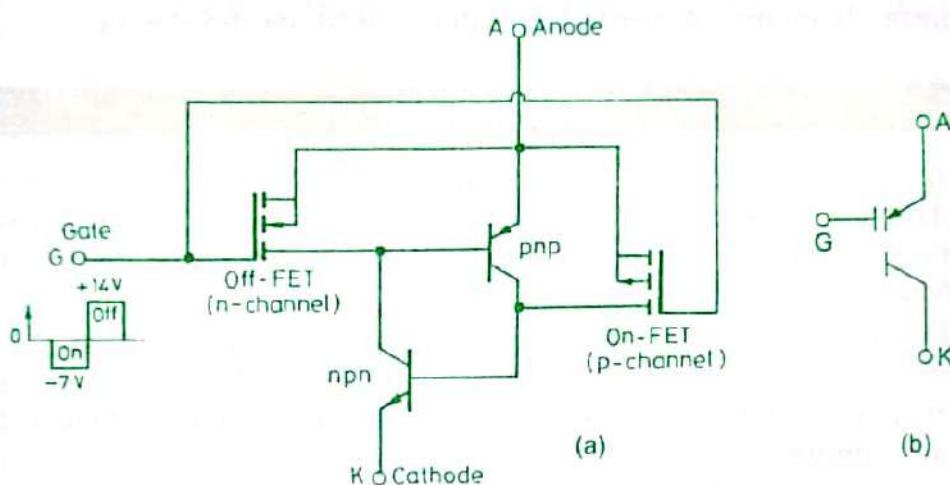


Fig. 2.28. MCT (a) equivalent circuit and (b) circuit symbol.

Turn-on Process. As stated above, MCT is turned-on by applying a negative voltage pulse at the gate with respect to anode. In other words, for turning-on MCT, gate is made negative with respect to anode by the voltage pulse between gate and anode. Obviously, MCT must be initially forward biased and then only a negative voltage be applied. With the application of this negative voltage pulse, on-FET (*p*-channel) gets turned on whereas off-FET is already off. With on-FET on, current begins to flow from anode A, through on-FET and then as the base current and emitter current of *npn* transistor and then to cathode K. This turns on *npn* transistor.

As a result, collector current begins to flow in *npn* transistor. As off-FET is off, this collector current of *npn* transistor acts as the base current of *pnp* transistor. Subsequently, *pnp* transistor is also turned on. Once both the transistors are on, regenerative action of the connection scheme takes place and the thyristor or MCT is turned on.

Note that on-FET and *pnp* transistor are in parallel when MCT is in conduction state. During the time MCT is on, base current of *npn* transistor flows mainly through *pnp* transistor because of its better conducting property.

Turn-off process. For turning-off the MCT, off-FET (or *n*-channel MOSFET) is energized by positive voltage pulse at the gate. With the application of positive voltage pulse, off-FET is turned on and on-FET is turned off. After off-FET is turned on, emitter-base terminals of *pnp* transistor are short circuited by off-FET. So now anode current begins to flow through off-FET and therefore base current of *pnp* transistor begins to decrease.

Further, collector current of *pnp* transistor that forms the base current of *npn* transistor also begins to decrease. As a consequence, base currents of both *pnp* and *npn* transistors, now devoid of stored charge in their *n* and *p* bases respectively, begin to decay. This regenerative action eventually turns off the MCT.

In recent literature, the MOS-controlled thyristor described above is termed as P-MCT type [8].

Static I-V characteristics. An MCT has static I-V characteristics as shown in Fig. 2.29. This characteristic is similar to static I-V characteristic of a GTO. Like GTO, MCT has low reverse voltage blocking capability. MCT can be turned-on and turned-off by gate signal just like a GTO. An MCT gets turned-on and turned-off through regenerative action like an SCR.

In MCT, forward on-state voltage drop increases slightly with anode current as in a thyristor. It is a voltage-controlled device like PMOSFET and IGBT. It is necessary to keep the gate signal applied during both turn-on and turn-off states. In case gate signal goes to zero, there may be a possibility of unwanted turn-on or turn-off of MCT due to high dv/dt values appearing across MCT [8].

An MCT has the following merits :

- (i) low forward conduction drop,
- (ii) fast turn-on and turn-off times,
- (iii) low switching losses, and
- (iv) high gate input impedance, which allows simpler design of drive circuits.

Main disadvantage of MCT is its low reverse voltage blocking capability.

MCT was commercially introduced in 1992. At that time, it was predicted that its use as a power-semiconductor device would be so vast that it might challenge the existence of most of the other devices like SCR, BJT, GTO, IGBT etc. This has, however, not happened because an MCT has (i) limited reverse-biased SOA and (ii) its switching frequency is much inferior to IGBT. At present, MCTs are being promoted for their use in soft switched converter topologies, where these inferiorities do not inhibit their use.

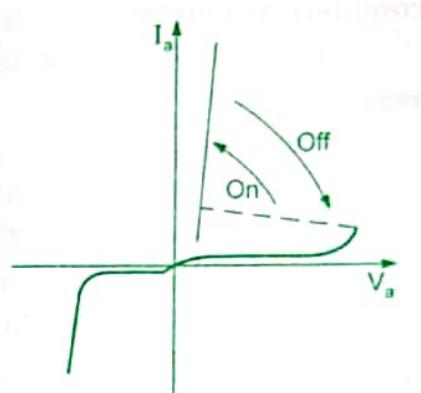


Fig. 2.29. Static I-V characteristics of an MCT.

2.11 NEW SEMICONDUCTING MATERIALS

At present, silicon enjoys monopoly as a semiconductor material for the commercial production of power-control devices. This is because silicon is cheaply available and semiconductor devices of any size can be easily fabricated on a single silicon chip. There are, however, new types of materials like gallium arsenide, silicon carbide and diamond which possess the desirable properties required for switching devices. At present, state-of-the-art technology for these materials is primitive compared with silicon, and many more years of research investment are required before these materials become commercially viable for the production of power-controlled devices.

Out of the new materials gallium arsenide, silicon carbide and semiconducting diamond, silicon-carbide possesses favourable characteristics for the manufacture of power-semiconductor devices. It is because silicon-carbide devices operate better than gallium arsenide devices. Also silicon-carbide technology is better developed than for the diamond. It is expected that silicon-carbide based devices will be commercially available quite soon. But diamond-based power devices will take a longer time to enter the commercial market.

Germanium is not used in the fabrication of thyristors because of the following reasons :

- (i) Germanium has much lower thermal conductivity ; its thermal resistance is, therefore, more. As a consequence, germanium thyristors suffer from more losses, more temperature rise and therefore lower operating life.
- (ii) Its breakdown voltage is much less than that of silicon. It means that germanium thyristor can be built for small voltage ratings only.
- (iii) Germanium is much costlier than silicon.

PROBLEMS

- 2.1.** (a) Why are semiconductor materials designated as p^+ , p^- , n^- , n^+ ? Explain.
 (b) What is p - n junction ? Discuss the formation of depletion layer in p - n junction.
 (c) What is barrier potential ? How are depletion layer and barrier potential effected by temperature ?
- 2.2.** (a) Explain the effect of forward bias and reverse bias on the depletion layer in a p - n junction.
 (b) How is the magnitude of breakdown voltage effected if a junction has highly doped (i) layers on its both sides and (ii) layer on its one side only.
 (c) Describe the structural features of power diodes. How do these differ from signal diodes ?
- 2.3.** (a) What is a diode ? Discuss i - v characteristics of power, signal and ideal diodes.
 (b) Describe reverse recovery characteristics of diodes. Show that reverse recovery time and peak inverse current are dependent upon storage charge and rate of change of current.
- 2.4.** (a) Describe the various types of power diodes indicating clearly the differences amongst them.
 (b) What is cut-in voltage in a diode ? What are other terms used for cut in voltage ?
 (c) Discuss the following terms for diodes :
 Softness factor, PIV, reverse recovery time, reverse recovery current.
 (d) For a power diode, the reverse recovery time is $3.9 \mu\text{s}$ and the rate of diode-current decay is $50 \text{ A}/\mu\text{s}$. For a softness factor of 0.3, calculate the peak inverse current and the storage charge.
[Ans. (d) 150 A, $292.5 \mu\text{C}$]

- 2.5.** (a) Discuss the power loss in a diode during the reverse recovery transients.
 (b) The forward characteristic of a power diode can be represented by $v_f = 0.88 + 0.015 i_f$. Determine the average power loss and rms current for a constant current of 50 A for 2/3 of a cycle.

[Hint. (b) With T as the time of a cycle, average power loss

$$= \frac{1}{T} \int_0^{2T/3} v_f \cdot I_f dt = \frac{2}{3} \cdot v_f I_f \text{ etc.}$$

[Ans. (b) 54.33 W, 40.825 A]

- 2.6.** (a) Enumerate the types of power transistors along with their circuit symbols.
 (b) What is a bipolar junction transistor? Why is it so called?
 Describe the types of BJTs with their circuit symbols.
 (c) Define α and β for BJT and develop a relation between the two. Why is α less than 1 and β more than 1?
 (d) Why is it preferable to use hard drive for BJT?
2.7. (a) What is the difference between β and forced β_f for BJTs?
 (b) What are the conditions under which a transistor operates as a switch?
 Discuss hard-drive and overdrive factors for BJT.
 (c) Show that collector current at saturation remains substantially constant even if base current is increased.
2.8. A bipolar transistor, with current gain $\beta = 50$, has load resistance $R_C = 10 \Omega$, dc supply voltage $V_{CC} = 120$ V and input voltage to base circuit, $V_B = 10$ V. For $V_{CES} = 1.2$ V and $V_{BES} = 1.6$ V, calculate
 (a) the value of R_B for operation in the saturated state
 (b) the value of R_B for an overdrive factor 6
 (c) forced current gain and
 (d) power loss in the transistor for both parts (a) and (b).

[Ans. (a) 35.354Ω (b) 5.892Ω (c) 8.33 (d) 14.6362 W, 16.537 W]

- 2.9.** (a) Explain the switching performance of BJT with relevant waveforms. Indicate clearly turn-on and turn-off times and their components.
 (b) Describe FBSOA and RBSOA for BJTs.

- 2.10.** (a) Describe the input and output characteristic for a BJT. Show the region of the transistor characteristic where it acts like a switch.
 (b) Typical switching waveforms for a power transistor are shown in Fig. 2.30. Show that switch-on energy

loss is given by $\frac{V_{CC} \cdot I_{CS}}{6} t_{on}$

Also obtain an expression for the average value of switch-on loss.

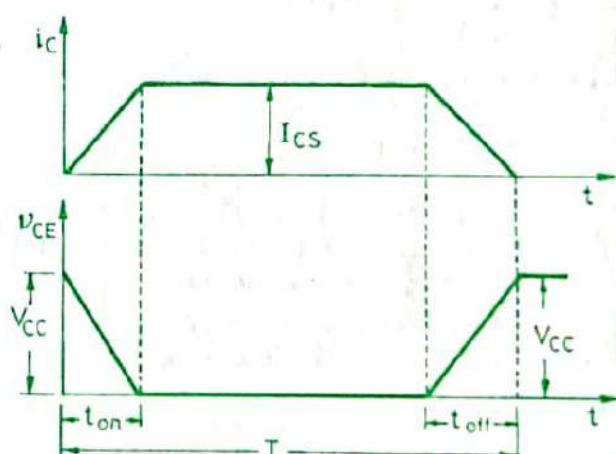


Fig. 2.30. Pertaining to Prob. 2.10 (b).

- (c) Derive expressions for the switch-off energy loss and also for its average value for the waveforms shown in Fig. 2.30.

$$\left[\text{Ans. (b)} \frac{V_{CC} \cdot I_{CS}}{6} f \cdot t_{on}, \text{(c)} \frac{V_{CC} \cdot I_{CS}}{6} t_{off}, \frac{V_{CC} \cdot I_{CS}}{6} f \cdot t_{off} \right]$$

- 2.11.** In case $I_{CS} = 80 \text{ A}$, $V_{CC} = 220 \text{ V}$, $t_{on} = 1.5 \mu\text{s}$ and $t_{off} = 4 \mu\text{s}$ for the switching waveforms shown in Fig. 2.30, find the energy loss during switch-on and switch-off intervals. Find also the average power loss in the power transistor for a switching frequency of 2 kHz.

Derive the expressions used.

[Ans. 4.4 mWs, 11.73 mWs, 32.267 W]

- 2.12.** (a) For the typical switching waveforms shown in Fig. 2.30 for a power transistor, find expressions that give peak instantaneous power loss during t_{on} and t_{off} intervals respectively.
 (b) In case $I_{CS} = 80 \text{ A}$, $V_{CC} = 220 \text{ V}$, $t_{on} = 1.5 \mu\text{s}$ and $t_{off} = 4 \mu\text{s}$, find the peak value of instantaneous power loss during t_{on} and t_{off} intervals respectively.

$$\left[\text{Ans. (a)} \frac{I_{CS} \cdot V_{CC}}{4}, \frac{I_{CS} \cdot V_{CC}}{4} \text{ (b) } 4400 \text{ W, } 4400 \text{ W} \right]$$

- 2.13.** A power transistor is used as a switch and typical waveforms are shown in Fig. 2.12 (a). The parameters for the transistor circuit are as under :

$$V_{CC} = 200 \text{ V}, V_{CES} = 2.5 \text{ V}, I_{CS} = 60 \text{ A}, t_d = 0.5 \mu\text{s}, t_r = 1 \mu\text{s}, \\ t_n = 40 \mu\text{s}, t_s = 4 \mu\text{s}, t_f = 3 \mu\text{s}, t_0 = 30 \mu\text{s}, f = 10 \text{ kHz}.$$

Collector to emitter leakage current = 1.5 mA.

Determine average power loss due to collector current during t_{on} and t_n . Find also the peak instantaneous power loss due to collector current during turn-on time.

Sketch the instantaneous power loss during t_{on} and t_n . [Ans. 20.5015 W, 60 W, 3037.97 W]

- 2.14.** Repeat Prob. 2.13 for obtaining average power loss during turn-off time and off-period, and also peak instantaneous power loss during fall time due to collector current.

Sketch the instantaneous power loss during turn-off time and off-period.

- 2.15.** Fig. 2.31 shows the switching characteristics for a power semiconductor device. Derive the expressions for energy loss during turn-on and turn-off periods, and also for the average switching loss. Sketch the variation of power loss during turn-on and turn-off periods.

For $V_s = 220 \text{ V}$, $I_a = 10 \text{ A}$, $t_1 = 1 \mu\text{s}$, $t_2 = 2 \mu\text{s}$, $t_3 = 1.5 \mu\text{s}$ and $t_4 = 3 \mu\text{s}$, find the average value of power-switching loss in the device for a switching frequency of 1 kHz.

$$\left[\text{Ans. } \frac{1}{2} V_s \cdot I_a (t_1 + t_2), \frac{1}{2} V_s I_a (t_3 + t_4), \frac{1}{2} V_s I_a f (t_{on} + t_{off}), 7.5 \text{ W} \right]$$

- 2.16.** (a) Explain the constructional details and working of low-power MOSFET and power MOSFET and bring out the differences between the two.
 (b) Discuss the transfer and output characteristics of power MOSFETs.

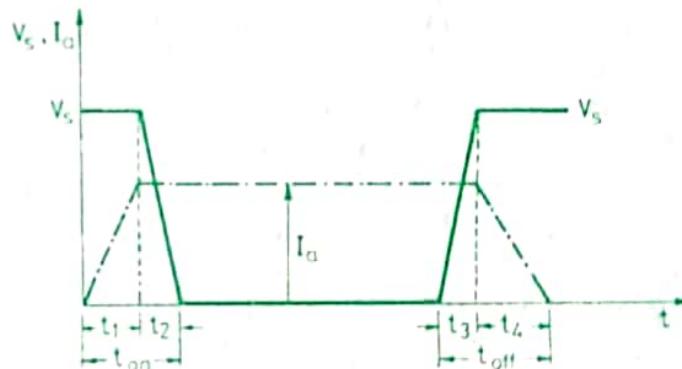


Fig. 2.31. Pertaining to Prob. 2.15.

[Ans. (a) Power diode (b) PMOSFET, SIT (c) Diode, BJT, IGBT, MCT
 (d) MCT (e) PMOSFET (f) SIT, SITH (g) BJT (h) Signal diode
 (i) Diode (j) BJT, MOSFET, IGBT, SIT, MCT, SITH and GTOI