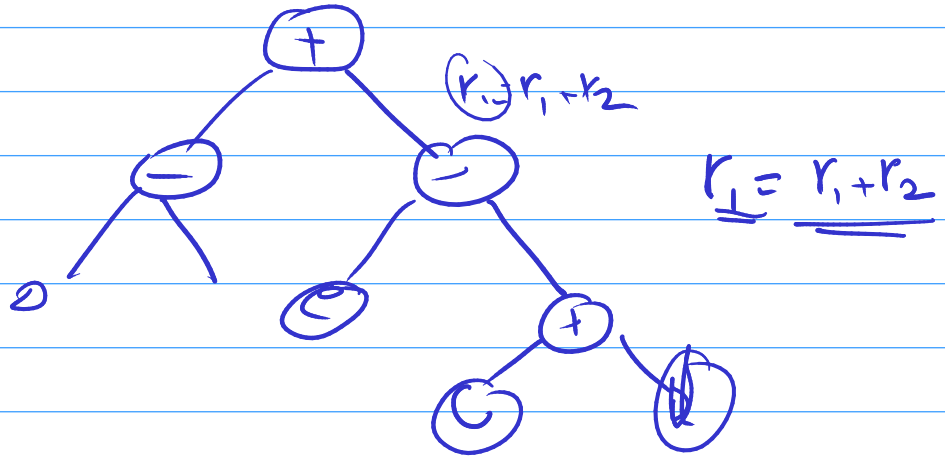
$(2+2+1+1+1)\times 500$

7×500

1 1 1 1 1

5



24 (34)

$34+(x-1)$

$12\times 4 = 48$ ns

$48+(x-1)12$

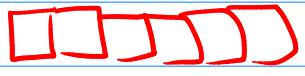
$11\times 4\times x$

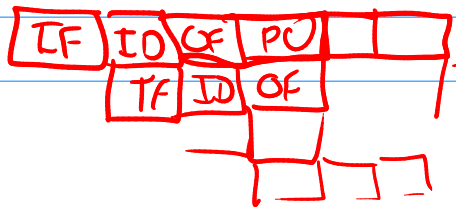
$36+12x = 44x$

$36 = 32x$

$\frac{9}{8}$

qmul	E2, R0, R1	3+3
Div	E5, R3, R4	6
ADD	E2, R5, E2	1
SUB	R5, E2, R6	1+1





A 5-stage pipelined processor has Instruction Fetch(IF),Instruction Decode(ID),Operand Fetch(OF),Perform Operation(PO)and Write Operand(WO)stages.The IF,ID,OF and WO stages take 1 clock cycle each for any instruction.The PO stage takes 1 clock cycle for ADD and SUB instructions,3 clock cycles for MUL instruction,and 6 clock cycles for DIV instruction respectively.Operand forwarding is used in the pipeline.What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
I0 :MUL R2 ,R0 ,R1	R2 ¬ R0 *R1
I1 :DIV R5 ,R3 ,R4	R5 ¬ R3/R4
I2 :ADD R2 ,R5 ,R2	R2 ¬ R5+R2
I3 :SUB R5 ,R2 ,R6	R5 ¬ R2-R6

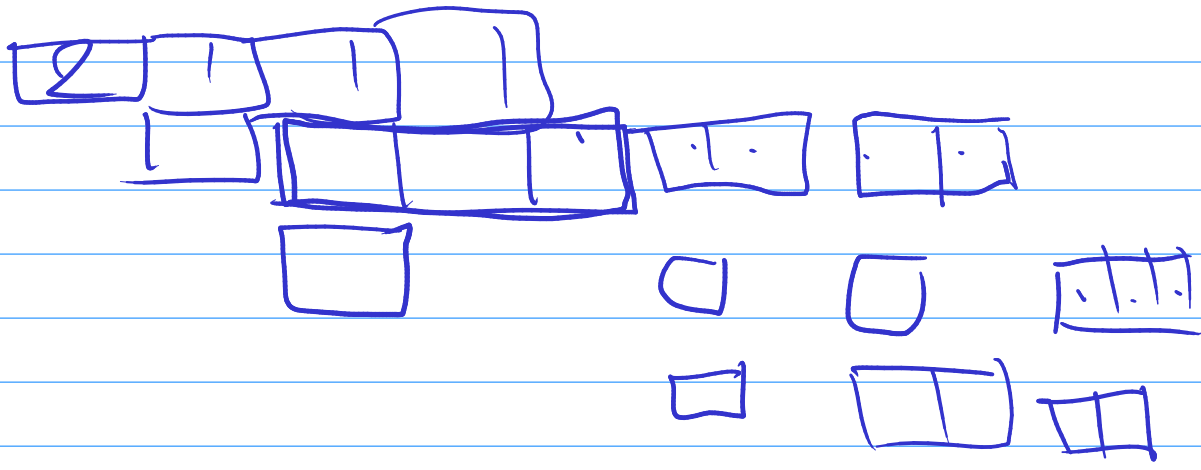
A 13

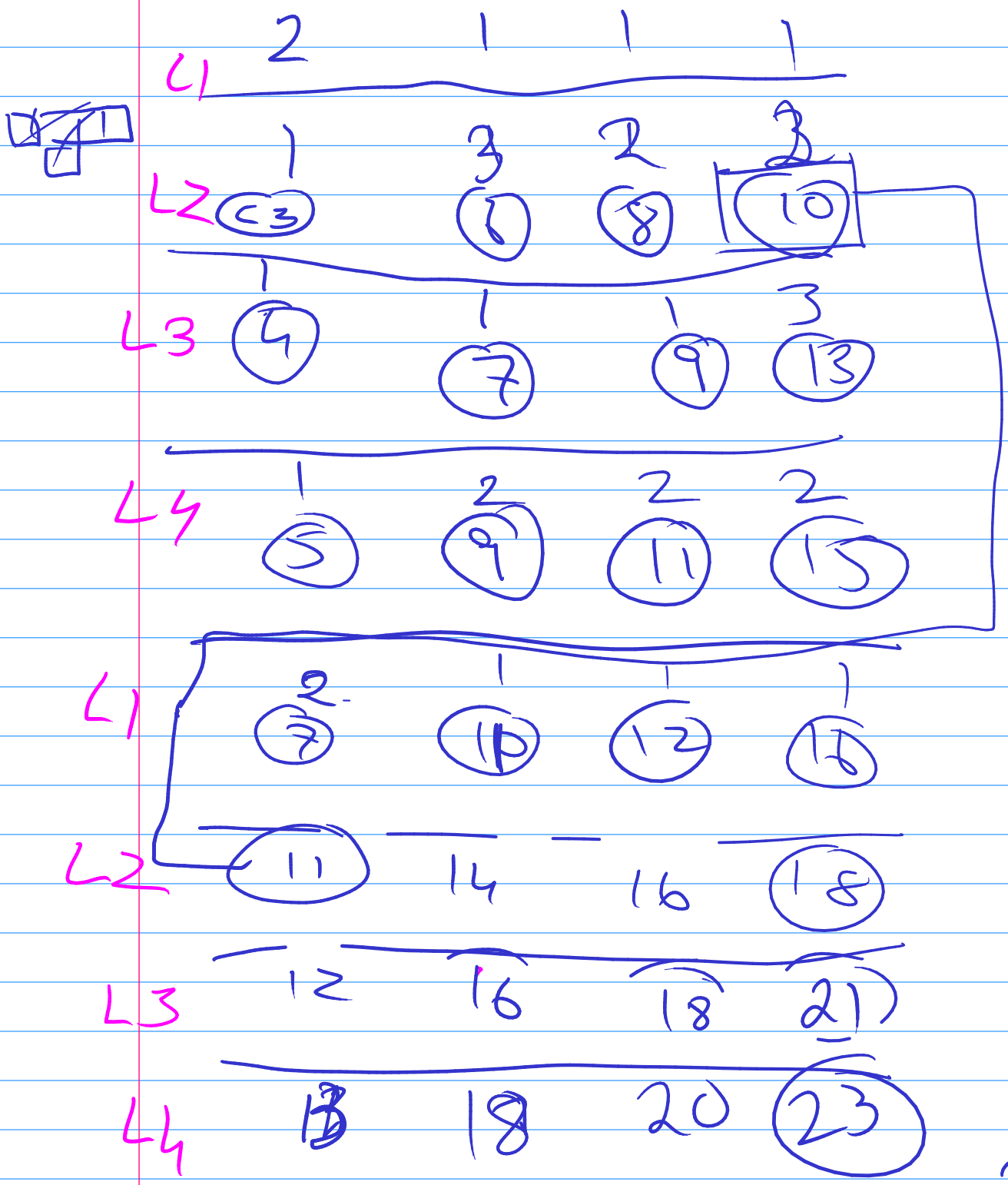
✔ 15

C 17

D 19

	S_1	S_2	S_3	S_4
I_1	2	1	1	1
I_2	1	3	1	1
I_3	1	1	1	3
I_4	1	2	2	2





Row major: GfG 2^{16} 16384 etc.

Column major, every word is loaded row major style into cache no spatial locality, ⇒ everything will miss!!