Q) 3)(iii) latency & Throughput

Q(4) 500ns → nonpipelined

100 programs → 5 stage, 20ns

(i) Speedup (ii) max achievable speedup

avg 5 instⁿ nets: $\frac{500}{100ns}$ $\frac{500}{180}$ 3.

speedup (1 prog $100 + 20(4) = 180ns$

100 prog: $100 + 20(5)(100) - 20$

$\frac{10080ns}{5000}$ $\frac{500000}{10080ns}$

4.96 ≈ 5 max achievable

time = (no of stages of a pipeline) + (total inst − 1) cct

(Q5) 40% data references

(1) Structural hazard 1.05 times higher

$\frac{1}{\frac{60}{100} \times 1.05 \times 1 + \frac{40}{100} \times 1.05 \times 5}$

$(\frac{6}{10} + \frac{20}{10}) \times \frac{1}{1.05} = \frac{26}{105}$

2.476 : 5 1

(i) avg instruction time = Clock cycle

Avg instruction time with structural hazard $= \left(1 + \frac{40}{100}\right) \times \frac{\text{clock cycle time}}{1.05}$

$\approx 1.3 \times$ Clock cycle time ideal

$\Rightarrow$ without structural hazard is better

NOTE: here we are assuming single clock cycle per instruction)