AN2814

SAMA5D2 Layout Recommendations

Introduction

SAMA5D2 Series is based on the ARM® Cortex®-A5 processor. It integrates various peripherals and communication interfaces in one chip, thereby increasing the complexity of the Printed Circuit Board (PCB).

How to place components and route critical traces while keeping signal integrity is a challenge for hardware designers. This document provides basic layout recommendations for some critical components of the SAMA5D2 platform, as well as layout examples for the SAMA5D2 in the various package types.

Reference Documents

Type	Document Title	Available	Ref. No.
Data Sheet	SAMA5D2 Series	www.microchip.com	DS60001476
User's Guide	SAMA5D2-XULT User's Guide		DS50002691
Design Files	SAMA5D2-XULT Design and Manufacturing Files		–

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1. SAMA5D2 Peripherals

The SAMA5D2 is a high-performance, power-efficient embedded MPU based on the ARM Cortex-A5 processor.

The SAMA5D2 features an internal multi-layer bus architecture associated with 32 DMA channels to sustain the high bandwidth required by the processor and the high-speed peripherals. The device offers support for DDR2/DDR3 (DLL off only) LPDDR/LPDDR2/LPDDR3/DDR3L (DLL off only) and x8 SLC/MLC NAND Flash memory up to 32-bit ECC.

The comprehensive peripheral set includes an LCD TFT controller with overlays for hardware-accelerated image composition (RGB) and an Image Sensor Controller (RGB). Connectivity peripherals include a 10/100 EMAC, USBs, CAN-FDs, UARTs, FLEXCOMs, SPIs and two QSPIs, DIO/SD/eMMCs, and I2Cs.

2. Layout Guideline

2.1 General Board Placement Strategies

Some general layout strategies for a SAMA5D2-based system board are listed below.

- First place the connectors of the board and any other items that have compulsory mechanical and location constraints; lock them on your layout so that any further displacement is made impossible.
- Place the MPU, DDR and Flash memories and oscillator parts as a first-level priority. The traces should be as short as possible with a minimal number of vias.
- Place the SD card, Ethernet PHY and LCD/ISC parts as a second-level priority.
- Place the decoupling capacitors (0.1 µF or smaller) as close as possible to each IC power pin, and place the bulk capacitors (1 µF or larger) properly on the PCB to charge the decoupling capacitors.
- As far as possible, avoid splitting ground planes, and avoid routing rapid switching(1) signals above the splits in ground planes, as that is a major source of Electro-Magnetic Interference (EMI).

Note:

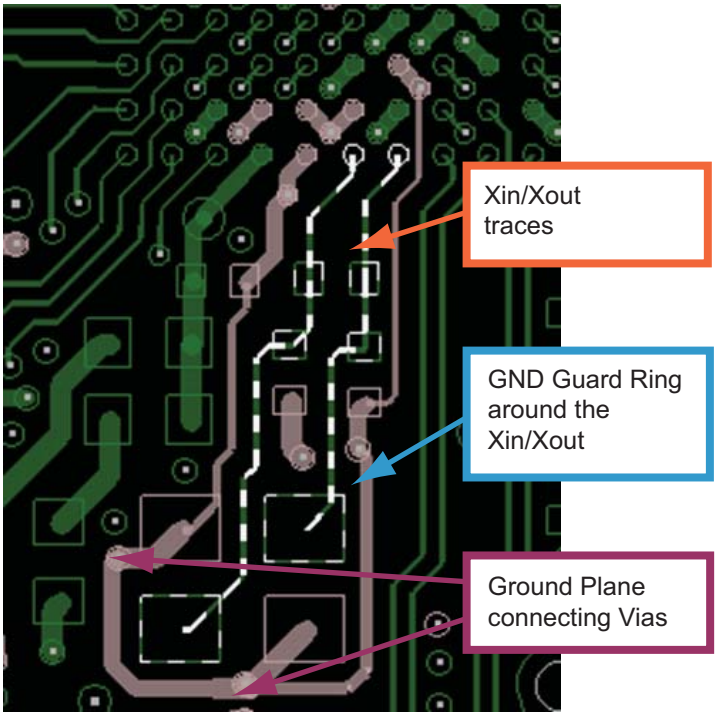
1. Having steep edges.

2.2 Clock

The SAMA5D2 device includes two clock inputs: a slow clock input, and a main clock input. In most cases, one crystal and two load capacitors are required for each input. A ground plane should be positioned under the crystal. It is recommended to shield the oscillator nets and pads with a ground ring connected to the board ground plane through several vias.

The crystal XIN/XOUT are signals of very low amplitude and high impedance; therefore, they must be particularly “protected” to ensure signal integrity. For this purpose, place the crystal part as close as possible to the MPU XIN/XOUT pins, and position a grounded ring around the XIN/XOUT nets, as close as possible to the IC pins.

Figure 2-1. Clock Layout Example



2.3 DDR Memory

The SAMA5D2 device supports several types of DDR memories, including DDR3, DDR3L, LPDDR3, DDR2, LPDDR2 and LPDDR1. The most commonly used memory types are DDR3L and LPDDR3.

The DDR memory controller interface includes:

- Four data lanes: DQS[3:0], DQSN[3:0], DM[3:0], DQ[31:0]
- ADDR/CMD/CTL signals: BA[2:0], A[13:0], RAS/CAS, CS, CKE, WE
- Clock signals: CK/CKn

Here are some recommendations for the data lane signal layout.

- In each data lane (e.g. lane0 includes DQ[7:0]/DM0/DQS0), the length difference between each signal and the respective DQS/DQSn signal should not exceed 100 mils(1).
- It is recommended to route all signals of the same data lane on the same layer.
- The DQS/DQSN signal pairs should be routed as differential traces. The length difference between the differential traces should not exceed 20 mils, with a controlled impedance of 100 ±10% Ohm.
- The impedance of any single-end signal trace should be 50 ±10% Ohm.

Here are some recommendations for the ADDR/CMD/CTL/CK signal layout.

- The length difference between the ADDR/CMD/CTL signal and the CK signal should not exceed 200 mils.
- It is recommended to route all those signals on the same layer.
- CK/CKn signals should be routed as differential traces. The length difference between the differential traces should not exceed 20 mils, with a controlled impedance of 100 ±10% Ohm.
- The impedance of any single-end signal trace should be 50 ±10% Ohm.

To minimize crosstalk, the recommended trace spacing is as follows:

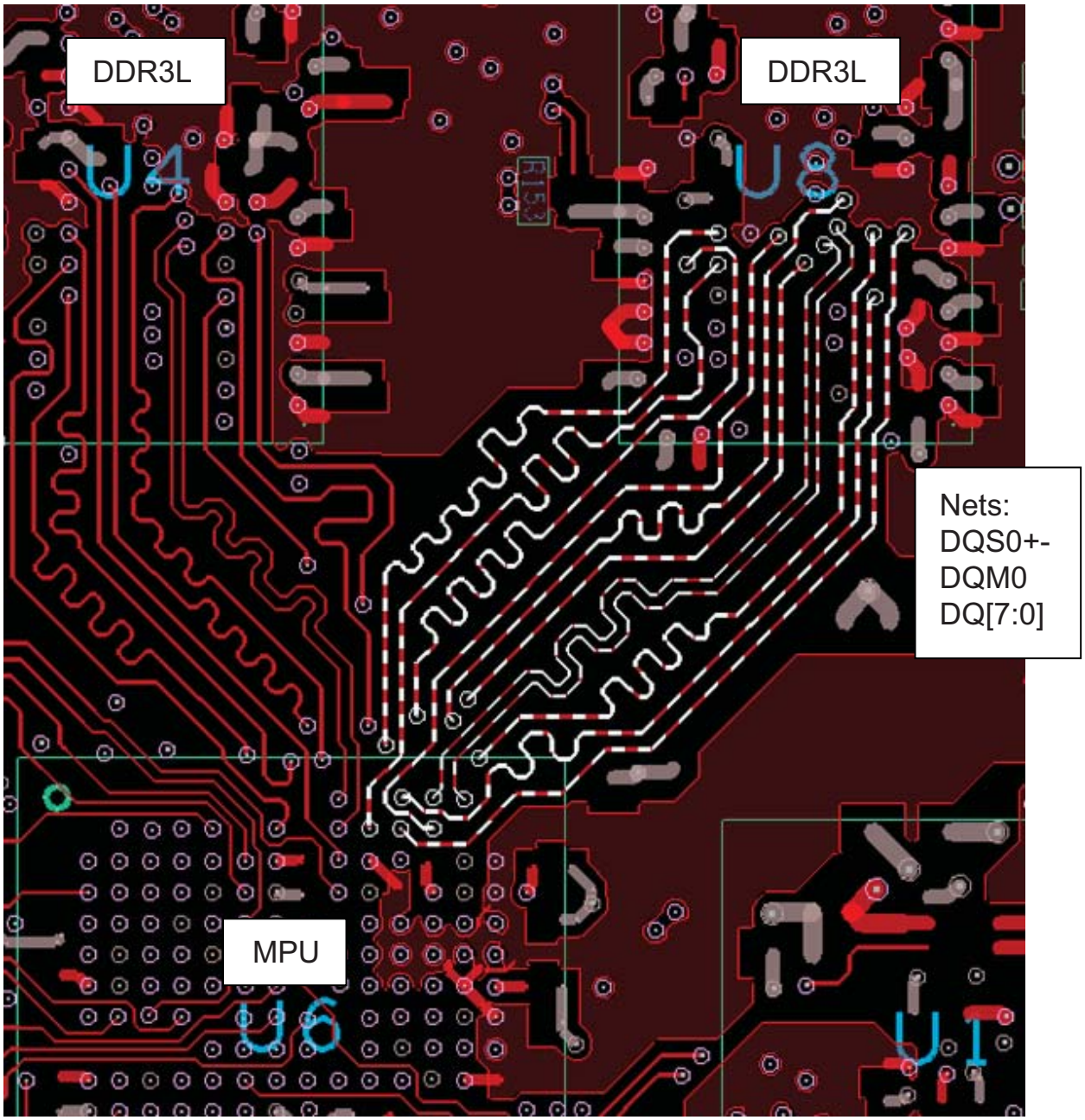
- In the same data lane: 8 to 12 mils
- Data lane signal to other signals: > 20 mils
- ADDR/CMD/CTL/CK to other signals: > 20 mils

Note:

1. 1 inch = 1000 mils = 25.4 mm

The figure below shows a layout example of DDR3L memory (only one data group is shown).

Figure 2-2. DDR3L Layout Example



2.4 USB Signal

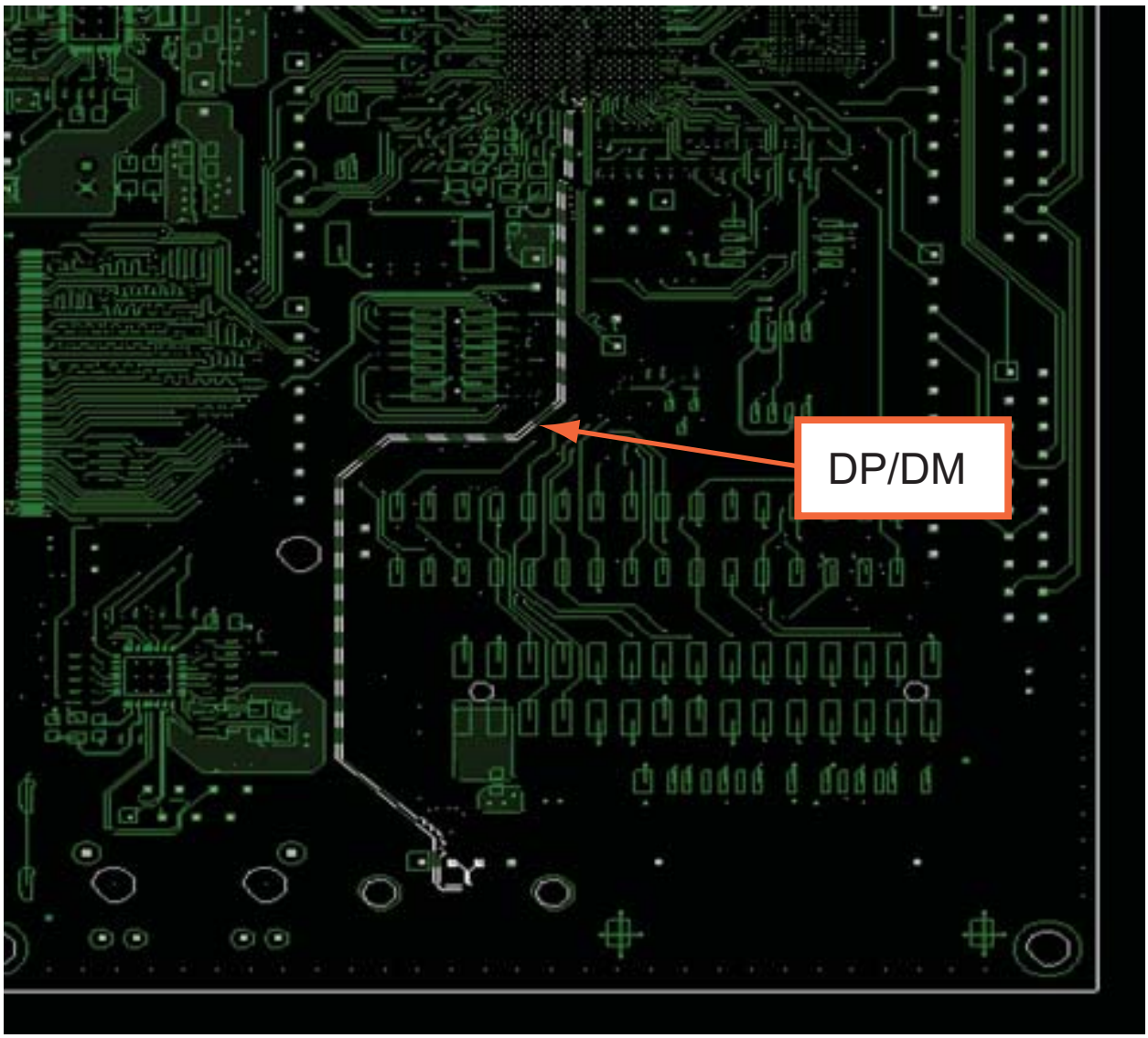
The USB ports in the SAMA5D2 device are compliant with USB v2.0 High-speed Specification.

The layout recommendations are:

- The USB DM and DP signals should be routed as differential traces and be perfectly parallel to each other.
- The reference plane should be continuous.
- If a routing layer must be changed, then both DM and DP signals should be transferred together to the other layer.
- The impedance of the differential traces should be 90 ±10% Ohm.

The figure below shows a layout example of USB traces which fan out from BGA on the top side, and go perfectly in parallel to the connector on the top side.

Figure 2-3. USB Traces Layout Example



2.5 Ethernet Part

The SAMA5D2 device has an on-chip Ethernet MAC that supports 10/100 Mbps Ethernet compatible with IEEE 802.3 standard; furthermore, it supports both MII and RMII interfacing to the PHY.

The Media Independent Interface (MII) signals include transmit data, receive data and control signals.

Here are some recommendations for the data lane signal layout.

- It is recommended to route all signals of the same data lane (TX or RX) on the same layer.
- The length difference between the TX data and TXCK lanes should not exceed 300 mils.
- The length difference between the RX data and RXCK lanes should not exceed 300 mils.
- The impedance of any single-end signal trace should be 50 ± 10% Ohm.

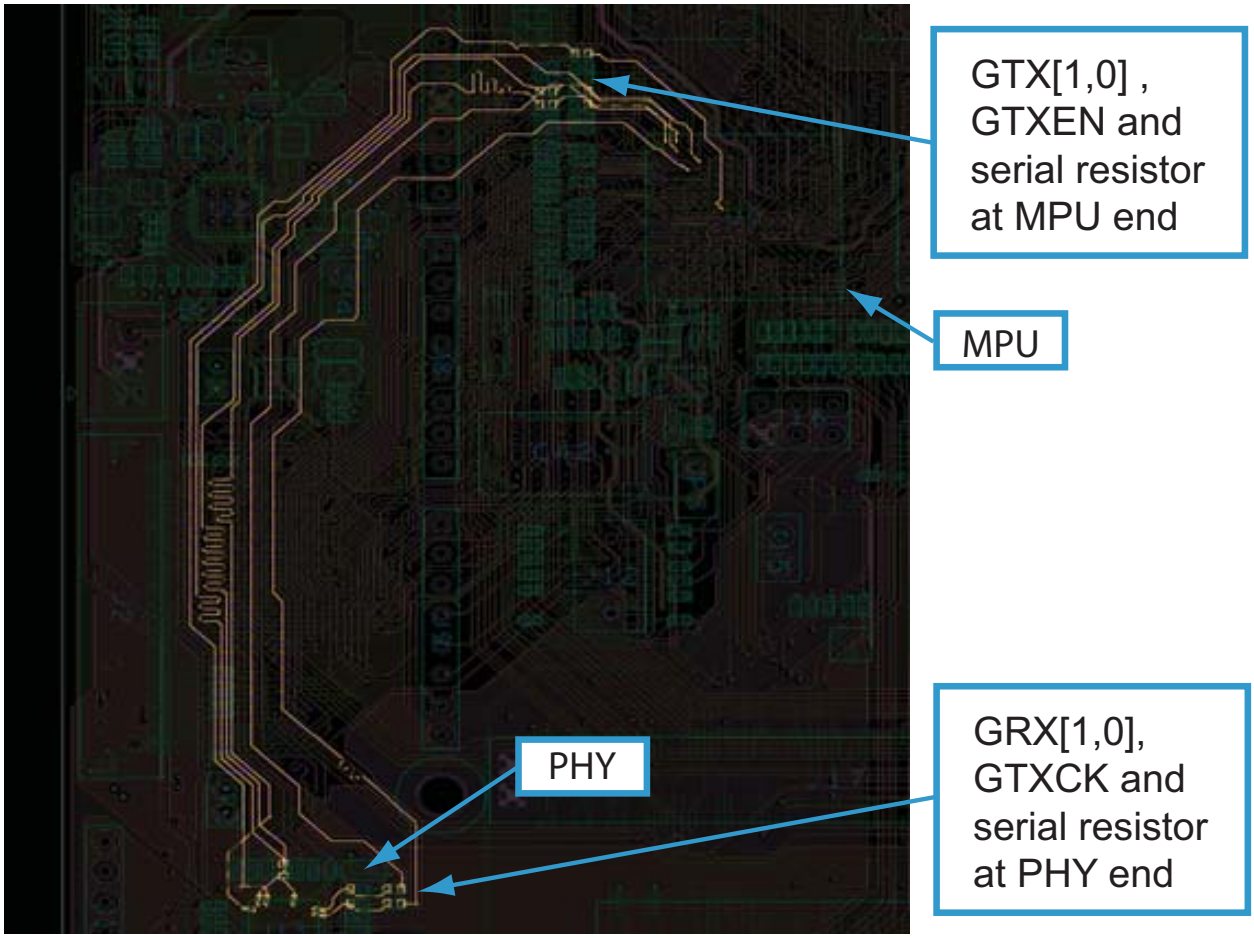
The Media Dependent Interface (MDI) (TX+/- or RX+/-) signals are routed from the PHY to the Ethernet transformers/connector and then further into the cable. The 100M-Base Ethernet cable has two pairs.

The following layout rules apply:

- Differential pairs (TX+/- or RX+/-) should be routed away from all other signals (with a clearance of at least three times the trace width).
- The length difference between the MDI differential pairs (TX+/- or RX+/- lines) should not exceed 20 mils.
- Route differential pairs (TX+/- or RX+/-) over solid ground plane and/or chassis ground plane to achieve a 100 Ohm differential (50 Ohm for single-ended traces) impedance.

The figure below shows an example of a RMII transmitter data trace layout.

Figure 2-4. RMII Transmitter Data Trace Layout Example



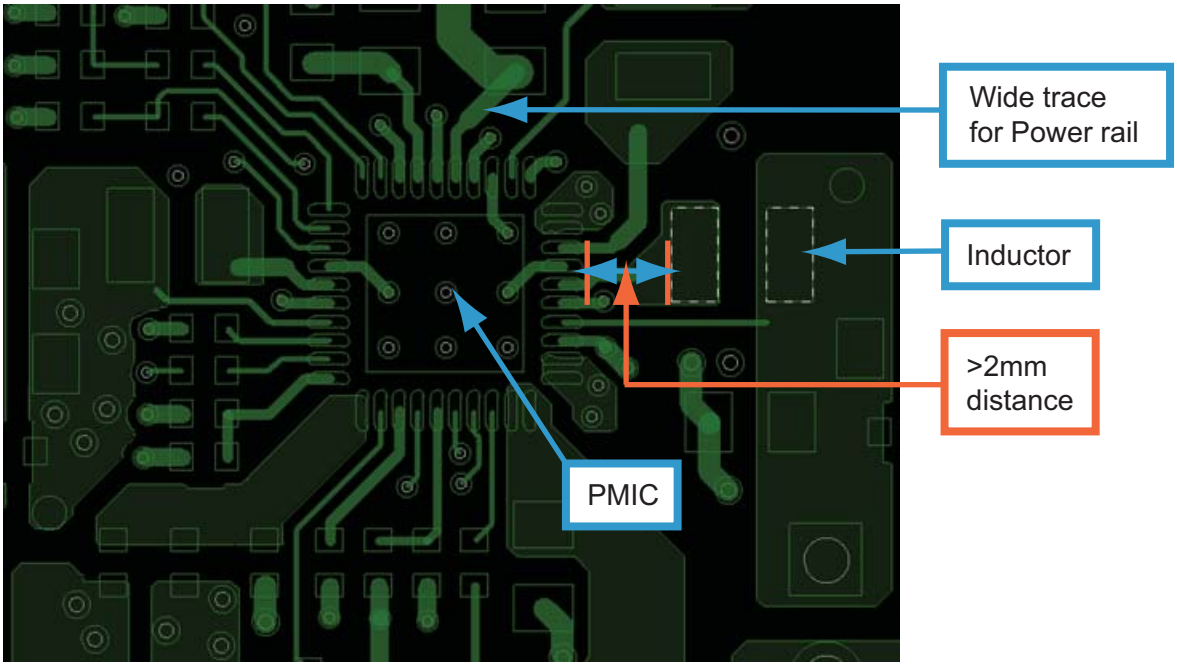
2.6 Power Management IC

A Power Management IC (PMIC) integrates several DCDC and LDO controllers in one chip and manages all the system power rails and their sequencing. The PMIC needs several external components such as inductors, capacitors and resistors.

The DCDC inductors must be close to the PMIC output pins. The inductors produce heat when the DCDC controller is operating. The PMIC is typically surrounded by three inductors; a sufficient air gap (at least 2 mm) must be reserved around each one of them to evacuate the heat.

The power traces should be wide enough for the current load. A minimum width of 20 mils is recommended (a 1-A current needs at least a 1-mm width). Generally, these traces should be enlarged after they fan out from the PMIC. The figure below shows an example of a PMIC circuit layout.

Figure 2-5. PMIC Circuit Layout Example



3. Layout Examples

The SAMA5D2 is available in three packages:

- BGA289: 289 pins, 0.8-mm pitch
- BGA256: 256 pins, 0.4-mm pitch
- BGA196: 196 pins, 0.75-mm pitch

This section describes several layout examples for different packages. The design files of the examples can be downloaded from www.microchip.com (*SAMA5D2_BGA_reference-layouts.zip*, available with this application note).

3.1 Layer Number Considerations

A PCB with a high number of layers is easier to layout and route; however, this also generates increased costs. The general stack-up for a SAMA5D2 board is normally 6 layers or 8 layers, depending on the components pitch size and circuit complexity. Below are the common 6-layer and 8-layer stack arrangements for reference.

6- layer model:

Layer 1---Signal (Microstrip), components side

Layer 2---Ground plane

Layer 3---Signal (Stripline)

Layer 4---Signal (Stripline)

Layer 5---Power plane

Layer 6---Signal (Microstrip)

8- layer model:

Layer 1---Signal (Microstrip), components side

Layer 2---Ground plane

Layer 3---Signal (Stripline)

Layer 4---Power plane

Layer 5---Ground plane

Layer 6---Signal (Stripline)

Layer 7---Ground plane

Layer 8---Signal (Microstrip)

3.2 BGA289 Layout Example (6-Layer Board)

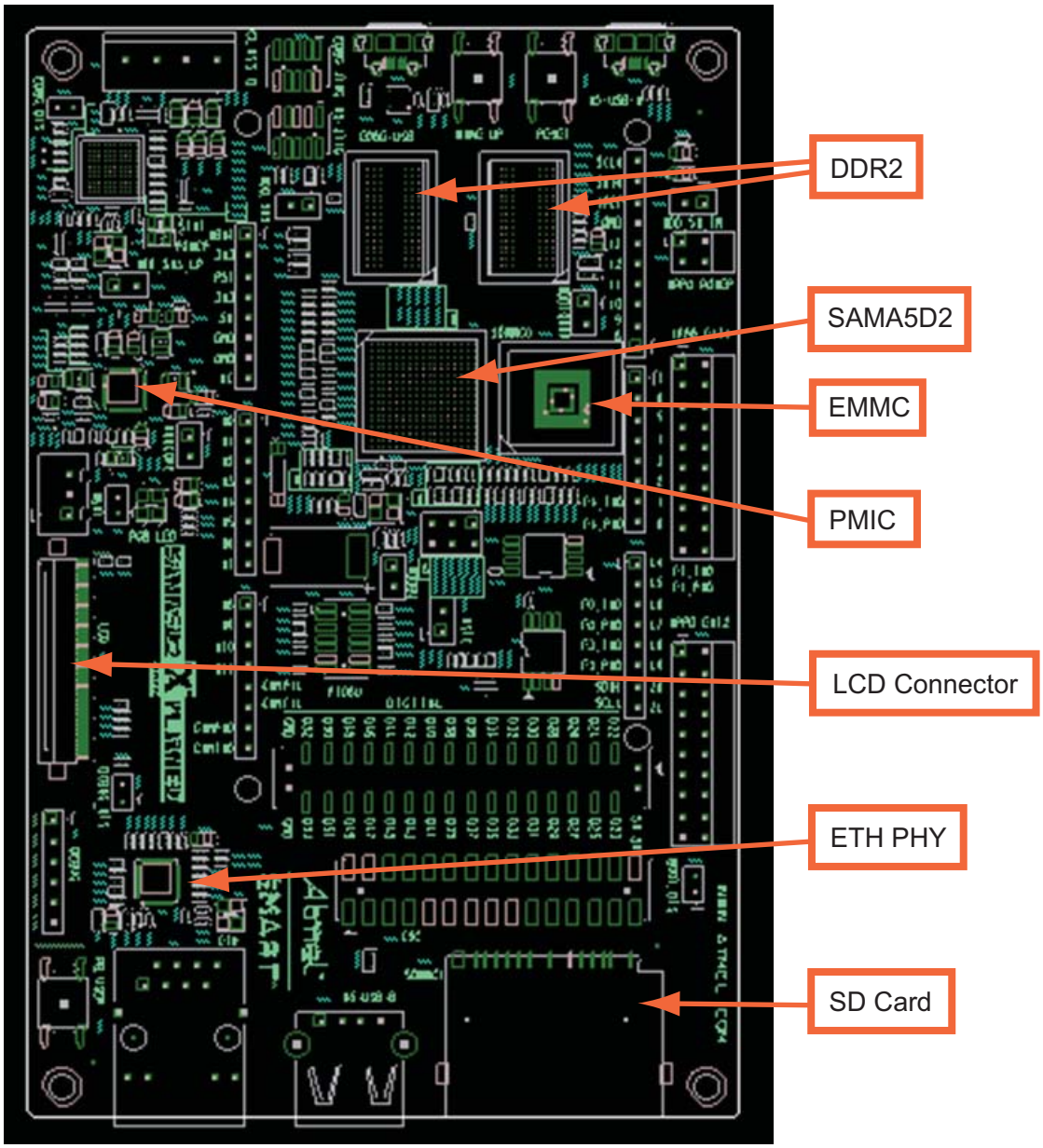
The SAMA5D2-XULT board is a good example of a SAMA5D2-BGA289 package layout. The 6-layer model is used.

3.2.1 Board Placement

The figure below is a PCB placement example for a SAMA5D2-based system.

- The Power Management IC (PMIC) part is at the top left of the PCB.
- Two 16-bit DDR2 chips are above SAMA5D2.
- The EMMC is on the right side of SAMA5D2.
- The Ethernet PHY is at the bottom left of the PCB.
- The LCD connector is at the left edge of the PCB.

Figure 3-1. SAMA5D2-based System PCB Placement Example

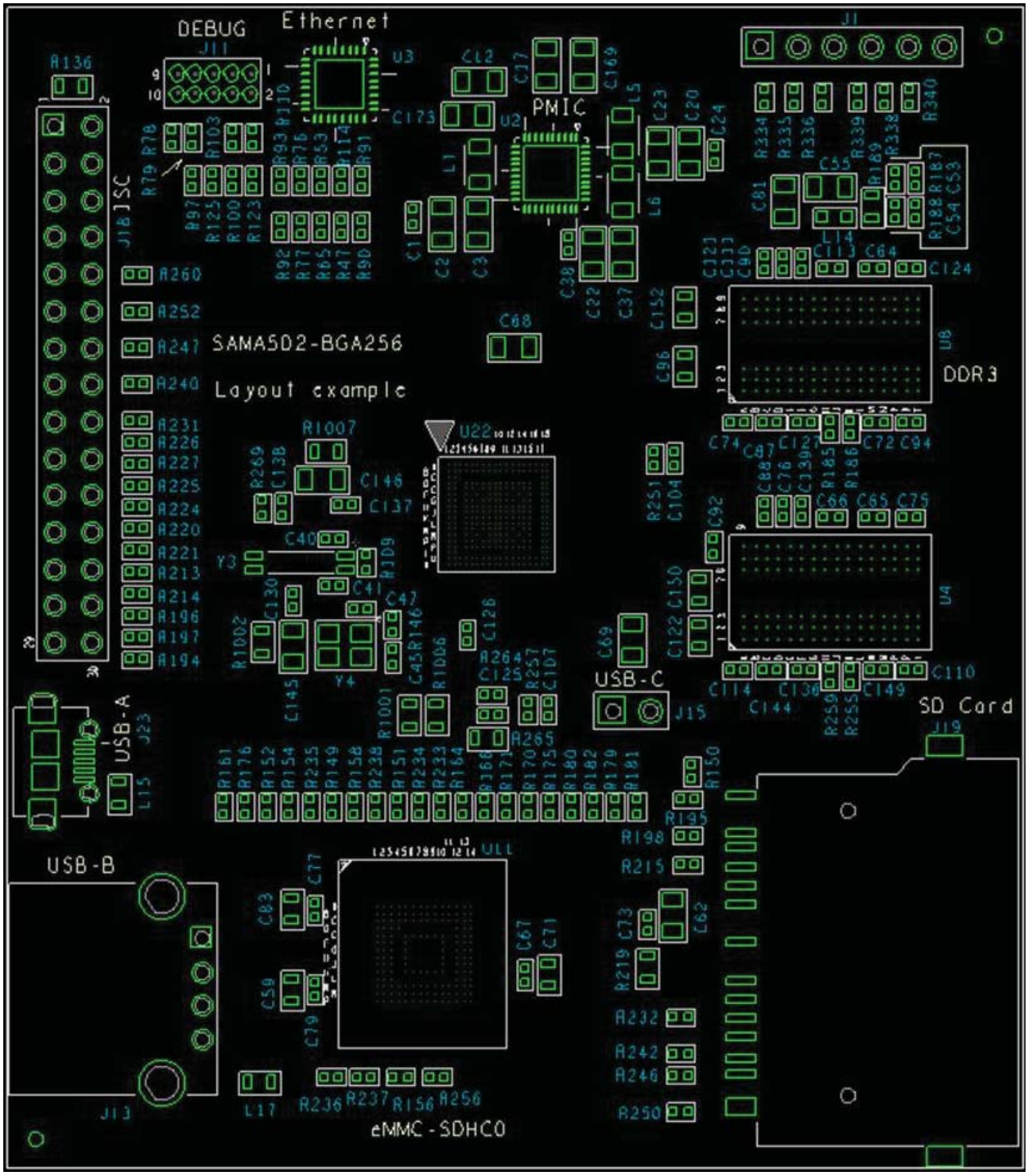


3.3 BGA256 Layout Example (8-Layer Board)

3.3.1 Board Placement

The figure below is a PCB placement example for a SAMA5D2-BGA256 8-layer board.

Figure 3-2. SAMA5D2-BGA256 8L Board Placement Example



3.3.2 Special Constraints and Considerations for a 0.4-mm Pitch

SAMA5D2-BGA256 uses a very small BGA package, with a 0.4-mm pitch. A three-stage laser-via process is needed for such a small pitch. Most of the BGA256 signals are fanned out from the top layer to the fourth layer through laser vias. Eight layers are needed to match the board complexity.

Since most BGA256 signals fan out from Layer 1 to Layer 4, the stack arrangement shown below is different from a typical 8-layer board.

Layer 1---Signal (Microstrip), components side

Layer 2---Ground plane

Layer 3---Signal (Stripline)

Layer 4---Signal (Stripline)

Layer 5---Power plane

Layer 6---Signal (Stripline)

Layer 7---Ground plane

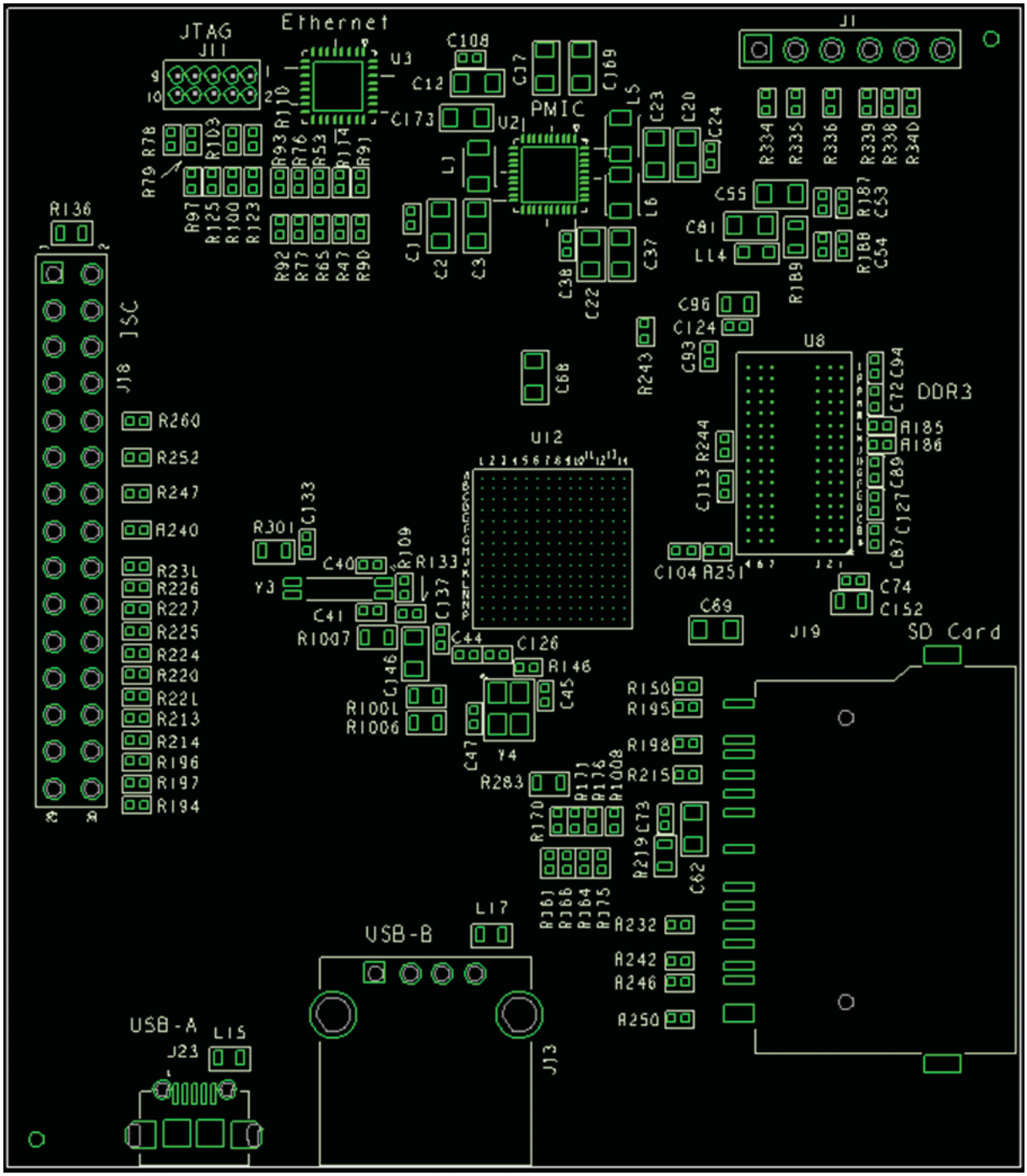
Layer 8---Signal (Microstrip)

3.4 BGA196 Layout Example (4-Layer Board)

3.4.1 Board Placement

The figure below is a PCB placement example for a SAMA5D2-BGA196 4-layer board.

Figure 3-3. SAMA5D2-BGA196 4L Board Placement Example



3.4.2 Special Constraints and Considerations for a 4-Layer Routing

For package BGA196, which has a 0.75-mm pitch, the signals can be fanned in two layers (top layer and bottom layer). Here is the stack arrangement:

Layer 1---Signal (Microstrip), components side

Layer 2---Ground plane

Layer 3---Power plane

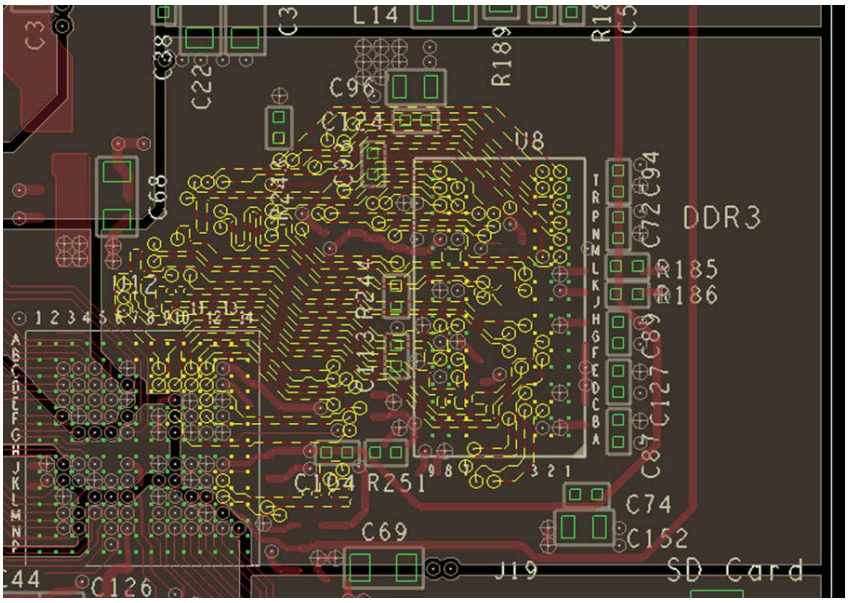
Layer 4---Signal (Microstrip)

Several high-speed DDR3 signals are placed on Layer 4 (bottom side), and the adjacent reference plane is the power plane (Layer 3). The power plane is split into several power domain areas, so care must be taken when routing those DDR3 signals on Layer 4, keeping them under a consistent power domain area(1) and never routing these traces across the power area splits.

Note:

1. In order to achieve a consistent impedance along the whole traces.

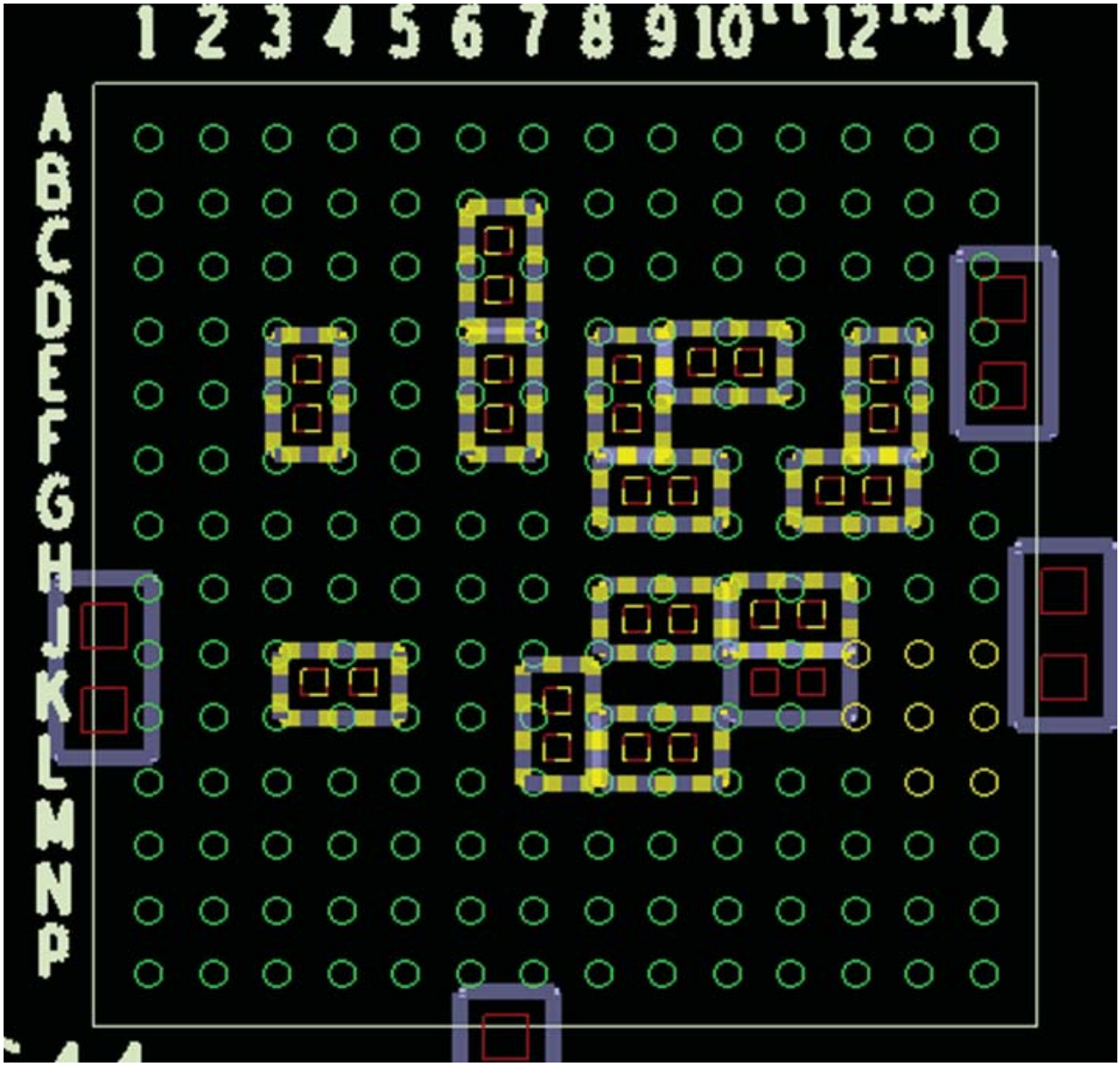
Figure 3-4. DDR3 Signals Reference Plane



As there are only two layers for BGA signals to fan out, it is very hard to place 0402 decoupling capacitors right beneath the SAMA5D2 chip (on the bottom side). To achieve a better power integrity, 0201 decoupling capacitors are used in this example.

The figure below is a PCB placement example for 0201 decoupling capacitors.

Figure 3-5. 0201 Decoupling Capacitors Placement Example (Bottom Side)

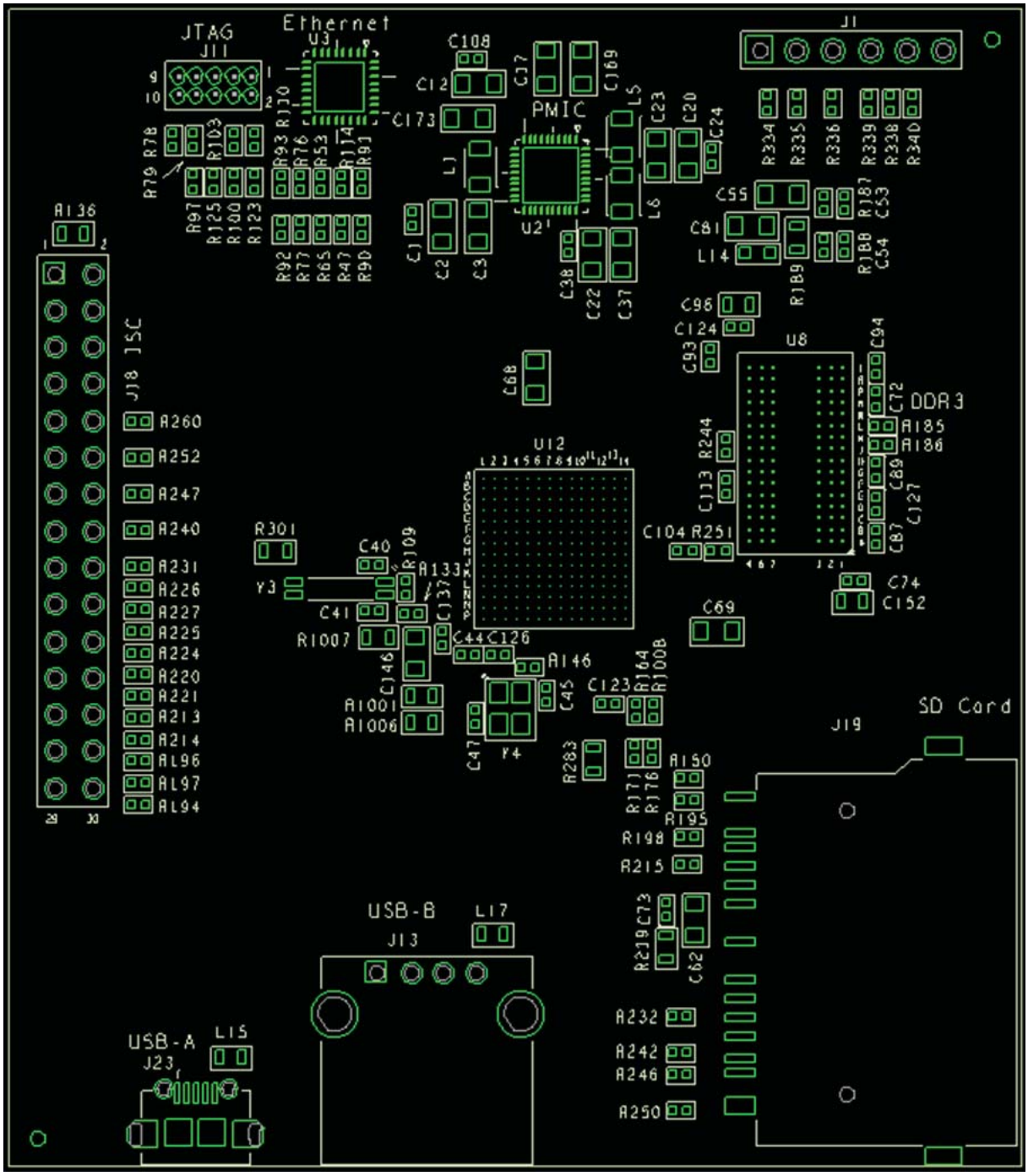


3.5 BGA196 Layout Example (6-Layer Board)

3.5.1 Board Placement

The figure below is a PCB placement example for a SAMA5D2 BGA196 6-layer board.

Figure 3-6. SAMA5D2 BGA196 6L Placement Example



3.5.2 Special Constraints and Considerations for a 6-Layer Routing

It is easy to fan out the signals as there are four signal layers.

Here is the stack arrangement:

Layer 1---Signal (Microstrip), components side

Layer 2---Ground plane

Layer 3---Signal (Stripline)

Layer 4---Signal (Stripline)

Layer 5---Power plane

Layer 6---Signal (Microstrip)

Try to route the very high-speed DDR3 data signals on Layer 1 and Layer 3, as there is a good ground plane nearby. Other signals like control and address signals can be routed on Layer 4 and Layer 6 that reference the power plane.

4. Conclusion

This Application Note briefly introduces the most critical aspects which need to be taken into consideration when designing a SAMA5D2-based system. For beginners, we recommend using these guidelines and also obtaining support from expert PCB design services if relevant skills are unavailable in house.

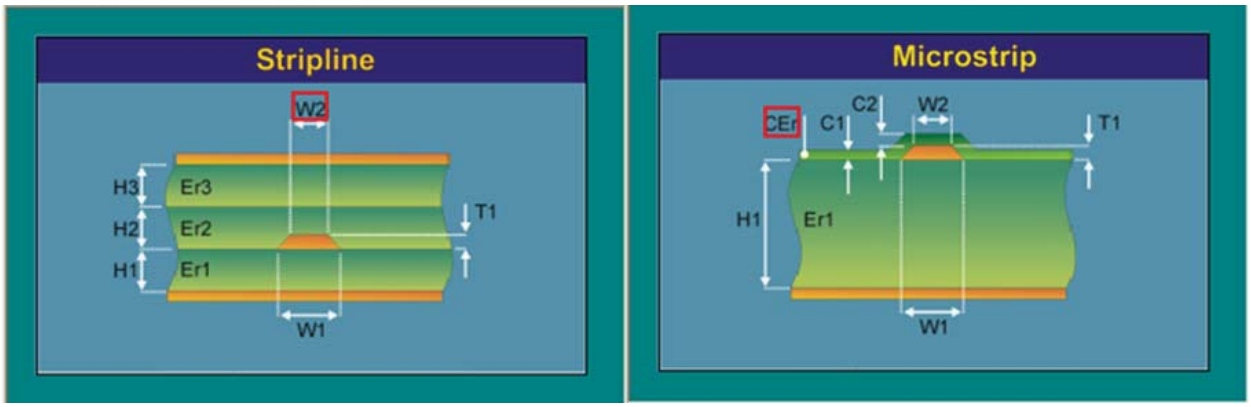
5. Appendices

5.1 Appendix A. PCB Stack-up Design General Knowledge

5.1.1 Transmission Line

Microstrip and Stripline are “transmission line” routing approaches that take the neighbouring power planes and PCB dielectric characteristics into consideration in order to achieve impedance-controlled traces. The impedance is determined by the parameters of the layer (both copper and dielectric), and it can be computed by software with parametric inputs.

Figure 5-1. Stripline and Microstrip Implementations



5.1.2 Board Impedance Control

To achieve signal integrity, board impedance control is mandatory, which means each trace should be treated as a transmission line and its impedance should be controlled to a special value. In most cases, the impedance of single-ended signals should be 50 Ohm, and the impedance of differential signals 90 or 100 Ohm. Factors including the stack arrangement, layer thickness and trace width should be considered when calculating the impedance. Generally, the PCB manufacturer arranges the thickness of copper and dielectric layers, and also adjusts the trace width or space between differential signals to achieve the required impedance.

5.2 Appendix B. Recommended Reading/Guidelines

We recommend reading the excellent “High-Speed Digital Design: A Handbook of Black Magic” by H. W. Johnson and M. Graham, published by Prentice Hall.

6. Revision History

6.1 Rev. A - 10/2018

DDR Memory: deleted constraint on length difference between data lane and CK signal. Corrected constraint on length difference between each signal and the respective DQS/DQSn signal from '50 mils' to '100 mils'.

- Template update: Moved from Atmel to Microchip template.

- The application note is assigned a new document number (DS00002814) and revision letter is reset to A.

--- Document number DS00002814 revision A corresponds to what would have been 44041 revision B.

- ISBN number assigned.

Document 44041A dated 16-Oct-15 superseded by this Microchip document DS00002814.

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