AN3345

How to Change SAMA5D2 Console UART Under Linux®

Introduction

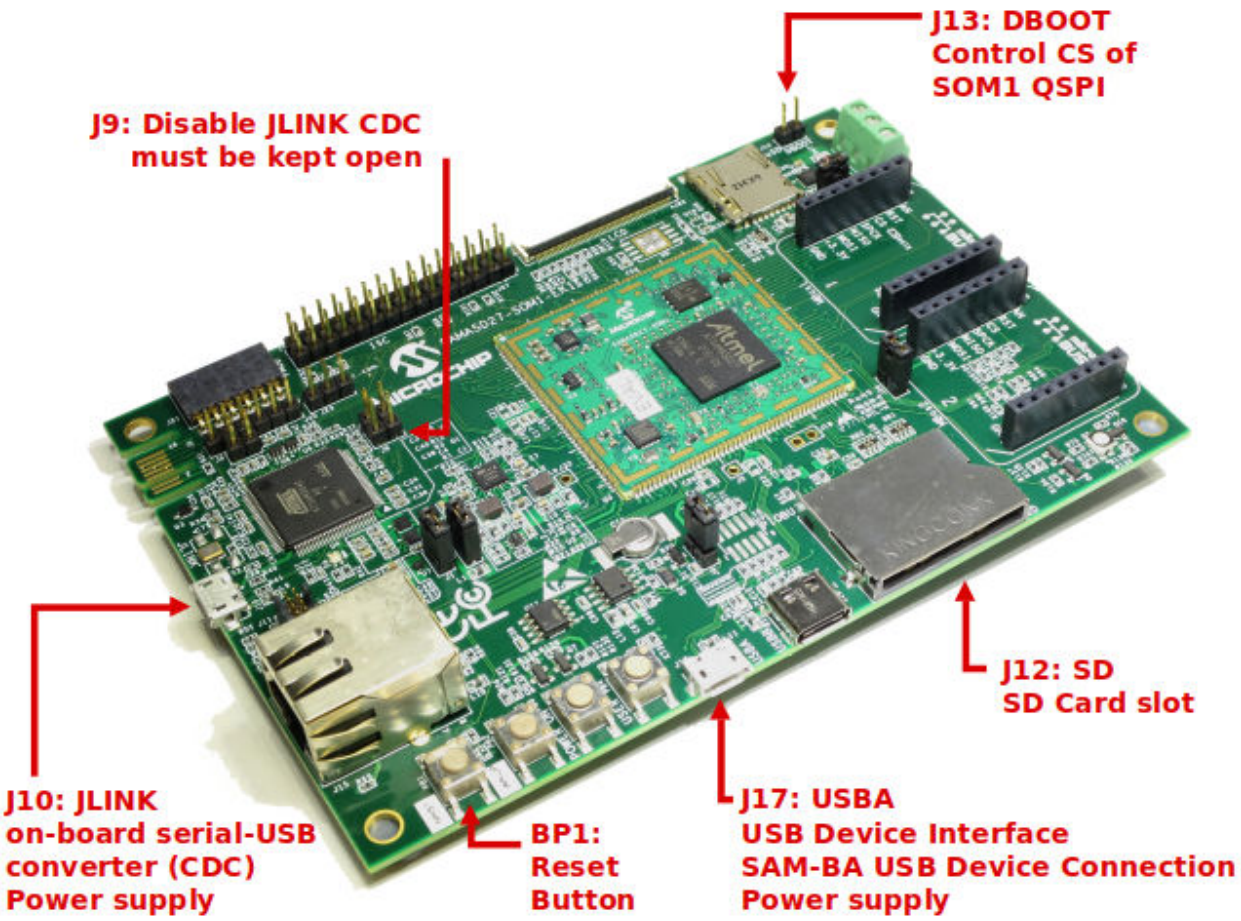
This application note describes how to switch the SAMA5D2 debug console from UART1 (default) to UART2 in every software involved in the startup of a Linux system: RomBOOT, Bootstrap, U-Boot, Kernel.

Reference Documents

Title	Reference	Available
SAMA5D2 Series Datasheet	DS60001476	https://www.microchip.com/design-centers/32-bit-mpus
SAMA5D27 SOM1 Kit1 User Guide	DS50002667	https://www.microchip.com/DevelopmentTools/ProductDetails/PartNO/ATSAMA5D27-SOM1-EK1

Prerequisites

- Hardware
  - PC
  - SAMA5D27 SOM1 Evaluation Kit (Part Number: ATSAMA5D27-SOM1-EK1)
  - SDCard
  - USB-to-serial cable (TTL level)
- Software
  This demo runs on the AT91 Linux platform built by Buildroot. The first step is to set up the AT91 Buildroot development environment. Refer to the web site: http://www.at91.com/linux4sam/bin/view/Linux4SAM/BuildRoot


J13: DBOOT
Control CS of
SOM1 QSPI
J9: Disable JLINK CDC
must be kept open
J12: SD
SD Card slot
J10: JLINK
on-board serial-USB
converter (CDC)
Power supply
BP1:
Reset
Button
J17: USBA
USB Device Interface
SAM-BA USB Device Connection
Power supply

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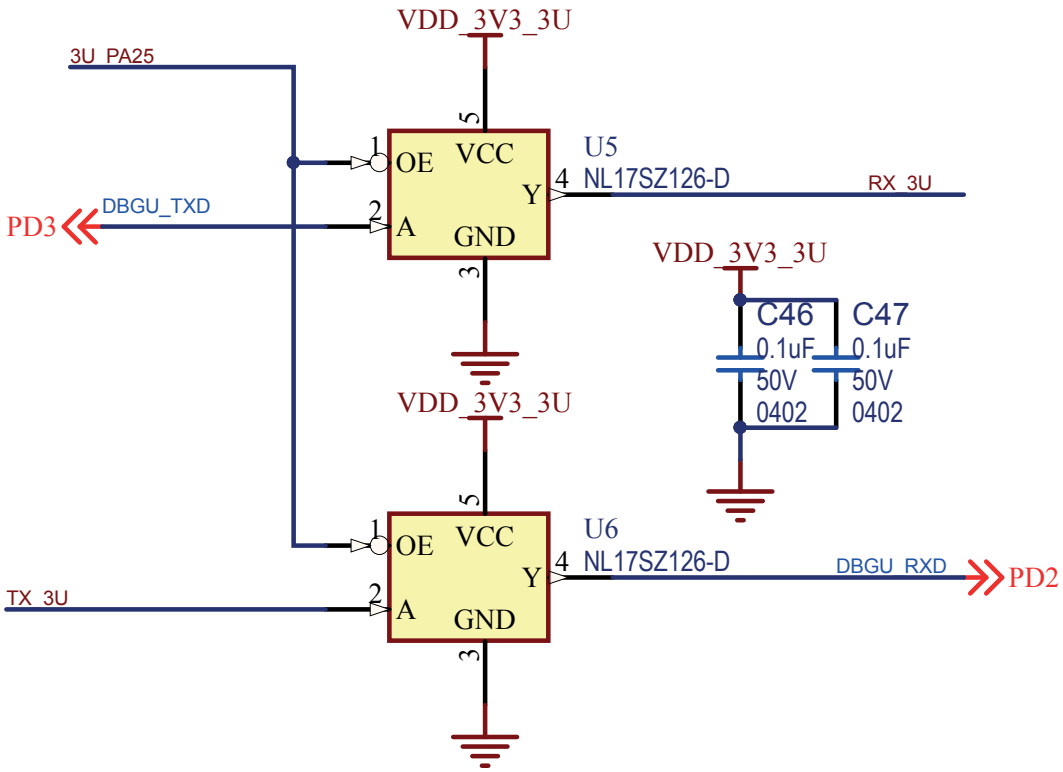
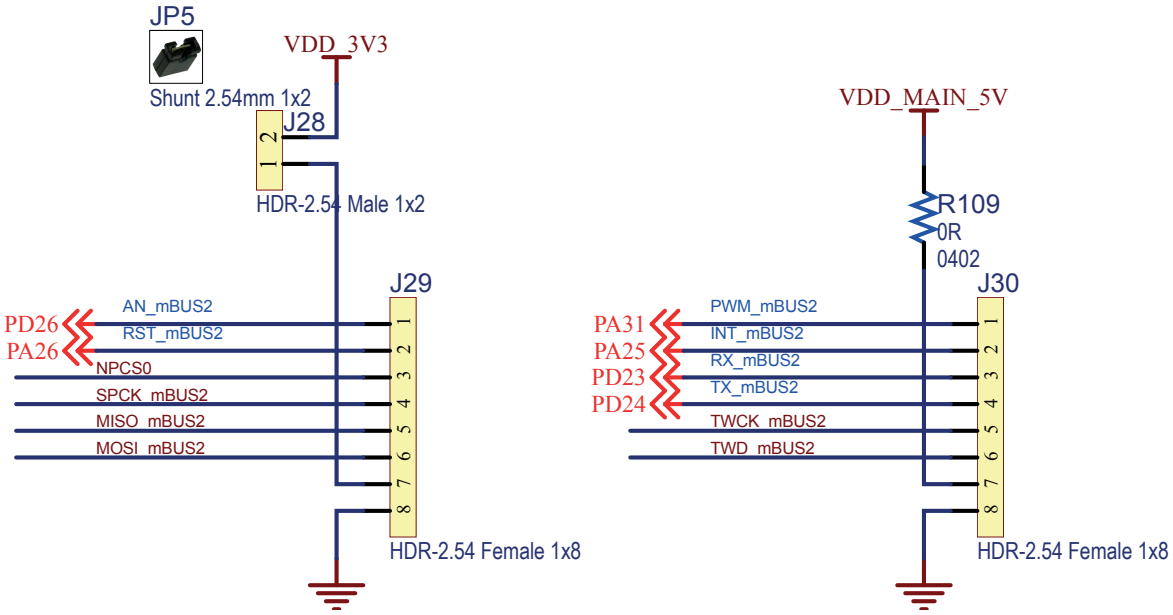
1. Hardware Design

1.1 Interface

On SAMA5D27-SOM1-EK1, the default debug console is UART1. This application note shows how to switch from UART1 to UART2.



- UART1
  - URXD1 → PD2 → J10 (USB CDC debug port)
  - UTXD1 → PD3 → J10 (USB CDC debug port)



- UART2
  - URXD2 → PD23 → RX_mBUS2
  - UTXD2 → PD24 → TX_mBUS2

1.2 Connection

Connect mikroBUS2 UART2 to the PC using the USB-to-Serial cable (TTL level):

J30_3 RX_mBUS2 → TXD

J30_4 TX_mBUS2 → RXD

J30_8 GND → GND

Refer to the following picture.


MICROCHIP
SAMA5D27-SOM1-EK1
Kingston
16GB

2. Software Design

The Microchip Linux platform was built using Buildroot with the following configuration:

```
atmel_sama5d27_som1_ek_mmc_dev_defconfig
```

To change the console UART, at91bootstrap3, U-Boot and the kernel must be updated as described below.

2.1 at91bootstrap3

- Action: need to change
- Location: buildroot-at91/output/build/at91bootstrap3-v3.8.11
- Sources: board/sama5d27_som1_ek/sama5d27_som1_ek.h

Update DBGU definition in board/sama5d27_som1_ek/sama5d27_som1_ek.h:

```
/*
 * DBGU Settings
 */
#define USART_BASE  AT91C_BASE_UART2
#define CONFIG_SYS_DBGU_RXD_PIN   AT91C_PIN_PD(23)
#define CONFIG_SYS_DBGU_TXD_PIN   AT91C_PIN_PD(24)
#define CONFIG_SYS_DBGU_ID    AT91C_ID_UART2
```

2.2 U-Boot

- Action: need to change
- Location: buildroot-at91/output/build/uboot-linux4sam_6.0
- Sources:
  - arch/arm/dts/at91-sama5d27_som1_ek.dts
  - board/atmel/sama5d27_som1_ek/sama5d27_som1_ek.c
  - configs/sama5d27_som1_ek_mmc_defconfig

Update stdout-path in arch/arm/dts/at91-sama5d27_som1_ek.dts:

```
chosen {
u-boot,dm-pre-reloc;
stdout-path = &uart2;

 // Set stdout-path from uart1 to uart2


};

uart2: serial@f8024000 {

 // Add uart2 device here


    pinctrl-names = "default";
    pinctrl-0 = <&pinctrl_uart2_default>;
    status = "okay";

 // Enable uart2 device


    u-boot,dm-pre-reloc;
};

pinctrl_uart2_default: uart2_default {

 // Add pin definition for uart2


    pinmux = <PIN_PD23__URXD2>,
```

```
<PIN_PD24__UTXD2>;
    bias-disable;
    u-boot,dm-pre-reloc;
};
```

Update board/atmel/sama5d27_som1_ek/sama5d27_som1_ek.c:

```
#ifdef CONFIG_DEBUG_UART_BOARD_INIT
static void board_uart1_hw_init(void)
{
  atmel_pio4_set_a_periph(AT91_PIO_PORTD, 2, ATMEL_PIO_PUEN_MASK);  /* URXD1 */
  atmel_pio4_set_a_periph(AT91_PIO_PORTD, 3, 0);  /* UTXD1 */

  at91_periph_clk_enable(ATMEL_ID_UART1);
}

static void board_uart2_hw_init(void)

 // Add function of uart2 hardware initialize


{
  atmel_pio4_set_a_periph(AT91_PIO_PORTD, 23, ATMEL_PIO_PUEN_MASK); /* URXD2 */
  atmel_pio4_set_a_periph(AT91_PIO_PORTD, 24, 0); /* UTXD2 */

  at91_periph_clk_enable(ATMEL_ID_UART2);
}

void board_debug_uart_init(void)
{
  board_uart2_hw_init();

 // Call uart2 hardware initialize function here


}
#endif
```

Update configs/sama5d27_som1_ek_mmc_defconfig:

```
CONFIG_DEBUG_UART_BASE=0xf8024000

 // Update from 0xf8020000 to 0xf8024000



CONFIG_BOOTARGS="console=ttyS2,115200 earlyprintk root=/dev/mmcblk0p2 rw rootwait"

 // Update console from ttyS0 to ttyS2
```

2.3 Kernel

- Action: no need to change
- Location: buildroot-at91/output/build/uboot-linux4sam_6.0
- Sources: arch/arm/boot/dts/at91-sama5d27_som1_ek.dts

With the default setting, UART2 is enabled in the kernel, so there is no need to update the kernel code. With other settings, the serial configuration must be updated in the kernel device tree in order to enable the required ttyS device. UART2 is defined as follows in the kernel device tree.

Device tree for UART2 in at91-sama5d27_som1_ek.dts:

```
aliases {
    serial0 = &uart1; /* DBGU */
    serial1 = &uart4; /* mikro BUS 1 */
    serial2 = &uart2; /* mikro BUS 2 */

 // The aliases of uart2 is serial2, then uart2 will be registered as ttyS2
```

```
    i2c1  = &i2c1;
    i2c2  = &i2c2;
};

uart2: serial@f8024000 {
pinctrl-names = "default";
pinctrl-0 = <&pinctrl_mikrobus2_uart>;
atmel,use-dma-rx;
atmel,use-dma-tx;
status = "okay";
 // UART2 was enabled with default setting


};

pinctrl_mikrobus2_uart: mikrobus2_uart {
pinmux = <PIN_PD23__URXD2>,
 // PD23 and PD24 was selected for UART2


<PIN_PD24__UTXD2>;
bias-disable;
};
```

2.4 RomBOOT

If a RomBOOT console UART change is required, refer to the description of the UART_CONSOLE field in the SAMA5D2 data sheet, section “Boot Configuration Word”:

Bits 15:12 – UART_CONSOLE[3:0] Selects the pins and UART interface used as a console terminal

Value	Name	Description
0	UART_1_IOSET_1	Use UART1 IO Set 1
1	UART_0_IOSET_1	Use UART0 IO Set 1
2	UART_1_IOSET_2	Use UART1 IO Set 2
3	UART_2_IOSET_1	Use UART2 IO Set 1
4	UART_2_IOSET_2	Use UART2 IO Set 2
5	UART_2_IOSET_3	Use UART2 IO Set 3
6	UART_3_IOSET_1	Use UART3 IO Set 1
7	UART_3_IOSET_2	Use UART3 IO Set 2
8	UART_3_IOSET_3	Use UART3 IO Set 3
9	UART_4_IOSET_1	Use UART4 IO Set 1
10	DISABLED	No console terminal
11	DISABLED	No console terminal
12	DISABLED	No console terminal
13	DISABLED	No console terminal
14	DISABLED	No console terminal
15	DISABLED	No console terminal

⚠WARNING “Boot Configuration Word” is a major configuration item for MPU booting. Before modifying it, make sure to refer to the “Boot Configuration” section in the SAMA5D2 Series data sheet and to understand the relationship between Fuse and BUREG.

The Boot Configuration Word can be updated using SAM-BA commands. See the following example.

```
$ sudo ./sam-ba -p usb -d sama5d2 -a bootconfig -c writecfg:bscr:valid,bureg0 -c
writecfg:bureg0:UART2_IOSET2
```

3. Hands-On


COM13 - Tera Term VT
File Edit Setup Control Window Help
AT91Bootstrap 3.8.11 (Fri Mar 22 16:00:05 CST 2019)
SD/MMC: Image: Read file u-boot.bin to 0x23f00000
MMC: ADMA supported
SD: Card Capacity: High or Extended
SD: Specification Version 3.0X
SD/MMC: Done to load image
<debug_uart>
U-Boot 2018.07-linux4sam_6.0 (Mar 22 2019 - 15:29:50 +0800)
CPU: SAMA5D27 1G bits DDR2 SDRAM
Crystal frequency: 24 MHz
CPU clock : 492 MHz
Master clock : 164 MHz
DRAM: 128 MiB
MMC: sdio-host@a0000000: 0, sdio-host@b0000000: 1
Loading Environment from FAT... *** Warning - bad CRC, using default environment
Failed (-5)
In: serial@f8024000
Out: serial@f8024000
Err: serial@f8024000
Net: eth0: ethernet@f8008000
Hit any key to stop autoboot: 0
45075 bytes read in 16 ms (2.7 MiB/s)
3980816 bytes read in 249 ms (15.2 MiB/s)
Flattened Device Tree blob at 21000000
Booting using the fdt blob at 0x21000000
Loading Device Tree to 27b47000, end 27b55012 ... OK
Starting kernel ...
Booting Linux on physical CPU 0x0
Linux version 4.14.73-linux4sam_6.0 (user@at91) (gcc version 6.4.0 (Buildroot 2018.02))
CPU: ARMv7 Processor [410fc051] revision 1 (ARMv7), cr=10c53c7d
CPU: PIPT / VIPT nonaliasing data cache, VIPT aliasing instruction cache
OF: fdt: Machine model: Atmel SAMA5D27 SOM1 EK
Memory policy: Data cache writeback
cma: Failed to reserve 64 MiB
CPU: All CPU(s) started in SVC mode.
Built 1 zonelists, mobility grouping off. Total pages: 32480
Kernel command line: console=ttyS2,115200 earlyprintk root=/dev/mmcblk0p2 rw rootwait
PID hash table entries: 512 (order: -1, 2048 bytes)
Dentry cache hash table entries: 16384 (order: 4, 65536 bytes)
Inode-cache hash table entries: 8192 (order: 3, 32768 bytes)
Memory: 119924K/131072K available (6144K kernel code, 231K rwdata, 1132K rodata, 1024K i
Virtual kernel memory layout:
vector : 0xffff0000 - 0xffff1000 (4 kB)
fixmap : 0xffc00000 - 0xfff00000 (3072 kB)
vmalloc : 0xc8800000 - 0xff800000 (880 MB)
lowmem : 0xc0000000 - 0xc8000000 (128 MB)
modules : 0xbf000000 - 0xc0000000 (16 MB)
.text : 0xc0008000 - 0xc0700000 (7136 kB)
.init : 0xc0900000 - 0xc0a00000 (1024 kB)
.data : 0xc0a00000 - 0xc0a39ca0 (232 kB)
.bss : 0xc0a3f304 - 0xc0a6ab9c (175 kB)
NR_IRQS: 16, nr_irqs: 16, preallocated irqs: 16
L2C-310 ID prefetch enabled, offset 2 lines
L2C-310 dynamic clock gating enabled, standby mode enabled
L2C-310 cache controller enabled, 8 ways, 128 kB
L2C-310: CACHE_ID 0x410000c9, AUX_CTRL 0x36020000
clocksource: pit: mask: 0x7fffffff max_cycles: 0x7fffffff, max_idle_ns: 11654027029 ns
sched_clock: 32 bits at 100 Hz, resolution 10000000ns, wraps every 21474836475000000ns
Console: colour dummy device 80x30
Calibrating delay loop... 326.86 BogoMIPS (lpj=1634304)

4. Revision History

4.1 Rev. A - 12/2019

First issue.

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