AN2836

Powering SAMA5D2 with ActivePMU™ PMICs

Scope

To support enhanced power supply applications on its SAMA5D2 series embedded MPUs, Microchip has selected two ActivePMU Power Management Integrated Circuits (PMICs) from the Active-Semi® portfolio:

- ACT8865—seven-channel (3 DC/DC converters + 4 LDO regulators) PMU
- ACT8945A—seven-channel (3 DC/DC converters + 4 LDO regulators) PMU with integrated linear Li-Po/Li-Ion battery charger

This application note provides developers with the following content:

- Recommended application schematics with associated functional descriptions
- A description of the PMIC Power-Saving Mode and its use with Microchip MPU low-power modes
- A high-level description of an available Linux® driver

Reference Documents

Document Type	Document Title	Literature Number	Available
Data Sheet	SAMA5D2 Series	DS60001476	https://www.microchip.com
Data Sheet	ACT8865	–	http://www.active-semi.com
Data Sheet	ACT8945A	–	http://www.active-semi.com

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1. Power Supply Overview of Microchip MPU Systems

1.1 SAMA5D2 Power Rails

SAMA5D2x MPUs power rails and their respective operating ranges are listed in Table 1-1. An approximate current consumption is provided for each rail in order to size the corresponding regulator. Accurate numbers and descriptions are provided in the device datasheet.

In most non-secure applications, the MPU subsystem (device + external memories) can be operated from three primary rails:

- 3.3V,
- 1.2V, and
- 1.8V, 1.5V or 1.35V depending on the type of external memory mounted on the board.

In secure applications of the SAMA5D2x device, or any application that requires writing into the fuse box of SAMA5D2x, an additional power rail at 2.5V is needed to supply the VDDFUSE input pin.

Additionally, SAMA5D2 has a special VDDBU pin to power its backup domain (32 kHz crystal oscillator, RTC, System Controller, etc.). When needed, and because of its ultra-low power consumption, this power domain can be maintained during power-down periods with a storage element such as a 3.0V lithium coin cell battery or a super-capacitor. Otherwise, applications can operate VDDBU on the main 3.3V power rail.

Table 1-1. SAMA5D2x Series Power Supply Inputs

Power Rail	Description	Range	Consumption
VDDCORE	Core logic	1.10 – 1.32V, 1.20V	0.2A
VDDUTMIC	USB device and host UTMI+ core logic	1.10 – 1.32V, 1.20V	0.02A
VDDPLLA	PLLA cell	1.10 – 1.32V, 1.20V	0.02A
VDDHSIC	USB HSIC interface I/O lines	1.10 – 1.32V, 1.20V	0.01A
VDDIODDR	LPDDR / DDR2 memory interface I/O lines	1.70 – 1.90V, 1.80V	0.05A
	LPDDR2 / LPDDR3 memory interface I/O lines	1.14 – 1.30V, 1.20V	
	DDR3L memory interface I/O lines	1.29 – 1.45V, 1.35V	
	DDR3 memory interface I/O lines	1.43 – 1.57V, 1.50V	
VDDIOP0	Peripheral I/O lines	1.65 – 3.60V	0.03A
VDDIOP1	Peripheral I/O lines	1.65 – 3.60V	0.03A
VDDIOP2	Peripheral I/O lines	1.65 – 3.60V	0.03A
VDDISC	Image sensor I/O lines	1.65 – 3.60V	0.03A
VDDSDMMC	SDMMC I/O lines	1.65 – 1.95V, 1.80V	0.03A
		3.00 – 3.60V, 3.30V	

.....continued

Power Rail	Description	Range	Consumption
VDDUTMII	USB host and device UTMI+ interface I/O lines	3.00 – 3.60V, 3.30V	0.02A
VDDOSC	Main oscillator and UTMI PLL	1.65 – 3.60V, 3.30V	0.01A
VDDAUDIOPLL	Audio PLL	3.00 – 3.60V, 3.30V	0.01A
VDDANA	Analog-to-Digital converter, peripheral touch controller analog front-end	1.65 – 3.60V, 3.30V	0.01A
VDDFUSE	Programmable fuse box	2.25 – 2.75V, 2.50V	0.05A
VDDBU	Backup domain	1.65 – 3.60V	0.0001A

In all modes other than Backup mode and Backup mode with DDR in self-refresh of the MPU, every power supply input must be powered to operate the device. The only exception to this rule is the VDDFUSE input, which can be left unpowered if the SAMA5D2x fuse box is not used in Write mode.

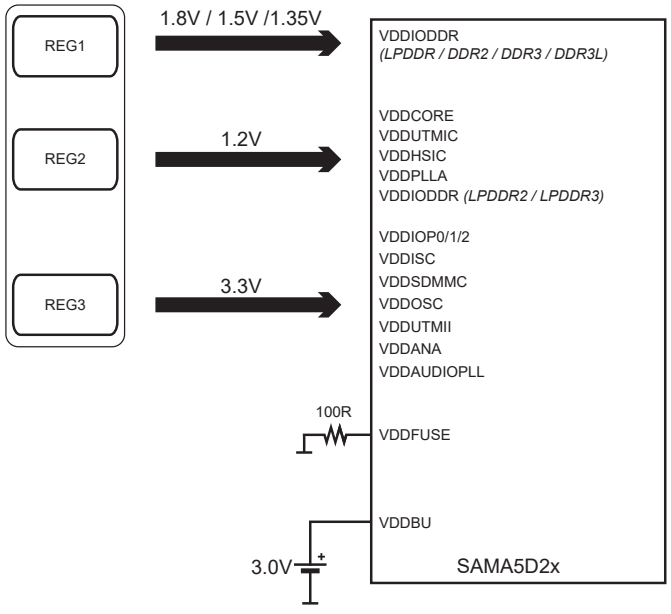
1.2 Power Supply Topologies and Power Distribution

1.2.1 3-channel Topology

In the simplest applications of SAMA5D2x, a 3-rail power supply topology can be used as shown in Figure 1-1. However, this supply schematic has the following limitations:

- The fuse box cannot be accessed in Write mode because VDDFUSE = 0V.
- The analog sections of the device (VDDANA, VDDOSC, VDDAUDIOPLL and VDDUTMII) are powered from the (noisy) digital 3.3V rail.

Figure 1-1. 3-channel Power Distribution Example on SAMA5D2x Series



1.2.2 5-channel Topology and Active-Semi PMICs

A 5-channel power supply topology can be used to lift the aforementioned limitations on the fuse box and on the analog circuits. In the following application schematic, the power supply based on Active-Semi PMICs follows this architecture:

- 3.3V (analog)
- 3.3V (digital)
- 1.8V or 1.5V or 1.35V (digital)
- 1.2V (digital)
- 2.5V (analog)

For maximum efficiency, the three digital power supplies channels are generated by three integrated step-down converters. The 3.3V and 2.5V analog rails are supplied by two integrated low-dropout (LDO) regulators. Power distribution to the MPU and its external components mainly depends on the external components themselves. As an example, a SAMA5D2x + LPDDR2 design operates VDDIODDR from the 1.2V rail whereas this power pin is fed by the 1.8V rail on a SAMA5D2x + DDR2 design.

1.2.2.1 VOUT1 Default Output Voltage

In order to cover all possible external memory configurations (LPDDR, DDR2, DDR3, DDR3L, LPDDR2 and LPDDR3), the VOUT1 output of Active-Semi PMICs has three possible default voltages at startup: 1.8V, 1.5V and 1.35V. Choosing one of these three default voltages on the application board is done through:

- the ordering code of the PMIC and,
- the configuration of the VSEL pin.

Please refer to the table below for detailed VOUT1 default configuration.

Table 1-2. VOUT1 Default Output Voltage Setting

	ACT8865	ACT8945A
Integrated ActivePath™ Charger	N/A	Yes
VOUT1 = 1.8V	Ordering code: ACT8865QI305 VSEL = 0	Ordering code: ACT8945AQI305 VSEL = 0
VOUT1 = 1.5V	Ordering code: ACT8865QI405 VSEL = 0	Ordering code: ACT8945AQI405 VSEL = 0
VOUT1 = 1.35V	Ordering code: ACT8865QI405 VSEL = VIN	Ordering code: ACT8945AQI405 VSEL = VIN

1.2.2.2 VOUT4 and VOUT5 LDOs

Active-Semi PMICs have four integrated LDO regulators (OUT4–OUT7) with low noise and high PSRR performance. OUT4 defaults to 2.5V at startup and is intended to supply the VDDFUSE power input of SAMA5D2x devices in applications accessing the fuse box in Write mode (e.g., secure applications). This supply channel can be reassigned to another external component or can be switched off by software in other types of applications. This output starts by default and must therefore be decoupled. OUT5 defaults to 3.3V at startup and is intended to feed the analog circuits of the SAMA5D2, namely VDDANA, VDDOSC, VDDAUDIOPLL, and VDDUTMII power input pins. For both OUT4 and OUT5 channels, the MPU power consumption on these rails leaves a large amount of output current available for other

external components. However, wiring an external component on OUT5 prevents this component from being powered off during operation as none of the SAMA5D2 inputs can be left unpowered.

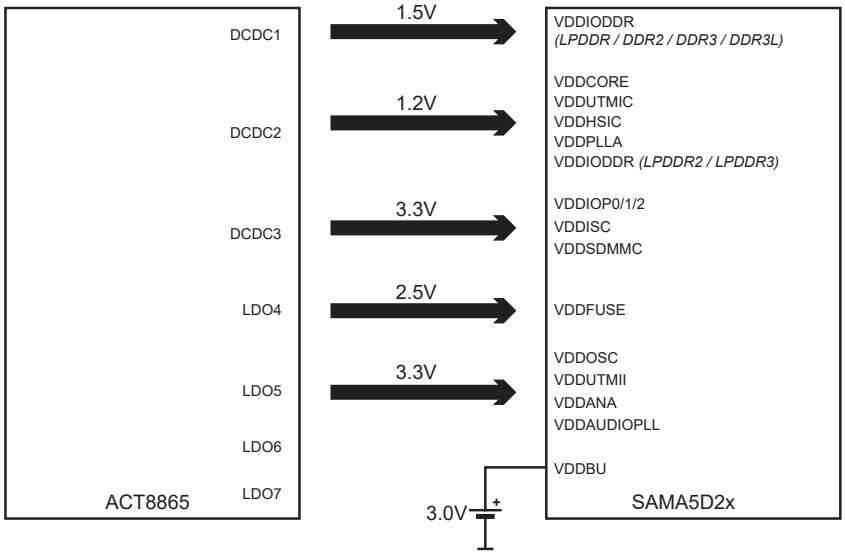
The remaining LDO channels (OUT6, OUT7) default to OFF at startup. They can be turned on and adjusted under software control through the I^2C link to supply a wide range of external components ranging from digital ICs to analog/RF ICs such as an audio codec or an RF transceiver.

The power supply sequencing of the five supply channels is ensured by the Active-Semi PMICs as per recommendations in the device datasheet. Therefore, the turn-on sequence is the following:

1. 3.3V (both LDO5 and DCDC3)
2. 1.8V or 1.5V or 1.35V (DCDC1)
3. 1.2V (DCDC2)
4. 2.5V (LDO4)

During this turn-on sequence (and similarly at turn-off), Active-Semi PMICs hold the SAMA5D2 NRST input in Active state (low).

Figure 1-2. Power Distribution Example on SAMA5D2x Series with ACT8865 (1.5V DDR3 Case)

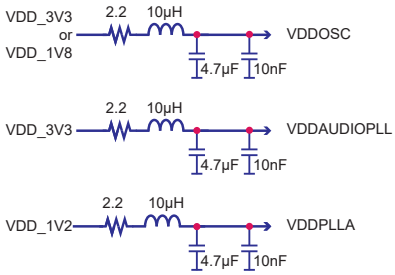


1.3 Analog and Clock Circuits Power Supply

SAMA5D2x devices have separate power supply inputs for their analog (ADC, PTC) and clock (oscillators, PLL) circuits. This allows to decouple these analog circuits from the digital (core and I/Os) activity of the device and thus generate less jittered clocks. Microchip highly recommends to feed these power supply inputs with low noise sources for applications where analog noise level or clock jitter is important (e.g., Hi-speed USB). A good approach is to use as much as possible the LDO outputs of the Active-Semi PMICs (e.g., VOUT5 for 3.3V rails).

For cases where these analog circuits are fed by a noisy rail, it is possible to use an LC low-pass filter as shown in Figure 1-3. Choosing a 20 kHz corner frequency is a good trade-off between component size/cost and the necessary high-frequency attenuation for clock circuits. The inductors must be sized for low DC resistance and good DC superimposition characteristics (TDK MLZ series and Taiyo Yuden CBM series are possible choices). The serial resistor in the filter schematic must be adjusted to take the inductor DCR into account. Inductor examples: Taiyo Yuden CBMF1608T100K (10 µH, 0.36Ω, 115 mA, 0603) and TDK MLZ1608N100L (10 µH, 0.6Ω, 60 mA, 0603).

Figure 1-3. Recommended Filter on Clock Circuit Power Supply



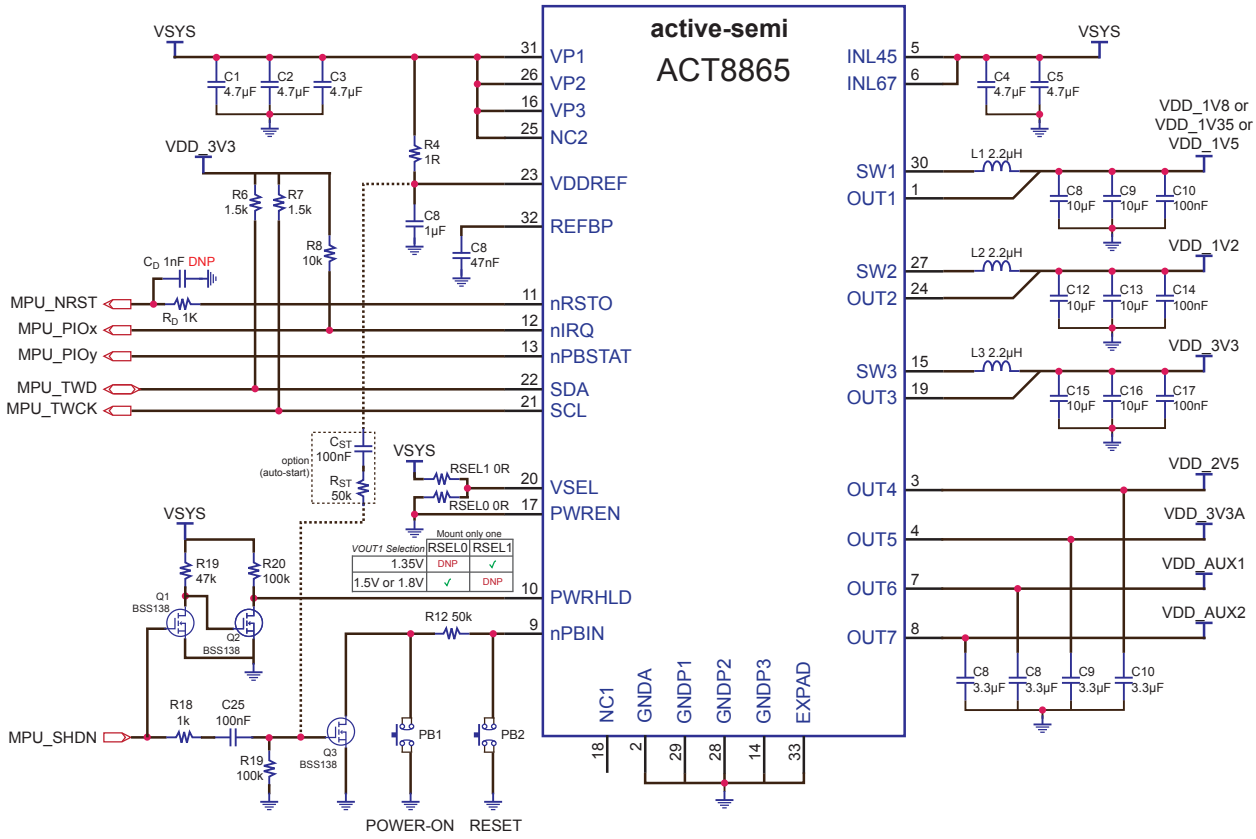
1.4 Power Supplies Monitoring

For sensitive applications, it is recommended to monitor the system input voltage (to detect an input power loss detection) and the regulated channel outputs. Active-Semi PMICs have an input supply monitor and a power-fail detector on each regulated output which can generate an interrupt upon a power-fail detection.

2. ACT8865 and ACT8945A: Reference Schematics and Description

2.1 ACT8865 Reference Schematic and Description

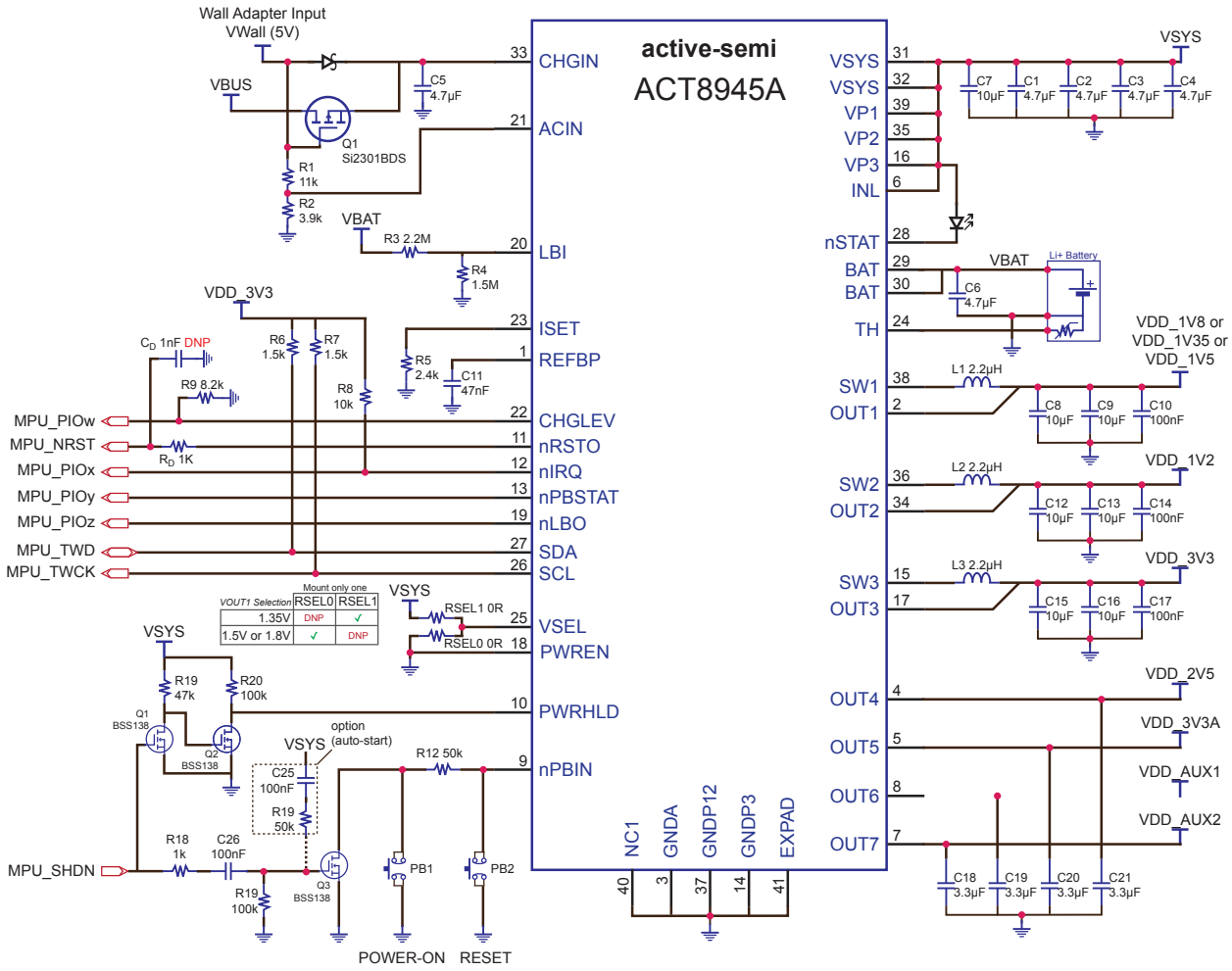
Figure 2-1. ACT8865 Reference Schematic



In this schematic, the power input is VSYS which can range from 3.5V to 5.5V to start the IC. VSYS feeds the DCDC power inputs (VP1, VP2 and VP3), the LDO regulators power inputs (INL45, INL67) and the reference voltage power input (VDDREF). This last pin is RC-filtered to attenuate high frequency noise on this sensitive part of the PMIC. VDD_1V8 (or VDD_1V5, or VDD_1V35), VDD_1V2, VDD_3V3, VDD_2V5, and VDD_3V3A are to be connected to the power supply inputs of the MPU. VDD_AUX1 and VDD_AUX2 are two available channels for the applications.

2.2 ACT8945A Reference Schematic and Description

Figure 2-2. ACT8945A Reference Schematic



In this schematic, the power inputs are the Li-Ion or Li-Po battery (VBAT), the Wall adapter (VWall) and the USB voltage VBUS. ACT8945A contains a battery charger and an automatic power switch function that allows the integrated regulators (DCDCs and LDOs) to run from a single voltage (VSYS) that is built from one of these three inputs. VSYS feeds the DCDC power inputs (VP1, VP2 and VP3) and the LDO regulators power input INL. VDD_1V8 (or VDD_1V5, or VDD_1V35), VDD_1V2, VDD_3V3, VDD_2V5, and VDD_3V3A are to be connected to the power supply inputs of the MPU. VDD_AUX1 and VDD_AUX2 are two channels available for applications.

2.3 Passive Components Selection and PCB Layout Recommendation

The passive components selection around the DCDCs and LDOs of Active-Semi PMICs is described in these components' datasheets. It is very important to follow these recommendations and to properly decouple the regulator inputs of these PMICS to limit the DCDCs switching currents into the ground and power planes.

A recommended PCB layout/placement is provided with the Active-Semi Evaluation Kit. This is a good starting point to place and route these PMICs. Moreover, Microchip recommends placing these PMICs as close as possible to the power source (input connector or regulator output) to limit again switching

currents into the ground and power planes. In case of inductive power source (long wires), it is good practice to decouple this input with large capacitors (> 47 µF).

2.4 Digital Interfaces

This section describes the following signals shared between the PMIC and the MPU:

- I^2C serial lines SDA and SCL
- nRSTO, nPBSTAT, nIRQ outputs

These signals are all of open-drain type and must be pulled-up to the appropriate power rail. As an example, the schematic in Figure 2-1 references some of these signals to the VDD_3V3 rail. Designers may use the programmable pull-up resistor integrated in the MPU I/O lines to save external resistors.

Two other inputs are available:

- VSEL—selection of the VDDCORE voltage
- CHGLEV—selection of the charge current

2.4.1 I^2C Interface

The Active-Semi PMICs are controlled as slave I^2C devices. They can be connected to any of the Two-Wire Interface (TWI) peripherals of the Microchip device. Depending on the programmed speed and the PCB layout parasitics, external pull-up resistors may be needed on the TWD and TWCK lines to ensure rising edges on these signals are fast enough. On the programming side, the TWI peripheral should be configured in Master mode as follows:

- 7-bit slave address
- one byte internal address
- one data byte
- transfer speed up to 400 kHz (Fast mode)
- 300 ns minimum hold time (HOLD field in SAMA5D2 register TWI_CWGR)

Important: In the application, if the I^2C lines connected to the PMIC are shared with other devices, it is important that these devices are powered by default at startup (use one of OUT1–OUT5 rails). Otherwise, connection of these lines to an unpowered device could create leakages from the MPU I/O pin to the unpowered device I/O pin, and even jeopardize normal operation of the I^2C lines.

2.4.2 nRSTO Output

The nRSTO signal is the active-low system reset signal. It should be connected to the NRST input of the MPU and pulled high with a 100 kOhms resistor to the VDD_3V3 rail. As a reminder, this input belongs to the VDDBU power domain and is neither internally pulled high nor low. Note that connecting the pull-up resistor to the VDDBU rail would create a leakage path to VIN (pull-up resistor + NRSTO protection diode in the PMIC) when VIN is 0. Therefore this is not recommended in systems where VDDBU is powered by a battery. The PMIC asserts nRSTO low in the following cases:

- during a start-up sequence
- during a shutdown sequence (either an automatic or a manual shutdown)
- upon a reset request on the nPBIN input

When the nPBIN pin is tied to ground through 0Ω (see PB2 in the reference schematic), a system reset is issued. The nRSTO line is asserted low as soon as the nPBIN is tied to ground and remains low 64 ms after the nPBIN is released.

2.4.3 nPBSTAT Output

The nPBSTAT output reflects the status of the nPBIN pin in VDDIO level (VDDIO being a generic name for the rail that supplies the MPU I/O pin to which nPBSTAT is connected). In the reference schematic, nPBSTAT defaults to VDD_3V3 and when PB1 is pressed nPBSTAT is asserted low by the PMIC. This line can be used as an interrupt source of the MPU or be polled by the MPU to implement “short” or “long” press detections and consequently start specific software routines. Note that pressing PB2 would also assert nPBSTAT (in addition to nRSTO).

2.4.4 nIRQ Output

The nIRQ line allows the PMIC to interrupt the MPU on various alarm cases:

- The programmable voltage system monitor detects a low input voltage.
- One or several regulated outputs drop(s) below the power-good threshold.
- A charger-related event is detected (e.g., input charger connection/disconnection, safety timeout).

nIRQ can be wired on any GPIO configured by software as an interrupt source. It is generally not useful to wire it on the MPU FIQ input.

2.4.5 VSEL Input

This input selects the VOUT1 default voltage. Depending on the PMIC ordering code, the function associated to this pin differs. Refer to 1.2.2.1 VOUT1 Default Output Voltage.

2.4.6 CHGLEV Input (ACT8945A)

This input selects the level of charging current. When high, the nominal charging current is used (e.g., 450 mA when the USB input is detected). When low, ACT8945A uses the “preconditioning” current, typically the nominal current divided by 5 (e.g., 90 mA for the USB case). It is recommended to pull down this input to ensure a low level on this pin under reset conditions of the MPU. If not pulled down, the MPU I/O that defaults to the “input-pull-up” state when nRSTO is low applies a ‘1’ to this input and hence forces the nominal charging current. In most cases, this is not an acceptable behavior as the nominal charging current should be first negotiated between a device and its host. The recommended maximum pull-down resistor value is 8.2 kΩ.

3. Functional Description of Typical Use Cases

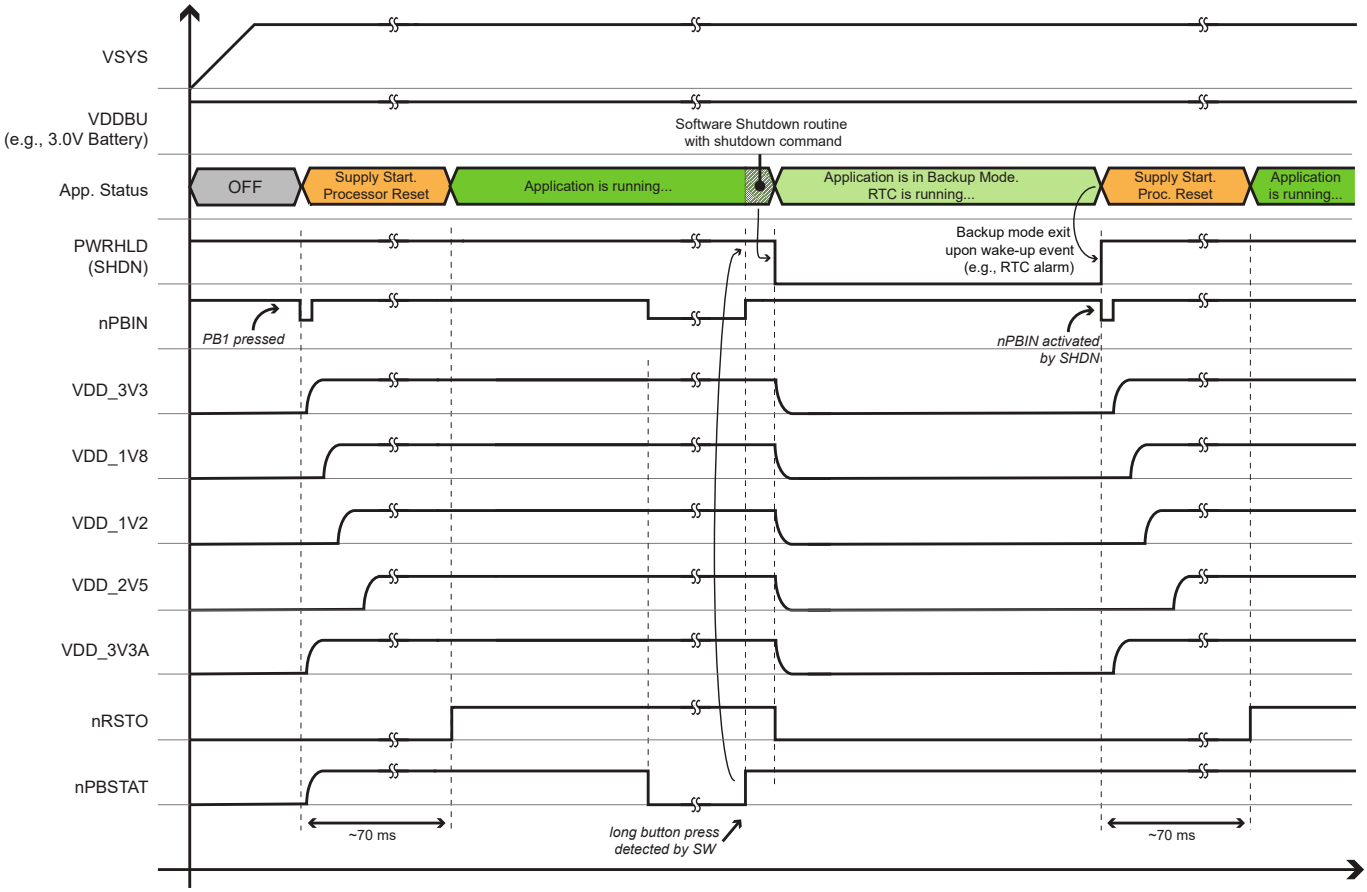
This section describes how Active-Semi PMICs can power on and power off the MPU power supplies. Two typical application case studies are used to support the functional description:

1. The first one is an application that switches between running and sleeping periods. The backup domain (VDDBU) of the MPU is powered by a storage element (e.g., a battery) and the power supplies are switched OFF when the MPU is in Backup mode. This case uses the shutdown controller of the MPU to enter and leave the Backup mode. See Figure 3-1.
2. The second one is an application that does not have a backup capability and where VDDBU is connected to VDD_3V3 (could be VDD_1V8). Obviously, when this application shuts down, the backup content (e.g., RTC, registers) is lost. See Figure 3-5.

As ACT8865 and ACT8945A only differ in the integration of a Battery Charger + Automatic Power Switch function, most of the following descriptions are common to both ICs. For simplicity, these application cases focus on non-battery-powered applications (ACT8865). Each important phase illustrated in the timing diagrams (e.g., first start-up, software shutdown) is described in detail in the following sections. The application input voltage is called VSYS which is either the PMIC input voltage (ACT8865) or the automatic power-switch output (ACT8945A).

3.1 Application With Backup Capability

Figure 3-1. Typical Application Timing Diagram: Application With Backup Capability (Case 1)



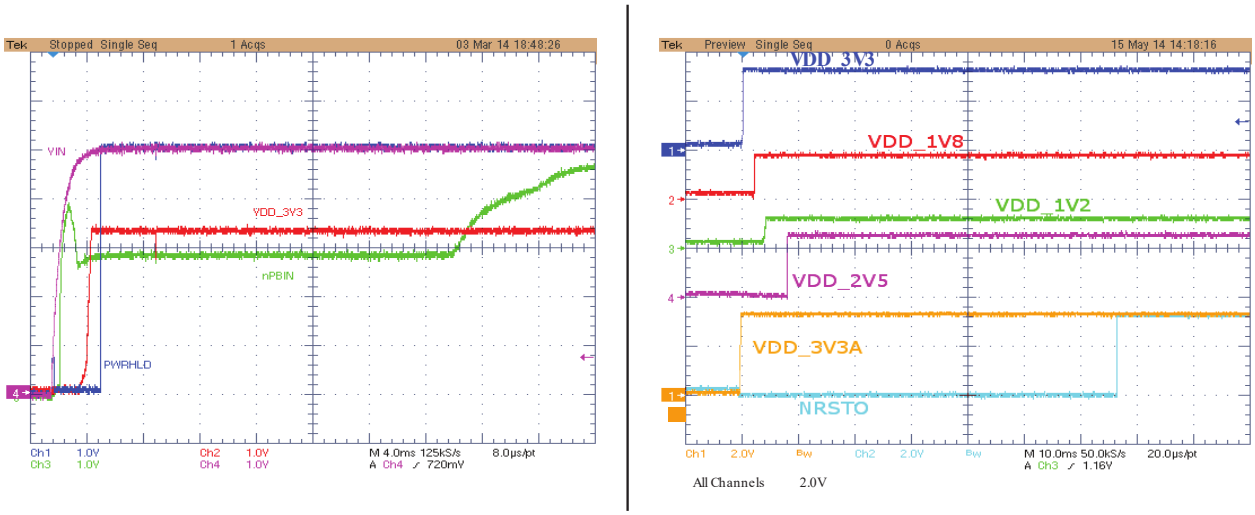
3.1.1 First Power-On

From an OFF state and when VSYS is greater than 3.5V, the application is powered up by asserting the nPBIN to ground through a 50 kΩ resistor, either manually with a user button (PB1) or automatically at VSYS ramp-up with the optional C_{ST}/R_{ST} network from VDDREF input (or VSYS in ACT8945A) to the Q3 gate. ACT8865/ACT8945A require their PWRHLD input to be held to '1' before the nPBIN pin is released. This is achieved by connecting the PWRHLD pin to the SHDN output of the Microchip MPU through the Q1/Q2 network. This "buffer" network prevents the VDDBU power supply from back-powering the main power supply when this supply is OFF or disconnected.

Note: As a general rule, to avoid extra leakages in the VDDBU power domain, the I/Os of the MPU belonging to the VDDBU power domain (WKUP, PIOBUx, RXD, COMPP, COMPN and SHDN) must not be directly connected to the I/Os of the PMIC. In case of direct connection, leakage paths from the VDDBU power domain to the main power domain can be created through the ESD protection diodes of these I/Os.

The SHDN pin, designed to control an external regulator enable pin, defaults to '1' (VDDBU level) before the system starts. At power-on, the PMIC sequences the ramp-up of the five rails (VDD_3V3 and VDD_3V3A, VDD_1V8 (or VDD_1V5 or VDD_1V35), VDD_1V2 and VDD_2V5) and de-asserts the nRSTO line after a typical 64 ms delay. The remaining channels (OUT6–OUT7) are enabled by software through the I^2C serial port.

Figure 3-2. Typical First Power-On Waveforms (Automatic Start with C_{ST} and R_{ST})



3.1.2 Power-On From Backup Mode

If the MPU is in Backup mode, i.e., with only VDDBU pin powered from a storage element, the system can wake up upon either an event on an input pin (WKUP, PIOBUx) or an event on an internal peripheral (RTC alarm, RXLP, ACC or security module). When such an event occurs, the MPU drives the SHDN pin up to '1' (VDDBU level). This transition on the SHDN output is applied to the gate of Q3 through R18/C26 to create a pulse low on nPBIN (through the 50 kΩ resistor) which makes the PMIC start. The high level on SHDN is also applied to the PWRHLD input of the PMIC as required.

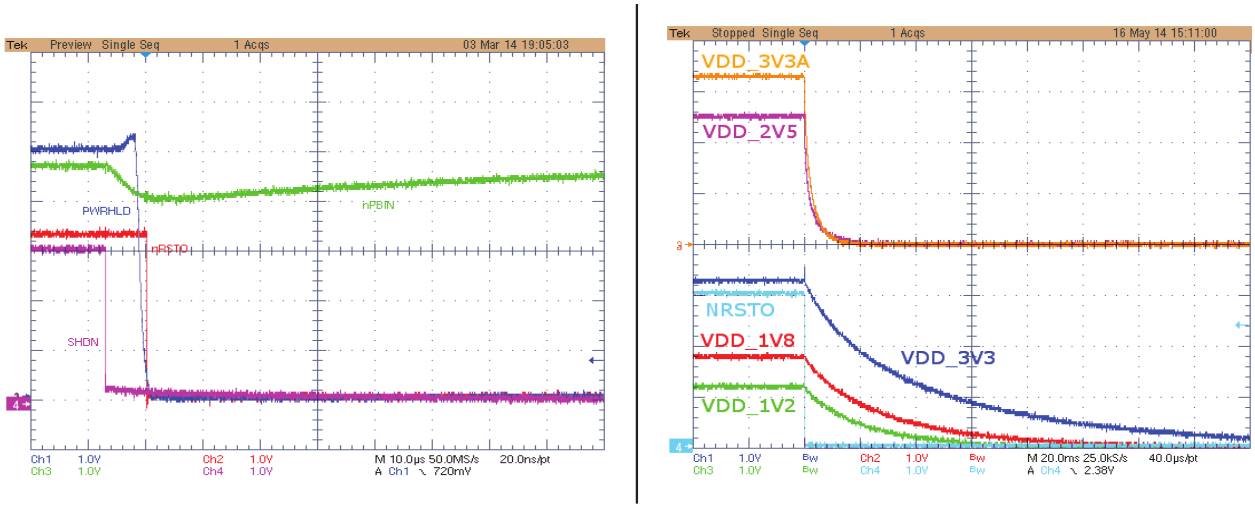
3.1.3 Software Power-Off

When running, the system can be shut down by first stopping the OUT6 and OUT7 LDO regulators through the I^2C interface and then de-asserting the PWRHLD pin of the PMIC. This de-assertion is done by issuing the shutdown command in the Shutdown Control Register of the MPU (SHDW_CR.SHDW = 1) which drives the SHDN pin down to '0'.

When the PWRHLD input falls, the PMIC shuts down which means the nRSTO line is asserted low and the regulators OUT1–OUT5 are simultaneously stopped.

Assertion of the shutdown command makes the MPU enter Backup mode. To exit this mode, the application must have configured the wake-up source (WKUP pin event, RTC alarm event, Analog Comparator event, etc.) before asserting the shutdown command. Refer to the Shutdown Controller (SHDWC) section and the Electrical Characteristics section (Low-power modes) of the Microchip device datasheet for further details.

Figure 3-3. Typical Software Power-Off Waveforms



Note: The ACT8865/ACT8945A PMICs have a special MSTROFF bit which can use an I^2C command to perform a power-off. When sending this command over the I^2C bus, the nRSTO line falls abnormally before the “stop-condition” of the I^2C transfer. Microchip does not recommend to use this method. In case this feature is to be used, it is advisable to install a few microseconds delay network (R_D/C_D) on the nRSTO line of the PCB.

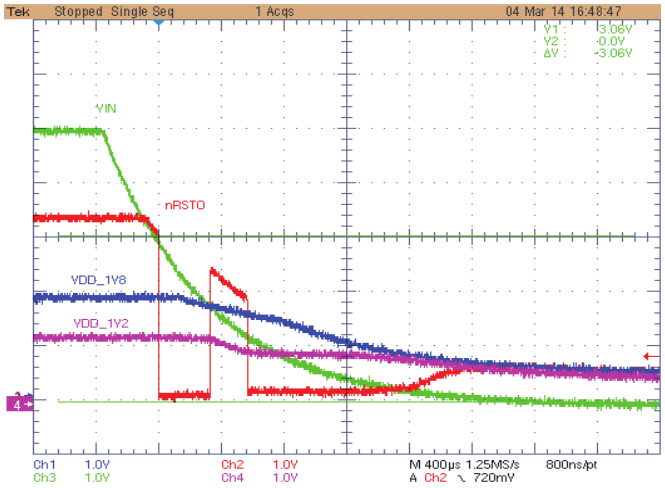
3.1.4 Power-Off Upon Input Power Loss

In case of input power loss (VSYS), the system power-off can also be managed by the PMIC. ACT8865/ ACT8945A integrate a programmable system voltage monitor that compares the VDDREF (ACT8865) or VSYS (ACT8945A) input to a programmable threshold set to 3.0V by default. If the input power falls below this threshold, one of two possible actions occurs:

- An “Under Voltage Alarm” interrupt is sent to the MPU through the nIRQ line and a software power-off is started by the application. In particular, for SAMA5D2x devices equipped with an external LPDDR2 or LPDDR3 memory, this flag can be used to avoid an “Uncontrolled Power-Off” of the LPDDR2 or LPDDR3 device.
- The PMIC initiates an automatic power-off sequence (without MPU intervention).

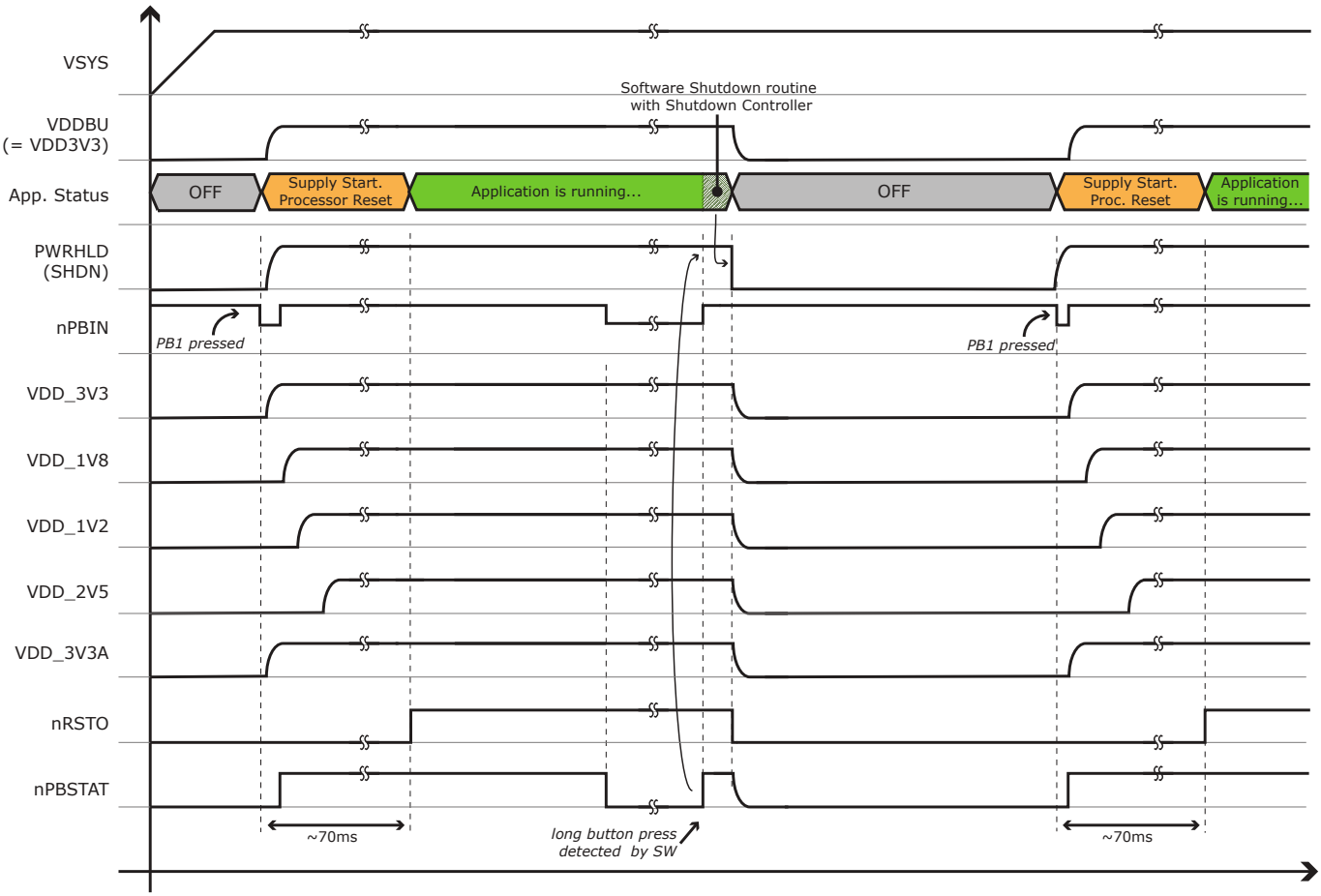
The behavior of the PMIC in response to the system voltage monitor is programmed by the nSYSMODE[] bit (see ACT8865/ACT8945A datasheets).

Figure 3-4. Typical Power-Off Waveforms in Case of Input Power Loss



3.2 Application Without Backup Capability

Figure 3-5. Typical Application Timing Diagram: Application Without Backup Capability (Case 2)



3.2.1 First Power-On

As with the previous application case, the system is powered up by asserting the nPBIN to ground through a 50 kΩ resistor. This assertion is either manual (PB1) or automatic (optional C_{ST}/R_{ST} network) and leads to the sequenced start-up of the five rails (VDD_3V3 and VDD_3V3A, VDD_1V8 (or VDD_1V5 or VDD_1V35), VDD_1V2 and VDD_2V5). The SHDN pin supplied by VDDBU (= VDD_3V3) is at 0V before the PMIC starts. When VDD_3V3 rises, the SHDN pin rises to '1' and drives the PWRHLD input of the PMIC to '1' as required.

3.2.2 Software Power-Off

To shut down the PMIC, the application must first stop the auxiliary LDO regulators (OUT6 and OUT7) through the I^2C interface and then de-assert the PWRHLD pin of the PMIC. As in the previous application case, this is achieved by issuing the shutdown command in the Shutdown Control Register (SHDW_CR.SHDW = 1) of the MPU. When this command is issued, SHDN falls which makes the PWRHLD input fall. The PMIC ties the nRSTO line to ground and the DC/DC converters are then simultaneously stopped.

3.2.3 Power-Off Upon Input Power Loss

Please refer to 3.1.4 Power-Off Upon Input Power Loss.

4. Active-Semi PMICs and Microchip MPUs Low-Power Modes

4.1 Active-Semi PMIC Power-Saving Mode

ACT8865 and ACT8945A integrated DCDCs feature a Power-Saving Mode (PSM) to reduce their power consumption at light output load. By default at startup, the DCDCs operate in fixed frequency Pulse Width Modulation (PWM) mode. This mode achieves the best ripple and regulation performance. Typically, when operated in PWM mode, the three DC/DC converters current consumption is about 20 mA @ 5V input voltage or 15 mA @ 3.7V.

To operate the DCDCs in PSM, the application needs to clear the MODE[] bits of registers REG1, REG2 and REG3 in the PMIC user interface. The current consumption is then reduced to 330 µA @ 5V input or 300 µA @ 3.7V. The penalty of this mode is a slightly higher output voltage ripple (about 10 mVpp compared to less than 5 mVpp in PWM) and higher transient output voltage under load steps. Figure 4-1 reports output voltage ripple on VDD_1V2 for both PSM and PWM mode. These curves are obtained with the following conditions: VIN = 5V, VDD_1V2 = 1.2V. The red curve is the switching node (SW2), and the blue curve is the output voltage AC-coupled at 10 mV/division.

Figure 4-1. Ripple Performance in PSM (Left) and PWM (Right) Modes

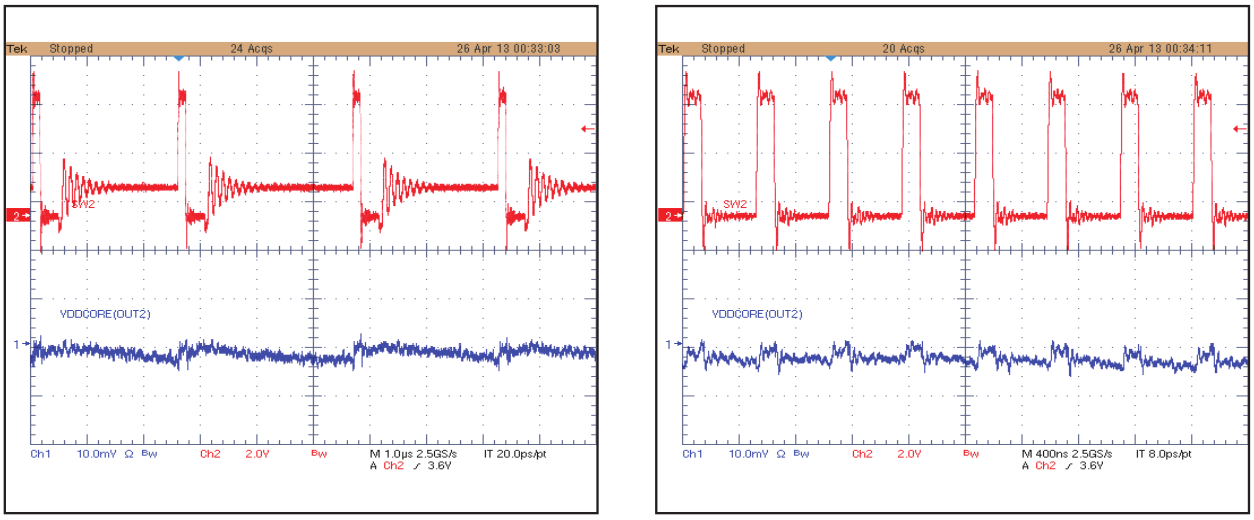
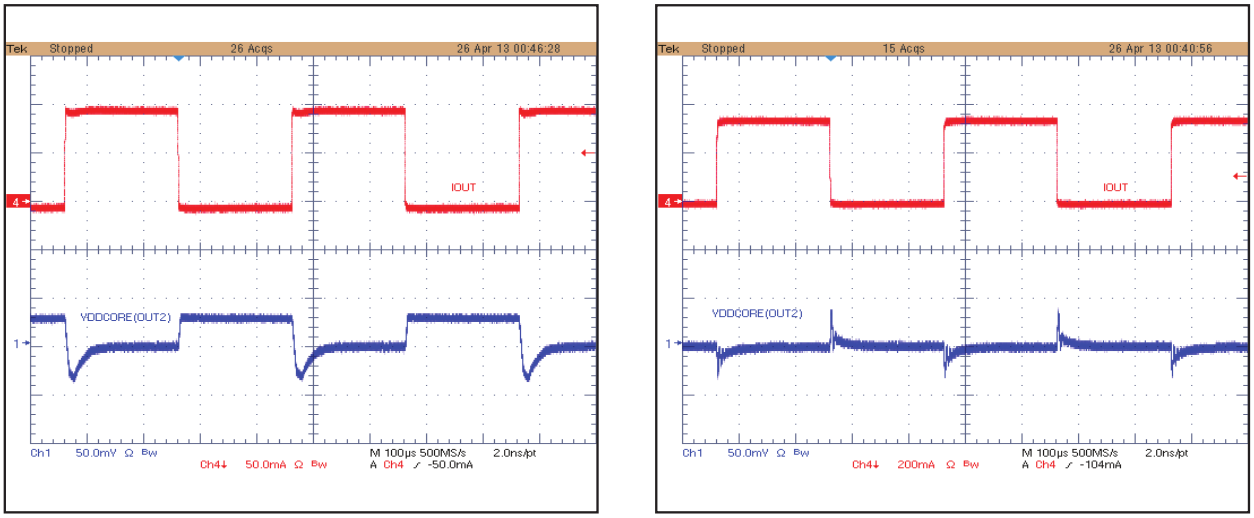


Figure 4-2 reports transient load regulation on VDD_1V2 for both PSM and PWM modes. The load step (red curve) is 0–100 mA in PSM and 0–500 mA in PWM mode. The rise and fall time of the load current is 1 µs. These curves are obtained with the following conditions: VIN = 5V, VDD_1V2 = 1.2V. The blue curve is the output voltage AC-coupled at 50 mV/division.

Figure 4-2. Transient Load Performance in PSM (Left) and PWM (Right) Modes



When the MODE[] bits of registers REG1, REG2 and REG3 are cleared, the DCDCs automatically transition from PWM mode to PSM at light load current and conversely transition back to PWM mode if the load current is increased (wake-up cases).

4.2 SAMA5D2x Series Low-Power Modes

Table 4-1 summarizes the low-power modes of SAMA5D2x devices with indicative power consumption figures at 25 °C. In Idle mode and in Ultra Low-Power mode, the power supplies are still ON with reduced power consumption and it is therefore relevant to set the DC/DC converters in PSM.

Table 4-1. Active Power Supplies in SAMA5D2x Low-Power Modes

Power Rail	Backup Mode	Idle Mode	Ultra Low-Power Mode
VDD_3V3	OFF	Application-dependent	200 µA(3)
VDD_1V8	OFF	Application-dependent	200 µA(3)
VDD_1V2	OFF	24 mA(1)	520 µA(2)
VDDBU	4.2 µA typical		

Note:

1. MCK at 166 MHz
2. MCK at 750 kHz
3. Typical conditions

For maximum regulation performance, the PSM should be activated as late as possible in the process of entering the Ultra Low-Power mode of the MPU. In a similar way, the PWM mode should be restored as soon as possible when re-entering Run mode.

5. Linux Driver Content and Description

5.1 Linux Voltage and Current Regulator Framework

The PMIC driver is implemented as a regulator driver under the voltage and current regulator framework. The framework is designed to provide a standard kernel interface to control voltage and current regulators. It provides the following four parts:

- Regulator Driver—The regulator is defined as a device that supplies power to other devices. The framework provides the interface to allow drivers to register the regulators and provide operations to the core.
- Consumer Driver—The consumer is defined as a device that is supplied by a regulator. The framework provides the interface to allow the consumer to complete the control over their supply voltage and current limit.
- Machine Special Setup Code—The framework provides an interface to allow the machine special setup code to create the voltage/current constraints for each regulator, and to create a regulator tree whereby some regulators are supplied by others. It is substituted by the device tree in the latest version.
- Userspace Interface—The framework also exports useful information to userspace via sysfs.

For more information about the Linux regulator framework, please see the Linux kernel document:

`Documentation/power/regulator/overview.txt.`

5.2 ACT8865 Regulator Driver

The ACT8865 regulator driver source code is available at:

```
drivers/regulator/act8865-regulator.c.
```

As mentioned above, the Active-Semi PMIC (ACT8865) is controlled as a slave I^2C device, so the ACT8865 regulator driver is implemented as an I^2C client driver using the i2c_driver model. The code configures the regulator_desc structure for each regulator and registers the regulators to the core by invoking devm_regulator_register(). To ease development, the register map library (regmap) and the helper functions are used.

5.3 Kernel Configurations to Enable ACT8865 Driver

The ACT8865 driver is enabled through the kernel configuration.

```
Device Drivers  --->
[*] Voltage and Current Regulator Support  --->
    <*> Active-semi act8865 voltage regulator
```

5.4 Declaring the Regulator Device Node

To make the regulators work, the ACT8865 device must be properly declared in the device tree files.

ACT8865 is declared as an I^2C client device with the I^2C slave address 0x5B assigned by the property ‘reg’.

More regulator properties defined as the regulator binding are available in the Linux kernel document:

`Documentation/devicetree/bindings/regulator/regulator.txt`

`Documentation/devicetree/bindings/regulator/act8865-regulator.txt`

For example, the regulator's device node on the SAMA5D2 Xplained board is declared as follows:

```
        i2c0: i2c@f8028000 {
                dmas = <0>, <0>;
                pinctrl-names = "default";
                pinctrl-0 = <&pinctrl_i2c0_default>;
                atmel,twd-hold-cycles = <25>;
                status = "okay";

                pmic: act8865@5b {
                    compatible = "active-semi,act8865";
                    reg = <0x5b>;
                    active-semi,vsel-high;
                    status = "okay";

                    regulators {
                        vdd_1v35_reg: DCDC_REG1 {
                            regulator-name = "VDD_1V35";
                            regulator-min-microvolt = <1350000>;
                            regulator-max-microvolt = <1350000>;
                            regulator-always-on;
                        };

                        vdd_1v2_reg: DCDC_REG2 {
                            regulator-name = "VDD_1V2";
                            regulator-min-microvolt = <1100000>;
                            regulator-max-microvolt = <1300000>;
                            regulator-always-on;
                        };

                        vdd_3v3_reg: DCDC_REG3 {
                            regulator-name = "VDD_3V3";
                            regulator-min-microvolt = <3300000>;
                            regulator-max-microvolt = <3300000>;
                            regulator-always-on;
                        };

                        vdd_fuse_reg: LDO_REG1 {
                            regulator-name = "VDD_FUSE";
                            regulator-min-microvolt = <2500000>;
                            regulator-max-microvolt = <2500000>;
                            regulator-always-on;
                        };

                        vdd_3v3_lp_reg: LDO_REG2 {
                            regulator-name = "VDD_3V3_LP";
                            regulator-min-microvolt = <3300000>;
                            regulator-max-microvolt = <3300000>;
                            regulator-always-on;
                        };

                        vdd_led_reg: LDO_REG3 {
                            regulator-name = "VDD_LED";
                            regulator-min-microvolt = <3300000>;
                            regulator-max-microvolt = <3300000>;
                            regulator-always-on;
                        };

                        vdd_sdhc_1v8_reg: LDO_REG4 {
                            regulator-name = "VDD_SDHC_1V8";
                            regulator-min-microvolt = <1800000>;
                            regulator-max-microvolt = <1800000>;
                            regulator-always-on;
                        };
                    };
                };
            };
```

The values of the regulators' properties are assigned by hardware design, such as regulator-min-microvolt and regulator-max-microvolt. It is good practice to name the 'regulator-name' property with the supply name in the schematic to ease system analysis.

5.5 Regulator Consumer Driver

The regulator consumer uses a regulator to change the power supply voltage or turn the power on/off. The consumer selects the regulator to use through the regulator mapping.

This mapping can be achieved through the device tree using the bindings below in the consumer node.

```
- <name>-supply: phandle to the regulator node
```

The name is used as the power supply ID to have access to its supply regulator.

The regulator framework provides the consumer driver interfaces that can be used to set and enable/disable the regulator voltage.

A detailed description of consumer interfaces is available in the Linux kernel document:

`Documentation/devicetree/bindings/regulator/consumer.txt.`

5.6 Regulator sysfs Entries

Useful regulator information can be read from the user space via sysfs. This method is useful to monitor device power consumption and status.

Refer to `Documentation/ABI/testing/sysfs-class-regulator`.

```
# cd /sys/class/regulator/
# ls
regulator.0  regulator.2  regulator.4  regulator.6
regulator.1  regulator.3  regulator.5  regulator.7
# ls regulator.2
device          name       state               suspend_standby_state
max_microvolts  num_users  subsystem           type
microvolts      of_node    suspend_disk_state  uevent
min_microvolts  power      suspend_mem_state
# cat regulator.2/name
VDD_1V2
# cat regulator.2/type
voltage
# cat regulator.2/state
enabled
# cat regulator.2/max_microvolts
1300000
# cat regulator.2/min_microvolts
1100000
# cat regulator.2/mi
microvolts      min_microvolts
# cat regulator.2/microvolts
1200000
```

6. Revision History

Doc. Rev.	Changes
DS00002836A	Format changes: • Moved from Atmel to Microchip template. • The application note is assigned a new document number (DS00002836) and revision letter is reset to A. Document number DS00002836A revision A corresponds to what would have been 44060 revision C. • ISBN number assigned. Updated Figure 2-1 and Figure 2-2 Added reference to Peripheral Touch Controller (PTC) in Analog and Clock Circuits Power Supply
44060B	Table 1-1: updated VDDCORE to 0.2A (was 0.4A). Updated first paragraph of nRSTO Output.
44060A	First release

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