



SAMA5D2 Discrete Power Supply Solution

APPLICATION NOTE

Scope

A wide variety of applications based on Atmel® | SMART SAMA5D2 embedded MPUs (eMPUs) can be powered from a low-cost power supply solution based on discrete components. This application note provides developers with a recommended application schematic and associated functional descriptions.

Reference Documents

Type	Title	Atmel Lit. No.
Datasheet	SAMA5D2 Datasheet	11267

Table of Contents

Scope.....	1
1. Power Supply Overview of Atmel SAMA5D2 Systems.....	3
1.1. Atmel SAMA5D2 Power Rails.....	3
1.2. Power Supply Topologies and Power Distribution.....	4
1.3. Clock Circuits Power Supply.....	5
1.4. Power Supplies Monitoring.....	5
2. Reference Schematic and Description.....	6
2.1. Basic Reference Schematic.....	6
2.2. Wake-Up and Shutdown Descriptions.....	7
3. Variations from the Reference Schematic.....	10
3.1. Applications Without Backup Battery.....	10
3.2. Start-up Circuit Examples.....	10
3.3. Input Power-Fail Detection.....	11
3.4. Discrete Components Selection.....	12
4. Revision History.....	13

1. Power Supply Overview of Atmel SAMA5D2 Systems

1.1. Atmel SAMA5D2 Power Rails

Atmel SAMA5D2x MPUs power rails and their respective operating ranges are listed in [Table 1-1](#). An approximate current consumption is provided for each rail in order to size the corresponding regulator. Accurate numbers and descriptions are provided in the device datasheet.

In most non-secure applications, the MPU subsystem (device + external memories) can be operated from three primary rails:

- 3.3V,
- 1.2V, and
- 1.8V, 1.5V or 1.35V depending on the type of external memory mounted on the board.

In secure applications of the SAMA5D2x device, or any application that requires writing into the fuse box of SAMA5D2x, an additional power rail at 2.5V is needed to supply the VDDFUSE input pin.

Additionally, Atmel SAMA5D2 has a special VDDDBU pin to power its backup domain (32 kHz crystal oscillator, RTC, System Controller, etc.). When needed, and because of its ultra-low power consumption, this power domain can be maintained during powerdown periods with a storage element such as a 3.0V lithium coin cell battery or a super-capacitor. Otherwise, applications can operate VDDDBU on the main 3.3V power rail.

Table 1-1. SAMA5D2x Series Power Supply Inputs

Power Rail	Description	Range	Consumption
VDDCORE	Core logic	1.10 – 1.32V, 1.20V	0.2A
VDDUTMIC	USB device and host UTMI+ core logic	1.10 – 1.32V, 1.20V	0.02A
VDDPLLA	PLLA cell	1.10 – 1.32V, 1.20V	0.02A
VDDHSIC	USB HSIC interface I/O lines	1.10 – 1.32V, 1.20V	0.01A
VDDIODDR	LPDDR / DDR2 memory interface I/O lines	1.70 – 1.90V, 1.80V	0.05A
	LPDDR2 / LPDDR3 memory interface I/O lines	1.14 – 1.30V, 1.20V	
	DDR3L memory interface I/O lines	1.29 – 1.45V, 1.35V	
	DDR3 memory interface I/O lines	1.43 – 1.57V, 1.50V	
VDDIOP0	Peripheral I/O lines	1.65 – 3.60V	0.03A
VDDIOP1	Peripheral I/O lines	1.65 – 3.60V	0.03A
VDDIOP2	Peripheral I/O lines	1.65 – 3.60V	0.03A
VDDISC	Image sensor I/O lines	1.65 – 3.60V	0.03A
VDDSDMMC	SDMMC I/O lines	1.65 – 1.95V, 1.80V	0.03A
		3.00 – 3.60V, 3.30V	

Power Rail	Description	Range	Consumption
VDDUTMII	USB host and device UTMI+ interface I/O lines	3.00 – 3.60V, 3.30V	0.02A
VDDOSC	Main oscillator and UTMI PLL	1.65 – 3.60V, 3.30V	0.01A
VDDAUDIOPLL	Audio PLL	3.00 – 3.60V, 3.30V	0.01A
VDDANA	Analog-to-digital converter, peripheral touch controller analog front-end	1.65 – 3.60V, 3.30V	0.01A
VDDFUSE	Programmable fuse box	2.25 – 2.75V, 2.50V	0.05A
VDDDBU	Backup domain	1.65 – 3.60V	0.0001A

In all modes other than Backup mode and Backup mode with DDR in self-refresh of the MPU, every power supply input must be powered to operate the device. The only exception to this rule is the VDDFUSE input, which can be left unpowered if the SAMA5D2x fuse box is not used in Write mode.

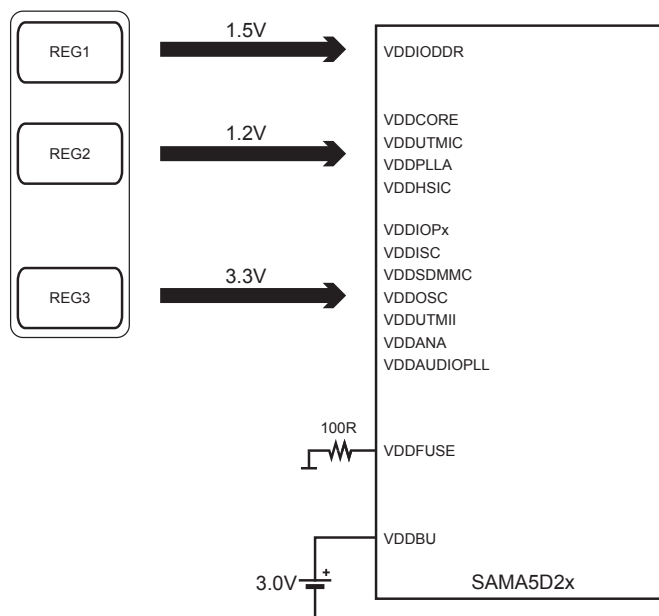
1.2. Power Supply Topologies and Power Distribution

For SAMA5D2-based systems, the lowest cost power supply solution is achieved by implementing a 3-rail topology (3.3V / 1.2V and 1.8V or 1.5V or 1.35V) as shown in the following figure. While optimized from a system cost perspective, this topology has the following limitations:

- The fuse box cannot be accessed in Write mode because VDDFUSE = 0V.
- The analog sections of the device (VDDANA, VDDAUDIOPLL, VDDOSC) are powered from the (noisy) digital 3.3V rail.

These limitations can be overcome by adding two regulators: one at 3.3V (for VDDANA, VDDAUDIOPLL, VDDOSC) and another one at 2.5V (for VDDFUSE). In such case, these regulators should be enabled and disabled along with the main 3.3V regulator.

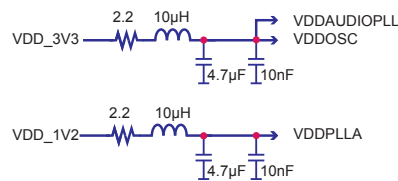
Figure 1-1. 3-channel Power Supply Example on SAMA5D2x Series Equipped with a 1.5V External Memory (DDR3)



1.3. Clock Circuits Power Supply

Atmel eMPUs have separate power supply inputs for their oscillators and PLL circuits. These analog circuits can be decoupled from the digital (core and I/Os) activity of the device and thus generate less jittered clocks. Atmel highly recommends feeding these power supply inputs with low-noise sources for applications where clock jitter is important (e.g., high-speed USB). The simplest way to do this is to filter the digital rails with an LC network as shown in the following figure. Choosing a 20 kHz corner frequency is a good trade-off between component size/cost and the necessary high-frequency attenuation for clock circuits. The inductors must be sized for low DC resistance and good DC superimposition characteristics (TDK MLZ series and Taiyo Yuden CBM series are possible choices). The serial resistor in the filter schematic must be adjusted to take the inductor DCR into account. Example of inductors: Taiyo Yuden CBMF1608T100K (10 μ H, 0.36 Ω , 115 mA, 0603) and TDK MLZ1608N100L (10 μ H, 0.6 Ω , 60 mA, 0603).

Figure 1-2. Recommended Filter on Clock Circuits Power Supply



1.4. Power Supplies Monitoring

Atmel MPU power rails are not internally monitored. In low-cost systems, when the input power can be removed without advising the application, it is recommended to monitor the input voltage to detect the input power loss. In this power-fail case, the application should start a power-off sequence. This is particularly relevant in SAMA5D2 systems equipped with LPDDR2 or LPDDR3 memories that can be damaged under repeated uncontrolled power-off sequences.

run at a lower voltage (e.g., 3.0V) if the maximum voltage applied to the eMPU power inputs is also limited (e.g., 2.8V, 2.5V or 1.8V).

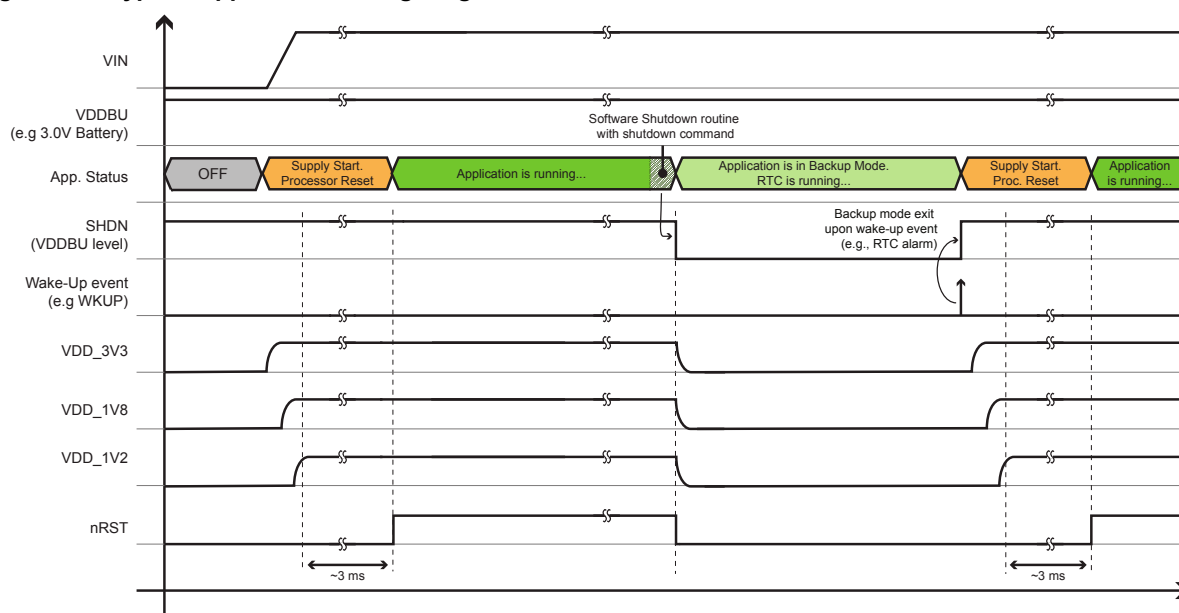
VIN supplies a linear low dropout regulator (U1) to build the VDD_3V3 voltage and a DC/DC buck regulator (U2) to build the VDD_1V8 (or VDD_1V5 or VDD_1V35) voltage. The VDD_1V2 voltage is built from the VDD_1V8 rail by the low input voltage low dropout regulator (U3).

The topology with only one DC/DC regulator is intended for low-cost systems where LDO regulators offer some cost advantages over DC/DC regulators. However, the principles described in this application note about the regulators' control are still applicable if the user replaces one or two LDO regulator(s) by one or two DC/DC regulator(s).

Low-cost discretes are used to control the regulators' enable pins (EN) and the NRST signal of the eMPU. As demonstrated below, this schematic ensures proper supply sequencing and reset assertion during power-up and power-down phases.

This power supply is designed to be controlled by the eMPU Shutdown Controller (SHDWC) and its SHDN pin. Refer to the section "Shutdown Controller (SHDWC)" in the SAMA5D2 datasheet for a complete description. In summary, SHDN is high when the eMPU is running, and SHDN is low when the eMPU goes to Backup mode or to OFF mode. The SHDN pin defaults to '1' (VDDDBU level) when VDDDBU is first applied. The following figure shows a typical application timing diagram, and in particular the use of the Shutdown Controller.

Figure 2-2. Typical Application Timing Diagram



2.2. Wake-Up and Shutdown Descriptions

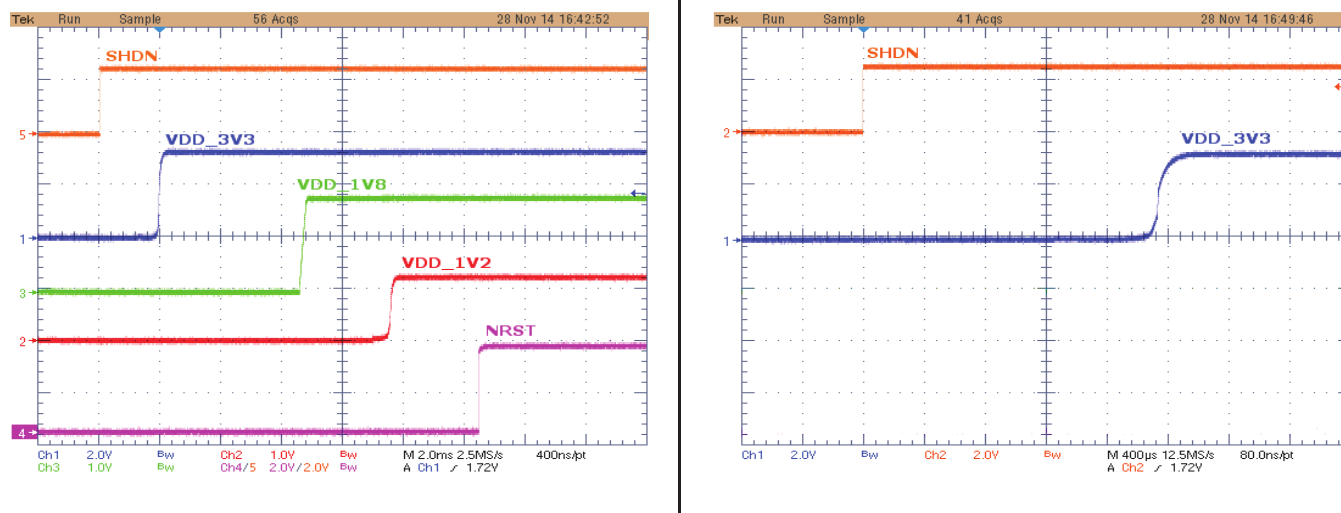
2.2.1. Wake-Up Description

The figure below shows the typical wake-up waveforms of the basic reference schematic power supply. In the left-hand image, upon a wake-up event (not shown here), the processor pulls the SHDN pin high (VDDDBU level, here 2.5V) and exits Backup mode. SHDN is applied through Q1 and Q2 to the enable pin of U1. The delay between SHDN and the start of regulator U1 is tuned with the $(R44 + R45) / C15$ network (here about 2 ms, shown in the right-hand image). U1 starts regulating the VDD_3V3 output to 3.3V which enables the U2 regulator through the $R48 / C18$ delay network (here about 5 ms). When U2

starts regulating VDD_1V8 at 1.8V (or VDD_1V5 at 1.5V or VDD_1V35 at 1.35V), it enables the regulator U3 through the R43 / C11 delay network (here about 3 ms). During this start-up phase, the processor is held in reset with its NRST pin driven by the PG (power-good) output of U3. U3 releases this output about 3 ms after VDD_1V2 has reached 90% of its final value.

The NRST input of the SAMA5D2 series belongs to the VDDDBU power domain and is neither internally pulled high nor low. Note that connecting the pullup resistor to the VDDDBU rail would create a leakage path to VIN (pullup resistor + protection diode in the PG pin of U3) when VIN is 0. Therefore, this is not recommended in systems where VDDDBU is powered by a battery.

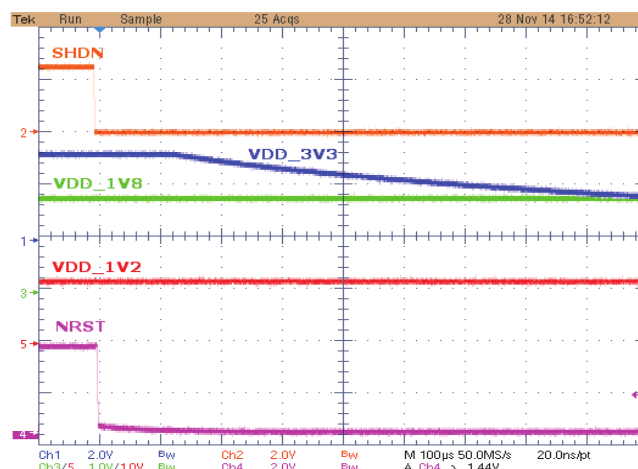
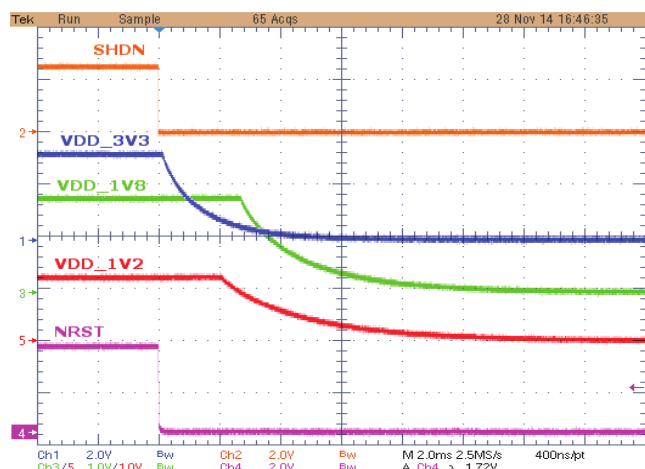
Figure 2-3. Wake-up Waveforms



2.2.2. Shutdown Description

The figure below shows the typical shutdown waveforms of the reference schematic power supply. In the left-hand image, upon a shutdown request in the Shutdown Control Register (SHDW_CR), the processor pulls the SHDN pin low and enters Backup mode. NRST is almost immediately pulled low through Q1, Q2 and Q3. The delay between the SHDN falling edge and the NRST signal assertion is less than 10 μs and depends on the R54-C_{STARTB} delay. C_{STARTB} is a sum of parasitic capacitances at node STARTB (Q1's drain capacitance, Q2 and Q3's gate capacitances). After the R45 / C15 delay (about 100 μs as depicted in the right-hand image), the enable pin of U1 falls. U1 stops and discharges its output capacitor through its internal discharge resistor. When VDD_3V3 falls, it discharges C18 through D1 and C11 and D2. The enable pins of U2 and U3 are pulled low, thus stopping these regulators.

Figure 2-4. Shutdown Waveforms

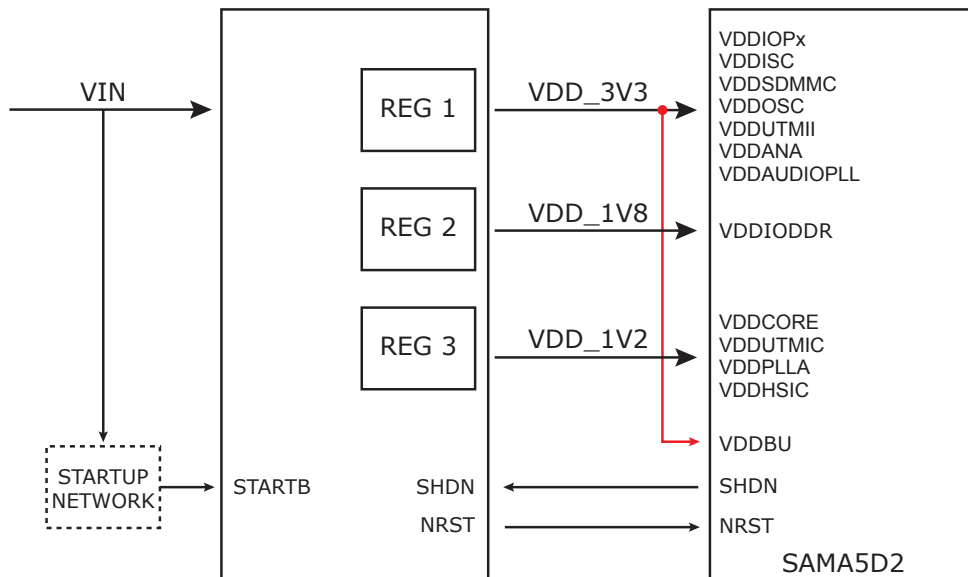


3. Variations from the Reference Schematic

3.1. Applications Without Backup Battery

When no backup functionality is required in an application, VDDBU can be fed by one regulator output instead of a storage element (e.g., a battery), as shown in the figure below. In this case, VDDBU is 0V before the power supply starts and SHDN, powered from the VDDBU rail, is also 0V. For this reason, the power supply of the reference schematic must be modified to start even when VDDBU = 0V. This is the purpose of the start-up network box shown in the following figure.

Figure 3-1. Applications Without Backup Battery



Each application has specific start-up event needs. Some examples of start-up events are:

- a start at VIN rise,
- a mechanical action, e.g. a push button,
- internal signals to trigger a power supply start.

From a generic usage perspective, note that forcing low the STARTB node (refer to [Basic Reference Schematic](#)) for a minimum of 5 ms is enough to start the power supply. Indeed, when STARTB is set to 0V, the U1 regulator starts after about 2 ms. As VDDBU is powered from VDD_3V3, VDDBU gets powered and the SHDN pin defaults to '1' (VDD_3V3 in this case). Q1 now forces STARTB to 0 V and the power supply does not need any further external intervention to keep working. A few examples of start-up networks are given in the following section.

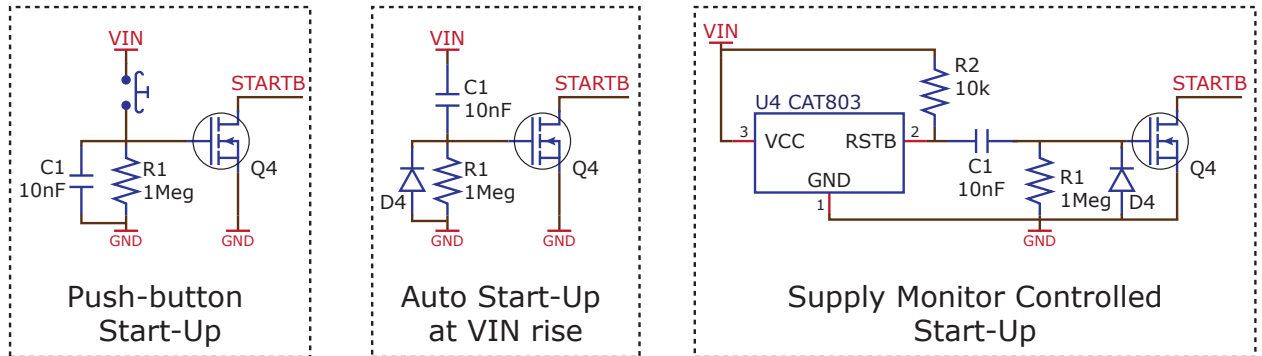
3.2. Start-up Circuit Examples

The following figure shows three examples of start-up circuits.

- In the first example, a push button start-up is implemented. As soon as the button is pressed, STARTB is pulled low, thus enabling the power supply to start.
- The second circuit is designed to start the power supply when VIN rises. The C1 / R1 network keeps Q4 in its ON state for about 10 ms. The disadvantage of this circuit is that it is not protected against out-of range VIN, i.e., it starts the power supply even with lower than acceptable VIN. For applications where VIN has a minimum guaranteed value, this circuit is suitable.

- The third start-up circuit is based on a supply monitor, thus ensuring safe VIN conditions to start the power supply. When VIN is above its internal threshold, the supply monitor releases its RSTB output after a specified delay (about 140 ms for CAT803 devices). Through C1, this transition is transmitted to Q4 which pulls STARTB low for about 10 ms and thus enables the power supply start-up.

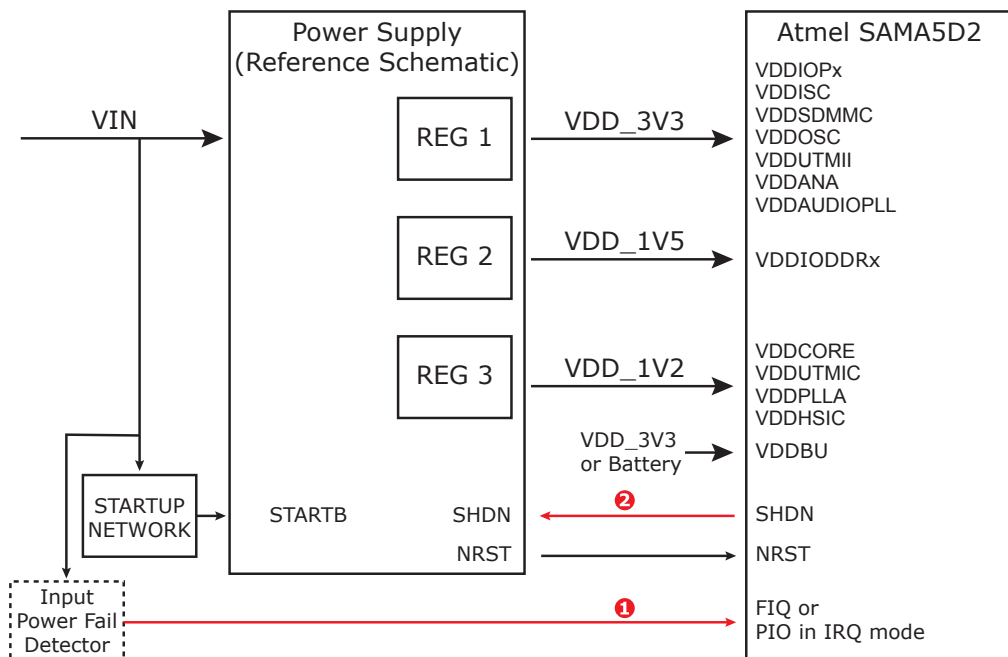
Figure 3-2. Examples of Start-up Circuits



3.3. Input Power-Fail Detection

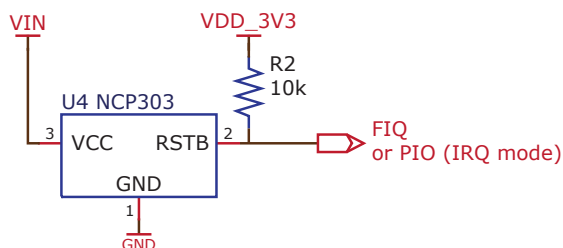
It is possible to add an input power-fail detection circuit to the [Basic Reference Schematic](#). The principle, described in the following figure, is to monitor the input voltage VIN and to warn the processor with an interrupt in case of power loss. The Fast Interrupt (FIQ) input or any I/O configured as an interrupt input may be used. Upon this interrupt request, a software power-off sequence is started during which some data storage and/or service shutdown may be performed depending on the remaining "ON" time. This power-off sequence then ends by setting bit SHDN in SHDN_CR. The SHDN pin falls down to 0, which turns off the power supply, as depicted in the figure below.

Figure 3-3. Power Loss Management Principle



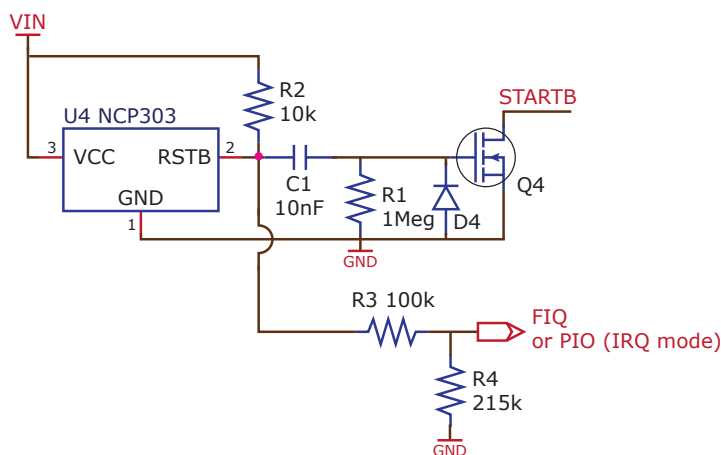
To monitor the input voltage VIN, several solutions are possible depending on available resources at system level. (e.g., a system with a voltage reference on-board requires a voltage comparator). The following figure shows one possible implementation using an integrated voltage monitor circuit.

Figure 3-4. Input Power-Fail Detection Example



In some applications, the input voltage monitor circuit may be used to generate both the STARTB signal and the interrupt signal. In such case, the voltage monitor output must not be directly connected to the SAMA5D2 I/O. It must be isolated by a series resistor as shown in the figure below. When VDD_3V3 is not started, if resistor R3 is not inserted, a leakage path is created through the internal protection diodes of the eMPU. This forces the output signal of the voltage detector U4 close to 0.6 V. Resistor R4 is inserted to scale down the VIN level of the monitor output to the VDD_3V3 level of the SAMA5D2 I/O used as an interrupt source. Due to the insertion of R3, the eMPU I/O is forced with a relatively high impedance. For this reason, the integrated pull-up and pull-down resistors of this I/O must be disabled.

Figure 3-5. Voltage Monitor at Start-Up and Shutdown



3.4. Discrete Components Selection

The discrete components listed in this application note are given as implementation examples. They are not strong recommendations. The reader may adapt the provided schematics to his specific needs and still keep the basic principles described in the previous sections. As the focus of this application note is the solution cost, only low-cost components are selected. This may lead to “over-sized” components compared to the real application need because they give the best price in this particular case. While cost and ease of procurement are the primary criteria for component selection, other criteria have to be considered to select other types of components:

- Regulators: Devices with an enable input and a power-good output ease the design of the power sequencing and reset generation circuits.
- NMOS transistors: Low threshold voltage (< 2V) devices are best to ensure safe commutation in all cases. Mind the minimum VDDBU specification of your application.
- Diodes: Any general-purpose, small signal device with a low reverse current specification (<20 nA at 20V and 25°C) is suitable.

4. Revision History

Doc. Rev.	Comments
B	Table 1-1 : updated VDDCORE to 0.2A (was 0.4A). Wake-up Description : added paragraph on NRST and VDDBU.
A	First issue

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