Universidade de Brasília — Faculdade UnB Gama

Teoria de Eletrônica Digital 2 - 1/2017

Teste 1 – 09/03/2017

Nome: RESOLUÇÃO **Matrícula:**__/_____

1. **Contadores** - Considerando o contador mostrado na **Fig. 1**, responda os itens abaixo.

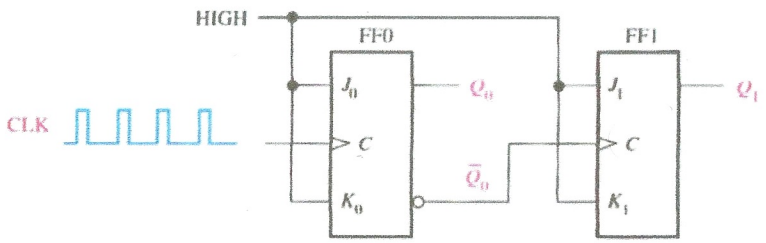


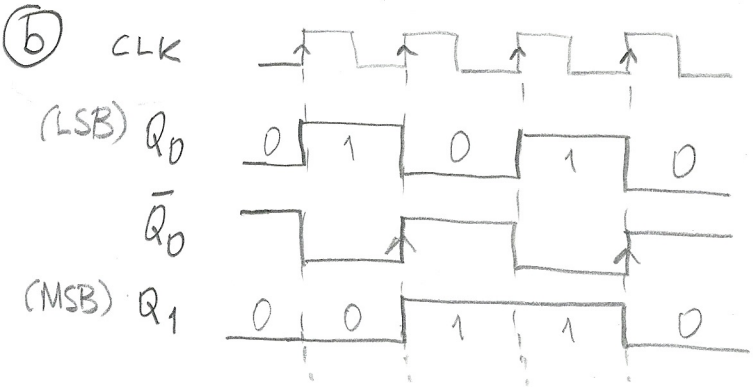
Fig. 1

a. Qual é o módulo do contador?
b. Esboce o diagrama de tempo e determine a sequência.
c. Repita o item **b** considerando que Q_0 está conectado à entrada de clock do FF1.
d. Repita o item **b** considerando que ambos os FFs estão conectados ao mesmo sinal de clock.

2. **Registradores de Deslocamento** - Responder o *Quiz*.

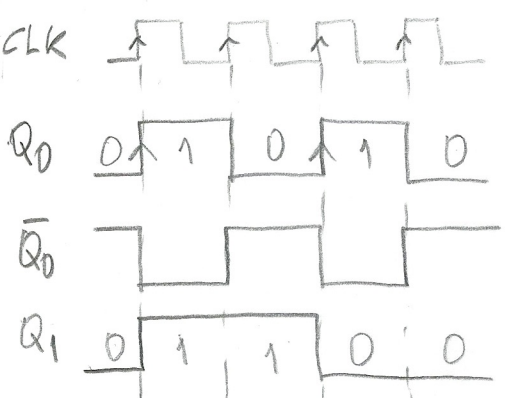
ⓐ 4 estados → Módulo 4

ⓑ



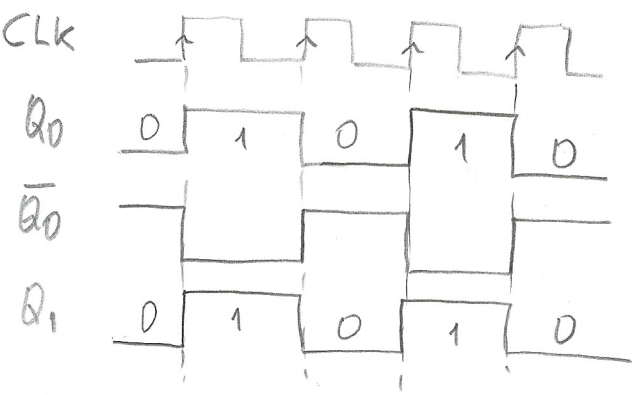
Sequência: 0, 1, 2, 3, 0 ...

ⓒ



Seq: 0, 3, 2, 1, 0, ...

ⓓ



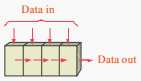
Sequência: 0, 3, 0, 3, 0...

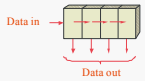
Para que o contador síncrono execute a sequência 0, 1, 2, 3, 0, ..., é necessário conectar Q_0 em J_1 e K_1.

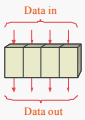
Quiz

1. The shift register that would be used to delay serial data by 4 clock periods is

a. 

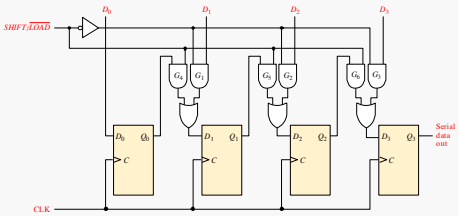
c. 

b. 

d. 

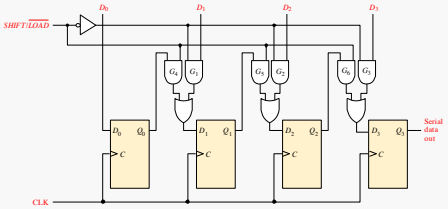
Quiz

2. The circuit shown is a
   a. serial-in/serial-out shift register
   b. serial-in/parallel-out shift register
   c. parallel-in/serial-out shift register
   d. parallel-in/parallel-out shift register



Quiz

3. If the *SHIFT*/$\overline{LOAD}$ line is HIGH, data
   a. is loaded from D_0, D_1, D_2 and D_3 immediately
   b. is loaded from D_0, D_1, D_2 and D_3 on the next CLK
   c. shifted from left to right on the next CLK
   d. shifted from right to left on the next CLK

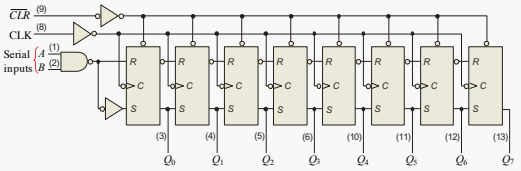


Quiz

4. A 4-bit parallel-in/parallel-out shift register will store data for
   a. 1 clock period
   b. 2 clock periods
   c. 3 clock periods
   d. 4 clock periods

Quiz

5. The 74HC164 (shown) has two serial inputs. If data is placed on the *A* input, the *B* input
   a. could serve as an active LOW enable
   b. could serve as an active HIGH enable
   c. should be connected to ground
   d. should be left open



Quiz

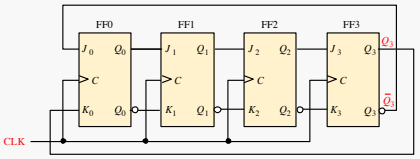
6. An advantage of a ring counter over a Johnson counter is that the ring counter
   a. has more possible states for a given number of flip-flops
   b. is cleared after each cycle
   c. allows only one bit to change at a time
   d. is self-decoding

Quiz

7. A possible sequence for a 4-bit ring counter is
   a. … 1111, 1110, 1101 …
   b. … 0000, 0001, 0010 …
   c. … 0001, 0011, 0111 …
   d. … 1000, 0100, 0010 …

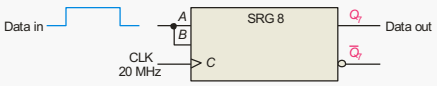
Quiz

8. The circuit shown is a
   a. serial-in/parallel-out shift register
   b. serial-in/serial-out shift register
   c. ring counter
   d. Johnson counter



Quiz

9. Assume serial data is applied to the 8-bit shift register shown. The clock frequency is 20 MHz. The first data bit will show up at the output in
   a. 50 ns
   b. 200 ns
   c. 400 ns
   d. 800 ns



Quiz

10. For transmission, data from a UART is sent in
    a. asynchronous serial form
    b. synchronous parallel form
    c. can be either of the above
    d. none of the above

Quiz

Answers:

1. a	6. d
2. c	7. d
3. c	8. d
4. a	9. c
5. b	10. a