PSoC® Creator™
Project Datasheet for Prototype

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Table of Contents

1 Overview

The Cypress PSoC 4 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M0 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 4200M series member PSoC 4 device. For details on all the systems listed above, please refer to the PSoC 4 Technical Reference Manual .

Figure 1. PSoC 4200M Device Series Block Diagram

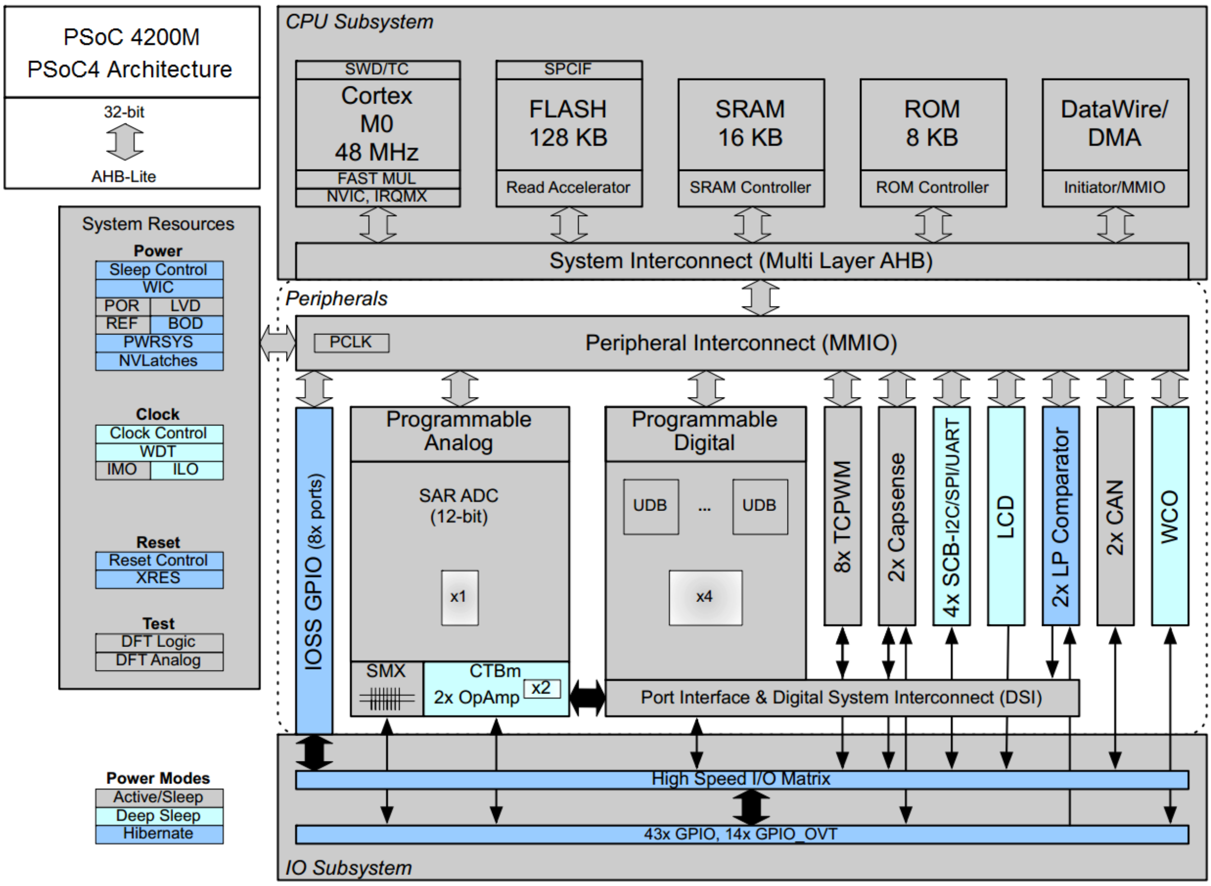


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C4247AZI-M485
Package Name	64-TQFP
Family	PSoC 4
Series	PSoC 4200M
Max CPU speed (MHz)	48
Flash size (kB)	128
SRAM size (kB)	16
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

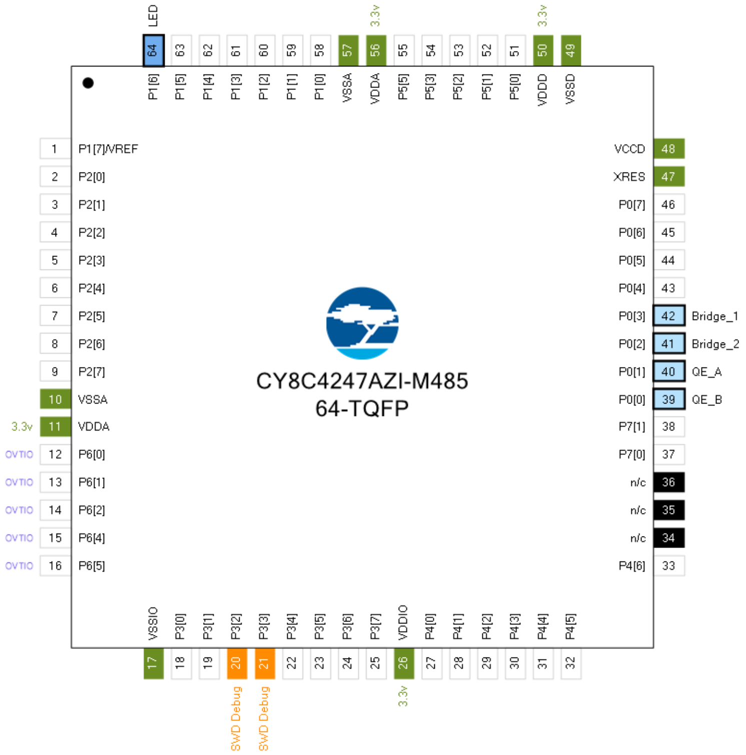
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	1	3	4	25.00 %
Interrupts	1	31	32	3.13 %
IO	7	44	51	13.73 %
Segment LCD	0	1	1	0.00 %
CapSense	0	2	2	0.00 %
Die Temp	0	1	1	0.00 %
CAN 2.0b	0	2	2	0.00 %
Serial Communication (SCB)	0	4	4	0.00 %
DMA Channels	0	8	8	0.00 %
Timer/Counter/PWM	3	5	8	37.50 %
UDB				
Macrocells	3	29	32	9.38 %
Unique P-terms	6	58	64	9.38 %
Total P-terms	6			
Datapath Cells	2	2	4	50.00 %
Status Cells	0	4	4	0.00 %
Control Cells	1	3	4	25.00 %
Control Registers	1			
Comparator/Opamp	0	4	4	0.00 %
LP Comparator	0	2	2	0.00 %
SAR ADC	0	1	1	0.00 %
DAC				
7-bit IDAC	0	2	2	0.00 %
8-bit IDAC	0	2	2	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
1	P1[7]/VREF	GPIO [unused], Dedicated		
2	P2[0]	GPIO [unused]		
3	P2[1]	GPIO [unused]		
4	P2[2]	GPIO [unused]		
5	P2[3]	GPIO [unused]		
6	P2[4]	GPIO [unused]		
7	P2[5]	GPIO [unused]		
8	P2[6]	GPIO [unused]		
9	P2[7]	GPIO [unused]		
10	VSSA	VSSA	Power	
11	VDDA	VDDA	Power	
12	P6[0]	OVT IO [unused]		
13	P6[1]	OVT IO [unused]		
14	P6[2]	OVT IO [unused]		
15	P6[4]	OVT IO [unused]		
16	P6[5]	OVT IO [unused]		
17	VSSIO	VSSIO	Power	
18	P3[0]	GPIO [unused]		
19	P3[1]	GPIO [unused]		
20	P3[2]	Debug:SWD_IO	Reserved	
21	P3[3]	Debug:SWD_CK	Reserved	
22	P3[4]	GPIO [unused]		
23	P3[5]	GPIO [unused]		
24	P3[6]	GPIO [unused]		
25	P3[7]	GPIO [unused]		
26	VDDIO	VDDIO	Power	
27	P4[0]	GPIO [unused]		
28	P4[1]	GPIO [unused]		
29	P4[2]	GPIO [unused]		
30	P4[3]	GPIO [unused]		
31	P4[4]	GPIO [unused]		
32	P4[5]	GPIO [unused]		
33	P4[6]	GPIO [unused]		
37	P7[0]	GPIO [unused]		
38	P7[1]	GPIO [unused]		
39	P0[0]	QE_B	Dgtl In	Res pull up
40	P0[1]	QE_A	Dgtl In	Res pull up
41	P0[2]	Bridge_2	Dgtl Out	Strong drive
42	P0[3]	Bridge_1	Dgtl Out	Strong drive
43	P0[4]	GPIO [unused]		
44	P0[5]	GPIO [unused]		
45	P0[6]	GPIO [unused]		
46	P0[7]	GPIO [unused]		
47	XRES	XRES	Dedicated	
48	VCCD	VCCD	Power	

Pin	Port	Name	Type	Drive Mode
49	VSSD	VSSD	Power	
50	VDDD	VDDD	Power	
51	P5[0]	GPIO [unused]		
52	P5[1]	GPIO [unused]		
53	P5[2]	GPIO [unused]		
54	P5[3]	GPIO [unused]		
55	P5[5]	GPIO [unused]		
56	VDDA	VDDA	Power	
57	VSSA	VSSA	Power	
58	P1[0]	GPIO [unused]		
59	P1[1]	GPIO [unused]		
60	P1[2]	GPIO [unused]		
61	P1[3]	GPIO [unused]		
62	P1[4]	GPIO [unused]		
63	P1[5]	GPIO [unused]		
64	P1[6]	LED	Software In/Out	Strong drive

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Dgtl Out = Digital Output

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	39	QE_B	Dgtl In	Res pull up
P0[1]	40	QE_A	Dgtl In	Res pull up
P0[2]	41	Bridge_2	Dgtl Out	Strong drive
P0[3]	42	Bridge_1	Dgtl Out	Strong drive
P0[4]	43	GPIO [unused]		
P0[5]	44	GPIO [unused]		
P0[6]	45	GPIO [unused]		
P0[7]	46	GPIO [unused]		
P1[0]	58	GPIO [unused]		
P1[1]	59	GPIO [unused]		
P1[2]	60	GPIO [unused]		
P1[3]	61	GPIO [unused]		
P1[4]	62	GPIO [unused]		
P1[5]	63	GPIO [unused]		
P1[6]	64	LED	Software In/Out	Strong drive
P1[7]/VREF	1	GPIO [unused], Dedicated		
P2[0]	2	GPIO [unused]		
P2[1]	3	GPIO [unused]		
P2[2]	4	GPIO [unused]		
P2[3]	5	GPIO [unused]		
P2[4]	6	GPIO [unused]		
P2[5]	7	GPIO [unused]		
P2[6]	8	GPIO [unused]		
P2[7]	9	GPIO [unused]		
P3[0]	18	GPIO [unused]		
P3[1]	19	GPIO [unused]		
P3[2]	20	Debug:SWD_IO	Reserved	
P3[3]	21	Debug:SWD_CK	Reserved	
P3[4]	22	GPIO [unused]		
P3[5]	23	GPIO [unused]		
P3[6]	24	GPIO [unused]		
P3[7]	25	GPIO [unused]		
P4[0]	27	GPIO [unused]		
P4[1]	28	GPIO [unused]		
P4[2]	29	GPIO [unused]		
P4[3]	30	GPIO [unused]		
P4[4]	31	GPIO [unused]		
P4[5]	32	GPIO [unused]		
P4[6]	33	GPIO [unused]		
P5[0]	51	GPIO [unused]		
P5[1]	52	GPIO [unused]		
P5[2]	53	GPIO [unused]		
P5[3]	54	GPIO [unused]		
P5[5]	55	GPIO [unused]		
P6[0]	12	OVT IO [unused]		

Port	Pin	Name	Type	Drive Mode
P6[1]	13	OVT IO [unused]		
P6[2]	14	OVT IO [unused]		
P6[4]	15	OVT IO [unused]		
P6[5]	16	OVT IO [unused]		
P7[0]	37	GPIO [unused]		
P7[1]	38	GPIO [unused]		

Abbreviations used in Table 4 have the following meanings:

- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Dgtl Out = Digital Output

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
Bridge_1	P0[3]	Dgtl Out
Bridge_2	P0[2]	Dgtl Out
Debug:SWD_CK	P3[3]	Reserved
Debug:SWD_IO	P3[2]	Reserved
GPIO [unused]	P3[7]	
GPIO [unused]	P4[3]	
GPIO [unused]	P4[4]	
GPIO [unused]	P4[2]	
GPIO [unused]	P4[0]	
GPIO [unused]	P4[1]	
GPIO [unused]	P5[2]	
GPIO [unused]	P0[4]	
GPIO [unused]	P5[0]	
GPIO [unused]	P0[6]	
GPIO [unused]	P0[5]	
GPIO [unused]	P7[1]	
GPIO [unused]	P4[6]	
GPIO [unused]	P5[1]	
GPIO [unused]	P7[0]	
GPIO [unused]	P0[7]	
GPIO [unused]	P2[6]	
GPIO [unused]	P2[5]	
GPIO [unused]	P2[7]	
GPIO [unused]	P1[4]	
GPIO [unused]	P1[5]	
GPIO [unused]	P2[4]	
GPIO [unused]	P2[0]	
GPIO [unused]	P4[5]	
GPIO [unused]	P2[1]	
GPIO [unused]	P2[3]	
GPIO [unused]	P2[2]	
GPIO [unused]	P3[1]	
GPIO [unused]	P3[0]	
GPIO [unused]	P3[4]	
GPIO [unused]	P3[6]	
GPIO [unused]	P3[5]	
GPIO [unused]	P5[3]	
GPIO [unused]	P1[2]	
GPIO [unused]	P1[3]	
GPIO [unused]	P1[1]	
GPIO [unused]	P5[5]	
GPIO [unused]	P1[0]	
GPIO [unused], Dedicated	P1[7]/VREF	
LED	P1[6]	Software In/Out
OVT IO [unused]	P6[4]	

Name	Port	Type
OVT IO [unused]	P6[5]	
OVT IO [unused]	P6[0]	
OVT IO [unused]	P6[1]	
OVT IO [unused]	P6[2]	
QE_A	P0[1]	Dgtl In
QE_B	P0[0]	Dgtl In

Abbreviations used in Table 5 have the following meanings:

- Dgtl Out = Digital Output
- Dgtl In = Digital Input

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
    - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Disallowed
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Chip Protection	Open

3.3 System Operating Conditions

Table 8. System Operating Conditions

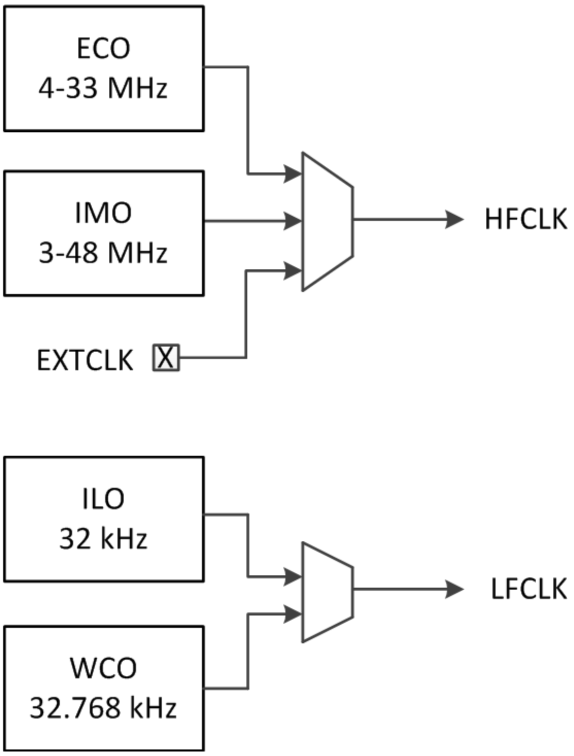
Name	Value
VDDA (V)	3.3
VDDD (V)	3.3
VDDIO (V)	3.3
Variable VDDA	True

4 Clocks

The clock system includes these clock resources:

- Two internal clock sources:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±2% at 3 MHz
  - 32 kHz Internal Low Speed Oscillator (ILO) output
- HFCLK can be generated using an external signal from EXTCLK pin
- Twenty clock dividers, each with 16-bit divide capability, 4 with fractional capability:
  - Any can be used for fixed-function blocks
  - Four can be used for the UDBs

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
DPLL_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
SysClk	NONE	HFClk	? MHz	48 MHz	±2	True	True
Direct_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
PLL1_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
PLL0_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
HFClk	NONE	Direct_Sel	48 MHz	48 MHz	±2	True	True
IMO	NONE		48 MHz	48 MHz	±2	True	True
ILO	NONE		32 kHz	32 kHz	±60	True	True
LFClk	NONE	ILO	? MHz	32 kHz	±60	True	True
RTC_Sel	NONE	None	? MHz	? MHz	±0	True	True
Timer2 (WDT2)	NONE	LFClk	? MHz	? MHz	±0	False	False
DigSig3	NONE		? MHz	? MHz	±0	False	False
ExtClk	NONE		24 MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False
DigSig4	NONE		? MHz	? MHz	±0	False	False
Timer1 (WDT1)	NONE	LFClk	? MHz	? MHz	±0	False	False
Timer0 (WDT0)	NONE	LFClk	? MHz	? MHz	±0	False	False
WCO	NONE		32.768 kHz	? MHz	±0.015	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

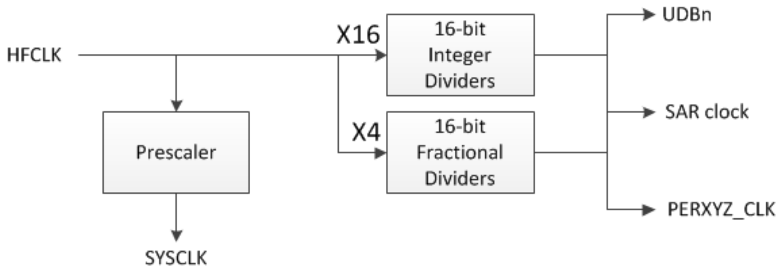


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clock_1	FIXED_-FUNCT-ION	HFClk	48 MHz	48 MHz	±2	True	True
Clock_3	DIGITAL	HFClk	1 kHz	1 kHz	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
PID_ISR	21	21	3

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 4 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x1FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 128 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- W - Full Protection

For more information on Flash memory and protection, please refer to:

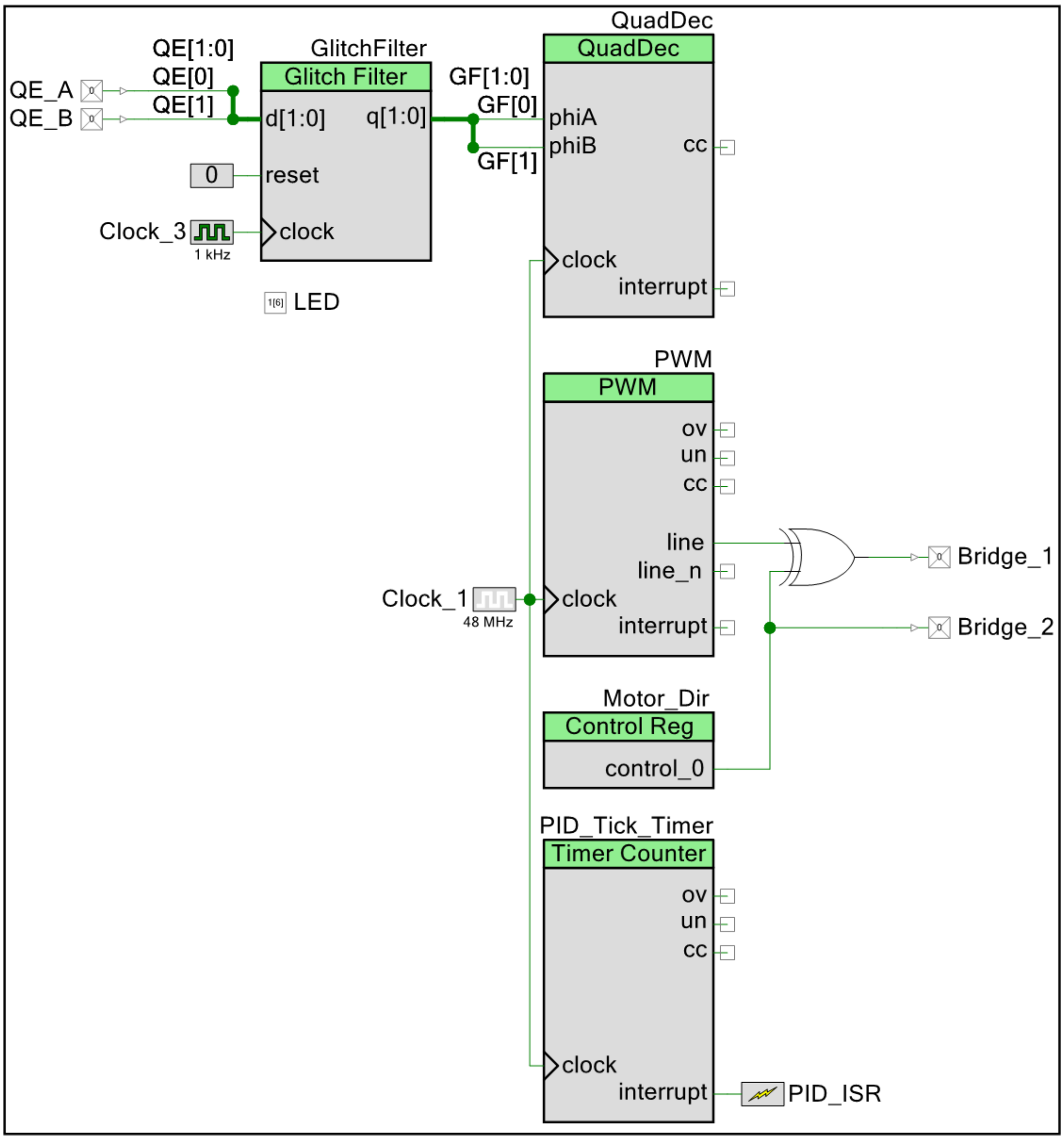
- Flash Protection chapter in the PSoC 4 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
    - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance GlitchFilter (type: GlitchFilter_v2_0)
- Instance Motor_Dir (type: CyControlReg_v1_80)
- Instance PID_Tick_Timer (type: TCPWM_P4_v2_10)
- Instance PWM (type: TCPWM_P4_v2_10)
- Instance QuadDec (type: TCPWM_P4_v2_10)

8 Components

8.1 Component type: CyControlReg [v1.80]

8.1.1 Instance Motor_Dir

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 13. Component Parameters for Motor_Dir

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.2 Component type: GlitchFilter [v2.0]

8.2.1 Instance GlitchFilter

Description: Removes unwanted pulses from a digital signal
Instance type: GlitchFilter [v2.0]
Datasheet: online component datasheet for GlitchFilter

Table 14. Component Parameters for GlitchFilter

Parameter Name	Value	Description
BypassFilter	None	Specifies the logic level to be directly propagated to the output.
GlitchLength	50	Defines the number of samples for which input has to be stable before being propagated to the output.
SignalWidth	2	Determines the bus width of d and q terminals.
User Comments		Instance-specific comments.

8.3 Component type: TCPWM_P4 [v2.10]

8.3.1 Instance PID_Tick_Timer

Description: 16-bit Timer Counter PWM (TCPWM)
Instance type: TCPWM_P4 [v2.10]
Datasheet: online component datasheet for TCPWM_P4

Table 15. Component Parameters for PID_Tick_Timer

Parameter Name	Value	Description
PWMCompare	65535	The initial value for the comparison register when in the PWM mode
PWMCompareBuf	65535	The initial value for the second comparison register when in the PWM mode
PWMCompareSwap	Disable swap	Determines whether the PWM swap check box is enabled or disabled
PWMCountMode	Level	Determines whether the PWM counter counts at level detection or in various modes of edge detection
PWMCountPresent	false	Determines if the PWM count signal is present and controls the visibility of the count pin
PWMDeadTimeCycle	0	Sets the number of cycles of dead time insertion
PWMInterruptMask	Terminal count mask	The mask used for enabling the interrupt bit in the PWM mode
PWMKillEvent	Asynchronous	Selects whether a PWM kill event is synchronous or asynchronous to the input clock
PWMLinenSignal	Direct Output	Selects whether the PWM line_n signal is inverted or is directly output
PWMLineSignal	Direct Output	Selects whether the PWM line signal is inverted or is directly output
PWMMode	PWM	Selects one of the three PWM modes - PWM, PWM with dead time insertion, or Pseudo random PWM
PWMPeriod	65535	The initial value for the period register when in the PWM mode
PWMPeriodBuf	65535	The initial value for the second period register when in the PWM mode
PWMPeriodSwap	Disable swap	Enables swap between the PWM period and period_buf registers
PWMPrescaler	0	Defines the prescaler used to divide the TCPWM clock to create the counter clock
PWMReloadMode	Rising edge	Determines whether the PWM reload signal is accepted at level detection or in various modes of edge detection
PWMReloadPresent	false	Determines whether the PWM reload signal is present and controls its pin visibility

Parameter Name	Value	Description
PWMRunMode	Continuous	Selects between continuous and one shot run mode for the PWM
PWMSetAlign	Left align	Selects the alignment of the PWM waveform to be either left, right, center or asymmetrically aligned
PWMStartMode	Rising edge	Determines whether the PWM start signal is accepted at level detection or in various modes of edge detection
PWMStartPresent	false	Determines whether the PWM start signal is present and controls its pin visibility
PWMStopEvent	Don't stop on Kill	Selects whether to kill the PWM on a stop signal or not
PWMStopMode	Rising edge	Determines whether the PWM stop signal is accepted at level detection or in various modes of edge detection
PWMStopPresent	false	Determines whether the PWM stop signal is present and controls its pin visibility
PWMSwitchMode	Rising edge	Determines whether the PWM switch signal is accepted at level detection or in various modes of edge detection
PWMSwitchPresent	false	Determines whether the PWM switch signal is present and controls its pin visibility
QuadEncodingModes	x1 Encoding mode	Selects one of the three quadrature decoder modes – x1, x2, or x4 encoding mode
QuadIndexMode	Rising edge	Determines whether the Quadrature Decoder index signal is accepted at level detection or in various modes of edge detection
QuadIndexPresent	false	Determines whether the Quadrature Decoder index signal is present and controls its pin visibility
QuadInterruptMask	Terminal count mask	The mask used to configure which Quadrature Decoder event causes an interrupt
QuadPhiAMode	Level	Determines whether the Quadrature Decoder PhiA signal is accepted at level detection or in various modes of edge detection
QuadPhiBMode	Level	Determines whether the Quadrature Decoder PhiB signal is accepted at level detection or in various modes of edge detection

Parameter Name	Value	Description
QuadStopMode	Rising edge	Determines whether the Quadrature Decoder stop signal is accepted at level detection or in various modes of edge detection
QuadStopPresent	false	Determines whether the Quadrature Decoder stop signal is present and controls its pin visibility
TCCaptureMode	Rising edge	Determines whether the Timer/Counter capture signal is accepted at level detection or in various modes of edge detection
TCCapturePresent	false	Determines whether the Timer/Counter capture signal is present and controls its pin visibility
TCCompare	65535	The initial value for the comparison register when in the Timer/Counter mode
TCCompareBuf	65535	The initial value for the second comparison register when in the Timer/Counter mode
TCCompareSwap	Disable swap	Determines whether the Timer/Counter swap check box is enabled or disabled
TCCompCapMode	Capture Mode	Selects whether the Timer/Counter capture or the compare mode is enabled
TCCountingModes	Counts up	Selects the count direction of the counter
TCCountMode	Level	Determines whether the Timer/Counter count signal is accepted at a level detect or at various modes of edge detection
TCCountPresent	false	Determines whether the Timer/Counter count signal is present and controls its pin visibility
TCInterruptMask	Terminal count mask	The mask used to determine which Timer/Counter event causes an interrupt
TCPeriod	60000	The initial value for the Timer/Counter period register
TCPrescaler	3	Selects the prescaler value to apply to the Timer/Counter clock
TCPWMCapturePresent	false	Determines whether the Unconfigured capture signal is present and controls its pin visibility
TCPWMConfig	Timer Counter	Selects the TCPWM mode - Unconfigured, Timer/Counter, PWM, or Quadrature Decoder

Parameter Name	Value	Description
TCPWMCountPresent	false	Determines whether the Unconfigured count signal is present and controls its pin visibility
TCPWMReloadPresent	false	Determines whether the Unconfigured reload signal is present and controls its pin visibility
TCPWMStartPresent	false	Determines whether the Unconfigured start signal is present and controls its pin visibility
TCPWMStopPresent	false	Determines whether the Unconfigured stop signal is present and controls its pin visibility
TCReloadMode	Rising edge	Determines whether the Timer/Counter reload signal is accepted at level detection or in various modes of edge detection
TCReloadPresent	false	Determines whether the Timer/Counter reload signal is present and controls its pin visibility
TCRunMode	Continuous	Selects whether the counter runs continuously or one shot
TCStartMode	Rising edge	Determines whether the start signal is accepted at level detection or in various modes of edge detection
TCStartPresent	false	Determines whether the Timer/Counter start signal is present and controls its pin visibility
TCStopMode	Rising edge	Determines whether the Timer/Counter stop signal is accepted at level detection or in various modes of edge detection
TCStopPresent	false	Determines whether the Timer/Counter stop signal is present and controls its pin visibility
User Comments		Instance-specific comments.

8.3.2 Instance PWM

Description: 16-bit Timer Counter PWM (TCPWM)
Instance type: TCPWM_P4 [v2.10]
Datasheet: online component datasheet for TCPWM_P4

Table 16. Component Parameters for PWM

Parameter Name	Value	Description
PWMCompare	32768	The initial value for the comparison register when in the PWM mode

Parameter Name	Value	Description
PWMCompareBuf	65535	The initial value for the second comparison register when in the PWM mode
PWMCompareSwap	Disable swap	Determines whether the PWM swap check box is enabled or disabled
PWMCountMode	Level	Determines whether the PWM counter counts at level detection or in various modes of edge detection
PWMCountPresent	false	Determines if the PWM count signal is present and controls the visibility of the count pin
PWMDeadTimeCycle	0	Sets the number of cycles of dead time insertion
PWMInterruptMask	None	The mask used for enabling the interrupt bit in the PWM mode
PWMKillEvent	Asynchronous	Selects whether a PWM kill event is synchronous or asynchronous to the input clock
PWMLinenSignal	Direct Output	Selects whether the PWM line_n signal is inverted or is directly output
PWMLineSignal	Direct Output	Selects whether the PWM line signal is inverted or is directly output
PWMMode	PWM	Selects one of the three PWM modes - PWM, PWM with dead time insertion, or Pseudo random PWM
PWMPeriod	65535	The initial value for the period register when in the PWM mode
PWMPeriodBuf	65535	The initial value for the second period register when in the PWM mode
PWMPeriodSwap	Disable swap	Enables swap between the PWM period and period_buf registers
PWMPrescaler	0	Defines the prescaler used to divide the TCPWM clock to create the counter clock
PWMReloadMode	Rising edge	Determines whether the PWM reload signal is accepted at level detection or in various modes of edge detection
PWMReloadPresent	false	Determines whether the PWM reload signal is present and controls its pin visibility
PWMRunMode	Continuous	Selects between continuous and one shot run mode for the PWM
PWMSetAlign	Left align	Selects the alignment of the PWM waveform to be either left, right, center or asymmetrically aligned

Parameter Name	Value	Description
PWMStartMode	Rising edge	Determines whether the PWM start signal is accepted at level detection or in various modes of edge detection
PWMStartPresent	false	Determines whether the PWM start signal is present and controls its pin visibility
PWMStopEvent	Don't stop on Kill	Selects whether to kill the PWM on a stop signal or not
PWMStopMode	Rising edge	Determines whether the PWM stop signal is accepted at level detection or in various modes of edge detection
PWMStopPresent	false	Determines whether the PWM stop signal is present and controls its pin visibility
PWMSwitchMode	Rising edge	Determines whether the PWM switch signal is accepted at level detection or in various modes of edge detection
PWMSwitchPresent	false	Determines whether the PWM switch signal is present and controls its pin visibility
QuadEncodingModes	x1 Encoding mode	Selects one of the three quadrature decoder modes – x1, x2, or x4 encoding mode
QuadIndexMode	Rising edge	Determines whether the Quadrature Decoder index signal is accepted at level detection or in various modes of edge detection
QuadIndexPresent	false	Determines whether the Quadrature Decoder index signal is present and controls its pin visibility
QuadInterruptMask	Terminal count mask	The mask used to configure which Quadrature Decoder event causes an interrupt
QuadPhiAMode	Level	Determines whether the Quadrature Decoder PhiA signal is accepted at level detection or in various modes of edge detection
QuadPhiBMode	Level	Determines whether the Quadrature Decoder PhiB signal is accepted at level detection or in various modes of edge detection
QuadStopMode	Rising edge	Determines whether the Quadrature Decoder stop signal is accepted at level detection or in various modes of edge detection
QuadStopPresent	false	Determines whether the Quadrature Decoder stop signal is present and controls its pin visibility

Parameter Name	Value	Description
TCCaptureMode	Rising edge	Determines whether the Timer/Counter capture signal is accepted at level detection or in various modes of edge detection
TCCapturePresent	false	Determines whether the Timer/Counter capture signal is present and controls its pin visibility
TCCompare	65535	The initial value for the comparison register when in the Timer/Counter mode
TCCompareBuf	65535	The initial value for the second comparison register when in the Timer/Counter mode
TCCompareSwap	Disable swap	Determines whether the Timer/Counter swap check box is enabled or disabled
TCCompCapMode	Capture Mode	Selects whether the Timer/Counter capture or the compare mode is enabled
TCCountingModes	Counts up	Selects the count direction of the counter
TCCountMode	Level	Determines whether the Timer/Counter count signal is accepted at a level detect or at various modes of edge detection
TCCountPresent	false	Determines whether the Timer/Counter count signal is present and controls its pin visibility
TCInterruptMask	Terminal count mask	The mask used to determine which Timer/Counter event causes an interrupt
TCPeriod	65535	The initial value for the Timer/Counter period register
TCPrescaler	0	Selects the prescaler value to apply to the Timer/Counter clock
TCPWMCapturePresent	false	Determines whether the Unconfigured capture signal is present and controls its pin visibility
TCPWMConfig	PWM	Selects the TCPWM mode - Unconfigured, Timer/Counter, PWM, or Quadrature Decoder
TCPWMCountPresent	false	Determines whether the Unconfigured count signal is present and controls its pin visibility
TCPWMReloadPresent	false	Determines whether the Unconfigured reload signal is present and controls its pin visibility

Parameter Name	Value	Description
TCPWMStartPresent	false	Determines whether the Unconfigured start signal is present and controls its pin visibility
TCPWMStopPresent	false	Determines whether the Unconfigured stop signal is present and controls its pin visibility
TCReloadMode	Rising edge	Determines whether the Timer/Counter reload signal is accepted at level detection or in various modes of edge detection
TCReloadPresent	false	Determines whether the Timer/Counter reload signal is present and controls its pin visibility
TCRunMode	Continuous	Selects whether the counter runs continuously or one shot
TCStartMode	Rising edge	Determines whether the start signal is accepted at level detection or in various modes of edge detection
TCStartPresent	false	Determines whether the Timer/Counter start signal is present and controls its pin visibility
TCStopMode	Rising edge	Determines whether the Timer/Counter stop signal is accepted at level detection or in various modes of edge detection
TCStopPresent	false	Determines whether the Timer/Counter stop signal is present and controls its pin visibility
User Comments		Instance-specific comments.

8.3.3 Instance QuadDec

Description: 16-bit Timer Counter PWM (TCPWM)
Instance type: TCPWM_P4 [v2.10]
Datasheet: online component datasheet for TCPWM_P4

Table 17. Component Parameters for QuadDec

Parameter Name	Value	Description
PWMCompare	65535	The initial value for the comparison register when in the PWM mode
PWMCompareBuf	65535	The initial value for the second comparison register when in the PWM mode
PWMCompareSwap	Disable swap	Determines whether the PWM swap check box is enabled or disabled

Parameter Name	Value	Description
PWMCountMode	Level	Determines whether the PWM counter counts at level detection or in various modes of edge detection
PWMCountPresent	false	Determines if the PWM count signal is present and controls the visibility of the count pin
PWMDeadTimeCycle	0	Sets the number of cycles of dead time insertion
PWMInterruptMask	Terminal count mask	The mask used for enabling the interrupt bit in the PWM mode
PWMKillEvent	Asynchronous	Selects whether a PWM kill event is synchronous or asynchronous to the input clock
PWMLinenSignal	Direct Output	Selects whether the PWM line_n signal is inverted or is directly output
PWMLineSignal	Direct Output	Selects whether the PWM line signal is inverted or is directly output
PWMMode	PWM	Selects one of the three PWM modes - PWM, PWM with dead time insertion, or Pseudo random PWM
PWMPeriod	65535	The initial value for the period register when in the PWM mode
PWMPeriodBuf	65535	The initial value for the second period register when in the PWM mode
PWMPeriodSwap	Disable swap	Enables swap between the PWM period and period_buf registers
PWMPrescaler	0	Defines the prescaler used to divide the TCPWM clock to create the counter clock
PWMReloadMode	Rising edge	Determines whether the PWM reload signal is accepted at level detection or in various modes of edge detection
PWMReloadPresent	false	Determines whether the PWM reload signal is present and controls its pin visibility
PWMRunMode	Continuous	Selects between continuous and one shot run mode for the PWM
PWMSetAlign	Left align	Selects the alignment of the PWM waveform to be either left, right, center or asymmetrically aligned
PWMStartMode	Rising edge	Determines whether the PWM start signal is accepted at level detection or in various modes of edge detection
PWMStartPresent	false	Determines whether the PWM start signal is present and controls its pin visibility
PWMStopEvent	Don't stop on Kill	Selects whether to kill the PWM on a stop signal or not

Parameter Name	Value	Description
PWMStopMode	Rising edge	Determines whether the PWM stop signal is accepted at level detection or in various modes of edge detection
PWMStopPresent	false	Determines whether the PWM stop signal is present and controls its pin visibility
PWMSwitchMode	Rising edge	Determines whether the PWM switch signal is accepted at level detection or in various modes of edge detection
PWMSwitchPresent	false	Determines whether the PWM switch signal is present and controls its pin visibility
QuadEncodingModes	x1 Encoding mode	Selects one of the three quadrature decoder modes – x1, x2, or x4 encoding mode
QuadIndexMode	Rising edge	Determines whether the Quadrature Decoder index signal is accepted at level detection or in various modes of edge detection
QuadIndexPresent	false	Determines whether the Quadrature Decoder index signal is present and controls its pin visibility
QuadInterruptMask	None	The mask used to configure which Quadrature Decoder event causes an interrupt
QuadPhiAMode	Level	Determines whether the Quadrature Decoder PhiA signal is accepted at level detection or in various modes of edge detection
QuadPhiBMode	Level	Determines whether the Quadrature Decoder PhiB signal is accepted at level detection or in various modes of edge detection
QuadStopMode	Rising edge	Determines whether the Quadrature Decoder stop signal is accepted at level detection or in various modes of edge detection
QuadStopPresent	false	Determines whether the Quadrature Decoder stop signal is present and controls its pin visibility
TCCaptureMode	Rising edge	Determines whether the Timer/Counter capture signal is accepted at level detection or in various modes of edge detection
TCCapturePresent	false	Determines whether the Timer/Counter capture signal is present and controls its pin visibility

Parameter Name	Value	Description
TCCompare	65535	The initial value for the comparison register when in the Timer/Counter mode
TCCompareBuf	65535	The initial value for the second comparison register when in the Timer/Counter mode
TCCompareSwap	Disable swap	Determines whether the Timer/Counter swap check box is enabled or disabled
TCCompCapMode	Capture Mode	Selects whether the Timer/Counter capture or the compare mode is enabled
TCCountingModes	Counts up	Selects the count direction of the counter
TCCountMode	Level	Determines whether the Timer/Counter count signal is accepted at a level detect or at various modes of edge detection
TCCountPresent	false	Determines whether the Timer/Counter count signal is present and controls its pin visibility
TCInterruptMask	Terminal count mask	The mask used to determine which Timer/Counter event causes an interrupt
TCPeriod	65535	The initial value for the Timer/Counter period register
TCPrescaler	0	Selects the prescaler value to apply to the Timer/Counter clock
TCPWMCapturePresent	false	Determines whether the Unconfigured capture signal is present and controls its pin visibility
TCPWMConfig	QuadDec	Selects the TCPWM mode - Unconfigured, Timer/Counter, PWM, or Quadrature Decoder
TCPWMCountPresent	false	Determines whether the Unconfigured count signal is present and controls its pin visibility
TCPWMReloadPresent	false	Determines whether the Unconfigured reload signal is present and controls its pin visibility
TCPWMStartPresent	false	Determines whether the Unconfigured start signal is present and controls its pin visibility
TCPWMStopPresent	false	Determines whether the Unconfigured stop signal is present and controls its pin visibility

Parameter Name	Value	Description
TCReloadMode	Rising edge	Determines whether the Timer/Counter reload signal is accepted at level detection or in various modes of edge detection
TCReloadPresent	false	Determines whether the Timer/Counter reload signal is present and controls its pin visibility
TCRunMode	Continuous	Selects whether the counter runs continuously or one shot
TCStartMode	Rising edge	Determines whether the start signal is accepted at level detection or in various modes of edge detection
TCStartPresent	false	Determines whether the Timer/Counter start signal is present and controls its pin visibility
TCStopMode	Rising edge	Determines whether the Timer/Counter stop signal is accepted at level detection or in various modes of edge detection
TCStopPresent	false	Determines whether the Timer/Counter stop signal is present and controls its pin visibility
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 4 register map is covered in the PSoC 4 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 4 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 4 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines