

CSE 1204

Digital Logic Design Laboratory



**Project Title: Digital Clock design
implementation skipping a specific value in
Logisim.**

Submitted by

Afifa Sultana(2107087)

H.M.AZROF(2107088)

Submitted to

1.MD.Shakhawat Hossain

Lecturer,

Department of CSE,KUET

2.Dipannita Biswas

Lecturer,

Department of CSE,KUET

DIGITAL CLOCK IMPLEMENTATION PROJECT:

Objectives:

1. To know about implementation of a digital clock properly .
2. To make a digital clock where a particular second is skipped in seconds and minutes.
3. To know about the basics of digital electronics where different components are required.
4. To know the overall idea about the asynchronous counter and flipflops.
5. To use the D flipflop and making the equations required.
6. To get equations using karnaugh map.
7. To use the seven segments display in the clock.
8. To design the skipped digital clock in the logisim perfectly.

Introduction:

In this project ,we create basic asynchronous counter with D flip flop.

And also use 7 segment display to show the digit.

D Flip Flop:

A D flip-flop is a type of digital circuit that stores a single bit of data. It has two inputs: a data input (D) and a clock input (CLK). When the clock input transitions from low to high, the value of the data input is transferred to the output of the flip-flop. The output will hold this value until the next clock transition. In other words, the D flip-flop acts as a "delayed" version of the data input, where the delay is determined by the clock signal. This makes it useful for synchronizing signals in digital systems.

Asynchronous Counter:

An asynchronous counter, also known as ripple counter, is a type of digital counter circuit where the flip-flops that make up the counter are not all clocked by the same clock signal. Instead, each flip-flop is clocked by the output of the previous flip-flop in the sequence.

In an asynchronous counter, the output of the first flip-flop serves as the clock input for the second flip-flop, the output of the second flip-flop serves as the clock input for the third flip-flop, and so on. This cascading effect creates a sequence of binary counts.

The advantage of an asynchronous counter is that it can be easily constructed using individual flip-flops and simple logic gates. However, it has a limitation in terms of speed since each flip-flop has to wait for the previous flip-flop to change its state before it can change its own state.

Asynchronous counters are commonly used in simple applications where speed is not critical, or when the counter needs to be reset to a specific count value.

7 segment Display:

A 7-segment display is a type of electronic display device that is commonly used to represent numerical digits. It consists of seven individual LED (light-emitting diode) or LCD (liquid crystal display) segments that are arranged in the shape of a rectangular figure "8". Each segment is labeled with a letter A through G, and an optional decimal point (DP) can be added to represent fractions or other symbols.

Components Required:

1.IC 7404

2.IC 7400

3.IC 7432

4.IC 7436

5.IC 7474

6.7 segment display

7.wire

8.LED

Design and Implementation of mod 10 counter:

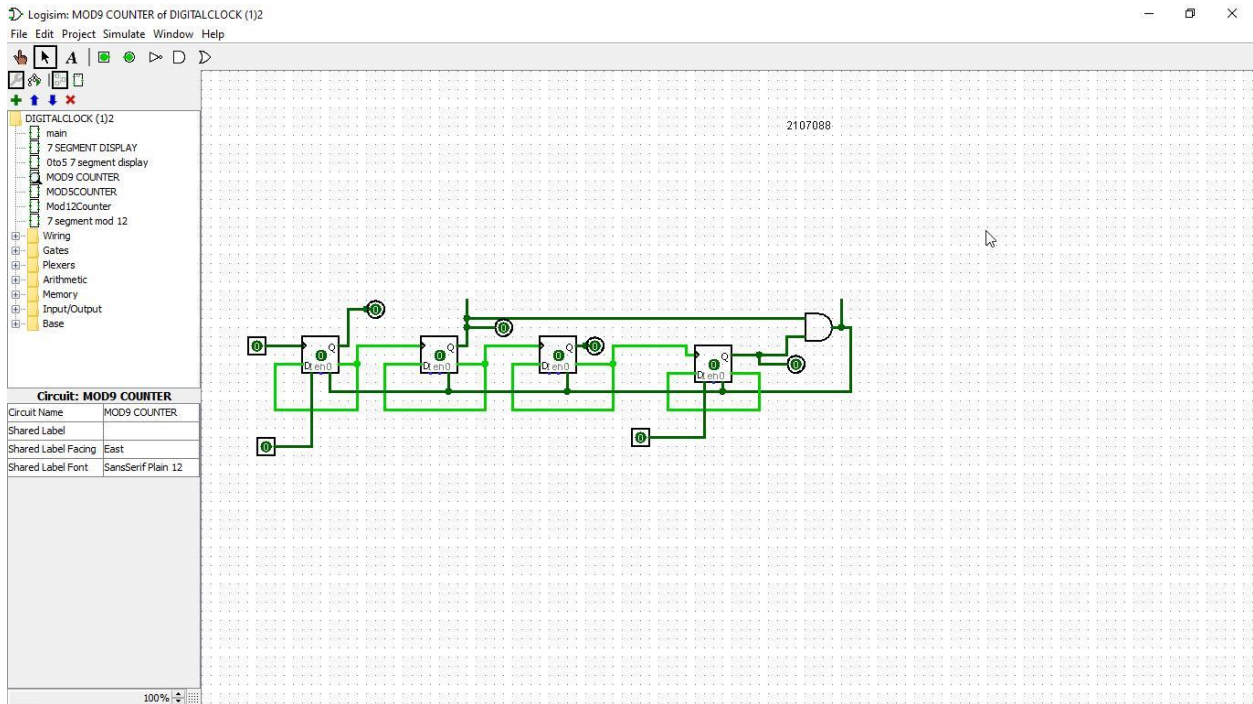
One's Unit Display:

1. **Modulo-10 Counter:** A modulo-9 counter is constructed using D flip-flops. This counter ensures that the seconds are represented within the range of 0 to 9 in . The counter's final output is taken as the basis for the one's unit display.

Truth table to reset after 9:

Decimal	Q3	Q2	Q1	Q0	R
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1

8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11-15					x



KMAP for Reset after 9:

Q1Q0 Q3Q2	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	x	x	x	x
10	1	1	x	0

$F(\text{RESET}) = Q3' + Q1'$ (When clear is active in 0)

F(RESET)=Q3Q1(When clear is active in 1)'

2. **Conversion to IC:** To maintain organization and modularity, the modulo-10 counter is converted into an integrated circuit (IC) module.
3. **Seven-Segment Logic:** The next step involves defining the Boolean expressions for the seven segments (A, B, C, D, E, F, G) for each digit from 1 to . These expressions are derived based on the output values of the modulo-10 counter.
4. **Truth Table for mod 7 segment:**

Creating a truth table for a 7-segment display logic can be a bit complex due to the number of segments (A, B, C, D, E, F, G) and the combinations required to display different decimal digits (0-9).

Digit	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1
10-15	x	x	x	x	x	x	x

K-map for mod 10:

For A:

cd ab	00	01	11	10
00	1		1	1
01		1	1	1
11	x	x	x	x
10	1	1	x	x

$$A = a + c + b'd' + bd$$

For B:

cd ab	00	01	11	10
00	1	1	1	1
01	1		1	
11	x	x	x	x
10	1	1	x	x

$$B = cd + b' + c'd'$$

For C:

cd ab	00	01	11	10
00	1	1	1	
01	1	1	1	1
11	x	x	X	x
10	1	1	X	x

$$C = b + c' + d$$

FOR D:

cd ab	00	01	11	10
00	1		1	1
01		1		1
11	x	x	x	x
10	1	1	x	x

$$D = a + cd' + b'c + b'd' + bc'd$$

For E:

Cd ab	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	x	x	x	x
10	1	0	X	X

$$E = b'd' + cd'$$

For F:

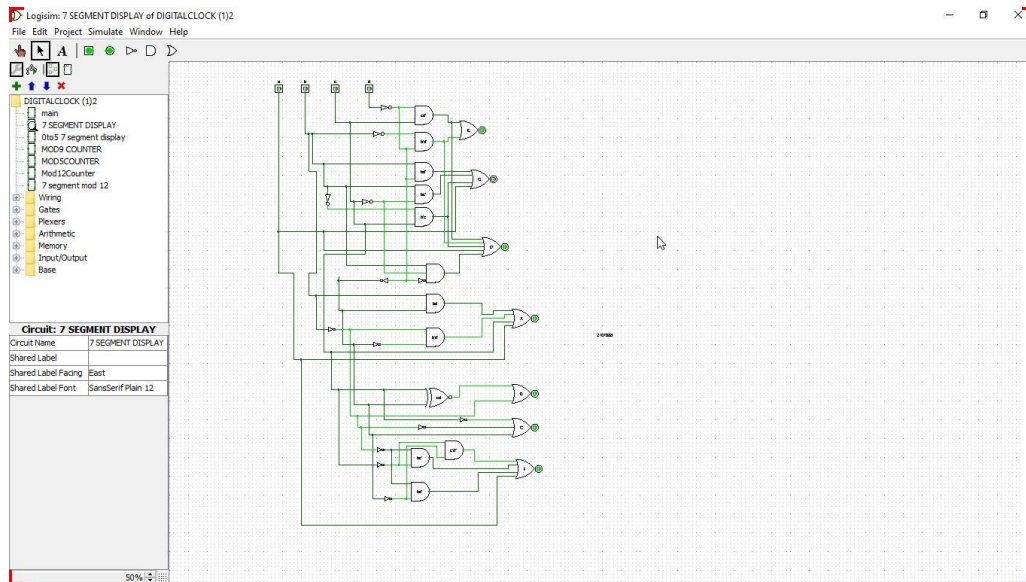
cd ab	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	x	x	x	x
10	1	1	X	X

$$F = a + c'd' + bc' + bd'$$

For G:

cd ab	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	x	x	x	x
10	1	1	x	x

$$G = a + bd' + bc' + b'c$$



5. **Seven-Segment Display IC:** The seven-segment display logic is encapsulated into another IC module to simplify the main circuit.

6. **Integration:** The one's unit seven-segment display IC is connected to the main circuit, and its outputs are mapped to the respective pins of the 7-segment display.

Design and Implementation of mod 5 counter:

One's Unit Display:

1. **Modulo-5 Counter:** A modulo-5 counter is constructed using D flip-flops. This counter ensures that the seconds and minutes are represented within the range of 0 to 5. The counter's final output is taken as the basis for the one's unit display.

Truth table to reset after 5:

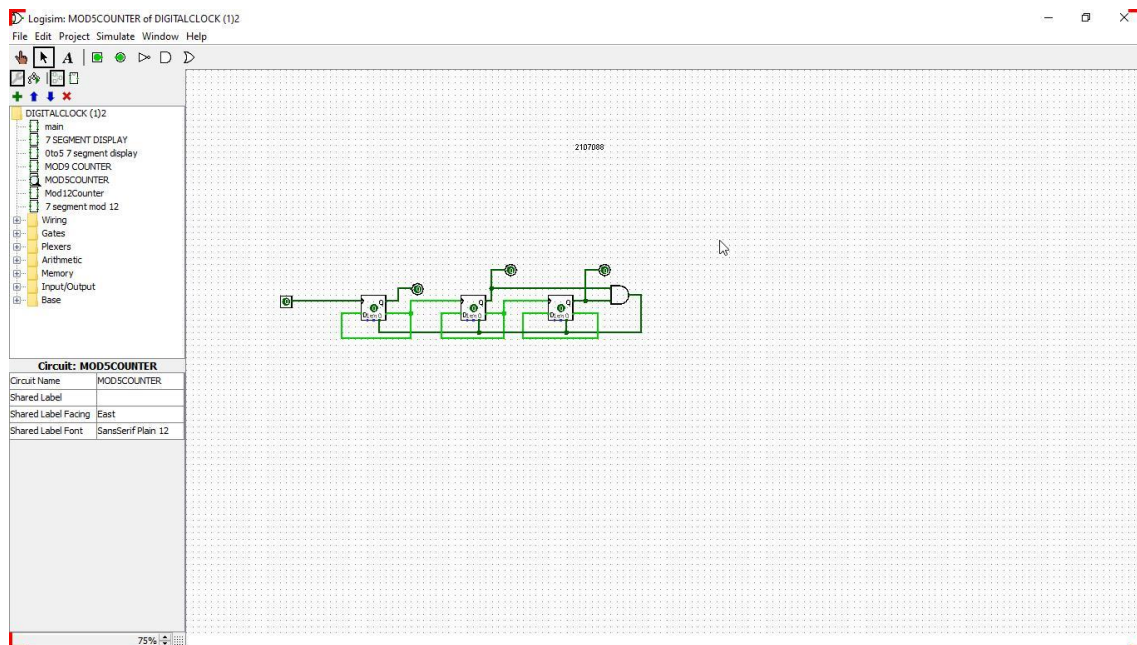
Decimal	Q3	Q2	Q1	Q0	R
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	0
7					x

KMAP for Reset after 5:

Q2Q1 Q3	00	01	11	10
0	1	1	1	1
1	1	1	X	0

$F(\text{RESET}) = Q3' + Q2'$ (When clear is active in 0)

$F(\text{RESET}) = Q3Q2$ (When clear is active in 1)'



2. **Conversion to IC:** To maintain organization and modularity, the modulo-5 counter is converted into an integrated circuit (IC) module.
3. **Seven-Segment Logic:** The next step involves defining the Boolean expressions for the seven segments (A, B, C, D, E, F, G) for each digit from 1 to . These expressions are derived based on the output values of the modulo-5 counter.
4. **Truth Table for mod 7 segment:**

Creating a truth table for a 7-segment display logic can be a bit complex due to the number of segments (A, B, C, D, E, F, G) and the combinations required to display different decimal digits (0-5).

Digit	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6-15	x	x	x	x	x	x	x

K-map for mod 7 Segment:

For A:

cd ab	00	01	11	10
00	1		1	1
01		1	X	X
11	x	x	x	x
10	X	X	x	x

$$A = b'd' + bd + c$$

For B:

cd ab	00	01	11	10
00	1	1	1	1
01	1		X	X
11	x	x	x	x
10	X	X	x	x

$$B = cd + c'd' + b'$$

For C:

cd ab	00	01	11	10
00	1	1	1	
01	1	1	X	X
11	x	x	x	x
10	X	X	x	x

$$C = c' + d$$

FOR D:

cd ab	00	01	11	10
00	1		1	1
01		1	X	X
11	x	x	x	x
10	X	X	x	x

$$D = b'c'd' + cd + bd$$

FOR E:

Cd ab	00	01	11	10
00	1			1
01			X	X
11	x	x	x	x
10	X	X	X	X

$$E = b'd'$$

For F:

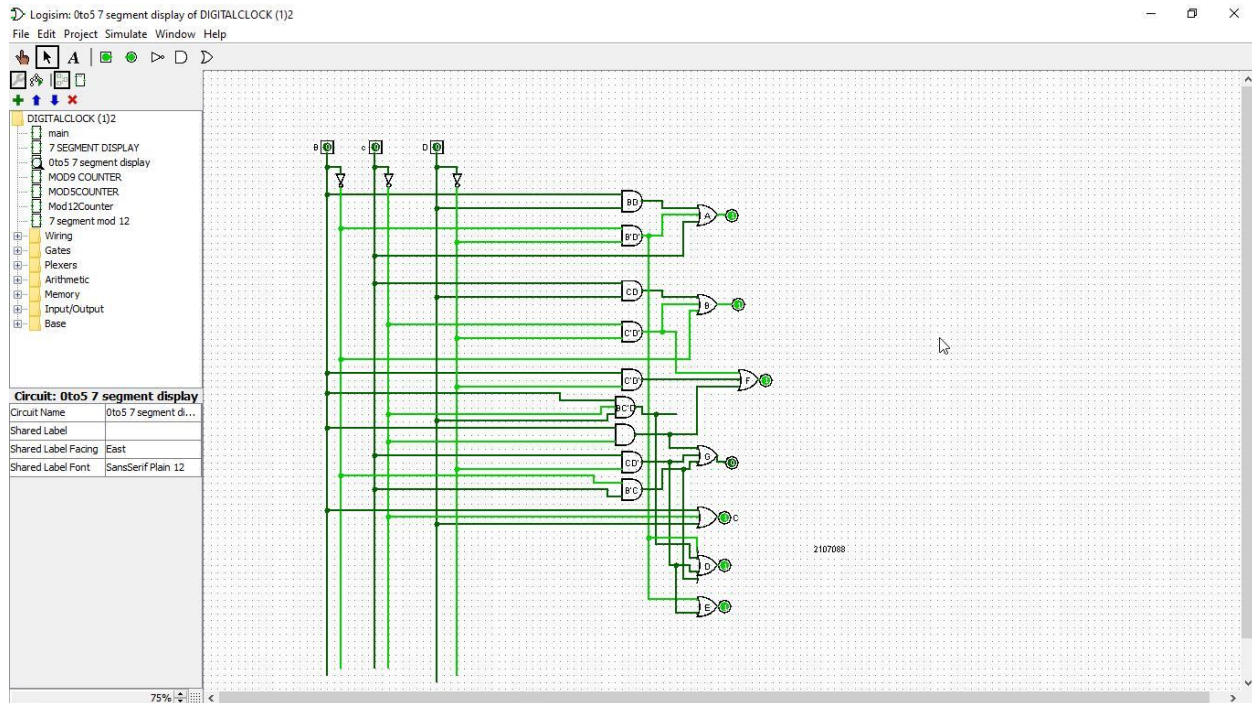
cd ab	00	01	11	10
00			1	1
01	1	1	X	X
11	x	x	x	x
10	X	X	x	x

$$F = c'd' + b$$

For G:

cd ab	00	01	11	10
00	1			
01	1	1	X	X
11	x	x	x	x
10	X	X	X	X

$$G = b + c$$



Seven-Segment Display IC: The seven-segment display logic is encapsulated into another IC module to simplify the main circuit.

5. **Integration:** The one's unit seven-segment display IC is connected to the main circuit, and its outputs are mapped to the respective pins of the 7-segment display.

To skip 28th second and minute:

In MOD 10 counter when 8 will come that means when 1000 appear and at the mean time when in MOD 5 counter 2 that means 010 will come then the MOD 10 counter will skip the 28th second. For this we should connect the output of the logic in the PRESET of MOD 10 counter which represents the LSB and MSB bit of the counter. Same thing have to be done in minutes skipping.

Design and Implementation of MOD 12 Counter:

One's Unit Display:

1. **Modulo-12 Counter:** The project begins by constructing a modulo-12 counter using D flip-flops. This counter ensures that the hours are represented within the range of 1 to 12 in a 12-hour format. The counter's final output is taken as the basis for the one's unit display.

Truth table:

Decimal	Q3	Q2	Q1	Q0	R
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13-15					x

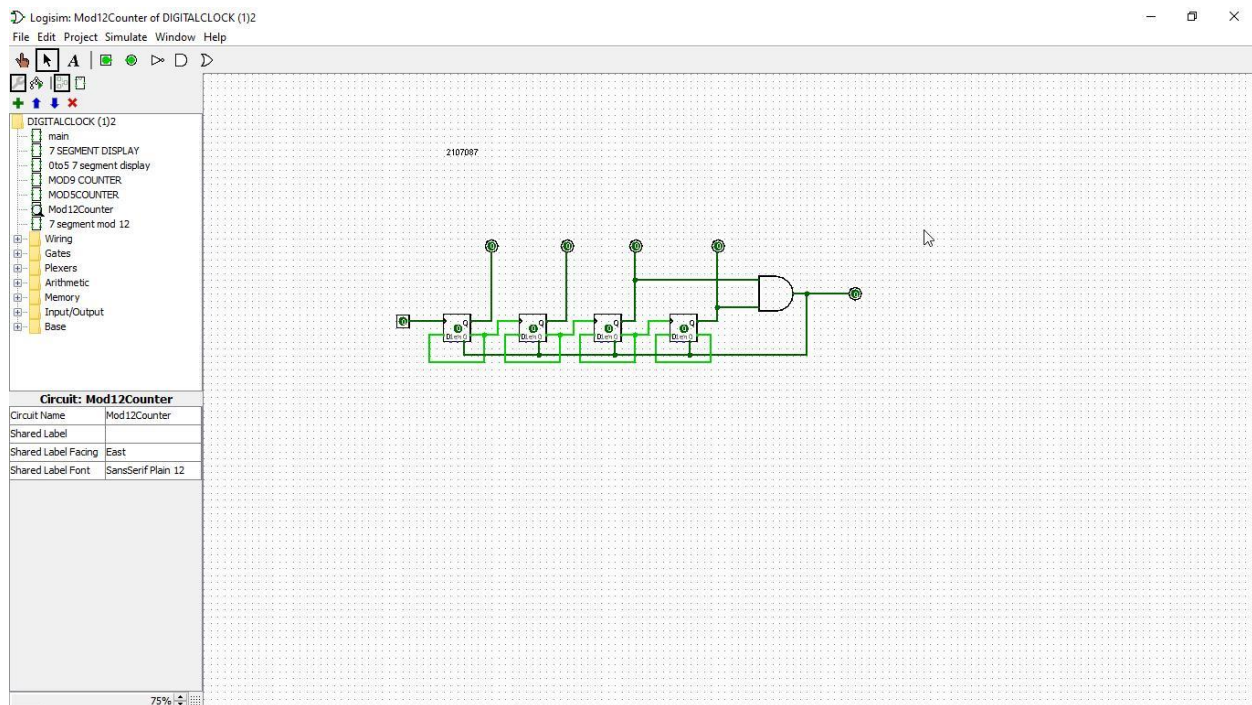
KMAP to reset after 11:

:

cd ab	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	x	x	x
10	1	1	1	1

$F(\text{RESET}) = a' + b'$ (When clear is active in 0)

$F(\text{RESET})' = ab$ (When clear is active in 1)



2. **Conversion to IC:** To maintain organization and modularity, the modulo-12 counter is converted into an integrated circuit (IC) module.

3. **Seven-Segment Logic:** The next step involves defining the Boolean expressions for the seven segments (A, B, C, D, E, F, G) for each digit from 1 to 12. These expressions are derived based on the output values of the modulo-12 counter.

4. **Truth Table for 7 segment:**

Creating a truth table for a 7-segment display logic can be a bit complex due to the number of segments (A, B, C, D, E, F, G) and the combinations required to display different decimal digits (0-9 or 1-12 in the case of a 12-hour clock).

Digit	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1
10	1	1	1	1	1	1	0
11	0	1	1	0	0	0	0
12-15	x	X	x	x	x	x	x

K-map for 7 segment:

For A:

cd ab	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	x	x	x	x
10	1	1	0	1

$$A = b'd' + a'c + ac' + bd$$

For B:

cd ab	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	x	x	x	x
10	1	1	1	1

$$B = c'd' + cd + b'$$

For C:

cd ab	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	x	x	x	x
10	1	1	1	1

$$C = a + b + c' + d$$

For D:

cd ab	00	01	11	10
00	1	0	1	0
01	1	1	0	1
11	x	x	x	x
10	1	1	0	1

$$D = b'd' + ac' + cd' + a'b'c + bc'd$$

For E:

cd ab	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	x	x	x	x
10	1	0	0	1

$$E = b'd' + cd'$$

For F:

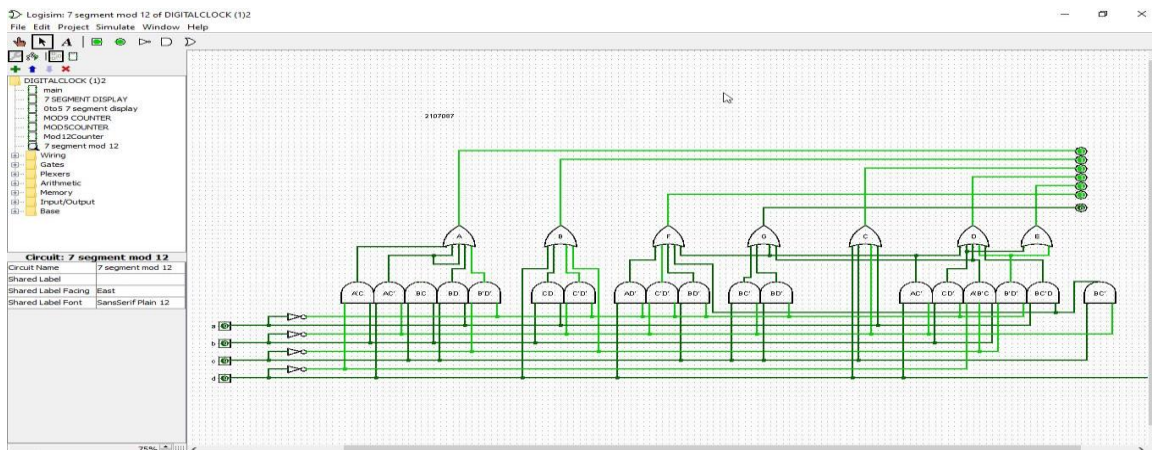
cd ab	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	x	x	x	x
10	1	1	0	1

$$F = c'd' + bc' + ac' + bd' + ad$$

For G:

cd ab	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	x	x	x	x
10	1	1	0	0

$$G = bd' + bc' + ac' + a'b'c$$



5. Seven-Segment Display IC: The seven-segment display logic is encapsulated into another IC module to simplify the main circuit.

6.Integration: The one's unit seven-segment display IC is connected to the main circuit, and its outputs are mapped to the respective pins of the 7-segment display.

Ten's Unit Display:

1. **Modulo-12 Counter:** Similar to the one's unit, a modulo-12 counter is implemented to represent the ten's unit. This counter ensures that the ten's unit advances only after twelve one's unit cycles.
2. **D Flip-Flop:** The final output of the modulo-12 counter for the ten's unit is connected to a D flip-flop, allowing the representation of the tens digit.
3. **Integration:** The ten's unit output is integrated into the main circuit and connected to the appropriate pins on the 7-segment display.

Simulation:

The designed circuit is simulated using Logisim, where the modulo-12 counters, 7-segment display logic, and their integration are tested. The simulation ensures that the hour display functions correctly and transitions between the one's and ten's units as expected, following the 12-hour format.

Discussion:

To create a digital clock in Logisim, we need to use a few basic components such as the clock generator, counter, and 7 segment display. Here are the steps followed to create a digital clock in Logisim: First, we created a clock generator module that generates clock pulses at a specific frequency. Next, we created a counter module that counts the number of clock pulses generated by the clock generator. We used a binary counter

for this purpose. We built this counter with using D flipflip. For this project we created mod-10, mod-5, mod-12 counter, mod-2 counter. We created a display module that displays the current time in hours, minutes, and seconds. For this, we used seven-segment displays. Once we have created these modules, we connected them together. We connected the output of the clock generator to the input of the counter and the output of the counter to the input of the display. We can adjust the frequency of the clock generator to see how it affects the time displayed on the seven-segment displays. In this project, we skipped the 28th second and 28th minute by creating a logic. In mod-10 counter when 8 will arrive and in mod-5 counter when 2 will arrive then the counter will skip the 28th second. And same for skipping 28th minute. For second count, At first the mod-10 counter is supplied by a clock pulse, and the mod-5 counter will receive clock pulse when mod-10 counter will count 8. For minute count, when the mod-5 counter will appear to 6 then a clock pulse will go to the mod-10 counter of minute section. And the mod-5 counter of minute will receive pulse when the mod-10 counter will arrive in 10.

At last mod-12 counter will receive clock pulse when the mod-5 counter of minute arrive 6. The mod-2 counter will receive clock pulse when the mod-10 counter will arrive at 12. The mod-12 and mod-2 counter both will reset at the same time when mod-12 counter will arrive at 12.

Conclusion:

In conclusion, the project of creating a digital clock with skip functionality using asynchronous counters, D flip-flops, and custom logic circuits in Logisim is a challenging and rewarding endeavor. It embodies the essence of digital electronics, from understanding fundamental concepts to applying advanced logic design techniques.

This project empowers individuals with valuable skills in digital logic design, problem-solving, and simulation. It underscores the importance of clear documentation and the significance of hands-on learning experiences in the field of electronics.

As we conclude this journey, it's essential to recognize that this project is a stepping stone to further exploration and innovation in the world of digital electronics. Whether for educational purposes, personal enrichment, or practical applications, the knowledge and skills gained from this project can open doors to countless possibilities in the ever-evolving field of digital technology.