Address Operation Statements

Comment

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/ Read an ARC instruction from main memory
   0: R[ir] ← AND(R[pc],R[pc]); READ;
                                              / 256-way jump according to opcode
   1: DECODE;
      / sethi
1152: R[rd] ← LSHIFT10(ir); GOTO 2047;
                                             / Copy imm22 field to target register
      / call
1280: R[15] ← AND(R[pc],R[pc]);
                                              / Save %pc in %r15
1281: R[temp0] \leftarrow ADD(R[ir],R[ir]);
                                              / Shift disp30 field left
1282: R[temp0] ← ADD(R[temp0], R[temp0]); / Shift again
1283: R[pc] \leftarrow ADD(R[pc], R[temp0]);
                                              / Jump to subroutine
      GOTO 0;
       / addcc
1600: IF R[IR[13]] THEN GOTO 1602;
                                              / Is second source operand immediate?
                                              / Perform ADDCC on register sources
1601: R[rd] ← ADDCC(R[rs1],R[rs2]);
      GOTO 2047;
1602: R[temp0] ← SEXT13(R[ir]);
                                              / Get sign extended simm13 field
1603: R[rd] ← ADDCC(R[rs1],R[temp0]);
                                              / Perform ADDCC on register/simm13
      GOTO 2047;
                                              / sources
      / andcc
1604: IF R[IR[13]] THEN GOTO 1606;
                                              / Is second source operand immediate?
                                              / Perform ANDCC on register sources
1605: R[rd] ← ANDCC(R[rs1], R[rs2]);
      GOTO 2047;
1606: R[temp0] ← SIMM13(R[ir]);
                                              / Get simm13 field
                                              / Perform ANDCC on register/simm13
1607: R[rd] ← ANDCC(R[rs1], R[temp0]);
      GOTO 2047;
                                              / sources
      / orcc
1608: IF R[IR[13]] THEN GOTO 1610;
                                             / Is second source operand immediate?
1609: R[rd] \leftarrow ORCC(R[rs1], R[rs2]);
                                              / Perform ORCC on register sources
      GOTO 2047;
1610: R[temp0] ← SIMM13(R[ir]);
                                             / Get_simm13 field
                                             / Perform ORCC on register/simm13 sources
1611: R[rd] ← ORCC(R[rs1],R[temp0]);
      GOTO 2047;
       / orncc
1624: IF R[IR[13]] THEN GOTO 1626;
                                              / Is second source operand immediate?
                                              / Perform ORNCC on register sources
1625: R[rd] ← NORCC(R[rs1], R[rs2]);
      GOTO 2047;
                                              / Get simm13 field
1626: R[temp0] ← SIMM13(R[ir]);
1627: R[rd] \leftarrow NORCC(R[rs1], R[temp0]);
                                              / Perform NORCC on register/simm13
      GOTO 2047;
                                              / sources
      / srl
1688: IF R[IR[13]] THEN GOTO 1690;
                                              / Is second source operand immediate?
1689: R[rd] \leftarrow SRL(R[rs1],R[rs2]);
                                              / Perform SRL on register sources
      GOTO 2047;
1690: R[temp0] ← SIMM13(R[ir]);
                                              / Get_simm13 field
                                              / Perform SRL on register/simm13 sources
1691: R[rd] ← SRL(R[rs1],R[temp0]);
      GOTO 2047;
      / jmpl
                                             / Is second source operand immediate?
1760: IF R[IR[13]] THEN GOTO 1762;
1761: R[pc] ← ADD(R[rs1],R[rs2]);
                                              / Perform ADD on register sources
      GOTO 0;
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