Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment # 3: Parity Bit Checker and Generator

Objective:

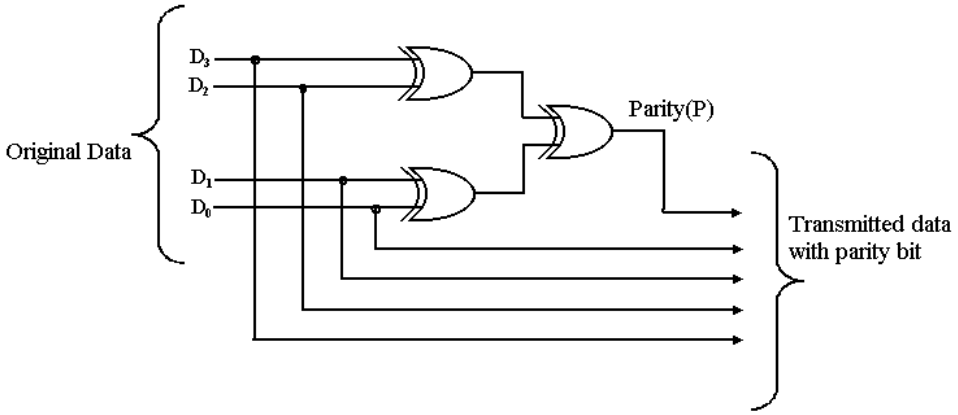
- To design and implement an even parity Generator and even parity checker using XOR gates. (IC-7486).

Required Components:

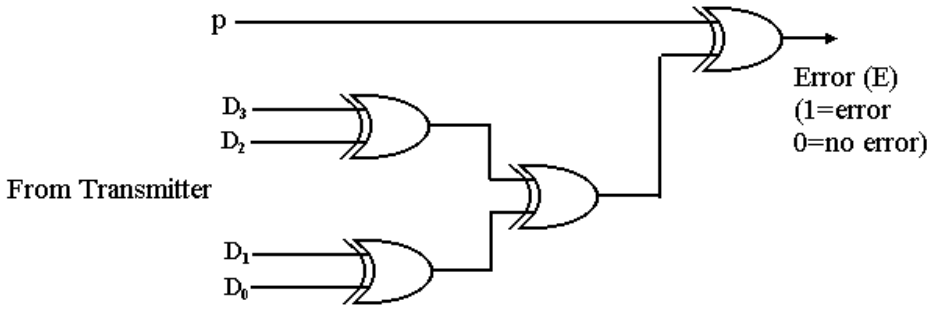
1. IC 7486 × 1

Diagrams:

Building an even parity generator using XOR Gates for 4-bit Data:



Building an even parity checker using XOR Gates for 4-bit Data:



Procedure:

- Construct the Circuits of both the parity bit generator and checker on the breadboard.
- Remember that each IC's pin 14 is connected to the "+5V" position of the DC Power Supply of AT-700, and pin 7 is connected to the "GND" position.
- Connect the inputs to the Data switches and outputs to any position of the LED Display.

Report:

Your report must have the following segments:

1. Name of the Experiment.
2. Objective.
3. Required Components.
4. Experimental Setup - Draw the Circuit Diagrams of the Parity bit checker and generator.
5. Results - Complete both of the following truth tables.

Truth Table for Parity Bit Generator:

	Data				Parity
	D_3	D_2	D_1	D_0	
a.	1	0	0	1	
b.	0	0	0	1	
c.	1	1	1	1	
d.	0	0	0	0	

Truth Table for Parity Bit Checker:

	Data					Error
	Parity	D_3	D_2	D_1	D_0	
a.	1	1	0	0	1	
b.	0	0	0	0	1	
c.	0	1	1	1	1	
d.	1	0	0	0	0	

6. Discussions -
   (a) Draw the circuit diagrams of 3-bit parity checker and generator using NOR gate(s) only
   (b) Draw the circuit diagrams of 5-bit parity checker and generator using NAND gate(s) only.