

CSE-260

Lab Report -1

Group - 04

Nafiz Shahriar Sami - 23201336

Eusha Kayenat - 23201303

Afnan Mohammad Hafiz - 23241004

Afifa Aman Elham - 23201043

Experiment #1: familiarization with fundamental Logic Gates.

Required Components for Experiment - 1:

1. IC 7408 x1
2. IC 7432 x1
3. IC 7404 x1
4. IC 7400 x1
5. IC 7402 x1
6. IC 7486 x1
7. IC 4077 x1
8. Bread board
9. Jumper wires

TOPIC NAME: _____

DAY: _____
TIME: _____ DATE: / /

NOT [pin layout 7404]

AND

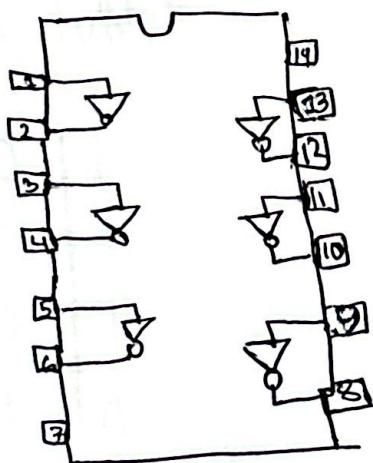
Truth Table

0	1
1	0

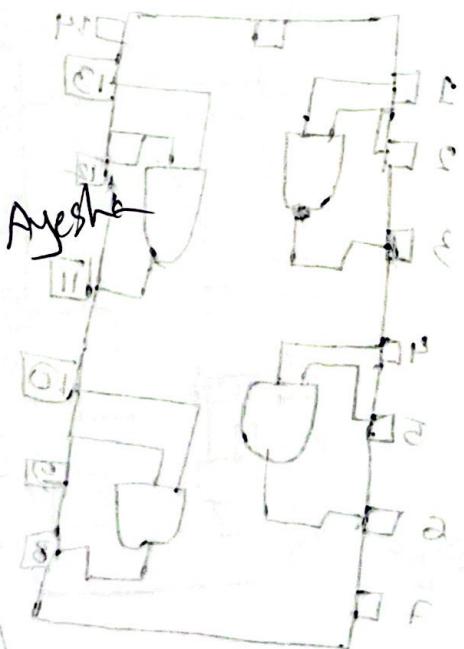
Output of NOT

0	0	0
0	0	1
0	1	0
1	1	1

Diagram



Board



GOOD LUCK

DAY: _____

TIME: _____

DATE: _____

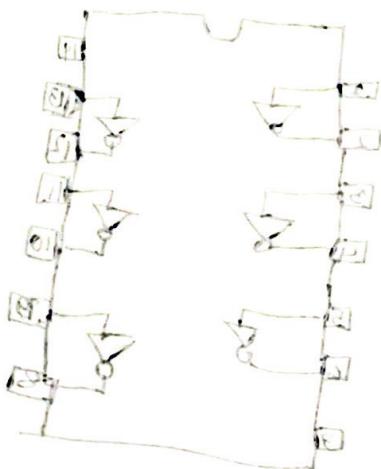
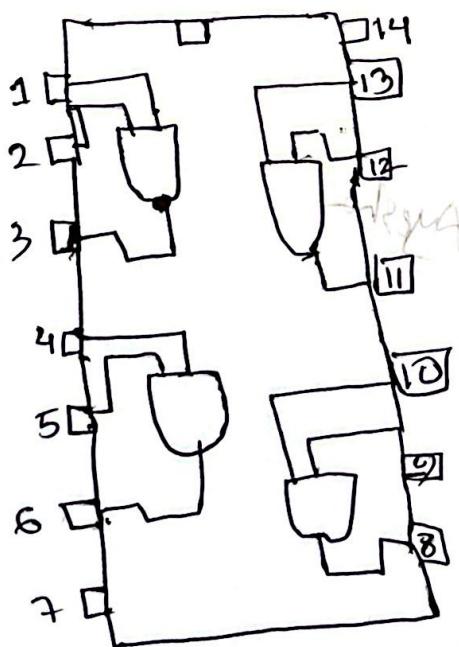
TOPIC NAME: _____

AND

Truth table

0	0	0
1	0	0
0	1	0
1	1	1

Diagram



GOOD LUCK™

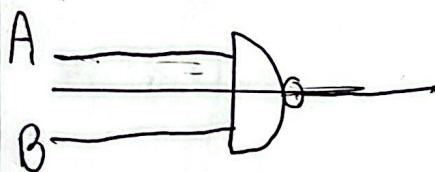
TOPIC NAME : _____

DAY : _____

TIME : _____

DATE : / /

NAND \rightarrow (AND + NOT) [Pin layout 7400]



$\overline{A \cdot B}$

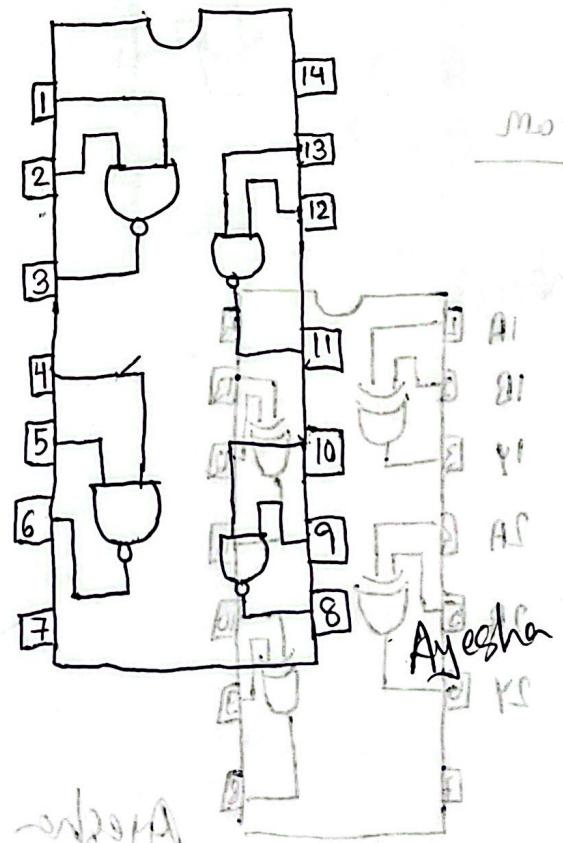
[Diagram]

Truth Table:

0	0	1
0	1	1
1	0	1
1	1	0

Diagram:

0	0	0
1	1	0
1	0	1
0	1	1



GOOD LUCK™

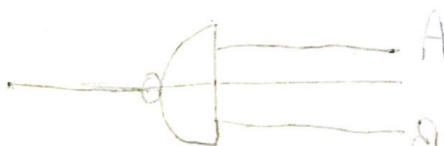
TOPIC NAME : _____ DAY : _____
TIME : _____ DATE : _____

XOR [Pin layout in 7486] (TON + QNA) ← AVIAN

Truth Table

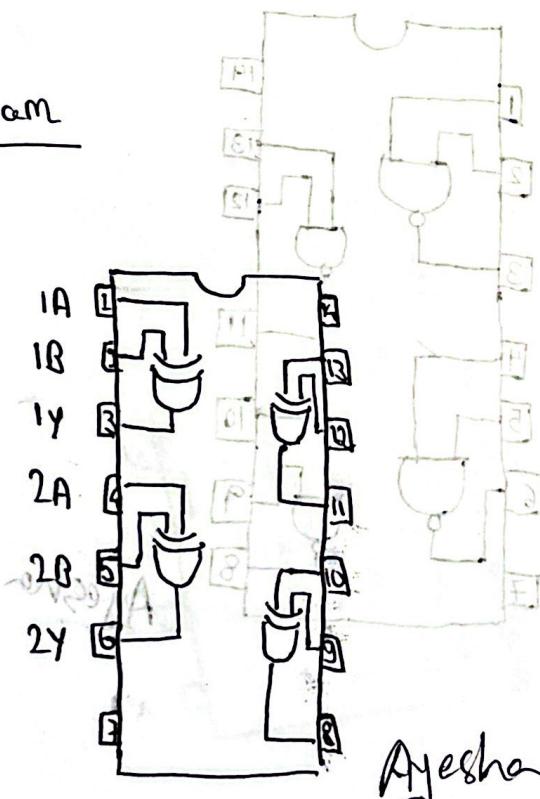
		[monjoi]
0	0	0
0	1	1
1	0	1
1	1	0

\overline{QA}



oldot short

Diagram



1	0	0
1	1	0
1	0	1
0	1	1

GOOD LUCK™

GOOD LUCK

TOPIC NAME : YAO

DAY : _____
TIME : _____
DATE : / /

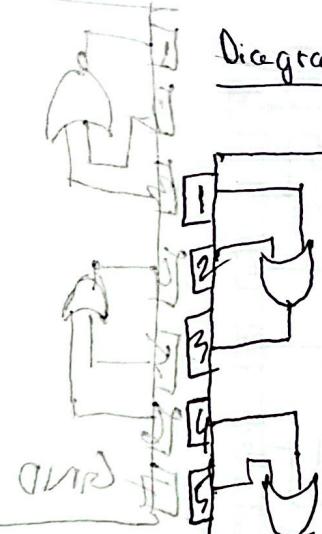
OR

SOP

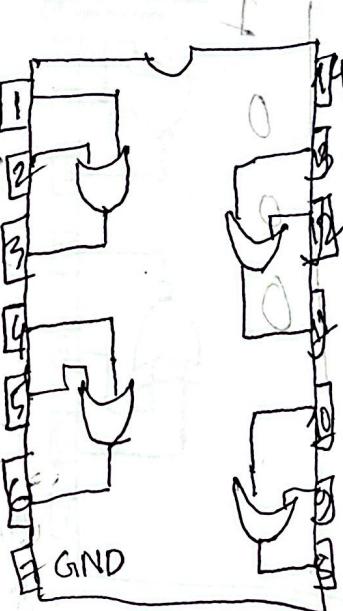
Truth Table

0	0	0	0
1	0	1	1
0	1	0	1
1	1	1	1

Ans 2nd



Ans 1st



Ans 1st

GOOD LUCK™

GOOD LUCK

TOPIC NAME: _____

DAY: _____
TIME: _____ DATE: _____

NOR

Truth table

0 0

1 0

0 1

1 1

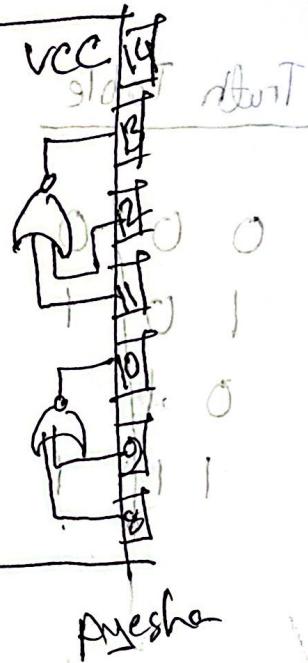
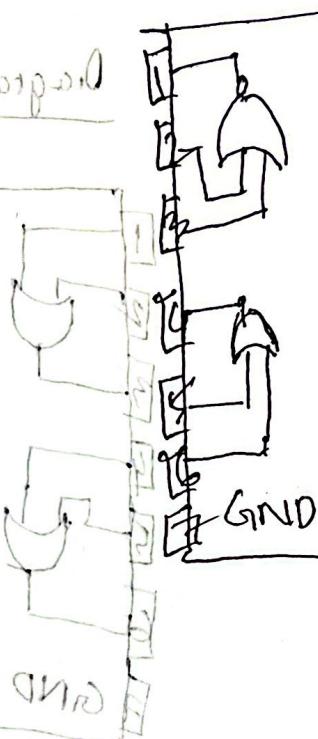
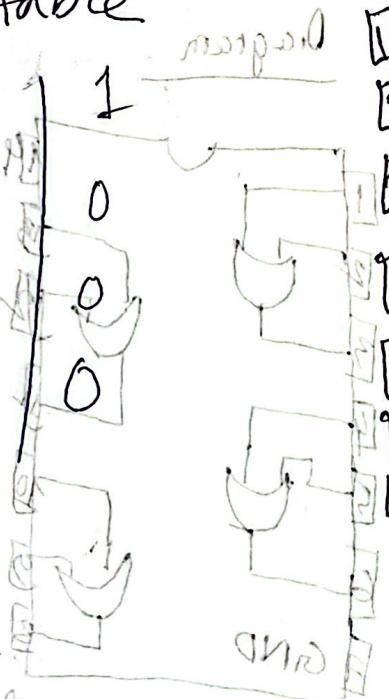
1

0

0

0

enbuff



GOOD LUCK

TOPIC NAME : _____

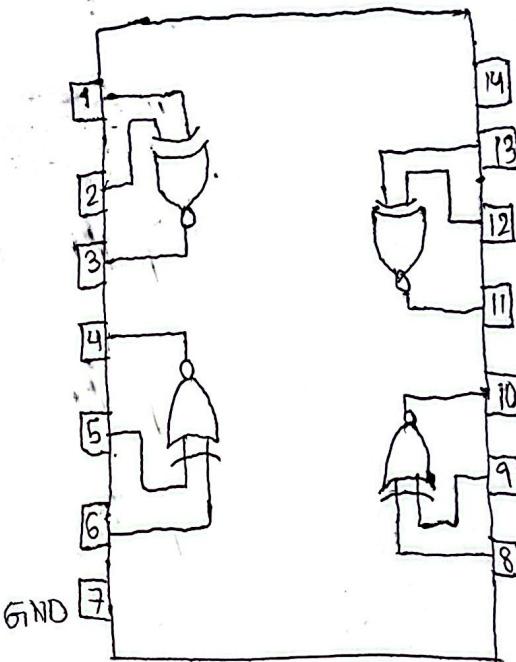
DAY : _____

TIME : _____ / /

X-NOR : (4077)

Truth Table

0	0	1
1	0	0
0	1	0
1	1	1



Ayesh

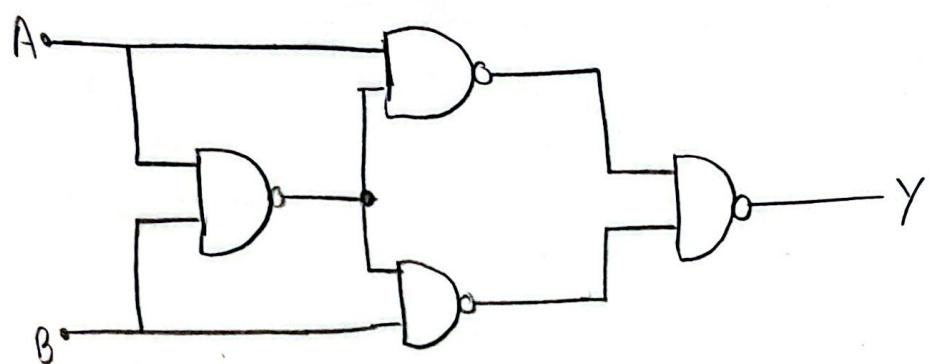
GOOD LUCK™

Experiment #2: Universal Gates, Application of Boolean Algebra.

Required Components:

1. IC 7400X1
2. IC 7402 X2
3. Bread board
4. Jumper wires

Circuit Diagram - 01

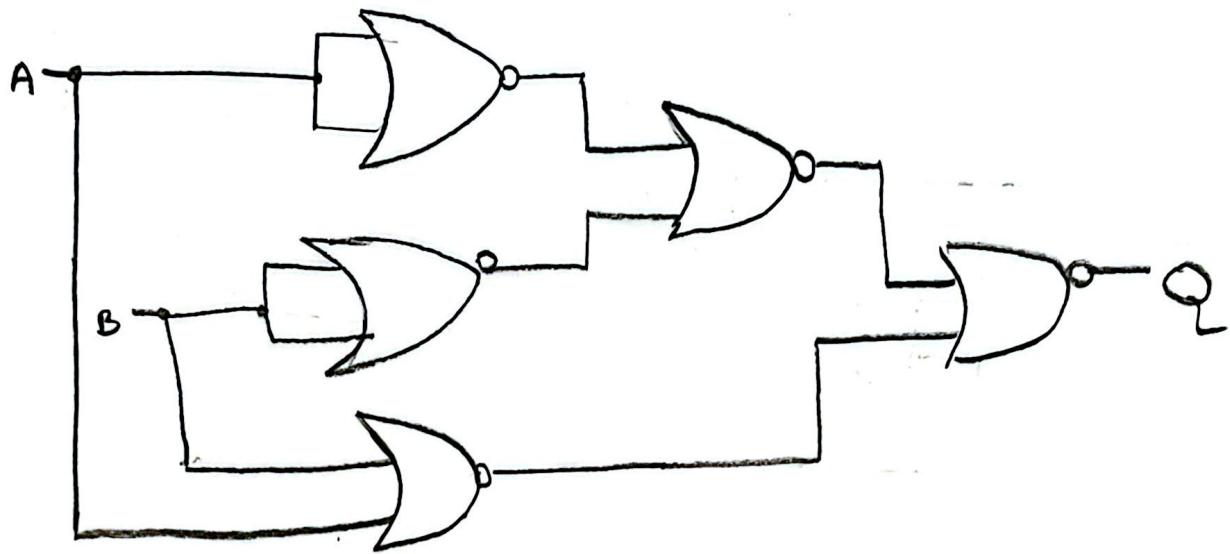


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Ayush

26.10.25

Circuit Diagram - 02



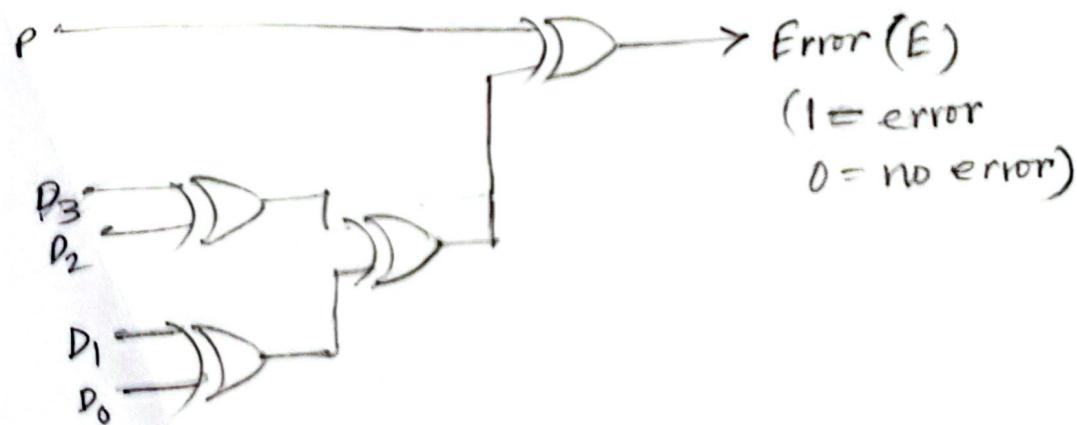
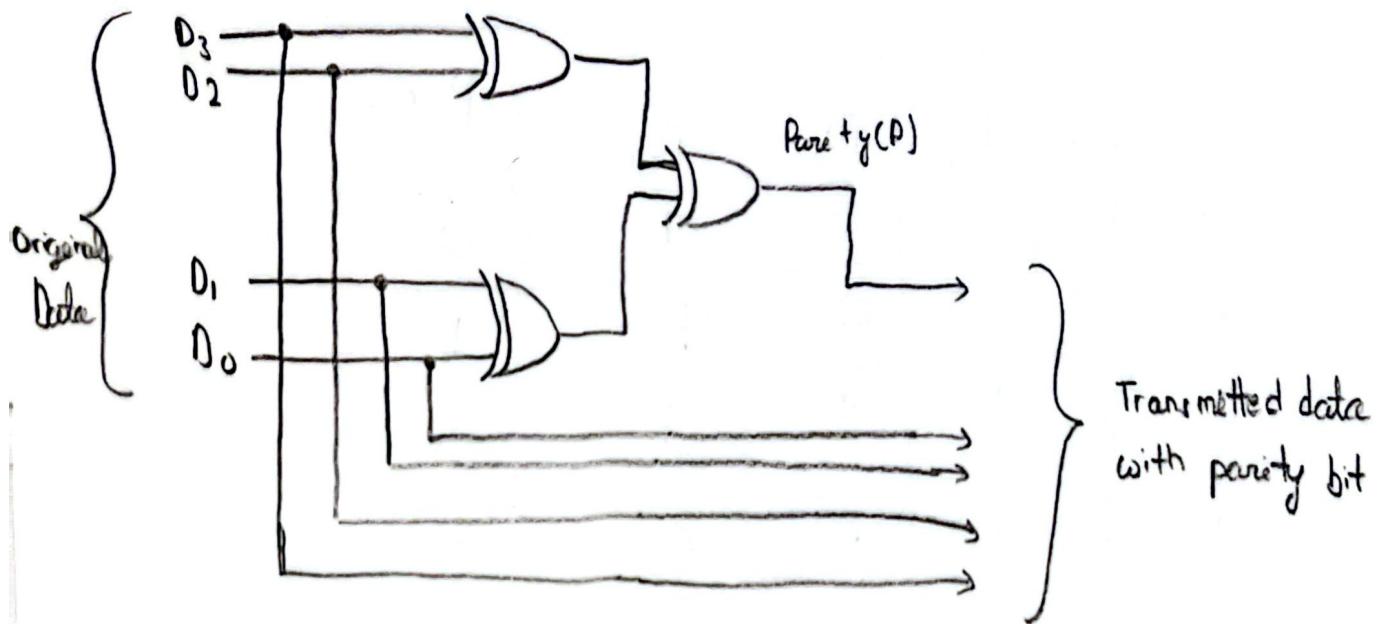
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Ayeshan
26.10.25

Experiment #3: Parity Bit Checker and Generator.

Required components:

1. IC 7486 x1



	Data				Parity
	D ₃	D ₂	D ₁	D ₀	
a	1	0	0	1	0
b	0	0	0	1	1
c	1	1	1	1	0
d	0	0	0	0	0

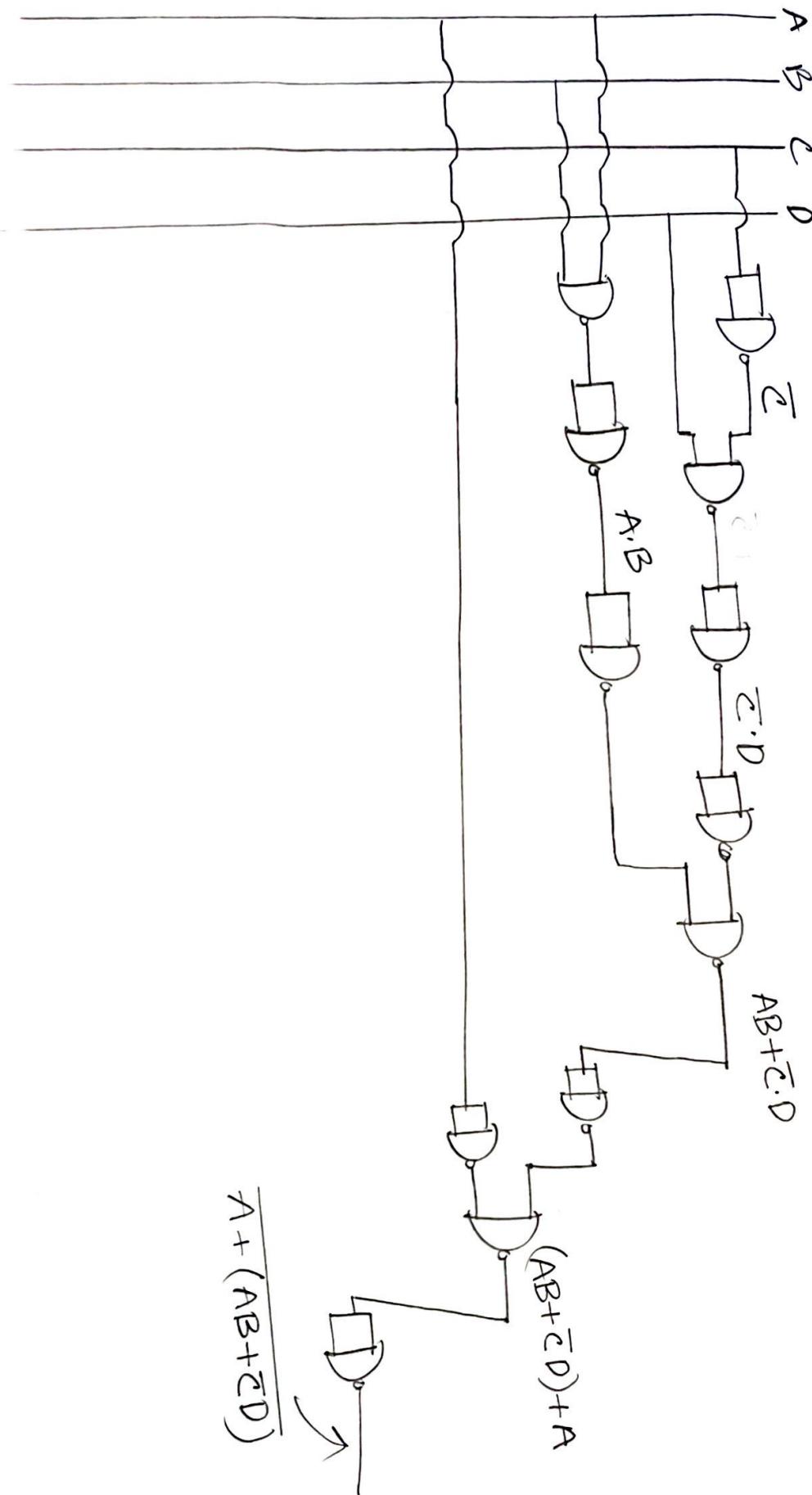
Ans

	Data					Error
	Parity	D ₃	D ₂	D ₁	D ₀	
a	1	1	0	0	1	1
b	0	0	0	0	1	1
c	0	1	1	1	1	0
d	1	0	0	0	0	1

0 → No error
1 → Error

Ans. to the ques. no. 1

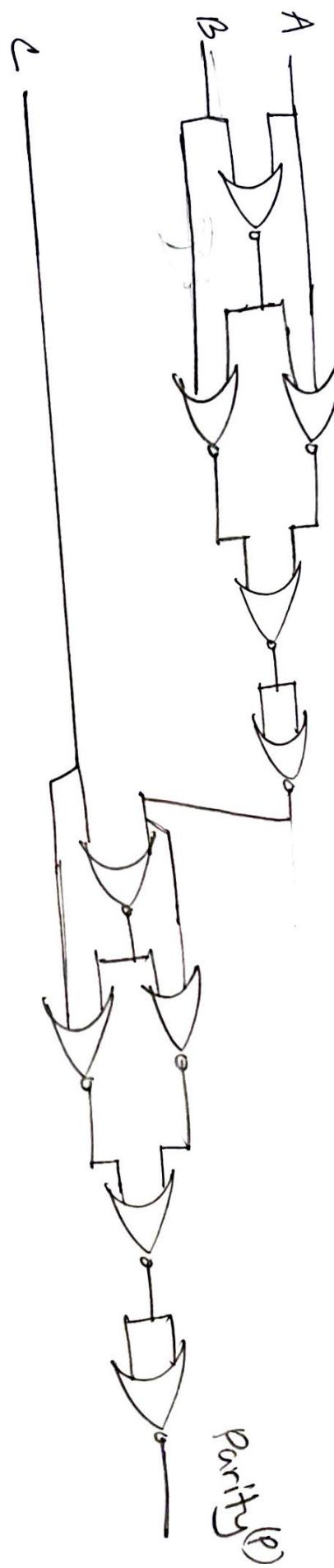
$\overline{(A + (AB + \overline{CD}))}$ using only NAND gate



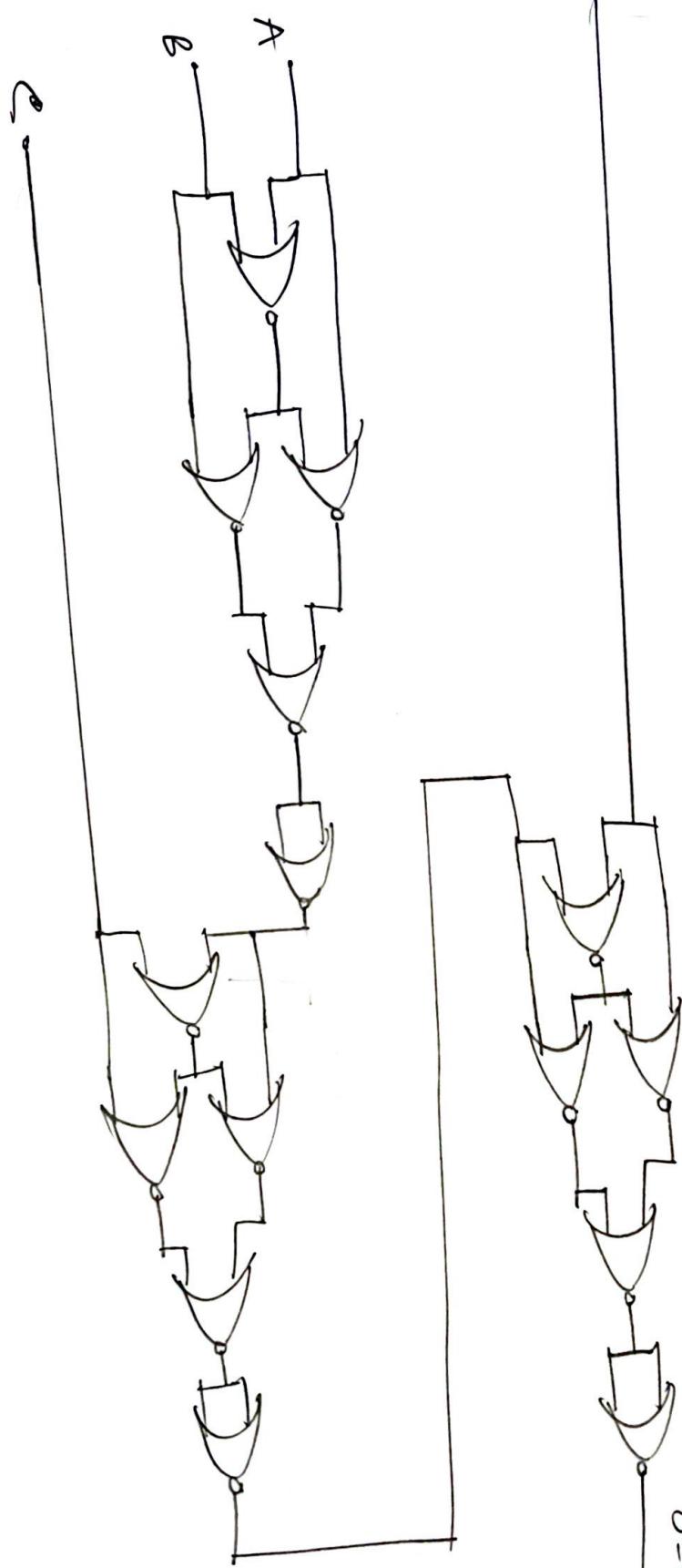
Ans. to the ques. no. 2

Generator:

using only NOR gates



Checker:



Error (E)
(1 = error,
0 = no error)