

CSE-260

Lab Report-02

Group-04

Nafiz Shahriar Sami (23201336)

Eusha Kayenat (23201303)

Afnan Mohammad Hafiz (23201004)

Afifa Aman Elham (23201043)

089-123

## Experiment #4: Design and Implementation of 4-bit Parallel Binary Adder

Required Components of for Lab-4:

1. IC 7408
2. IC 7432
3. IC 7486
4. IC 7483

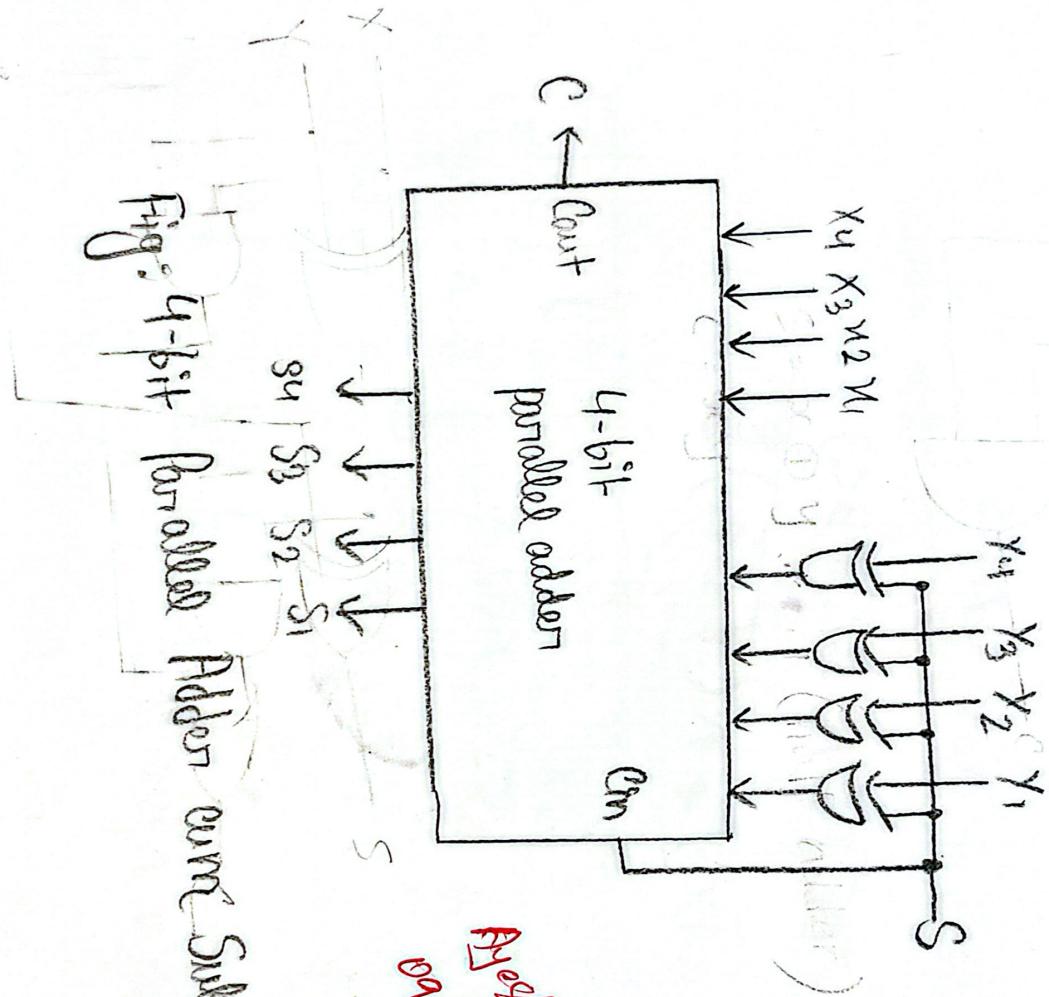


Fig: 4-bit parallel Adder ohne Subtraktor

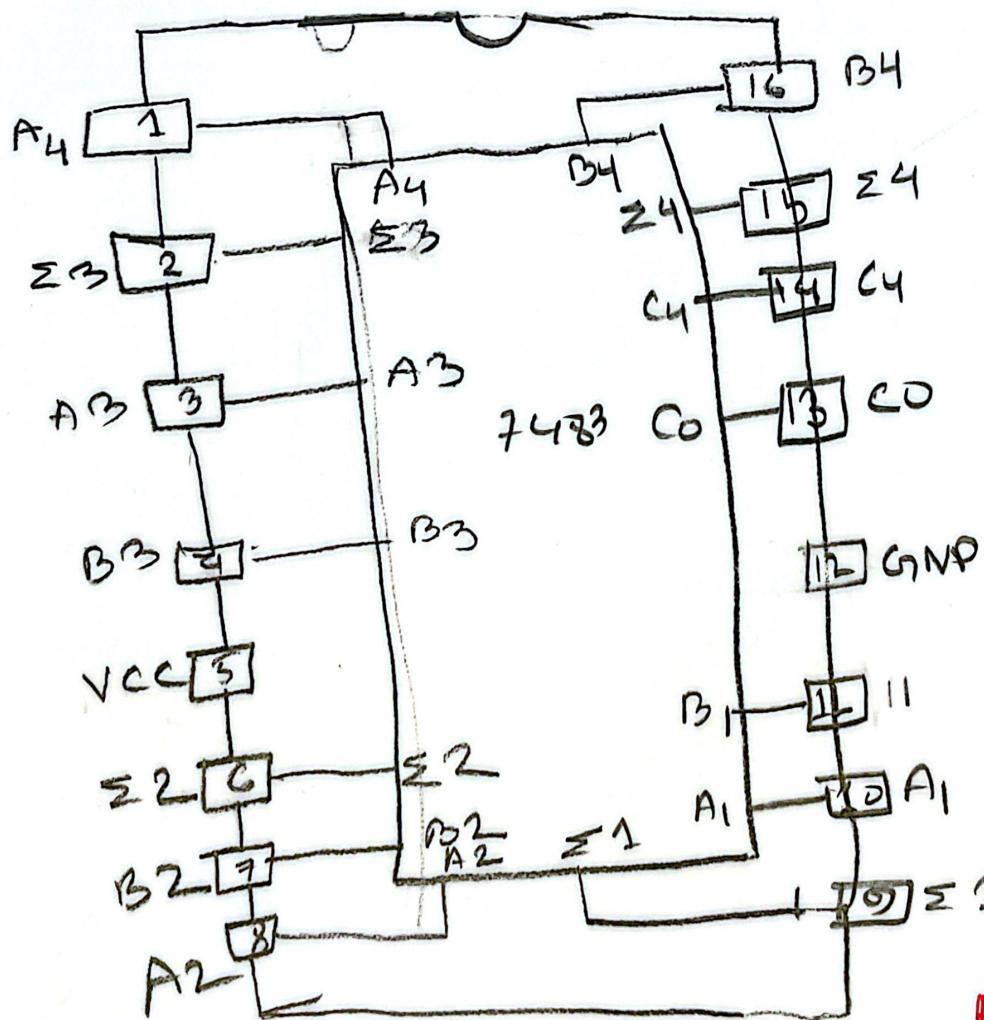
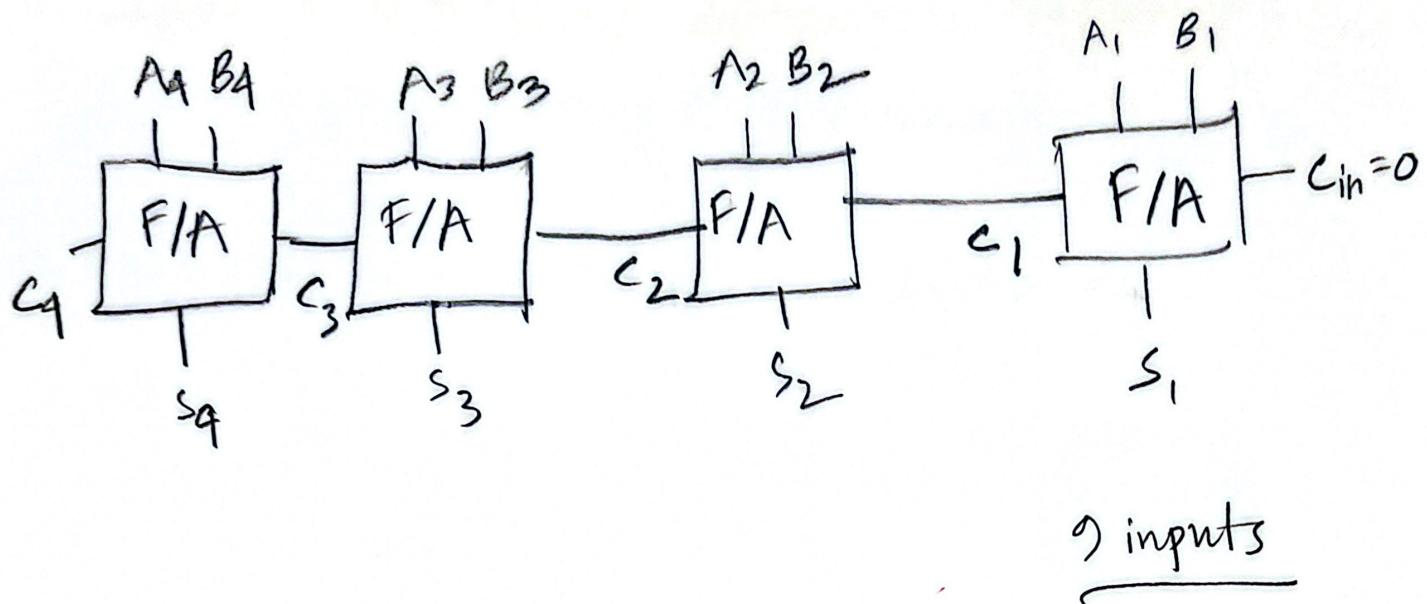
	A	B	Cin	C4	S4	S3	S2	S1
a.	0000	1000	0	0	1	0	0	0
b.	1100	1101	0	1	0	0	0	1
c.	1110	0011	0	1	0	0	0	1
d.	1111	1111	0	1	1	1	1	0

Ajedra  
09.11.25

	A	B	Cin	C4	S4	S3	S2	S1
a.	1100	1000	1	0	0	1	0	0
b.	1100	1101	0	1	1	0	0	1
c.	1110	0011	1	0	1	0	1	1
d.	1111	1111	0	1	1	1	1	0

Ajedra  
09.11.25

## 4-bit P/A:



Ayasha  
09-11-25

# Experiment # 5: Implementation of 4-bit Magnitude Comparator.

Required Components for Lab-5:

1. IC 7408
2. IC 7432
3. IC 7404
4. IC 4077

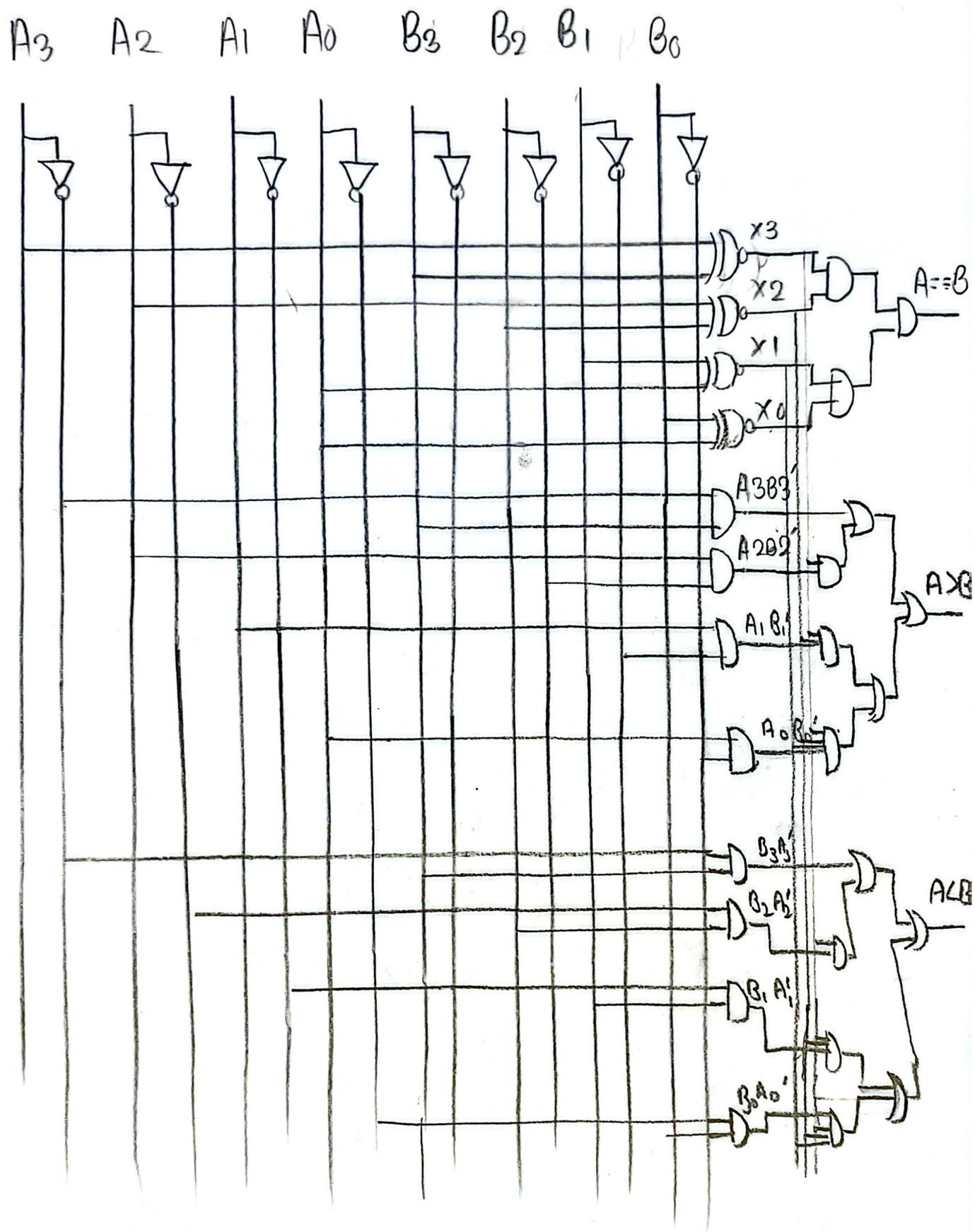


Рисунок  
 16.11.25

	A	B	$A == B$	$A > B$	$A < B$
a.	1011	0101	0	1	0
b.	0100	1001	0	0	1
c.	1000	1000	1	0	0
d.	1101	1110	0	0	1
e.	1001	1001	1	0	0
f.	0010	0001	0	1	0

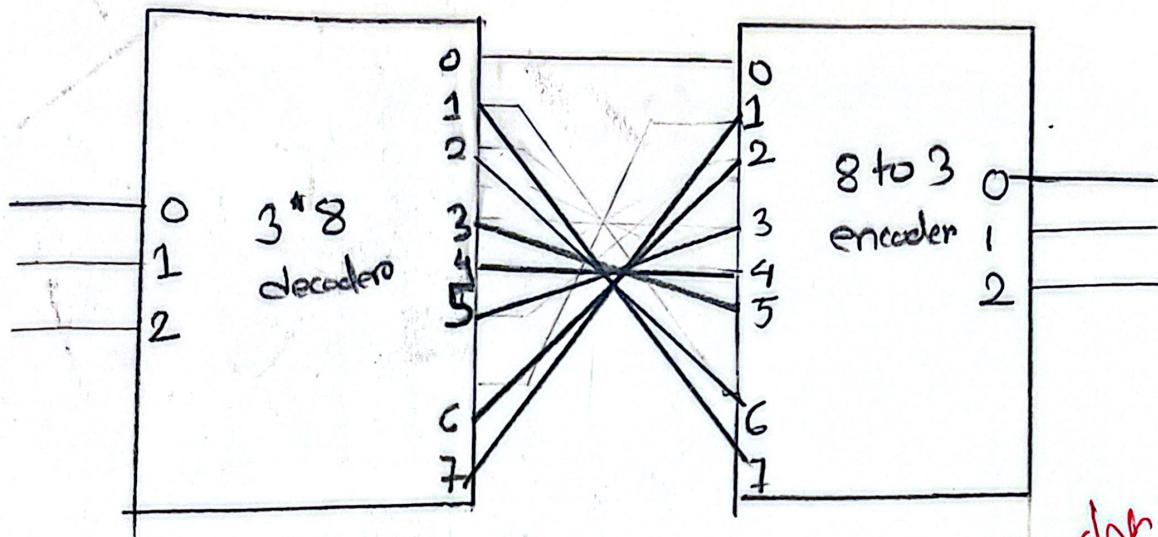
Ayesha  
16-11-25

Experiment # 6 : Design circuits using encoder & decoder

Required Components for Lab-6:

1. IC 74138

2. IC 74148



Ayesh  
07-12-25

# Experiment #7: Function Implementation Using MUX.

Required Components for Lab-7:

1. IC 74153
2. IC 7408
3. IC 7432
4. IC 7404

$$F(A, B, C, D) = \Sigma(1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13)$$

	$I_0$	$I_1$	$I_2$	$I_3$
$\bar{A}\bar{B}$	0	1	2	3
$\bar{A}B$	4	5	6	7
$A\bar{B}$	8	9	10	11
$AB$	12	13	14	15

$B$        $1$        $\bar{A}$        $\bar{A} + \bar{B}$

$$I_0 = \bar{A}\bar{B} + AB$$

$$= B(\bar{A} + A) = B$$

$$I_2 = \bar{A}\bar{B} + \bar{A}B$$

$$= \bar{A}(B + \bar{B}) = \bar{A}$$

$$I_1 = \bar{A}\bar{B} + \bar{A}B + \bar{A}\bar{B} + AB$$

$$= \bar{A}(\bar{B} + B) + A(\bar{B} + B)$$

$$= \bar{A} + A$$

$$= 1$$

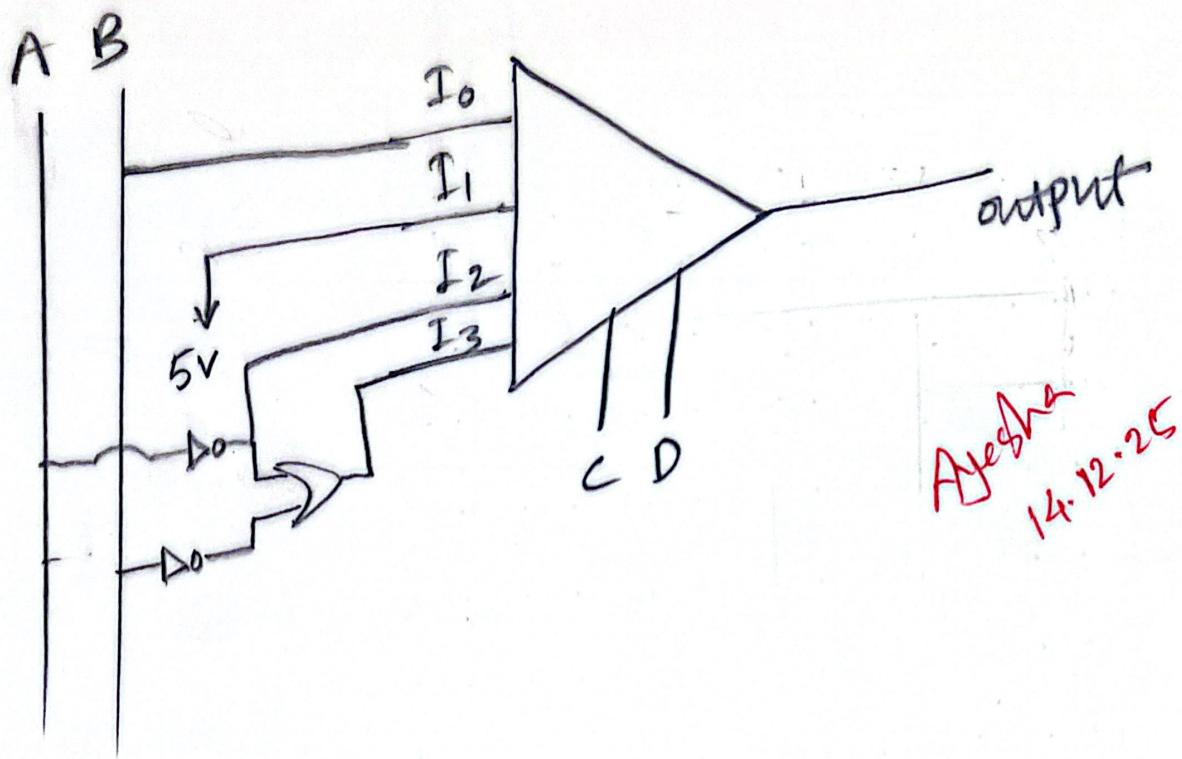
$$I_3 = \bar{A}\bar{B} + \bar{A}B + A\bar{B}$$

$$= \bar{A}(\bar{B} + B) + A\bar{B}$$

$$= \bar{A} + A\bar{B}$$

$$= (\bar{A} + A)(\bar{A} + \bar{B})$$

$$= (\bar{A} + \bar{B})$$



Ayesha  
14.12.25

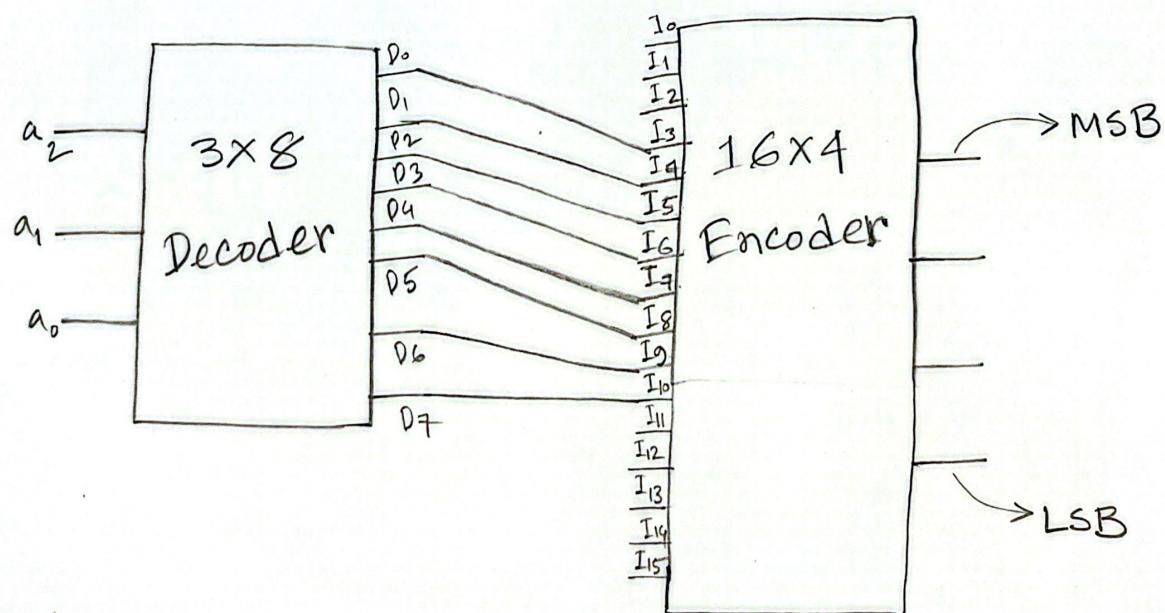
Q1: Design circuit that takes a 3-bit number as input and outputs the corresponding excess-3 using encoder and decoder.

Ans: since it is a 3-bit input, maximum number would be,

$$\begin{matrix} a_2 & a_1 & a_0 \\ 1 & 1 & 1 \end{matrix} \rightarrow 7$$

$$\text{excess-3}, 7+3=10$$

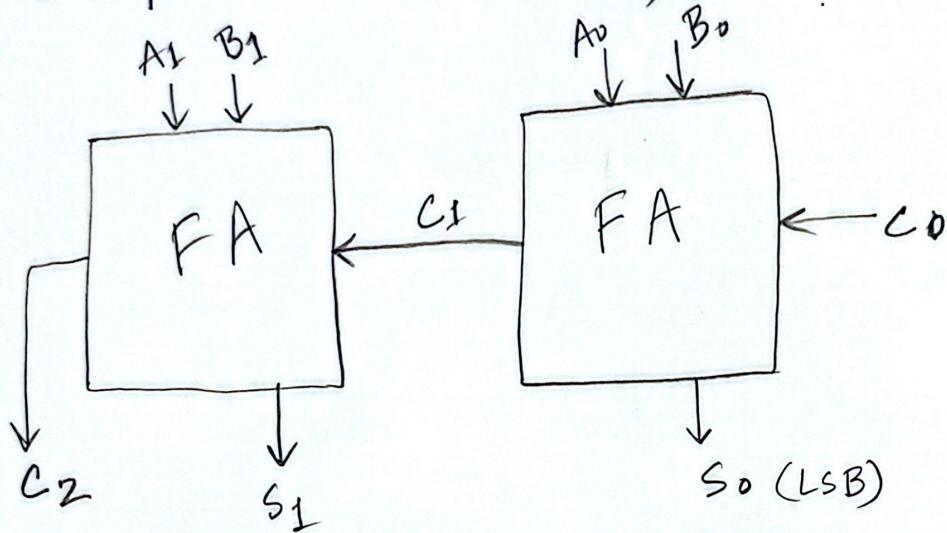
needs 4 bit to represent now,



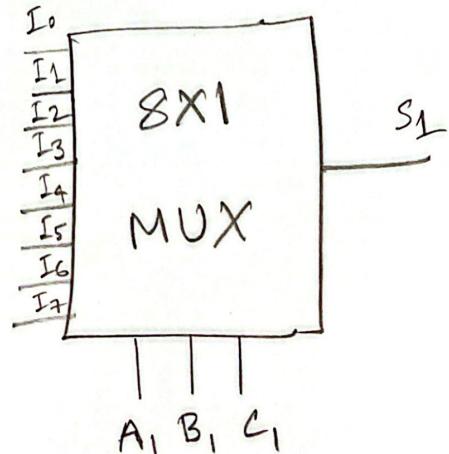
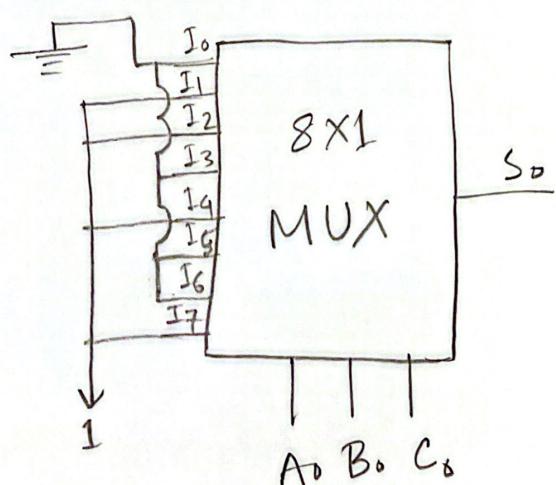
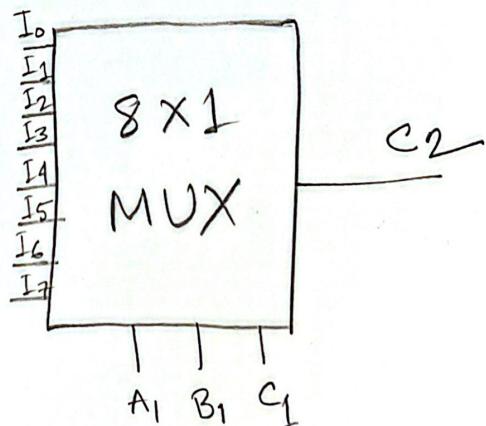
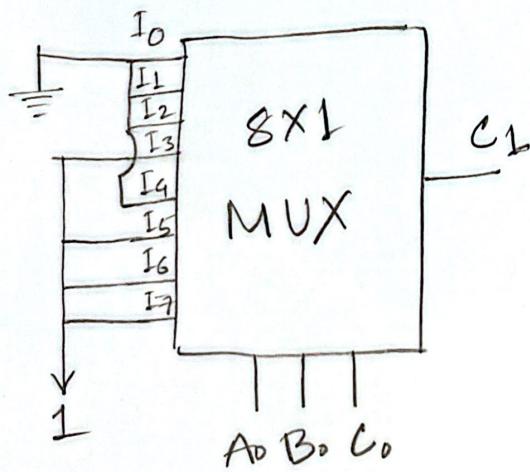
using a  $3 \times 8$  decoder and  $16 \times 4$  encoder we can design a circuit that takes a 3-bit input and output corresponding excess-3.

Q2: Design a 2-bit Parallel Adder using exactly four 8:1 MUX(s).

a 2-bit parallel adder has;



to make this with 4, 8x1 MUX(s):



## Discussion:

In the lab 4, 5, 6, 7 we have learned and implemented the use cases of MUX, decoder, encoder, parallel adder etc. Each of these components were new to us, but some of them had a few things in common. Most of them had enable or strobe enable pin(s). In terms of enable pins we had to learn a new concept called "active low." Practically we did not face any difficulties. There was a slight problem with the trainer board which caused a bit of confusion during an experiment. Otherwise, the whole experience of working in a electronic lab was amazing with two good faculties helping us and guiding whenever needed. Overall, the labs 4-7 were fun, educative and challenging to complete.