

# DLOGY Micropower Precision, Dual/Quad CMOS Rail-to-Rail Input/Output Amplifiers

## **FEATURES**

- Maximum Offset Voltage of 25µV (25°C)
- Maximum Offset Drift of 0.7µV/°C
- Maximum Input Bias:

1pA (25°C) 50pA (≤85°C)

- Micropower: 54μA per Amp
- 95dB CMRR (Min)
- 100dB PSRR (Min)
- Input Noise Voltage Density: 16nV/√Hz
- Rail-to-Rail Inputs and Outputs
- 2.7V to 5.5V Operation Voltage
- LTC6078 Available in 8-Lead MSOP and 10-Lead DFN Packages; LTC6079 Available in 16-Lead SSOP and DFN Packages

## **APPLICATIONS**

- Photodiode Amplifier
- High Impedance Sensor Amplifier
- Microvolt Accuracy Threshold Detection
- Instrumentation Amplifiers
- Battery Powered Applications

## DESCRIPTION

The LTC®6078/LTC6079 are dual/quad, low offset, low noise operational amplifiers with low power consumption and rail-to-rail input/output swing.

Input offset voltage is trimmed to less than  $25\mu V$  and the CMOS inputs draw less than 50pA of bias current. The low offset drift, excellent CMRR, and high voltage gain make it a good choice for precision signal conditioning.

Each amplifier draws only  $54\mu A$  current on a 3V supply. The micropower, rail-to-rail operation of the LTC6078/LTC6079 is well suited for portable instruments and single supply applications.

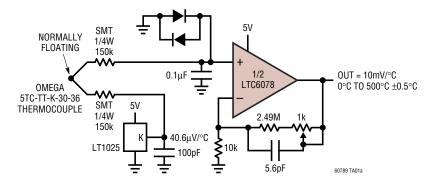
The LTC6078/LTC6079 are specified on power supply voltages of 3V and 5V from -40 to 125°C. The dual amplifier LTC6078 is available in 8-lead MSOP and 10-lead DFN packages. The quad amplifier LTC6079 is available in 16-lead SSOP and DFN packages.

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## TYPICAL APPLICATION

#### Thermocouple Signal Conditioner



AMPLIFIER PROTECTED TO ±190V, ACCIDENTAL CONTACT

14 LTC6078MS8 V<sub>S</sub> = 3V V<sub>CM</sub> = 0.5V T<sub>A</sub> = 25°C T<sub>A</sub>

Vos Distribution



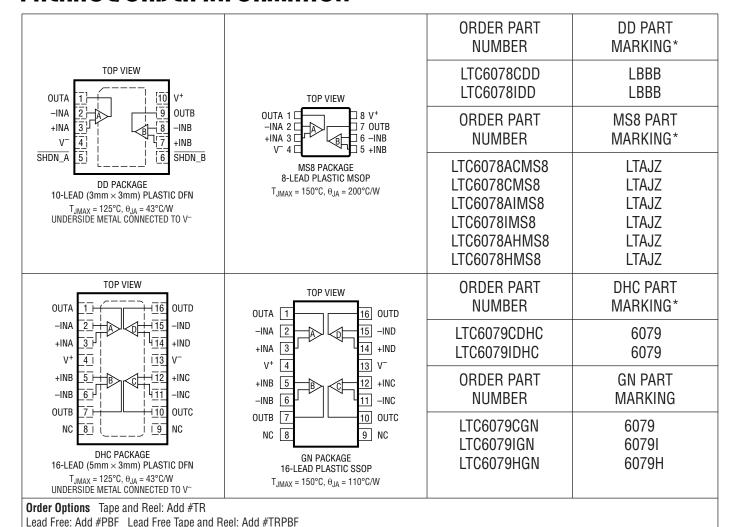
## **ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Total Supply Voltage (V+ to V-)	6V
Input Voltage	
Output Short Circuit Duration (Note 2) .	Indefinite
Operating Temperature Range (Note 3)	
LTC6078C, LTC6079C	–40°C to 85°C
LTC6078I, LTC6079I	
LTC6078H, LTC6079H	40°C to 125°C
(Not Available in DFN Package)	

Specified Temperature Range (Note 4)	
LTC6078C, LTC6079C	0°C to 70°C
LTC6078I, LTC6079I	–40°C to 85°C
LTC6078H, LTC6079H	–40°C to 125°C
Junction Temperature	
DFN Packages	125°C
All Other Packages	150°C
Storage Temperature Range	
DFN Packages	–65°C to 125°C
All Other Packages	–65°C to 150°C
Lead Temperature (Soldering, 10 Sec)	300°C

## PACKAGE/ORDER INFORMATION



Consult LTC Marketing for parts specified with wider operating temperature ranges.

Lead Free Part Marking: http://www.linear.com/leadfree/

LINEAR TECHNOLOGY

<sup>\*</sup>The temperature grades and parametric grades are identified by a label on the shipping container.

## **ELECTRICAL CHARACTERISTICS** The $\bullet$ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$ . Test conditions are $V^+ = 3V$ , $V^- = 0V$ , $V_{CM} = 0.5V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			C,	I SUFFI)	(ES	I	H SUFFIX	X	UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	1
V <sub>0S</sub>	Offset Voltage (Note 5)	LTC6078MS8, LTC6078AMS8, LTC6078DD, LTC6079DHC LTC6078AMS8 LTC6078MS8 LTC6079GN LTC6078DD LTC6079DHC	V <sub>CM</sub> = 0.5V, 2.5V V <sub>CM</sub> = 0.5V, 2.5V V <sub>CM</sub> = 0.5V, 2.5V V <sub>CM</sub> = 0.5V V <sub>CM</sub> = 0.5V V <sub>CM</sub> = 0.5V V <sub>CM</sub> = 0.5V V <sub>CM</sub> = 0.5V	• • • •		±7 ±7 ±20 ±25 ±30 ±30	±25 ±30 ±70 ±97 ±115 ±120 ±150		±7 ±25 ±30 ±35	±25 ±95 ±135 ±165	μV μV ν μV μV μV
ΔV <sub>0S</sub> /ΔΤ	Input Offset Voltage Drift (Note 5)	LTC6078AMS8 LTC6078MS8 LTC6078DD, LTC6079GN LTC6079DHC		• • •		±0.2 ±0.3 ±0.3	±0.7 ±1.1 ±1.4 ±1.8		±0.2 ±0.3	±0.7 ±1.1 ±1.4	μV/°C μV/°C μV/°C μV/°C
I <sub>B</sub>	Input Bias Current (Note 6)	V <sub>CM</sub> = V <sup>+</sup> /2 V <sub>CM</sub> = V <sup>+</sup> /2		•		0.2 10	1 50		0.2 150	1 350	pA pA
I <sub>OS</sub>	Input Offset Current (Note 6)	$V_{CM} = V^{+}/2$ $V_{CM} = V^{+}/2$		•		0.1 0.5	25		0.1 10	100	pA pA
e <sub>n</sub>	Input Noise Voltage	0.1Hz to 10Hz				1			1		μV <sub>P-P</sub>
	Input Noise Voltage Density	f = 1kHz f = 10kHz				18 16			18 16		nV/√Hz nV/√Hz
i <sub>n</sub>	Input Noise Current Density (Note 8)					0.56			0.56		fA/√Hz
	Input Common Mode Range			•	V <sup>-</sup>		V+	V-		V+	V
C <sub>DIFF</sub>	Differential Input Capacitance					10			10		pF
C <sub>CM</sub>	Common Mode Input Capacitance					18			18		pF
CMRR	Common Mode Rejection Ratio	All Packages LTC6078AMS8 LTC6078AMS8 LTC6078MS8 LTC6078MS8 LTC6079GN LTC6079GN LTC6078DD, LTC6079DHC LTC6078DD, LTC6079DHC	V <sub>CM</sub> = 0V to 3V V <sub>CM</sub> = 0V to 3V V <sub>CM</sub> = 0V to 1.7V V <sub>CM</sub> = 0V to 3V V <sub>CM</sub> = 0V to 1.7V V <sub>CM</sub> = 0V to 3V V <sub>CM</sub> = 0V to 1.7V V <sub>CM</sub> = 0V to 3V V <sub>CM</sub> = 0V to 3V V <sub>CM</sub> = 0V to 3V V <sub>CM</sub> = 0V to 1.7V	• • • • • • •	95 87 91 85 89 84 88 83 87	110 105 103 102 102 102 102 100 100		95 87 91 85 89 84 88	110 103 103 100 102 100 102		dB dB dB dB dB dB dB
PSRR	Power Supply Rejection Ratio	V <sub>S</sub> = 2.7V to 5.5V		•	100 97	120		100 97	120		dB dB
V <sub>OUT</sub>	Output Voltage, High (Referred to V <sup>+</sup> )	No Load  Source = 0.2mA  Source = 2mA		•	35 350	1 15 150		40 400	1 15 150		mV mV mV
	Output Voltage, Low (Referred to V <sup>-</sup> )	No Load   I <sub>SINK</sub> = 0.2mA   I <sub>SINK</sub> = 2mA		•		1 10 100	30 300		1 10 100	35 350	mV mV mV
A <sub>VOL</sub>	Large-Signal Voltage Gain	$R_{LOAD} = 10k, 0.5V \le V_{OUT} \le 2.5V$		•	115	130		110	125		dB
I <sub>SC</sub>	Output Short-Circuit Current	Source Sink		•	5 7	10 14		4 6	10 14		mA mA
SR	Slew Rate	A <sub>V</sub> = 1				0.05			0.05		V/µs
GBW	Gain-Bandwidth Product (f <sub>TEST</sub> = 10kHz)	R <sub>L</sub> = 100k		•	420 360	750		420 320	750		kHz kHz
Φ0	Phase Margin	R <sub>L</sub> = 10k, C <sub>L</sub> = 200pF				66			66		Deg
t <sub>S</sub>	Settling Time 0.1%	A <sub>V</sub> = 1, 1V Step				24			24		μs



## **ELECTRICAL CHARACTERISTICS** The $\bullet$ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$ . Test conditions are $V^+ = 3V$ , $V^- = 0V$ , $V_{CM} = 0.5V$ unless otherwise noted.

SYMBOL	PARAMETER CONDITIONS				C, I SUFFIXES			H SUFFIX			
				MIN	TYP	MAX	MIN	TYP	MAX		
Is	Supply Current (per Amplifier)	No Load	•		54	72 78		54	72 80	μA μA	
	Shutdown Current (per Amplifier)	Shutdown, $V_{\overline{SHDN}} \le 0.8V$ , LTC6078DD	•		0.3	1				μА	
$V_S$	Supply Voltage Range	Guaranteed by the PSRR Test	•	2.7		5.5	2.7		5.5	V	
	Channel Separation	f <sub>S</sub> = 10kHz, R <sub>L</sub> = 10k		-110 -110			dB				
	Shutdown Logic	SHDN High, LTC6078DD SHDN Low, LTC6078DD	•	2		0.8	2		0.8	V	
t <sub>ON</sub>	Turn on Time	V <sub>SHDN</sub> = 0.8V to 2V, LTC6078DD			50			50		μs	
t <sub>OFF</sub>	Turn off Time	V <sub>SHDN</sub> = 2V to 0.8V, LTC6078DD		2 2			μs				
	Leakage of SHDN Pin	V <sub>SHDN</sub> = 0V, LTC6078DD			0.6					μА	

The ullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ . Test conditions are  $V^+ = 5V$ ,  $V^- = 0V$ ,  $V_{CM} = 0.5V$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C, I SUFFIXES				UNITS		
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OS</sub>	Offset Voltage	LTC6078MS8, LTC6078AMS8, LTC6078	.5V .5V .5V .5V .5V		±10 ±10 ±20 ±25 ±30 ±30	±30 ±35 ±75 ±102 ±120 ±125 ±155		±10 ±25 ±30 ±35	±30 ±100 ±140 ±170	μV μV μV μV μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 7)	LTC6078AMS8 LTC6078MS8 LTC6078DD, LTC6079GN LTC6079DHC	•		±0.2 ±0.3 ±0.3	±0.7 ±1.1 ±1.4 ±1.8		±0.2 ±0.3	±0.7 ±1.1 ±1.4	μV/°C μV/°C μV/°C μV/°C
I <sub>B</sub>	Input Bias Current	V <sub>CM</sub> = V <sup>+</sup> /2 V <sub>CM</sub> = V <sup>+</sup> /2	•	,	0.2 10	1 50		0.2 150	1 350	pA pA
I <sub>OS</sub>	Input Offset Current	$V_{CM} = V^{+}/2$ $V_{CM} = V^{+}/2$	•	,	0.1 0.5	25		0.1 10	100	pA pA
e <sub>n</sub>	Input Noise Voltage	0.1Hz to 10Hz			1			1		μV <sub>P-P</sub>
	Input Noise Voltage Density	f = 1kHz f = 10kHz			18 16			18 16		nV/√Hz nV/√Hz
i <sub>n</sub>	Input Noise Current Density (Note 8)				0.56			0.56		fA/√Hz
	Input Common Mode Range		•	V-		V <sup>+</sup>	V-		V+	V
C <sub>DIFF</sub>	Differential Input Capacitance				10			10		pF
C <sub>CM</sub>	Common Mode Input Capacitance				18			18		pF

## **ELECTRICAL CHARACTERISTICS** The $\bullet$ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25$ °C. Test conditions are $V^+ = 5V$ , $V^- = 0V$ , $V_{CM} = 0.5V$ unless otherwise noted.

SYMBOL	PARAMETER CONDITIONS			C,	C, I SUFFIXES			H SUFFIX		
				MIN	TYP	MAX	MIN	TYP	MAX	
CMRR	Common Mode Rejection Ratio	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	•	91 90 94 88 90 86 90 86 90	105 105 105 100 105 100 105 100 105		91 90 94 88 90 86 90	105 105 105 100 105 100 105		dB dB dB dB dB dB dB
PSRR	Power Supply Rejection Ratio	V <sub>S</sub> = 2.7V to 5.5V	•	100 97	120		97	120		dB dB
V <sub>OUT</sub>	Output Voltage, High (Referred to V <sup>+</sup> )	No Load  SOURCE = 0.5mA  SOURCE = 5mA	•	50 500	2 20 200		55 550	2 20 200		mV mV mV
	Output Voltage, Low (Referred to V <sup>-</sup> )	No Load I <sub>SINK</sub> = 0.5mA I <sub>SINK</sub> = 5mA	•		1 15 150	40 400		1 15 150	45 450	mV mV mV
A <sub>VOL</sub>	Large-Signal Voltage Gain	$R_{LOAD} = 10k, \ 0.5V \le V_{OUT} \le 4.5V$		115	130		110	125		dB
I <sub>SC</sub>	Output Short-Circuit Current	Source Sink		14 14	25 25		12 12	25 25		mA mA
SR	Slew Rate	A <sub>V</sub> = 1			0.05			0.05		V/µs
GBW	Gain-Bandwidth Product (f <sub>TEST</sub> = 10kHz)	R <sub>L</sub> = 100k	•	420 360	750		420 320	750		kHz kHz
$\Phi_0$	Phase Margin	$R_L = 10k, C_L = 200pF$			66			66		Deg
ts	Settling Time 0.1%	A <sub>V</sub> = 1, 1V Step			24			24		μs
Is	Supply Current (per Amplifier)	No Load	•		55	74 82		55	74 84	μA μA
	Shutdown Current (per Amplifier)	Shutdown, $V_{\overline{SHDN}} \le 1.2V$ , LTC6078DD			1.5	5		1.5	5	μА
V <sub>S</sub>	Supply Voltage Range	Guaranteed by the PSRR Test		2.7		5.5	2.7		5.5	V
	Channel Separation	$f_S = 10kHz, R_L = 10k$			-110			-110		dB
	Shutdown Logic	SHDN High, LTC6078DD SHDN Low, LTC6078DD		3.5		1.2	3.5		1.2	V V
t <sub>ON</sub>	Turn on Time	V <sub>SHDN</sub> = 1.2V to 3.5V, LTC6078DD			50			50		μs
t <sub>OFF</sub>	Turn off Time	V <sub>SHDN</sub> = 1.2V to 3.5V, LTC6078DD			2			2		μs
	Leakage of SHDN Pin	V <sub>SHDN</sub> = 0V, LTC6078DD			0.6					μA

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted.

**Note 3:** The LTC6078C/LTC6079C and LTC6078I/LTC6079I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6078H/LTC6079H are guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 4: The LTC6078C/LTC6079C are guaranteed to meet specified

performance from 0°C to 70°C. The LTC6078C/LTC6079C are designed, characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LTC6078I/LTC6079I are guaranteed to meet specified performance from -40°C to 85°C. The LTC6078H/LTC6079H are guaranteed to meet specified performance from -40°C to 125°C.

Note 5:  $V_{OS}$  and  $V_{OS}$  drift are 100% tested at 25°C and 125°C.

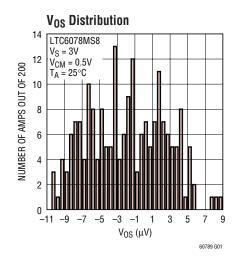
**Note 6:**  $I_B$  and  $I_{OS}$  are guaranteed by the  $V_S = 5V$  test.

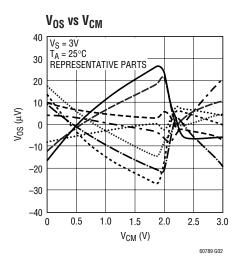
**Note 7:**  $V_{OS}$  drift is guaranteed by the  $V_S = 3V$  test.

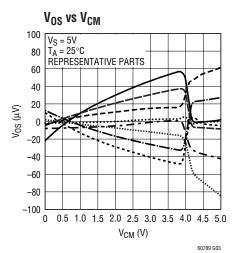
**Note 8:** Current noise is calculated from  $i_n = \sqrt{2qI_B}$ , where  $q = 1.6 \cdot 10^{-19}$  coulomb.

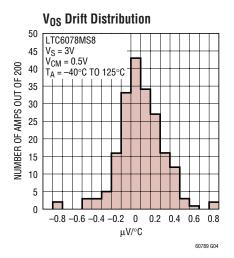


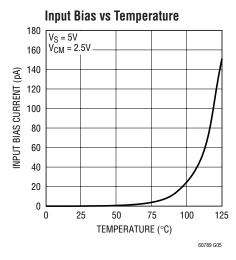
## TYPICAL PERFORMANCE CHARACTERISTICS

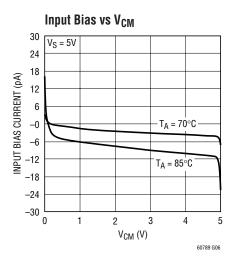


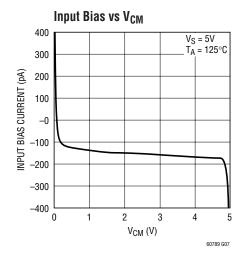


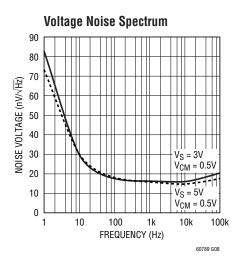


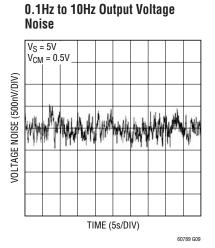






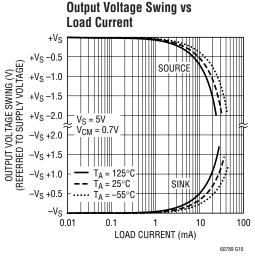


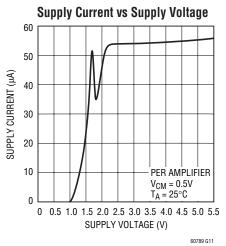


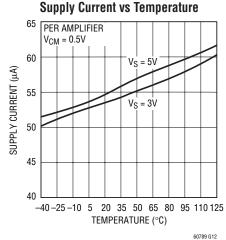


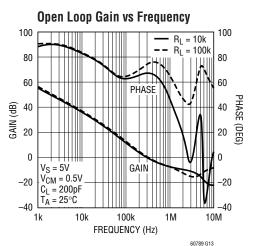


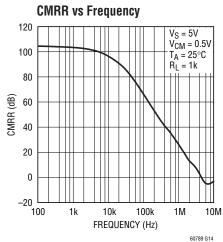
## TYPICAL PERFORMANCE CHARACTERISTICS

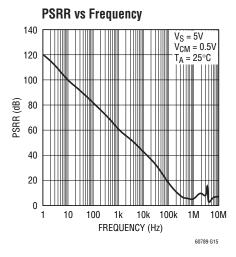


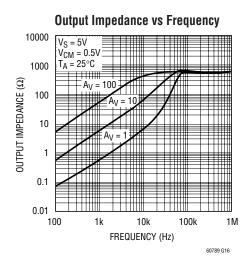


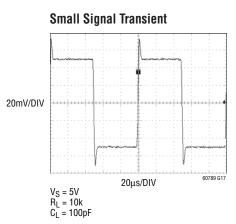


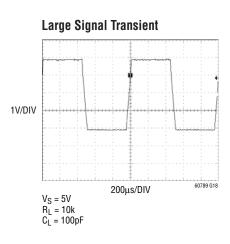








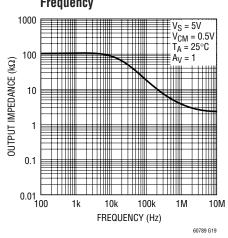


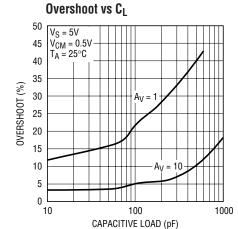


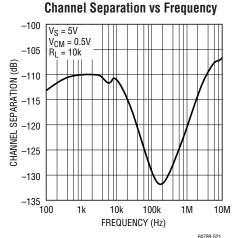
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## TYPICAL PERFORMANCE CHARACTERISTICS

Disabled Output Impedence vs Frequency







## PIN FUNCTIONS

**OUT:** Amplifier Output

-IN: Inverting Input

+IN: Noninverting Input

V+: Positive Supply

V-: Negative Supply

**SHDN\_A**: Shutdown Pin of Amplifier A, active low and only valid for LTC6078DD. An internal current source pulls the pin to V<sup>+</sup> when floating.

**SHDN\_B**: Shutdown Pin of Amplifier B, active low and only valid for LTC6078DD. An internal current source pulls the pin to V<sup>+</sup> when floating.

NC: Not internally connected.

60789 G20

**Exposed Pad:** Connected to V<sup>-</sup>.



## APPLICATIONS INFORMATION

### **Preserving Input Precision**

Preserving input accuracy of the LTC6078/LTC6079 requires that the application circuit and PC board layout do not introduce errors comparable or greater than the  $10\mu V$  typical offset of the amplifiers. Temperature differentials across the input connections can generate thermocouple voltages of 10's of microvolts so the connections to the input leads should be short, close together and away from heat dissipating components. Air current across the board can also generate temperature differentials.

The extremely low input bias currents (0.2pA typical) allow high accuracy to be maintained with high impedance sources and feedback resistors. Leakage currents on the PC board can be higher than the input bias current. For example,  $10G\Omega$  of leakage between a 5V supply lead and an input lead will generate 500pA! Surround the input leads with a guard ring driven to the same potential as the input common mode to avoid excessive leakage in high impedance applications.

## **Input Clamps**

Large differential voltages across the inputs over very long time periods can impact the precisely trimmed input offset voltage of the LTC6078/LTC6079. As an example, a 2V differential voltage between the inputs over a period of 100 hours can shift the input offset voltage by tens of microvolts. If the amplifier is to be subjected to large differential input voltages, adding back-to-back diodes between the two inputs will minimize this shift and retain the DC precision. If necessary, current-limiting series resistors can be added in front of the diodes, as shown in Figure 1. These diodes are not necessary for normal closed loop applications.

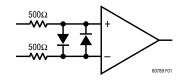


Figure 1. Op Amp with Input Voltage Clamp

#### **Capacitive Load**

LTC6078/LTC6079 can drive capactive load up to 200pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the ouput and the load further increases the amount of capacitance the amplifier can drive.

#### **SHDN** Pins

Pins 5 and 6 are used for power shutdown on the LTC6078 in the DD package. If they are floating, internal current sources pull Pins 5 and 6 to V+ and the amplifiers operate normally. In shutdown, the amplifier output is high impedance, and each amplifier draws less than 2µA current.

When the chip is turned on, the supply current per amplifier is about  $35\mu A$  larger than its normal values for  $50\mu s$ .

#### Rail-to-Rail Input

The input stage of LTC6078/LTC6079 combines both PMOS and NMOS differential pairs, extending its input common mode voltage range to both positive and negative supply voltages. At high input common mode range, the NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between 1.3V and 0.9V below the positive supply.

## **Thermal Hysteresis**

Figure 2 shows the input offset hysteresis of LTC6078MS8 for 3 thermal cycles from  $-45^{\circ}$ C to  $90^{\circ}$ C. The typical offset shift after the 3 cycles is only  $1\mu$ V.

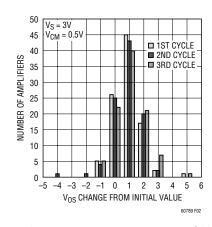


Figure 2. V<sub>OS</sub> Thermal Hysteresis of LTC6078MS8



## APPLICATIONS INFORMATION

## **PC Board Layout**

Mechanical stress on a PC board and soldering-induced stress can cause the  $V_{OS}$  and  $V_{OS}$  drift to shift. The DD and DHC packages are more sensitive to stress. A simple way to reduce the stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board edge acts as a stress boundary, or a region where the flexure of the board is minimum. The package should always be mounted so that the leads absorb the stress and not the package. The package is generally aligned with the leads paralled to the long side of the PC board.

The most effective technique to relieve the PC board stress is to cut slots in the board around the op amp. These slots can be cut on three sides of the IC and the leads can exit on

the fourth side. Figure 3 shows the layout of a LTC6078DD with slots at three sides.

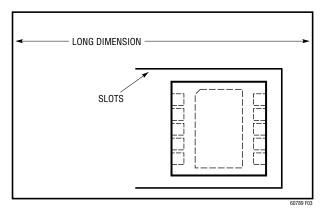
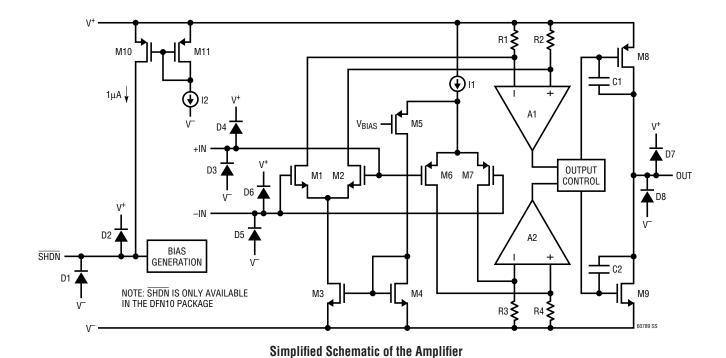
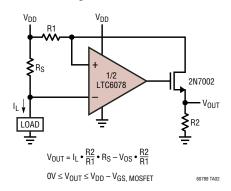


Figure 3. Vertical Orientation of LTC6078DD with Slots

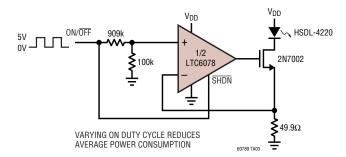
## SIMPLIFIED SCHEMATIC



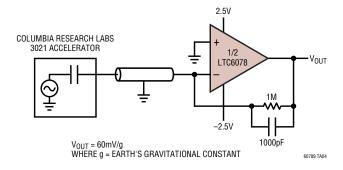
### 2.7V High Side Current Sense



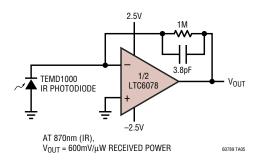
#### Low Average Power IR LED Driver



#### **Accelerometer Signal Conditioner**

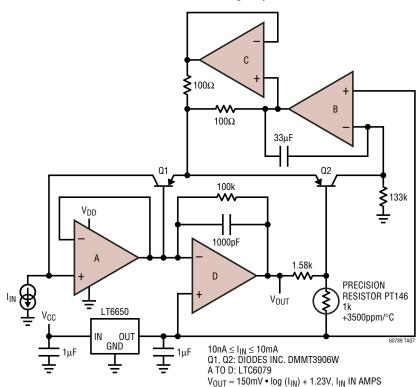


#### **Photodiode Amplifier**

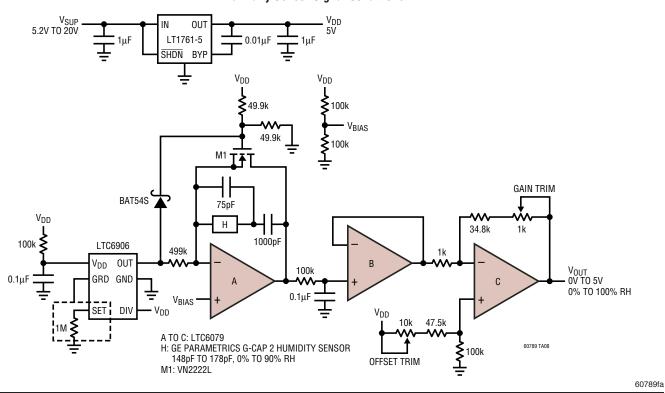


/ LINEAR

### **6 Decade Current Log Amplifier**

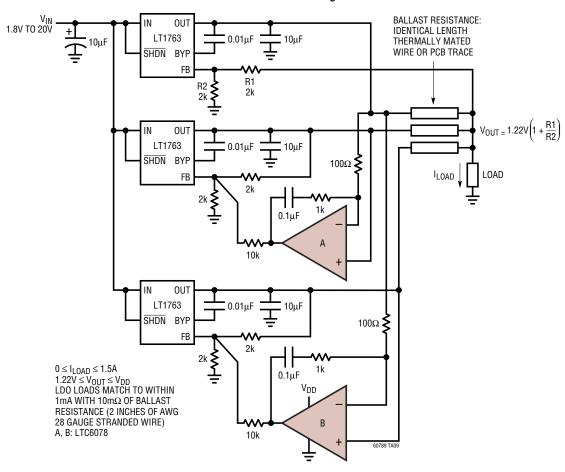


#### **Humidity Sensor Signal Conditioner**

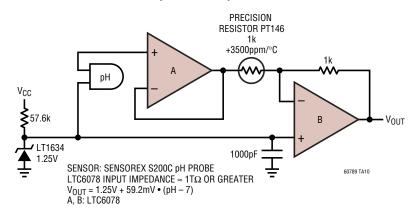




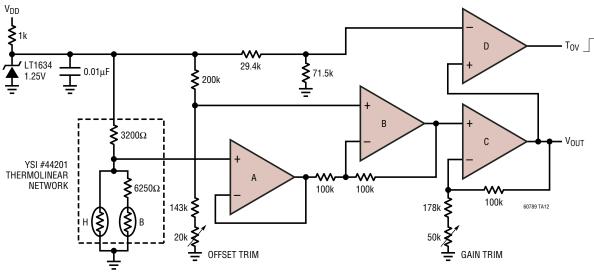
#### **LDO Load Balancing**



#### pH Probe Amplifier

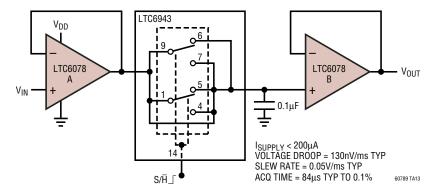


#### Thermistor Amplifier with Overtemperature Alarm

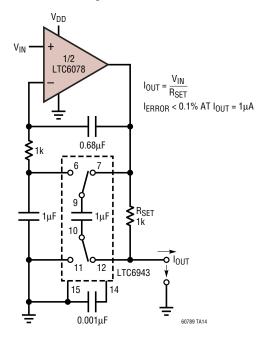


A TO D: LTC6079, V<sub>DD</sub> = 2.7V TO 5.5V, V<sub>SS</sub> = GND V<sub>OUT</sub> = 0  $\rightarrow$  1V FOR 0°C TO 100°C, LINEAR T<sub>OV</sub>  $\rightarrow$  HIGH WHEN T  $\geq$  90°C

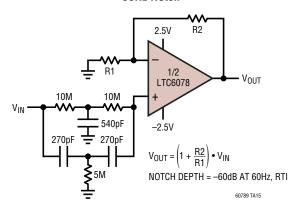
#### **Precision Sample-and-Hold**



### **Precision Voltage-Controlled Current Source**

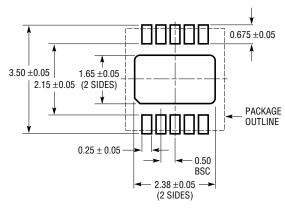


#### **60Hz Notch**

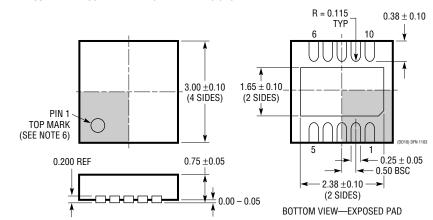


## $\begin{array}{c} \text{DD Package} \\ \text{10-Lead Plastic DFN (3mm} \times \text{3mm)} \end{array}$

(Reference LTC DWG # 05-08-1699)



#### **RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS



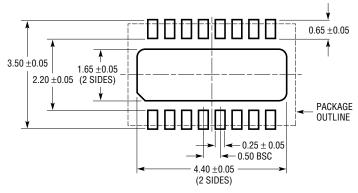
#### NOTE:

- DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
- 2. DRAWING NOT TO SCALE
- 3. ALL DIMENSIONS ARE IN MILLIMETERS
- 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
- 5. EXPOSED PAD SHALL BE SOLDER PLATED
- 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

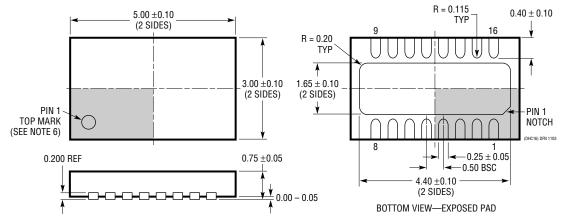


#### **DHC Package** 16-Lead Plastic DFN (5mm × 3mm)

(Reference LTC DWG # 05-08-1706)



#### **RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS

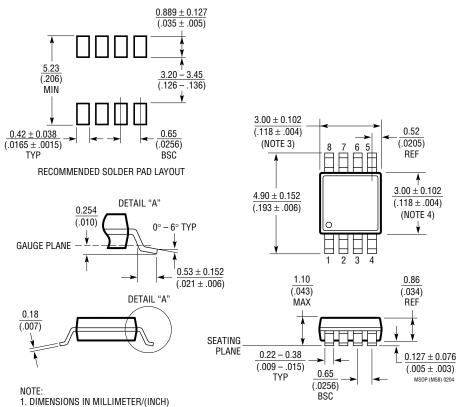


- NOTE:
- 1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
  2. DRAWING NOT TO SCALE
- 3. ALL DIMENSIONS ARE IN MILLIMETERS
- 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
- 5. EXPOSED PAD SHALL BE SOLDER PLATED
- 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



#### **MS8 Package** 8-Lead Plastic MSOP

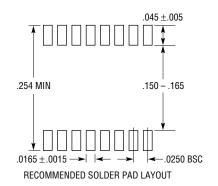
(Reference LTC DWG # 05-08-1660)

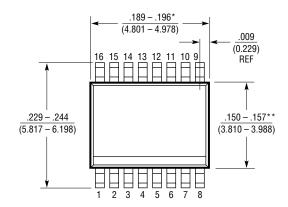


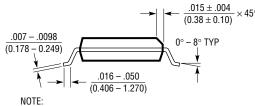
- 2. DRAWING NOT TO SCALE
- DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
- 4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE 5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

#### **GN Package** 16-Lead Plastic SSOP (Narrow .150 Inch)

(Reference LTC DWG # 05-08-1641)

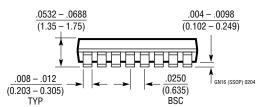




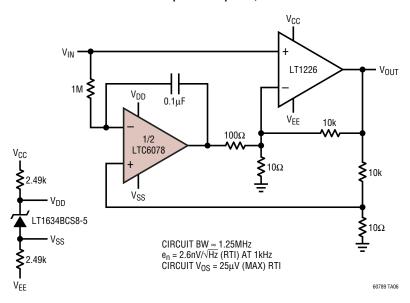




- 1. CONTROLLING DIMENSION: INCHES
- 2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
- 3. DRAWING NOT TO SCALE
- \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
- \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE



#### DC Accurate Composite Amplifier, Gain of 1000



## **RELATED PARTS**

PART NUMBER	DESCRIPTION	COMMENTS
LTC2051/LTC2052	Dual/Quad Zero-Drift Op Amps	3μV V <sub>OS</sub> , 30nV/°C V <sub>OS</sub> Drift
LT6011/LT6012	Dual/Quad Precision Op Amps	60μV V <sub>OS</sub> , I <sub>B</sub> = 300pA, I <sub>S</sub> = 135μA