Afsal K

Electrical and Electronics Engineering Student
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Objective

Motivated and detail-oriented third-year B.Tech student in Electrical and Electronics Engineering at CUSAT, seeking a 2-month internship in VLSI design and FPGA development. Eager to apply academic training and certification-backed skills in RTL design, digital logic, and Verilog HDL programming to contribute meaningfully to real-world projects. Demonstrated experience with hardware simulation tools and digital circuit implementation.

Education

B.Tech in Electrical and Electronics Engineering 2022 – Present
School of Engineering, CUSAT (Cochin University of Science and Technology)

Higher Secondary (Class 12) - Science Stream 2020 – 2022
Kalladi HSS, Kumarumputhur *91%*

SSLC (Class 10) 2020
GHS Karakurissi *96%*

Technical Skills

HDL & Digital Design: Verilog HDL, VHDL (basic), RTL Design, Digital Logic Design, FSM Implementation
FPGA & EDA Tools: Xilinx Vivado, Intel Quartus Prime (basic), ModelSim, Synopsys VCS (basic)
Programming Languages: Python, C/C++, Assembly (basic)
Simulation & Debugging: LTspice, Multisim, MATLAB (basic), Cadence (exposure)
Documentation & Tools: LaTeX, Technical Documentation, Design Specifications, Git (basic)
Soft Skills: Problem Solving, Critical Thinking, Team Collaboration, Time Management

Relevant Certifications

- **VLSI CAD: Logic to Layout** – University of Illinois at Urbana-Champaign (Coursera)
- **Introduction to FPGA Design for Embedded Systems** – University of Colorado Boulder (Coursera)
- **Hardware Description Languages for FPGA Design** – University of Colorado Boulder (Coursera)

Academic Projects

ESP8266-Based Automated Water Level Control and Pump Protection System

- Designed and implemented a microcontroller-based water management system using ESP8266 WiFi module
- Engineered automated pump control with false-trigger delay mechanism using digital logic
- Developed dry-run protection with 60-second timer algorithm to prevent pump damage
- Implemented WiFi-based IoT remote monitoring and manual override capability
- Utilized optocoupler isolation techniques for controller safety in high-voltage environments

Pediatric Pneumonia Prediction Using Deep Learning

- Developed a medical image classification model using transfer learning techniques with DenseNet-161
- Trained the neural network on labeled pediatric pneumonia chest X-ray dataset
- Modified CNN architecture for binary classification output (pneumonia vs. normal)
- Achieved 94% accuracy in early detection and diagnosis of pediatric respiratory infections
- Utilized Python, PyTorch, and data augmentation techniques for model improvement

VLSI/FPGA Projects

Single-Cycle MIPS Processor Subset

- Designed and simulated a complete CPU architecture with fetch, decode, execute, memory, and writeback stages
- Implemented instruction set including arithmetic (ADD, SUB), memory (LW, SW), and branch (BEQ) operations
- Utilized Verilog HDL for RTL design and functional simulation in ModelSim
- Synthesized design in Vivado for performance and resource utilization analysis

UART Communication Module

- Developed UART transmitter and receiver modules using finite state machine methodology
- Implemented standard 9600 baud rate serial communication with configurable parameters
- Created protocol for start/stop bit detection, data framing, and error checking
- Verified functionality through comprehensive waveform simulation and timing analysis

Digital System Components

- **Universal Shift Register:** 4-bit bidirectional register with parallel load, shift-left/right capabilities
- **8-bit Register File:** Dual-port memory structure supporting simultaneous read/write operations
- **4-bit ALU:** Arithmetic Logic Unit with ADD, SUB, AND, OR operations and overflow detection
- **Priority Encoder:** 8-to-3 encoder implementation with enable signal and valid output indicators

State Machine Implementations

- **Vending Machine Controller:** Moore FSM design for coin detection, product selection and dispensing
- **Traffic Light Controller:** Synchronized multi-way intersection controller with configurable timing
- **Clock Divider:** Frequency divider converting 50 MHz input to programmable lower frequencies
- All designs implemented in Verilog HDL with comprehensive testbenches and timing verification

Extracurricular & Activities

- Active Member, Electrical Engineering Students Association (EESA) and IEEE Student Branch
- Technical Team Member, YUVA Execom Team - Organized technical workshops and events
- Core Member, Horizon Club - Participated in innovation challenges and project competitions
- Participant in multiple Hackathons and Ideathons focusing on hardware solutions
- Volunteered in technical workshops on FPGA Programming, Embedded Systems, and IoT applications

Additional Technical Certifications

- **Introduction to Python for Cybersecurity** – Infosec
- **Web Application Technologies and Django** – University of Michigan
- **Cloud Computing with AWS** – DevTown