COMSATS University Islamabad
Vehari Campus

Department of Computer Science

Assignment 2 – Fall 2025

Class: BSSE | Date: Oct 18, 2025

Course: Digital Logic Design | Instructor: Syeda Zoupash Zahra

CLO-2: Apply Boolean Algebra and K-Map techniques for gate level minimization of digital circuits, and represent the digital functions in canonical and standard forms.

Question 01:

Given the Boolean function Q(a,b,c,d,e) represented in canonical form, where:

$$Q(a,b,c,d,e)=\sum m(0,1,2,3,9,11,17,19,23,25,29,31)+d(4,7,13,14,21,30)$$

- Construct a Karnaugh Map for the given function Q(a,b,c,d,e)
- Simplify the Boolean expression by grouping the cells in the K-Map and identify the minimized Boolean expression.

Question 02:

Using the Karnaugh Map provided, simplify the following Boolean function based on the variables A,B,C, and D:

0	0	X	0
1	1	0	0
1	0	0	1
1	X	1	1

a) Interpret the K-Map shown and identify all possible groupings for minimization.
b) Derive the simplified Boolean expression for the function by grouping 1's (minterms) and incorporating don't-care conditions where applicable.

- **Deadline**: Tuesday, 21st October, 2025 (4:30 PM)
- Solve all the given questions on paper and submit on CUOnline before deadline.