

## Lecture 7 - Rajeer

CS 3810 - Computer Organization

MIPS Instruction Set

Reduced  
IS computer

more  
efficient  
in terms of  
processor  
usage

RISC  
e.g. MIPS  
architecture

CISC  
e.g. x86, ARM,  
IBM & Power

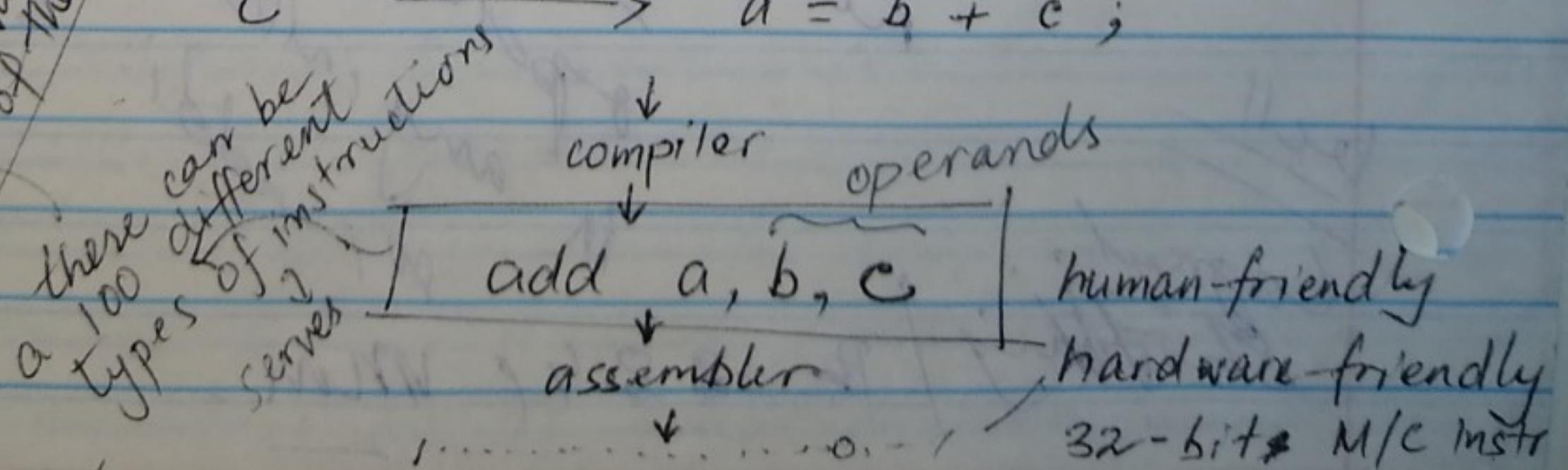
every  
computer  
comes  
with  
an  
ISA.  
①

What's the purpose of  
an IS?

The IS lies at the H/w S/w  
interface in a computer  
system.

Let's understand this  
through a simplistic  
example :-

$$C \rightarrow a = b + c ;$$



32 bits 32 b

4 Bytes 4B

usually

> 1 a line of C will converted to multiple lines of ~~it~~ instructions assembly instructions.

Skip slide p<sup>17</sup> on discussion of IS design  
slide # 18 - 21

> There may be different ways you may generate compiler assembly code, some may be better than others.

(use the term

temporary location)

slide # 5, # 6

[No discussion on floating point operations.]

$$f = (g + h) - (i + j)$$

Compiler is more likely to generate the code on

the left. (although temporaries are used)

[Due the design of the PL & compiler ... but it all depends]

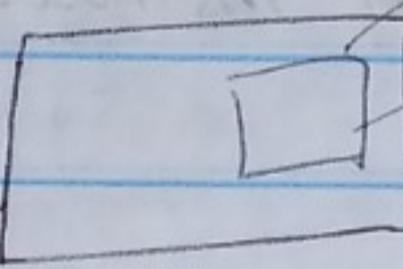
## Lecture #8

### Operand Locations

In x86 → 8 regs.

In MIPS → 32 regs.

Processor



Register file containing a set of registers (132)  
(each taking 32 bits of size 32 bits)

① In C all vars

are located

in the memory.

memory (8GB/

16GB/32GB)

Accessing memory is expensive.

To avoid repeatedly accessing memory, move values from memory to register addl, & sub

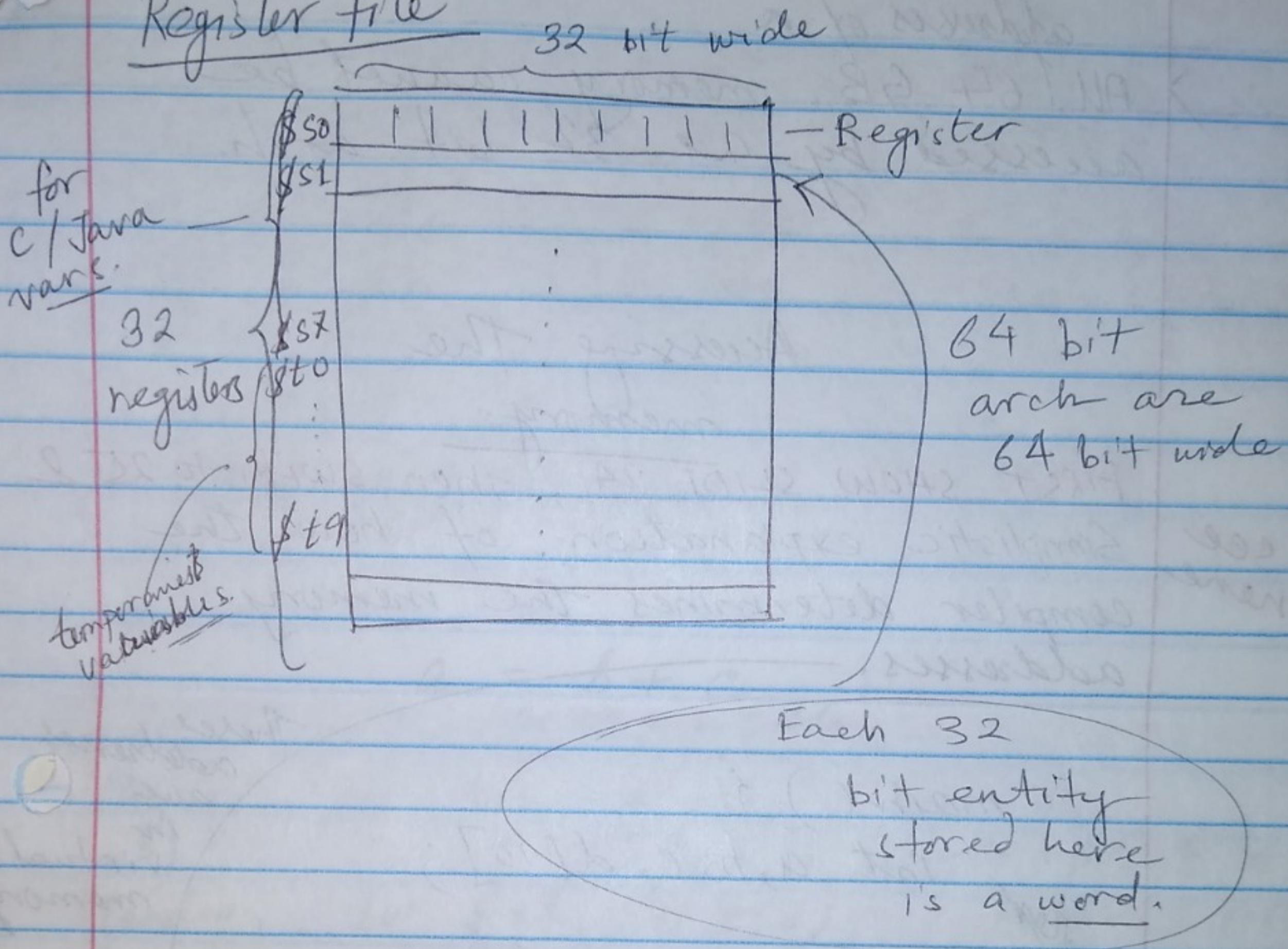
MIPS, in fact, instructions, in fact, require operands to be register values only.

So, registers are used as a scratchpad.

Note register file is much smaller than the memory.

~~Tradeoffs~~ less registers for more expensive data transfer, more registers means more expensive resources for the processor (real estate).

## Register file



## Question

> How many addresses can a 32-bit word encode / represent?

$$\begin{aligned}2^{32} &= 2^{10} \times 2^{10} \times 2^{10} \times 2^2 \\&= 1K \times 1K \times 1K \times 4 \\&\equiv 4 \text{ GB billion values}\end{aligned}$$

> If you assume each address to refer to a 4-byte entity & you have 4 billion unique addresses,

addresses of a

> All 164 GB memory cannot be accessed by a ~~32~~ 32 bit arch

# Accessing The memory.

see  
none

FIRST SHOW SLIDE 24, then switch to 25, & Simplistic explanation of how the compiler determines the memory addresses.

```
main() {  
    int a, b, c, d[10];
```

③ Computer creates a mapping (var : virtual address)

② each address refers to a particular byte of memory.

byte# 0 4 8  
(base addr)

starts at  
base  
of the rods

④ each int is 4 bytes

These addresses are in virtual memory

## Virtual memory

A piece of white paper with handwritten text. At the top, there are four vertical lines of varying heights, with a horizontal blue ink line above them. To the right of these lines, the word "Parrot" is written in cursive. Below the lines, the number "14" is circled in red ink, followed by the letters "GB".

- ⑤ compiler knows what's where in memory register from the table
- ⑥ compiler also know base address from register \$t0 (lets say its stored there)

Now, say we have,

$$a = b + c$$

the 1st available register

b) (loading)  $lw \$s0, 4(\$t0)$

c) (loading)  $lw \$s1, 8(\$t0)$

add  $\$s2, \$s0, \$s1$

→ add # to  
address in t0,  
& move the  
value to  
\$s0.

(corresponds  
to address  
a)

(store  
in a  
var mom)  $sw \$s2, 0(\$t0)$

## Immediate Operands

> Previously, we had, instructions like,

add \$s0, \$s1, \$s2

addi \$s0, \$s1, 1000

Say u want to add 1000 to \$s0

We use,

addi \$

There has to be at least 1 operand as a register

addi \$s0, \$zero, 1000