Slip No:1 EXAM SEAT NO:_____

2½/60

THE MAHARAJA SAYAJIRAO UNIVERSITY OF BARODA
FSBE III (Computer Science and Engineering)
CSE1503 COMPUTER ORGANIZATION

Date: 4/12/2023, Monday Time: 3:00to 6:00 Max Marks: 80

N.B.: Make suitable assumptions whenever required and mention clearly

SECTION I

Q.1 (a) Show the hardware implementation for the following statements. The registers are 4-bits in length: [4]

T_0 : A ← R0
T_1 : A ← R1
T_2 : A ← R2
T_3 : A ← R3

(b) Design an arithmetic circuit with one selection variable s and two data inputs A and B. When s = 0, the circuit performs the addition operation F = A + B. When s = 1, the circuit performs the increment operation F = A + 1. [5]

(c) Discuss the Microprogram Control method of control organization. [6]

Q.2 Attempt any FIVE [25]

(i) Discuss memory transfer operation in processor organization. Discus with suitable example.

(ii) Show the hardware implementation for addition of sign 2's complement numbers.

(iii) How a 4-bit status register can be designed?

(iv) Discuss the Sequence Register and Decoder method of control organization.

(v) Draw the flow chart for derivation of the algorithm of sign magnitude addition and subtraction with reference to hard wired control organization.

(vi) Draw formulation of a set of instructions for the computer with the formats for data and instruction words.

SECTION II

Q.3 (a) Write common execute cycle operations of a digital computer. [6]

(b) Discuss the method to handle simultaneous requests from I/o devices. [6]

Q.4 (a) Explain timing and control signals generated for a typical computer. [6]

OR

(a) Discuss organization of bit cells in a memory chip [6]

(b) Write a short note on flash memory. [6]

Q.5 (a) Discuss I/O interface for an input device. [6]

(b) Compare the temporal and data parallel processing methods briefly. [5]

(c) Discuss <u>any one</u> method to reduce Pipeline delay due to branch during instruction level parallel processing. [5]

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