Raven Memory Mapped I/O

Address (bytes)	Function	
0x00 00 00 00	Flash SPI / overlaid SRAM (1k words) start of memory block	
0x00 10 00 00	Reset vector	
0x01 00 00 00	Flash SPI start of memory block	Program to run starts here.
0x02 00 00 00	SPI master config bit 31 MEMIO enable (reset = 1) 0 = bit-bang mode bit 22 DDR enable bit 21 QSPI enable bit 20 CRM enable bits 19-16 Read latency cycles bits 11-8 I/O output enable bits (bit bang mode) bit 5 Chip select line (bit bang mode) bit 4 Serial clock line (bit bang mode) bits 3-0 Data bits (bit bang mode)	
0x02 00 00 04	UART clock divider select (system clock freq. / baud rate)	
0x02 00 00 08	UART data (returns 0xffffffff if receiver buffer is empty)	
0x03 00 00 00	GPIO input/output data (lower 16 bits)	16 bits of general-purpose digital
0x03 00 00 04	GPIO input enable (1 = input, 0 = output)	
0x03 00 00 08	GPIO pullup enable (1 = pullup, 0 = none)	
0x03 00 00 0c	GPIO pulldown enable (1 = pulldown, 0 = none)	
0x03 00 00 10	ADC0 enable (low bit 1 = enabled, 0 = disabled)	
0x03 00 00 14	ADC0 data (10 bits) read-only	
0x03 00 00 18	ADC0 done (low bit 1 = done, 0 = busy) read-only	
0x03 00 00 1c	ADC0 start conversion (low bit 1 = convert, 0 = reset)	
0x03 00 00 20	ADC0 clock source (low 2 bits) 0 = RC osc 1 = SPI SCK 2 = Xtal clock 3 = XCLK pin	ADC can be manually clocked via the SPI SCK or XCLK pins, or automatically clocked at the rate of the crystal or the RC oscillator.
0x03 00 00 24	ADC0 input source (low 2 bits) 0 = external pin 1 = VDD1V8 2 = DAC 3 = comparator P input	ADC normally reads the value of an external pin, but for testing can be set to read the internal values of the core power supply, DAC, or the comparator P input pin.
0x03 00 00 30	ADC1 enable (low bit 1 = enabled, 0 = disabled)	
0x03 00 00 34	ADC1 data (10 bits) read-only	
0x03 00 00 38	ADC1 done (low bit 1 = done, 0 = busy) read-only	
0x03 00 00 3c	ADC1 start conversion (low bit 1 = convert, 0 = reset)	
0x03 00 00 40	ADC1 clock source (low 2 bits) 0 = RC osc 1 = SPI SCK 2 = Xtal clock 3 = XCLK pin	
0x03 00 00 44	ADC1 input source (low 2 bits) 0 = external pin 1 = bandgap 2 = VDD3V3 3 = VSS	ADC can be calibrated by setting input to the 3.3V power supply and ground, and can be used to read the bandgap voltage.

Raven Memory Mapped I/O (continued)

Address (bytes)	Function	
0x03 00 00 50	DAC enable (low bit 1 = enabled, 0 = disabled)	
0x03 00 00 54	DAC value (10 bits)	
0x03 00 00 60	Comparator enable (low bit 1 = enabled, 0 = disabled)	
0x03 00 00 64	Comparator N input source (low 2 bits) 0 = external pin 1 = DAC 2 = bandgap 3 = VDD1V8	Comparator can have one input set to a known internal value, either the DAC output, the bandgap voltage, or the core supply voltage.
0x03 00 00 68	Comparator P input source (low 2 bits) 0 = external pin 1 = DAC 2 = bandgap 3 = VDD1V8	
0x03 00 00 6c	Comparator output destination (low 2 bits) 0 = none 1 = GPIO(0) 2 = GPIO(1) 3 = IRQ(9)	Comparator output can be seen directly on GPIO 0 or 1, or used to trigger CPU interrupt IRQ 9. GPIOs 0 and 1 cannot be used for general-purpose I/O when selected for comparator output.
0x03 00 00 70	RC oscillator enable (low bit, 1 = enabled, 0 = disabled)	
0x03 00 00 74	RC oscillator output destination (low 2 bits) 0 = none 1 = GPIO(2) 2 = GPIO(3) 3 = GPIO(4)	RC oscillator output can be passed directly to GPIO 2, 3, or 4. These cannot be used as general-purpose I/O when selected for RC oscillator output.
0x03 00 00 80	SPI configuration byte (low 8 bits) (read-only) Value currently fixed at zero	Most bits of the SPI register map are mirrored to memory locations and can be read by the CPU. These bits are read-only and cannot be modified.
0x03 00 00 84	SPI master enables (low 2 bits) (read-only) bit 0 = 1.8V regulator enable bit 1 = Crystal oscillator enable	
0x03 00 00 88	SPI PLL config (low 7 bits) (read-only) bit 0 = PLL current bias enable bit 1 = PLL VCO enable bit 2 = PLL CP enable bits 3-6 = PLL frequency trim	
0x03 00 00 8c	SPI manufacturer ID (low 12 bits) (= 0x0456) (read-only)	
0x03 00 00 90	SPI product ID (low 8 bits) (= 0x02) (read-only)	
0x03 00 00 94	SPI mask revision (low 4 bits) (= 0x00) (read-only)	
0x03 00 00 98	SPI PLL bypass mode (low bit) (read-only)	
0x03 00 00 a0	Crystal output destination (low 2 bits) 0 = none 1 = GPIO(5) 2 = GPIO(6) 3 = GPIO(7)	The crystal oscillator clock (before the PLL) can be coupled to any of GPIO pins 5, 6, or 7. These GPIOs cannot be used as general-purpose I/O when selected for crystal oscillator clock output.

Raven Memory Mapped I/O (continued)

Address (bytes)	Function	
0x03 00 00 a4	PLL clock output destination (low 2 bits) 0 = none 1 = GPIO(8) 2 = GPIO(9) 3 = GPIO(10)	The PLL clock (crystal oscillator clock multiplied up by 8 times) can be viewed on any of GPIO 8, 9, or 10. These GPIOs cannot be used as general-purpose I/O when selected for PLL clock output. It is unlikely that a full-speed (100MHz) clock will be able to toggle the GPIO at full swing, but a slower clock (5 MHz crystal / 40 MHz core clock) should have a proper output.
0x03 00 00 a8	Trap output destination (low 2 bits) 0 = none 1 = GPIO(11) 2 = GPIO(12) 3 = GPIO(13)	The CPU fault state (trap) can be viewed at GPIO 11, 12, or 13, as a way to monitor the CPU trap externally.
0x03 00 00 b0	IRQ 7 input source (low 2 bits) 0 = none 1 = GPIO(0) 2 = GPIO(1) 3 = GPIO(2)	The GPIO inputs can be used as IRQ event sources and passed to the CPU through IRQ channels 7 and 8. When used as IRQ sources, the corresponding GPIO channel must be first configured as an input.
0x03 00 00 b4	IRQ 8 input source (low 2 bits) 0 = none 1 = GPIO(3) 2 = GPIO(4) 3 = GPIO(5)	
0x03 00 00 c0	Analog output select (low bit) 0 = DAC 1 = bandgap	A single op-amp configured as an analog buffer can be selected to mirror the analog DAC output or the bandgap output.
0x03 00 00 c4	Analog output bias enable (low bit, 1 = enabled, 0 = disabled)	
0x03 00 00 c8	Analog output enable (low bit, 1 = enabled, 0 = disabled)	
0x03 00 00 d0	Bandgap enable (low bit, 1 = enabled, 0 = disabled)	
0x03 00 00 e0	Over-temperature alarm enable (low bit, 1 = enabled, 0 = disabled)	
0x03 00 00 e4	Over-temperature value (low bit, read-only)	
0x03 00 00 e8	Over-temperature destination (low 2 bits) 0 = none 1 = GPIO(14) 2 = GPIO(15) 3 = IRQ(10)	The over-temperature sensor triggers at 133 degrees C. It can be viewed at GPIO 14 or 15, or used as an IRQ source to the CPU.