Raven rev 0 SPI register definition: January 4, 2018

Register Address	msb 7	6	5	4	3	2	1	lsb 0	comments
0x00	SPI status and control								unused/undefined for now.
0x01	mask revision (= 0x0)				manufacturer_ID[11:8] (= 0x4)				read-only
0x02	manufacturer_ID[7:0] (currently undefined, = 0x56)								read-only
0x03	product_ID (= 0x02)								read-only
0x04	xtal osc. enable	1.8V regulator enable	PLL VCO enable	PLL CP enable	PLL trim[3:0]				default 0xf0
0x05	unused							PLL bypass	default 0x00
0x06	unused							CPU IRQ	default 0x00
0x07	unused							CPU reset	default 0x00
0x08	unused							CPU trap	read-only
0x09	undefined, use TBD								all undefined registers read 0x00

NOTES: These registers access values that are impossible to reach using the CPU.
(1) The crystal oscillator drives the CPU clock, so it cannot be turned on and off from inside the CPU. By default it is enabled.
(2) The 1.8V regulator supplies power to the CPU, so it cannot be disabled from the CPU. By default it is enabled.
(3) The PLL generates the high-speed clock from the low-speed crystal, acting as an 8x clock multiplier. By default it is enabled, and has zero trim.
(4) PLL bypass allows the CPU to completely bypass the crystal and PLL and be driven directly by a signal on the XCLK pin.
(5) CPU IRQ is a dedicated interrupt that can be applied to the CPU from the SPI for test purposes.
(6) CPU reset allows the CPU to be reset independently of the power-on-reset circuit.
(7) CPU trap is the fault signal from the CPU. If raised, then the CPU has encountered a bad instruction and has stopped.

Under normal working conditions, the SPI should not need to be accessed unless it is to adjust the clock speed of the CPU. All other functions are purely for test and debug.

All values in the SPI registers are exported to the CPU and can be viewed (read-only) in memory-mapped space (see the memory map documentation).

Errata (updated February 2019):

1. The bits of register 0x04 read as shown above but must be written in the reverse order of bits.

2. The PLL CP enable is nonfunctional as the corresponding output bit in the SPI block is hard-coded to force logic 1 always.

SPI protocol definition

All input is in groups of 8 bits. Each byte is input msb first.

Every command sequence requires one command word (8 bits) followed by one address word (8 bits) followed by one or more data words (8 bits each), according to the data transfer modes defined below.

Addresses are read in sequence from lower values to higher values.

Therefore groups of bits larger than 8 should be grouped such that the lowest bits are at the highest address. Any bits additional to an 8-bit boundary should be at the lowest address.

Data are captured from the register map in bytes on the falling edge of the last SCK before a data byte transfer. Multi-byte transfers should ensure that data do not change between byte reads.

CSB pin must be low to enable an SPI transmission. Data are clocked by pin SCK, with data valid on the rising edge of SCK. Output data are received on the SDO line. SDO is held high-impedance when CSB is high and at all times other than the transfer of data bits on a read command. SDO outputs become active on the falling edge of SCK, such that data are written and read on the same SCK rising edge.

After CSB is set low, the SPI is always in the "command" state, awaiting a new command.

The first transferred byte is the command word, interpreted according to Table 1 below.

Table 1: Command words

00000000	No operation
10000000	Write in streaming mode
01000000	Read in streaming mode
11000000	Simultaneous Read/Write in streaming mode
10nnn000	Write in n-byte mode (up to 7 bytes).
01nnn000	Read in n-byte mode (up to 7 bytes).
11nnn000	Simultaneous Read/Write in n-byte mode (up to 7 bytes).

All other words are reserved and act as no-operation if not defined by the SPI slave module.

The two basic modes of operation are "streaming mode" and "n-byte mode". In "streaming mode" operation, data are sent or received continuously, one byte at a time, with the internal address incrementing for each byte. Streaming mode operation continues until CSB is raised to end the transfer.

In "n-byte mode" operation, the number of bytes to be read and/or written is encoded in the command word, and may have a value from 1 to 7 (note that a value of zero implies streaming mode). After n bytes have been read and/or written, the SPI returns to waiting for the next command. No toggling of CSB is required to end the command or to initiate the following command.