FAULT TOLERANT DIGITAL SYSTEM

A PROJECT REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE AWARD OF THE DEGREE

OF

BACHELOR OF TECHNOLOGY

IN

[ELECTRONICS AND COMMUNICATION]

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CANDIDATE'S DECLARATION

I, (Arpit Garg, 2K20/EC/047) & Agam sharma(2K20/EC/16) student of B. Tech. (Electronics and Communication) hereby declare that the project Dissertation titled "FAULT TOLERANT DIGITAL SYSTEM" which is submitted by us to the Department of Electronics and Communication, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Bachelor of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: New Delhi

Date: APRIL 2023

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CERTIFICATE

I hereby certify that the project Dissertation titled “FAULT TOLERANT DIGITAL SYSTEM” which is submitted by Arpit garg (2K20/EC/047) [Electronics and Communication], Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of the Bachelor of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi
Date: April 2023

Professor Kriti Suneja
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ABSTRACT

This article presents a fault-tolerant digital system design and development strategy to improve the reliability of hardware devices. Based on the general conclusion that digital hardware plays an important role in the implementation of large control systems, a triple modular redundant (TMR) solution was proposed for development. For this purpose, the well-known 1-bit configuration has been expanded and expanded to control all digital control systems. Computer simulations show that hardware solutions meet all requirements and can be used for testing and implementation. Its design solutions and results are well suited for the development and expansion of various digital crime systems, from the security of servo applications to the reliability of communication drag and drop hardware.
A fail-safe system is a computer or software designed to continue to operate despite hardware or software failure or failure. Fault tolerance is achieved through many techniques and strategies that ensure that the system continues to function correctly or at least fails properly when a fault or malfunction occurs.

Two ways to create digital fault tolerant system:

Replication: This includes critical equipment such as systems, storage devices, or connections on the network so that if one fails, the other can operate without interrupting the process. . Replication can be implemented at various levels, including hardware replication, software replication, and data replication.

Check and Correction: Techniques such as error correction code (ECC) or checksums are used to identify and correct errors in data or instructions.
These techniques add additional information or instructions to identify and correct errors that may occur during transmission or processing.

In this paper we described how a triple modular circuit (TMR) could be made in order to avoid any single module fault if it occurs. Also, we have added one control module to check which module is faulty.

Overall, fault tolerance is an important consideration in critical systems, such as those used in aerospace, defense, transportation, telecommunications, and other industries where system failures can have severe consequences. Properly designed fault-tolerant digital systems can provide high availability, reliability, and resilience, ensuring continuous operation even in the presence of faults or failures.

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INTRODUCTION

According to a general rule definition, a fault-tolerant digital system is one that can continue to correctly perform its specified functions even in the presence of hardware faults and failures, or unwanted software errors. Shortly expressed, fault tolerance is a behavior that enables a digital system to achieve fault-tolerant operation. Therefore, the failure of a component in such a hardware system does not inhibit the system's general ability to continue its error-free operation and to execute its design-imposed functions. On the other hand, fault tolerance is also strongly linked with other additional requirements such as safety, reliability, maintainability, or testability.

However, modern digital control systems require increased safety and reliability in their utilization, leading to more and more complex automated systems, with sophisticated structures and hardware architectures. Despite the exponentially increasing technological improvements reached in microelectronics, faults remain unavoidable even in last generation hardware architectures, being the main cause of failures or damages. This shortcoming led researchers involved in digital systems implementation to pay more attention to the fault problem in microelectronics both from theoretical or experimental point of view. As a result, a huge amount of technical literature becomes available in the topic, with high quality solutions and international research results. This paper is focused mainly to particularize and extend a well-known hardware redundancy strategy to servo drive applications.

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of one or more faults within some of its components. If its operating quality decreases at all, the decrease is proportional to the severity of the failure, as compared to a naively designed system, in which even a small failure can cause total breakdown. Fault tolerance is particularly sought after in high-availability, mission-critical, or even life-critical systems. The ability of maintaining functionality when portions of a system break down is referred to as graceful degradation.

A fault-tolerant design enables a system to continue its intended operation, possibly at a reduced level, rather than failing completely, when some part of the system fails. The term is most commonly used to describe computer systems designed to continue more or less fully operational with, perhaps, a reduction in throughput or an increase in response time in the event of some partial failure. That is, the system as a whole is not stopped due to problems either in the hardware or the software. An example in another field is a motor vehicle designed so it will continue to be drivable if one of the tires is punctured, or a structure that is able to retain its integrity in the presence of damage due to causes such as fatigue, corrosion, manufacturing flaws, or impact.

TMR (TRIPLE MODULAR REDUNDANCY):

The great majority of researchers involved in fault-tolerant digital systems design and development generally agree that the physical replication of hardware is the most common form of hardware redundancy implementation. This means that very similar hardware units or modules execute the same functions and attributes in the fault-tolerant digital system, implementing the same tasks and control strategies. When one of those modules enters in the failure state, a fault-free unit is ready to take over the faulted ones functionality and attributes. Such kind of physical redundancy can be implemented with three main strategies: passive-, active-, and hybrid techniques. Briefly expressed, the passive hardware redundancy means that the fault-tolerance is achieved by masking the occurred fault, without requiring any intervention on the part of the system or operator. In fact, this technique is based on the idea to hide occurrence of faults rather than detect them. In this way the hardware faults are masked, and prevent faults from resulting in errors.

The active approach of hardware redundancy (often also called dynamic method) implements fault tolerance by detecting the existence of faults and performing the same certain actions to remove the faulty hardware from the considered digital system. Therefore, the active fault detection technique also uses fault location and fault recovery methods in an attempt to achieve fault tolerance. It means that the system can be physically reconfigured to tolerate faults. Obviously, hybrid techniques combine the advantages of both passive and active approaches. However, as the microelectronic components become smaller and less expensive, in a same way the expenses of replicated hardware decreases continuously and the hardware redundancy concept becomes more practical. Certainly, the most common form of passive hardware redundancy is the TMR. There three perfectly identical modules perform the same functions and tasks inside the digital system with a majority decision element determining the output of the system.

In this module, we'll be having three hardware modules of the same tasks, and one TMR voter which will be producing the majority input bit.

It can be accomplished with truth table below:

M1,M2,M3 are the respective outputs of three hardware modules:

M1	M2	M3	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

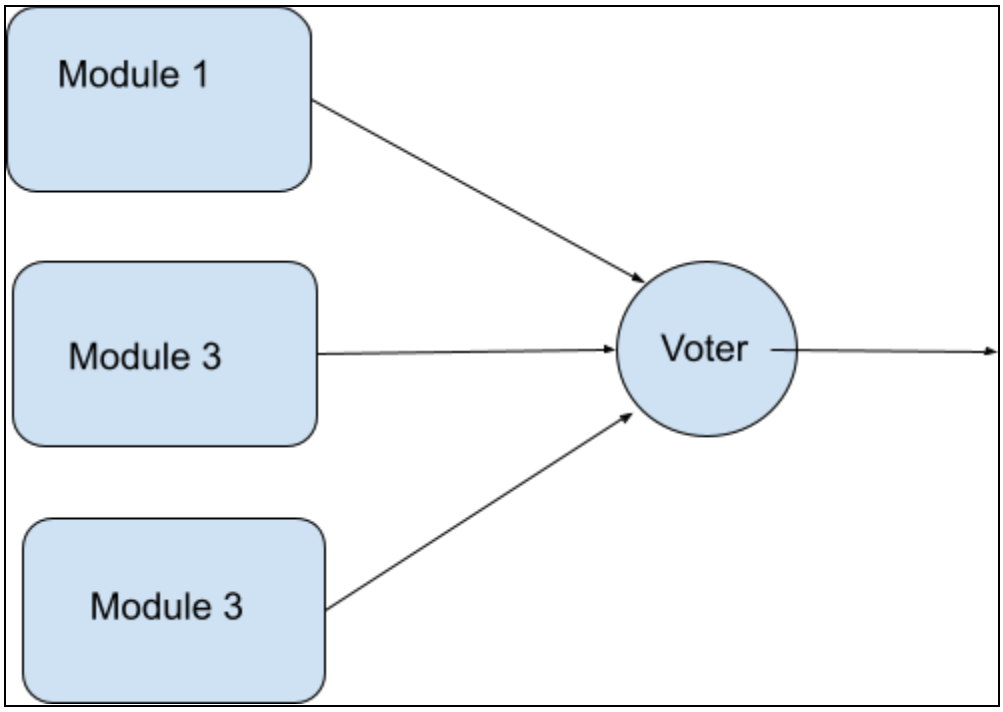


Fig 1: Schematic Diagram of TMR fault tolerant system

From the truth table of TMR functionality,

Output I(say)=M1M2 + M2M3 + M3M1;

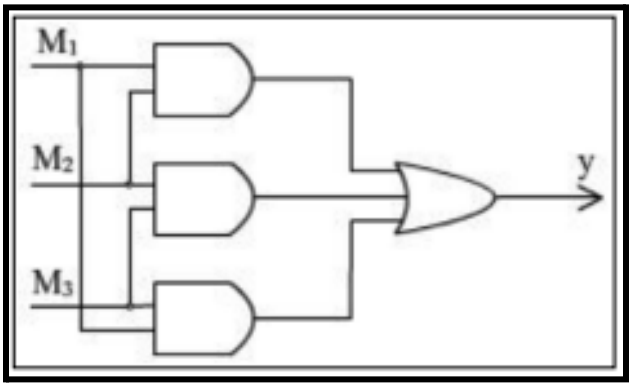


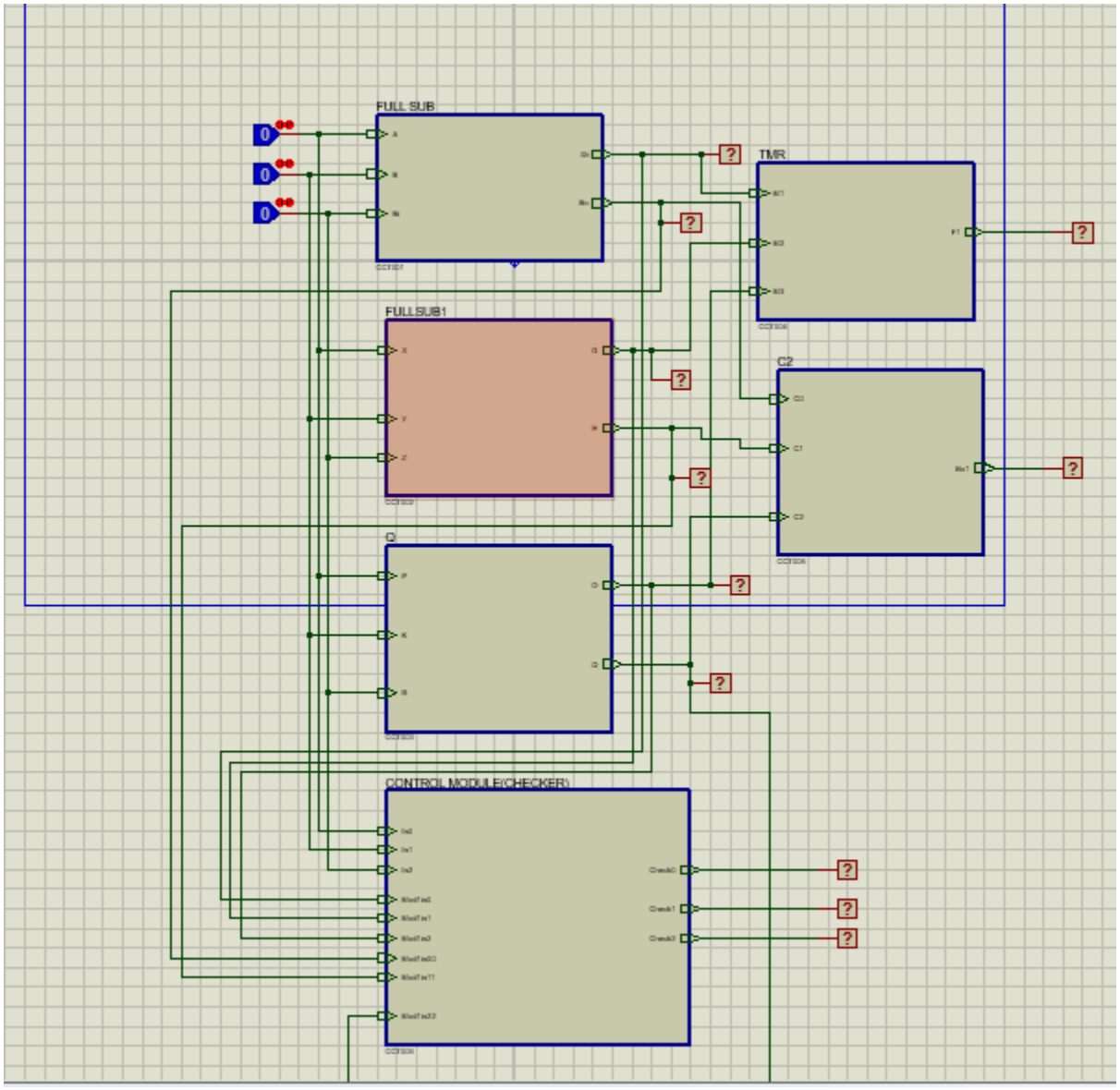
Fig 2 Gate level model of TMR for 1 bit

SIMULATION OF A FAULT-TOLERANT HARDWARE REDUNDANT SYSTEM USING TMR STRATEGY

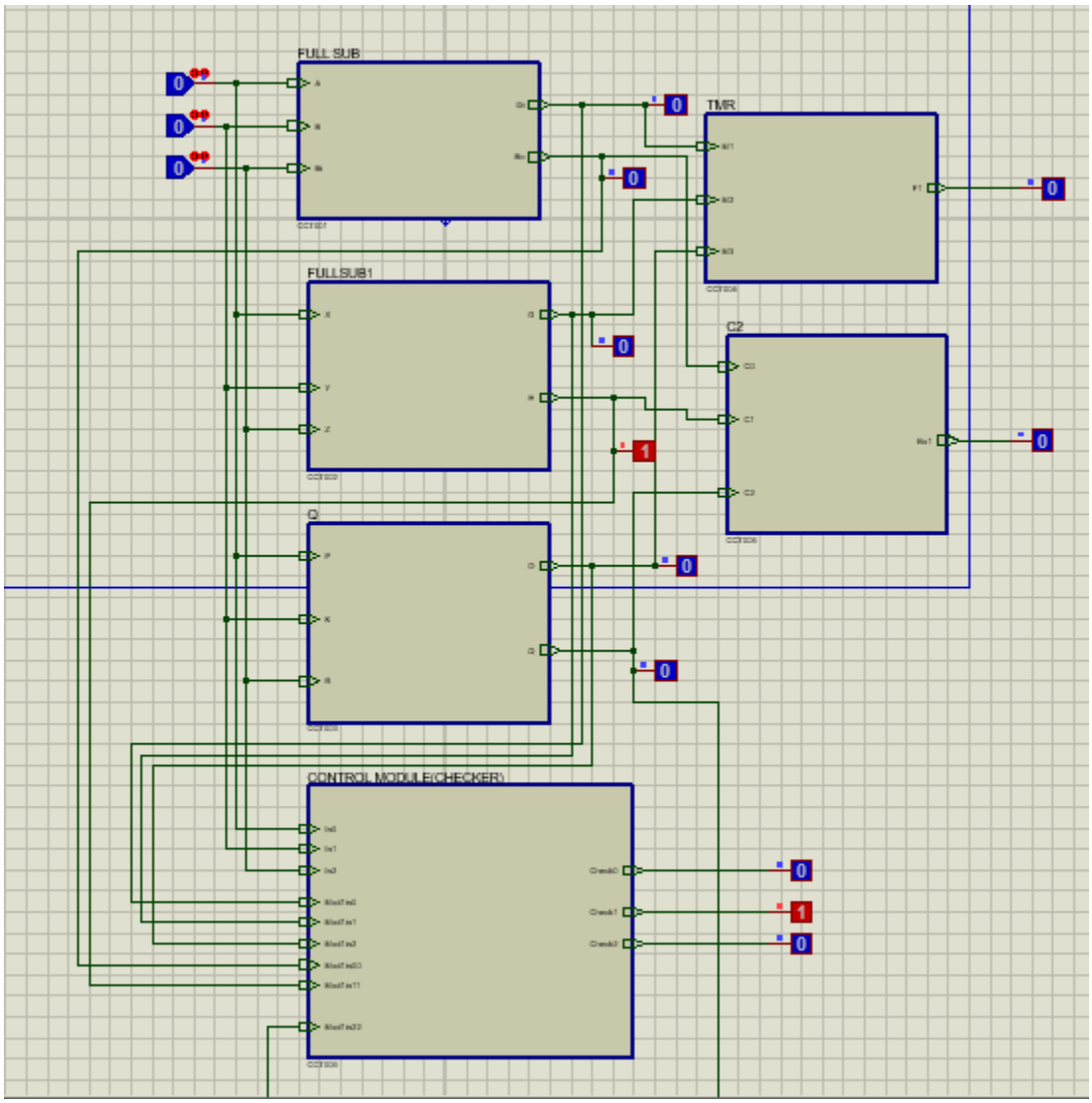
In the simulation portion, we have implemented a full subtractor circuit in proteus with TMR along with a control MODULE.

The theoretical approaches introduced in the previous paragraph represent an adequate background to modeling and simulating various fault-tolerant hardware structures using the TMR strategy. For a more convincing presentation, in a first step a hardware redundant system embedding analogue voter has been simulated in Matlab/Simulink software environment

The Schematic of the circuit in proteus:



Now in this circuit we have used a subcircuit library to use these full subtractor circuits as subcircuits. Now this control module will indicate which of the three hardware machines is faulty.



As we see three inputs are [0 0 0] and output should also be [0 0], this output is correct at the output itself but we see the second machine is associated with some fault to give carry as 1 instead of zero. It indicates some error and the control module identifies the machine by set check bits.

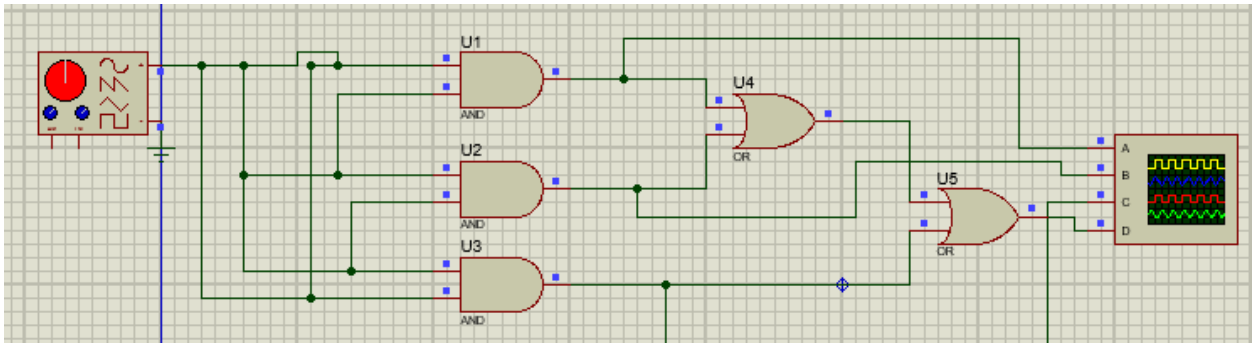
Also if somehow the say for input:

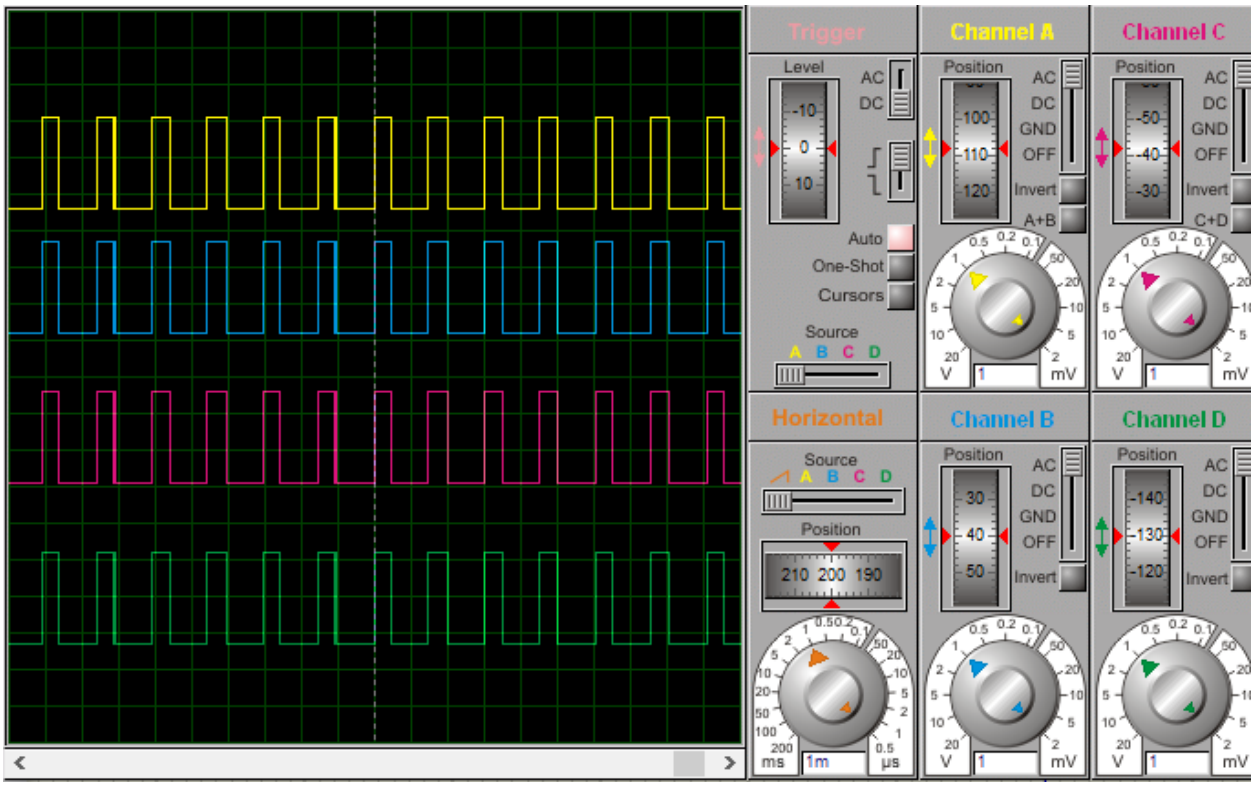
[0 1 0] output would be [1 1]

That means the fault is masked or redundant so CM will not indicate any error in that situation.

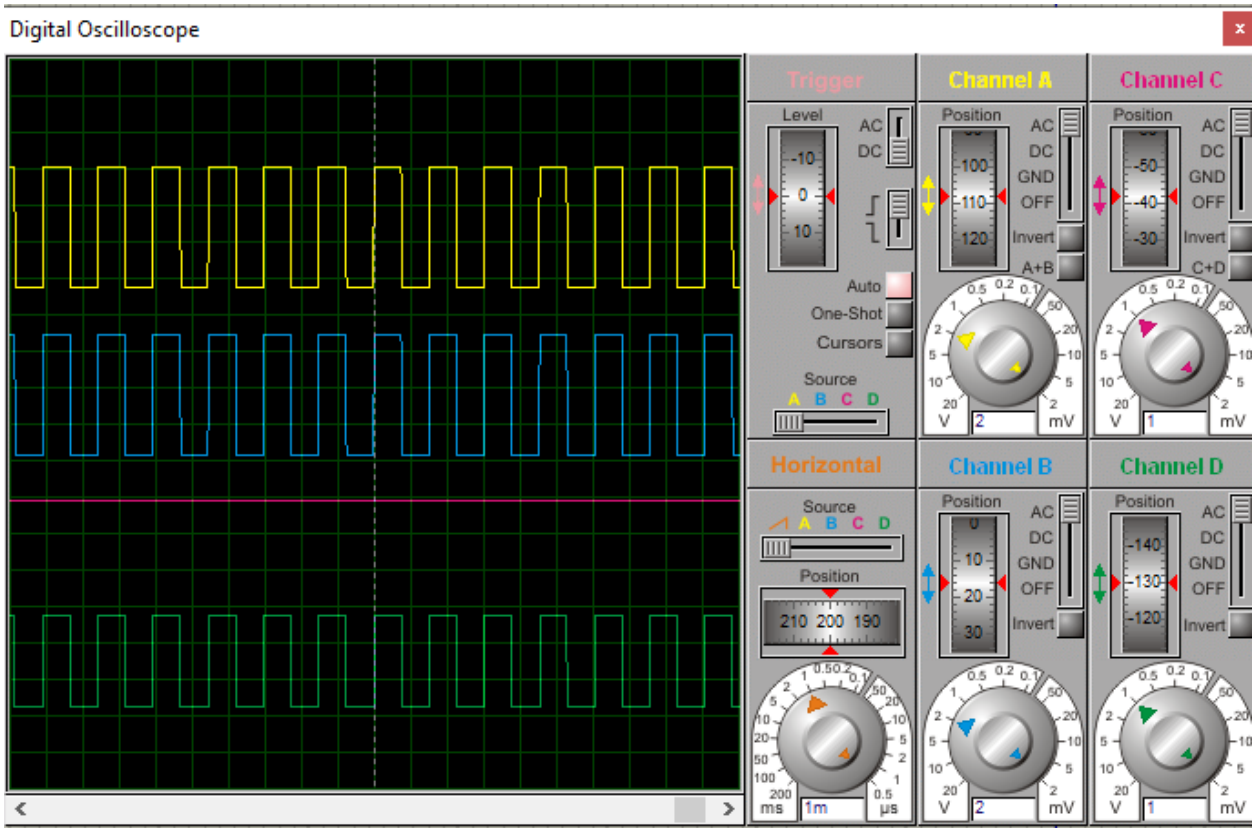
TESTING OF TMR WITH DIFFERENT SETS OF INPUTS

Suppose, we have square pulse input to the TMR module.





But if one of the input is associated with some fault then the output waveform would look like this


Digital Oscilloscope
Trigger
Level
AC
DC
Auto
One-Shot
Cursors
Source
A B C D
Channel A
Position
AC
DC
GND
OFF
Invert
A+B
V
mV
Channel C
C+D
Horizontal
210 200 190
ms
µs
Channel B
Channel D

CONCLUSION:

This article introduces the design and implementation concept of hardware failure management using the concept of triple mode redundancy. This use of low-voltage electronics protects against faults in the digital circuit and represents a very simple way to use inexpensive and reliable constituencies that operate according to most decisions. Extending the well-known 1-bit majority voter configuration to n-bit decision blocks seems to be a solution for the design and implementation of various digital crime systems such as So development and security servo application to be trusted. parallel and distributed computing hardware architecture.

Reliability and availability

Critical Infrastructure

Data Integrity and Protection

Safety and Security

Business Continuity

Compliance and Regulations

Cost Efficiency
In summary, fault-tolerant digital systems must provide reliability, availability, safety, security, data integrity, business continuity and control management across a wide variety of industries and businesses.

Use fail-safe strategies and techniques to reduce the risk and consequences of failure, and ensure critical systems remain operational and reliable even if they fail or fail.

REFERENCES

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Design of Various Adders Using Self Fault Detecting Full Adder J.Dhanasekar, Aarthy Balan, R. Akshara, P. Anusuya, S.Deepa

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