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SINGLE EVENT UPSETS IN NMOS MICROPROCESSORS*

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ABSTRACT

Three advanced 16-bit NMOS microprocessors have been observed to suffer single event upset at a rate varying between one upset for every 8 x 10^{10} to one for every 2 x 10^{12} n/cm^2-upset for cyclotron-produced neutrons with an average energy of 14 MeV. These rates are expected to vary, probably upward, with different types of programs. The errors are inferred to occur in memory-like components of the microprocessors. Many of the errors caused the microcomputer to cease normal operations. This is the first direct experimental verification of logic upsets in microprocessors from neutrons.

INTRODUCTION

Soft errors or single event upsets have become a topic of widespread interest for the vendors and users of microelectronics in the three years since the discovery of the effect. May and Woods[1] showed unequivocally that trace amounts of radioactive uranium and thorium in the IC packages decay and produce high energy alpha particles. These particles can deposit sufficient charge in the collection volume of a single dynamic RAM (random access memory) cell to cause that one cell to lose the information stored there. Guenzer et al[2] and Wyatt et al[3] showed that dynamic RAMs could be upset by alpha particles produced by nuclear reactions in silicon induced by high energy neutrons and protons thus establishing the need for the study of microcircuit upset susceptibilities to such radiations.

Despite the now voluminous literature on single event upset in memories there has been little reported work on upsets in logic circuits. Binder et al[4] attributed some observed upsets in a TTL flip-flop on an operational satellite to cosmic ray effects but it has been only recently that the effect has been verified experimentally[5]. Another recent experiment[6] reported upsets in a bipolar microprocessor as a result of heavy particle irradiation. The mechanisms for logic single event upset are expected to resemble those for memories. However in random logic, relatively few of the gates are being exercised at any one time so that the number of observed upsets will be much lower than in a memory in which the upsets are accumulated during the period between read-outs. Also in logic circuits, the emphasis of speed over low power causes a more ready availability of power supply current to neutralize deposited charge and thereby reduces upset susceptibility. Also an upset in a register is not necessarily propagated to the outside, i.e., observed, if the upset contents of that register are not used before that register is intentionally reset. The upset rate is expected to be dependent upon the details of the programming of the microcomputer. It is nonetheless expected at some degree of logic integration that significant numbers of single event upsets will be observed.

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The observation of upsets in microprocessors is important because of the operational difficulty such upsets will cause. Because upsets in memories occur in a predictable fashion on repetitive structures, the upsets can be detected and corrected with a relatively low overhead in time, cost and complexity by the use of error correction circuitry. However such techniques are not so readily available in logic. Also the operation of a logic device, particularly of the complexity of a microprocessor, in not as predictable as a memory, so that occasional checks for errors are not likely to remove randomly occuring errors before they become inextricably intertwined in the calculation or control of the calculation.

EXPERIMENTAL METHOD

The Motorola MC68000, the Zilog Z8002, and the Advanced Micro Devices AmZ8002A were chosen for the tests in order to ascertain if individual devices in commercially available random logic had become sufficiently small to be susceptible to single event upsets from large fluences of neutrons and protons. The MC68000 chip contains some 68,000 transistors[7], and when operating at 5 Volts, dissipates 0.625 Watts by actual measurement. If the switching energy is equated with the ratio of the power to the functional throughput, then at 8 MHz, the switching energy is about 1.1 pJ. This is equivalent to the energy deposited by ionization from a 7-MeV alpha particle. The above arguement is rough since not all gates switch during every clock cycle. On the other hand, some transistors are bound to have lower switching energies than the average.

The microprocessors were exposed at perpendicular incidence to neutrons in an irradiation procedure similar to previous memory tests[2]. However a different beam port was used which produced a lower flux, approximately 1.5 x 10^8 n/cm^2-s. The beam was well characterized[8,9] and was very uniform over a 5 cm square inside which the DIP package of the microprocessor was centered. The MC68000 acted as the processor for the Motorola MEX68KDM Design Module microcomputer board and was normally operated at 8 MHz. The 8002, the non-segmented version of the Z8000, acted as the processor for the Zilog Z8000 Development Module microcomputer board and was normally operated at 3.9 MHz. The microprocessor was connected to its computer board socket with a flat ribbon cable. For the 68000 a 15 cm cable was used since a 30 cm cable produced errors due to timing problems. A 90 cm cable was used for the 8002.

The programs for the 8002 and the 68000 were similar. A simple operation, such as an addition of two fixed numbers, was performed. The calculated result was then compared with the contents of another memory location known to contain the correct answer. If the two values disagreed, an error message was printed. If the values were in agreement, another type of calculation was performed and compared. The operations tested on the 8002 were addition, subtraction, multiplication and division, a total of 31 machine instructions. The operations tested on the 68000 were an unsigned multiply, a multiple register move, an add immediate, an AND immediate, an exclusive OR immediate and a sequence of memory to register moves, labelled "SEQ", for a total of 155 instructions. The arithmetic errors were confirmed by

printing out the calculated results. At the end of the sequence of calculations and compares, the program jumped back and the loop was repeated continually. The 8002 looped 65,536 times in about ten seconds when operated at 3.9 MHz. The 68000 operating at 8 MHz took about 10 seconds for 131,072 loops. At the end of a major loop, a simple message was printed to indicate that normal operation was continuing.

EXPERIMENTAL RESULTS

The results of the testing of the 8002 are given in Table I. The majority of the errors were in arithmetic operations. The higher susceptibility of the multiply and divide relative to addition and subtraction is understandable if the complexity of the machine instructions is taken into account. The addition and subtraction requires 4 clock cycles while the multiplication takes 70 and the division about 100. The incorrect answer sometimes differed by single bits from the correct values; two or three bit differences were common. Sometimes the bits were random. Other times a zero was the effective operand.

The miscellaneous errors includes cases such as error flags when the printed results indicate no error or incorrect printing. There were many errors which effectively removed control of the processor from the monitor program. In some of these an externally applied non-maskable interrupt would cause the computer to go through its initialization procedure and operation would proceed. In other cases, the program was apparently overwritten in the RAM. To restart, the test program needed to be reloaded into the RAM.

It is seen that the Z8002 and the AmZ8002 had upset susceptibilities differing by about an order of magnitude although they were nominally interchangeable parts. Inspection of the delidded chips revealed the two to be laid out the same. The two dice were the same size, 238 by 256 mils and had minimum feature sizes of 4 microns[10].

The different upset rates may possibly be explained by the different input currents, 249mA for the AmZ8002A and 143 mA for the Z8002 at V_{CC} = 5V. These measured values differ from the maximum electrical specification of I_{CC} = 300 mA for the 8002. If this power is proportionately distributed, their critical energies on the nodes of the AmZ8002 are 75% larger than on the Z8002 so that fewer of the reaction induced particles have sufficient energy to upset the device.

Table I. Number of upsets in two types of 8002 microprocessors according to failure mode.

Upset Type	Z8002	AMZ8002A
Program Stop, Restartable	9	1
Program Stop, Fatal	12	1
Addition	2	1
Subtraction	4	0
Multiplication	11	1
Division	22	3
Miscellaneous	5	2
Total	65	8
Total Fluence (n/cm^2)	2.4×10^{12}	3×10^{12}
Fluence/Upset (n/cm^2-upset)	3.7×10^{10}	3.8×10^{11}

Three different Z8002's were tested, each with a different date code. The sensitivities differed by up to a factor of 2.8. The AmZ8002's with the same date code differed in their upset sensitivity by a factor of two. Such variation was previously encountered in dynamic RAMs. It does not appear as though different types of failures were favored in one particular chip although the statistics are too poor to make a definitive statement.

Tests on the 8002 were run at two different clock frequencies, 2.46 MHz and 3.9 MHz on the same chips. For both the Z8002 and the AmZ8002, the observed upset rate per incident neutron was the same within the statistics, which were 6 events for the Z8002 and 4 events for the AmZ8002. At the higher clock frequency, there were 60% more operations. The absence of a corresponding increase in upset rate indicates that the upsets were not associated with the transitions in signal but were instead equally likely to occur at any time during which the microprocessor was in some state, that is, the upset was a static not a dynamic effect.

Table II: Upsets in MC68000 microprocessor according to failure mode and clock rate.

Clock Rate Date Code	Device #1 8 MHz 8047	Device #2 8 MHz 8111	Device #3 8 MHz 8111	Device #3 4 MHz 8111
Upset Type				
Program Stop, Fatal	8	5	5	6
Transient	0	1	0	0
ANDI	2	0	0	1
ADDI	0	1	1	0
EORI	1	0	2	0
MULU	1	0	0	1
MOVEM	0	0	1	0
"SEQ"	0	0	0	1
Total	12	7	9	9
Total Fluence (n/cm^2)	1.01×10^{12}	1.38×10^{12}	1.0×10^{12}	1.0×10^{12}
Upset Fluence (n/cm^2-upset)	8×10^{10}	2×10^{11}	1.4×10^{11}	1.1×10^{11}

The data for the MC68000 is given in Table II, which gives the number of upsets for various failure modes. The third through eighth entries correspond to the various machine operations which were calculated. Only 30% of the upsets were caught by the software testing. The rest of them, except for one faulty printed output, resulted from a change in the stored program. Two-thirds of these caused the processor to cease execution of the program. With an externally applied interrupt, control was returned to the PROM-stored monitor program but the program required rereading into RAM to reexecute. On one upset, use of the external interrupt did not cause the monitor to restart. However when the power was removed and then reapplied, operation of the microprocessor returned to normal. Such behavior is similar to non-fatal single event latchup as previously reported for memories[11]. However latchup is not normally expected in NMOS integrated circuits.

The variation of upset rates between devices, whether of the same or different date codes, is about a factor of two, not large in comparison with other soft error test results. A change in clock rate had little effect on the upset rate, just as in the case of the 8002's. The upset rate, measured in upsets per neutron for the 68000 fell between the Z8002 and the AmZ8002. However if the higher speed and complexity of the 68000 is taken into account, the 68000 is at least as good as any of the 8002's.

MODELING

The test results from neutron irradiation of NMOS integrated circuit can be used as an estimate for the maximum alpha particle sensitivity of a silicon device. The yield of reaction products is given by

$$Y = \text{Flux} \cdot N \cdot \text{Sigma} \cdot \text{Area} \cdot \text{Length} \qquad (1)$$

where Flux is the neutron flux, N is the atomic density of the target material, Sigma is the reaction cross section, Area is the target area and Length is a characteristic distance. The reaction cross section for the production of alpha particles is approximately[2] 100 mb. The characteristic length will be taken to be 3.7 microns. This length is the range of a 1.1 MeV alpha particle which can ionize 300,000 electrons, the reported critical charge[12] on the 68000, and which also is near the minimum feature sizes in the microprocessors. Equation (1) then predicts an alpha particle yield over the area and within a characteristic depth of 1.9×10^{-6} of the neutron flux. Thus an upset fluence of 10^{11} n/cm^2-upset corresponds to an alpha production of 1.9×10^5 alpha/cm^2. If a typical alpha emission rate from a package of 3.8 alpha/cm^2.hr is used, an upset is expected every 50,000 hours or 5.7 years. Even this calculation overestimates the problem since possible shielding by inert material may reduce the alpha particle flux and some of the experimentally observed neutron induced upsets may result from reaction products other than the alpha particle.

The manufacturer has performed[12] a soft error analysis on the MC68000 which is much simpler than the model of Bradford[13] but is more appropriate for the uncertain parameters. Any single event effects are assumed to be associated with the 2% of the die area, i.e., 0.02×44.6 mm^2 = 0.892 mm^2, that contains dynamic cells. The charge stored on the node is given as 750,000 electrons and the critical-charge as 300,000 electrons which corresponds to 1.1 MeV of ionization energy in silicon. If the simple model of Equation (1) is used, then an alpha particle yield is predicted of one alpha per 6×10^7 n/cm^2. This value differs significantly from the experimentally determined upset rate of about 10^{11} n/cm^2-upset. It is known that not every alpha particle will upset a cell it is crossing. In 16K dynamic RAMs the efficiency of alpha particles in producing upset is 1.5% according to May and Wood[1] or 0.1% according to Campbell et al[14]. The difference may be the different memory types tested. A further factor contributing to this difference is that the program was inefficient at testing register upset since data was left in single registers only for one or two instructions at a time so that both the effective area and the duty cycle are reduced.

Instead of using the total sensitive die area, an estimate can be made based on only one 16-bit word being sensitive at any one time. The dynamic storage elements are 33 microns long and are described as resembling bit lines so that a width of 6 micron will be estimated. The total area of the sensitive 16-bit word is then 3168 micron^2. If this reduced area is used in Equation (1), then the production rate of alpha particles capable of causing upset is calculated at one per 1.6×10^{10} n/cm^2 much closer to agreement with the experimental value of about 10^{11} n/cm^2-upset. The considerations of alpha efficiency factors and of multiple sensitive words are countervailing and will probably have the effect of somewhat increasing the calculated value. If these arguments are correct, then the upset rates measured here are expected to be lower than those expected with a microprocessor that is operating close to its capacity with all its registers being used and relied upon.

CONCLUSIONS

Two types of 16-bit NMOS microprocessors from three manufacturers have been tested for upset from neutrons and have been found to suffer between one upset per 8×10^{10} to one per 2×10^{12} n/cm^2. It is expected that the upset rates will increase when the testing program more fully utilizes the register storage capacity.

The microprocessors from one vendor were found to be significantly less upset prone than nearly identical microprocessors from another vendor. It is postulated that the higher supply current on the less susceptible one implies a higher critical charge.

None of the microprocessors showed a significant variation of upset rate with clock frequency. The upsets are therefore not dynamic, i.e., associated with electrical transistions, but are static, i.e., are caused by events after the circuit has reached a steady state. Upset rates were consistent with a model of upsets occuring in a few registers. This implies that the use of a microprocessor whose speed and complexity is greater than necessary will result in higher than necessary upset rates.

Variations of upset rates between devices of the same or different date codes were no larger than expected and comparable to values measured on RAMs.

Upsets were observed to be of various types. Some resulted in incorrect calculated values; the larger fraction caused the computer to cease execution of its program. This latter type of error creates doubt that a purely software approach can be used to correct for microprocessor errors. The microprocessor in many cases would not be able to retain control.

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