Fault-Tolerant ICs: The Reliability of TMR Yield-Enhanced ICs

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Reader Aids—
Purpose: Tutorial
Special Math needed for derivations: Probability and statistics
Special math needed to use results: Same
Results useful to: IC designers, system designers, reliability analysts

Abstract—**The use of triple modular redundancy (TMR) for reliability enhancement is well known. This paper presents a simple method for predicting the reliability of integrated circuits (ICs) which use TMR for yield enhancement. A simple yield-model is included as it is necessary to factor in the effect of consumption of redundancy paths due to wafer fabrication defects. TMR implementation is briefly discussed as well.**

1. INTRODUCTION

In integrated circuit (IC) design, the use of active *on-chip* redundancy to achieve economic yields particularly for very large scale integration (VLSI) and wafer scale integration (WSI) circuits is becoming more attractive. The application of triple modular redundancy (TMR) to enhance system reliability is well documented [1-4]. The application of redundancy schemes for system reliability enhancement is explored in [5-6]. One commercial application of active on-chip error correction (redundancy) for reliability enhancement of electrically-erasable read-only memory (EEPROM) devides is described in [7]. A general overview of redundancy schemes to enhance yield is provided in [8]. Methods for implementing redundancy schemes are discussed in [9-10]. TMR can be effectively used on-chip to enhance both IC yield and reliability. However, portions of the on-chip redundancy will be consumed by defects in the wafer fabrication process and will not be available to provide protection against failures (defects) in field use. This paper provides a simple mathematical model which expresses the reliability of the IC, taking wafer fabrication defects into account.

Assumptions

1. The time to failure distribution for each copy of all triples is exponential.
2. Each copy of every logic triple has two states, operating and failed.
3. States of the logic triples are mutually statistically-independent.

Notation

Y	yield of entire IC in wafer fabrication
Y_s	yield of serial (non-redundant) portion of the IC
Y_3	yield of TMR portion of the IC
P_i, Q_i	yield of one copy of logic triple i; $P_i = \exp(-A_iD)$, $Q_i \equiv 1 - P_i$.
A_i	area of one copy of logic triple i
D	defect surface density
$R(t)$	reliability of entire IC
$R_s(t)$	reliability of serial (non-redundant) portion of IC $= \exp(-\lambda_1 t)$
$R_3(t)$	reliability of TMR portion if IC
R_i, F_i	reliability of one copy of logic triple i; $R_i = \exp(-\lambda_{2i}t)$, $F_i \equiv 1 - R_i$
t	operating time (field use)
λ_1	field failure rate of serial portion of IC
λ_{2i}	field failure rate of one copy of logic triple i
I_i	defect-free triple indicator = 1, for logic triple i when defect-free from fabrication, = 0 otherwise
MTTF	mean time to failure for entire IC
T	service life of IC in field application

2. IMPLEMENTATION OF TMR

TMR can be implemented by partitioning the IC logic into modules which are then triplicated, each triple being terminated by a majority gate or voter. The majority voter can be triplicated as well. The actual circuit layout depends upon the IC technology employed. This allows one defective copy in any triple with the defective copy being outvoted by the remaining two good copies. In triples where two defective copies exist, with one copy stuck-low and one copy stuck-high, a correct vote occurs with the non-defective copy breaking the tie. This compensation of defects is well treated in [4] and is not discussed further here. Also, there may be many portions of logic which are connected to more than one terminating majority voter. Where extensive logic-sharing has occurred, it is easy to count some portions of the logic more than once since such a portion terminates at more than one majority voter. Analysis of this logic sharing is well treated in [2] and also is not discussed further here. In all cases where one defective copy exists, it is masked by TMR so that the correct logic function occurs. It is important to provide adequate diagnostic circuitry to determine the location of all defective copies even though they are adequately masked by the majority voters. A hybrid approach can be used whereby two defective copies of a triple can be tolerated by providing a fusible link (within each copy) that can be programmed, thus

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enabling the third non-defective copy to operate alone unimpeded by the defective copies. Also, to enhance field reliability, it is necessary to fuse out two copies of any triple where only one copy is defective.

3. YIELD

The yield of the TMR yield enhanced IC can be expressed as:

$$Y = Y_s Y_3,$$

where Y_s accounts for catastrophic defects which are not masked by TMR. Y_3 accounts for those defects that are either masked by TMR or recovered by fuse programming:

$$Y_3 = \prod_{i=1}^{k} (P_i^3 + 3Q_i P_i^2 + 3P_i Q_i^2). \quad (1)$$

This is simply a product of those terms of the multinomial distribution for the probability of 0, 1, 2 defects occurring in each logic triple. The simplified Poisson equation, $P = \exp(-A_i D)$, is used for single-copy yield. Other yield models exist which are more detailed taking physical attributes of the IC technology [9] and defect clustering [10] into account.

4. RELIABILITY

The reliability of the TMR yield-enhanced IC is:

$$R(t) = R_s(t)\, R_3(t).$$

where $R_s(t)$ includes catastrophic failures not masked by TMR. $R_3(t)$ includes those defects masked by TMR:

$$R_3(t) = \prod_{i=1}^{k} [I_i(R_i^3 + 3F_i R_i^2) + (1 - I_i)R_i]. \quad (2)$$

The first term in (2) is simply the expansion of those terms of the multinomial distribution for the probability of 0, 1 failure occurring for those logic triples which are defect-free from wafer fabrication. The second term in (2) concerns those logic triples which have exhausted the redundancy due to wafer fabrication defects with two copies disabled by fuse programming which enables the third non-defective copy to operate alone.

$$\text{MTTF} = \int_0^\infty R(t)\, dt. \quad (3)$$

This can be a difficult integral to solve. If one considers only MTTF over the service life of the IC then —

$$\text{MTTF} = \int_0^T R(t)dt/[1 - R(T)]. \quad (4)$$

This may still be difficult to solve. An approximation to simplify this integral which performs well for $R(T) > 0.5$ is:

$$\text{MTTF} \approx (T/2)\,[1 + R(T)]/[1 - R(T)], \quad R(T) > 0.5. \quad (5)$$

If $R(T) > 0.9$, an even simpler approximation is:

$$\text{MTTF} \approx T/[1 - R(T)], \quad R(T) > 0.9. \quad (6)$$

These approximations are studied in [11]. A Markov model for reliability which also takes wafer-fabrication defects into account is provided in [10]. The simpler model provided here may be preferred because of the simpler computation.

5. ACKNOWLEDGMENT

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REFERENCES

[1] J. A. Abraham, "Reliability analysis of digital systems protected by massive redundancy", *PhD Thesis*, Department of Electrical Engineering, Stanford University, 1984 Aug.

[2] J. A. Abraham, D. P. Siewiorek, "An algorithm for the accurate reliability evaluation of triple modular redundancy networks", *IEEE Trans. Computers*, vol C-23, 1974 Jul, pp 682-692.

[3] D. P. Siewiorek, R. S. Swarz, *The Theory and Practice of Reliable System Design*, Digital Press, 1982.

[4] D. P. Siewiorek, "Reliability modelling of compensating module failures in majority voted redundancy", *IEEE Trans. Computers*, vol C-24, no. 5, 1975 May, pp 525-533.

[5] F. P. Mathur, P. T. deSousa, "Reliability models of NMR systems", *IEEE Trans. Reliability*, vol R-24, 1975 Jun, pp 108-113.

[6] F. P. Mathur, P. T. deSousa, "Reliability modeling and analysis of General Modular Redundant Systems", *IEEE Trans. Reliability*, vol R-24, 1975 Dec, pp 296-299.

[7] T. Haifley, "Endurance of EEPROMs utilizing on-chip error correction", *IEEE Trans. Reliability*, see pp 000-000 in this issue.

[8] W. R. Moore, "A review of fault tolerant techniques for the enhancement of integrated circuit yield", *Proc. IEEE*, vol 74, 1986 May, pp 684-698.

[9] T. E. Mangir, "Sources of failures and yield improvement for VLSI and restructurable interconnects for RVLSI and WSI: Part I-sources of failures and yield improvement for VLSI", *Proc. IEEE*, vol 72, 1984 Jun, pp 690-709.

[10] I. Koren, D. K. Pradhan, "Yield and performance enhancement through redundancy in VSLI and WSI multiprocessor systems", *Proc. IEEE*, vol 74, 1986 May, pp 699-711.

[11] A. K. Bhatt, T. O. Haifley, "Evaluating MTBF approximations for simple maintained systems", *IEEE Trans. Reliability*, vol R-35, 1986 Jun, pp 137-138.

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