Partitioning Triple Modular Redundancy for Single Event Upset Mitigation in FPGA

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Abstract—**The mitigation of single event upsets (SEUs) in field programmable gate arrays (FPGAs) is an increasingly important subject as both the static random access memory (SRAM) cells and the logic circuits in FPGAs are susceptible to SEUs. Among all SEU mitigation techniques, the triple modular redundancy (TMR) has become the most common practice because of its straightforward implementation and reliable results. The methodologies to perform partitioning TMR insertion to reduce SEUs in the FPGA logic paths are presented in this paper. It is proved that the maximal probability of two simultaneous errors decreases dramatically with the number of logic partitions in the TMR designs. It is reduced from 66.67% for minimum logic partition to 4.44% for maximum logic partition for the test circuit. The results presented in this paper suggest that there is a tradeoff between the number of logic partitions and combination property of TMR designs. For ground-based systems such as nuclear power plant (NPPs), where the overhead is insignificant, especially compared to reliability requirements, the maximum partition can be the best. While in space applications where area is at a premium, the optimal logic partition should be the medium partition.**

Keywords-single event upset (SEU); field programmable gate array (FPGA); triple modular redundancy (TMR); logic partition

I. INTRODUCTION

Field programmable gate arrays (FPGAs) are being increasingly utilized in many applications due to their low cost, re-configurability and low design turn-around time. But both the static random access memory (SRAM) cells and the logic circuits in FPGAs are susceptible to single event effects (SEEs).

Toyota's massive recall of more than 9 million vehicles worldwide for its sticky gas pedals causing sudden and unintended acceleration, beginning in November last year, might be caused by cosmic rays. That is reported in LiveScience by Chow on March 26, 2010.

The space radiation environment is composed of various particles generated by solar and galactic activity. The particles can be classified as two major types: (1) charged particles such as electrons, protons, Helium nuclei and heavy ions, and (2) electromagnetic radiation (photons), which can be x-rays or gamma rays. Of the various radiation types, protons are the most abundant charged particles in deep space. Within the Earth's atmosphere and at the ground level, neutrons are the most frequent cause of single event upsets (SEUs).

When a charged particle strikes a sensitive node in FPGAs, as a drain in an off state transistor, it generates a transient current pulse that can turn the gate of the opposite transistor on. The effect can produce an inversion in the stored value (in other words, a bit flip in the memory cell). This is called a SEU and it is the main consequence of the transient effect. When a charged particle hits a combinational logic block, it also generates a transient current pulse. This phenomenon is called a single event transient (SET). SETs may propagate and upset the overall logic state if sampled by latches, or may dissipate. Another mode in which a SEE can cause disruption of electrical systems is by turning on the complementary metal oxide semiconductor (CMOS) parasitic bipolar transistors between well and substrate—inducing a latch-up [1]. The only difference between single event latch-up (SEL) and electrical latch-up is that the current injection that turns on the parasitic bipolar elements is provided by the radiation instead of an electrical overvoltage. SEL can be debilitating since its occurrence may necessitate a full chip power cycling to remove the condition, and in some cases can cause permanent damage.

Several SEU mitigation techniques have been proposed in literature to avoid the effects of faults in FPGA. These techniques cover a wide range of methods which can be classified as fabrication process-based, design-based and recovery techniques [2]. Among all SEU mitigation techniques, triple modular redundancy (TMR) has become the most common practice because of its straightforward implementation and reliable results. However, TMR introduces significant overhead because of its full hardware redundancy. For ground-based systems such as nuclear power plant (NPP), the overhead is insignificant, especially compared to reliability requirements. While in space applications where area and power are at a premium, circuit designers are constantly looking for ways to increase the efficiency of TMR, for example, using selective TMR. Samudrala et al. proposed the Selective TMR method which uses signal probabilities to find the SEU-sensitive sub-circuits of a design [3]. Chandrasekhar *et al*. proposed a modification to this method which operates on look-up tables (LUTs) rather than logic gates [4]. Almukhaizim *et al*. proposed another technique based on a selective addition

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of redundant wires that can prevent the distorted signal from propagating to an output or a storage element [5].

This paper is organized as follows. In section II, a proposed partitioning TMR methodology is presented, and formulae for calculating the maximal probability of two simultaneous soft errors are derived. In Section III, a dot product of two vectors circuit is used as a case study. Four different versions of this design were implemented and compared in terms of area, performance, and sensitivity to soft error. Section IV is the conclusions.

II. PROPOSED PARTITIONING TMR METHODOLOGY

The TMR mitigation scheme uses three identical logic circuits performing the same task in parallel with corresponding outputs being compared through majority voters. This is demonstrated in Fig. 1. The use of three redundant majority voters eliminates these as single point of failure and provides the triple logic path outputs which are connected to the triple redundant inputs of the next module. The majority voters perform a very important task in the TMR approach. When a soft error occurs in TMR designs, the majority voters could remove the upset effects from the final output. But when there are two soft errors appearing simultaneously in two distinct redundant logic block, such as redundant logic 0 and redundant logic 2 in Fig. 1, the majority voters may not vote the correct output.

A more efficient TMR approach is the logic partitioning TMR, as shown in Fig. 2, where the TMR design is partitioned into n logic blocks and each of them has three identical logic parts performing the same task in tandem with corresponding outputs being compared through majority voters. When two soft errors occur in this TMR design simultaneously, there can be three different situations according to their positions, i.e., upsets '*a*', '*b*' and '*c*', as presented in Fig. 2. Apparently, both upsets '*b*' and upset '*c*' will not provoke any faults in the final output, because of the function of majority voters. Only upset '*a*', which has two simultaneous soft errors appearing separately in the two distinct redundant logic parts that are voted by the same voter, could affect the final output, because the TMR approach may not vote the correct output in this case.

In order to reduce the probability that upsets affect two distinct redundant logic blocks driving the same voter, we can partition the redundant logic parts into smaller logic blocks with majority voters. Then two simultaneous soft errors from distinct redundant logic blocks can be voted by different majority voters, just like the upset '*c*' in Fig. 2. Apparently the upset '*c*' cannot cause an error in the TMR output, which increases the robustness of the TMR.

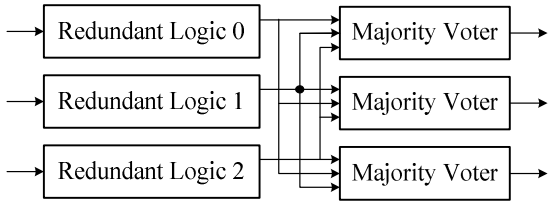

Figure 1. Triple modular redundancy with three majority voters.

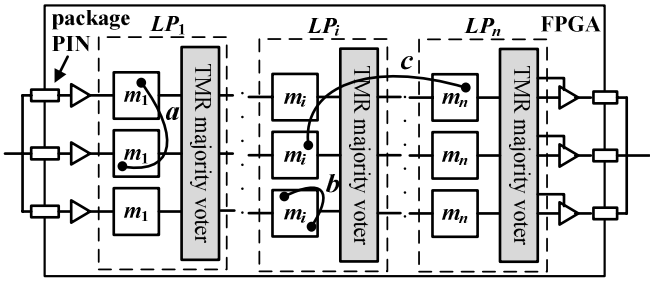

Figure 2. TMR scheme with logic partitions in FPGA.

However, small size block partitions require large number of majority voters that may be too costly in terms of area and performance. Alternatively, placing majority voters only at the last output increases the probability of faults. Calculation of the probability of error can help to identify the best amount of TMR majority voters in the final design, taking all factors into consideration, such as area, performance and sensitivity to soft error [6].

In Fig. 2, the symbol LP_i represents the i^{th} logic partition and m_i represents the number of sensitive nodes of each redundant logic part in the i^{th} logic partition (LP_i). Obviously, the number of sensitive nodes of each redundant logic block in the same logic partition is equal.

As discussed above, when the TMR design encounters upset '*a*', which has two simultaneous errors appearing separately in the two distinct redundant logic blocks that are voted by the same voter, as depicted in Fig. 2, majority voters will become invalid. The maximal probability of this kind of error $[P_{\text{E}}]_{\max}$ can be expressed as

$$[P_{\text{E}}]_{\max} = \frac{\binom{3}{2}\binom{m_1}{1}\binom{m_1}{1} + \binom{3}{2}\binom{m_2}{1}\binom{m_2}{1} + \ldots + \binom{3}{2}\binom{m_n}{1}\binom{m_n}{1}}{\binom{(3m_1 + 3m_2 + \ldots + 3m_n)}{2}} \quad (1)$$

where n is the number of logic partitions in the whole TMR design and m_i represents the number of sensitive nodes in each redundant logic block of the i^{th} logic partition. The function $\binom{p}{q}$ denotes the number of q-combinations from a given set S of p elements and can be computed by the formula

$$\binom{p}{q} = \frac{p!}{q!(p-q)!}. \quad (2)$$

In (1), the numerator is the probability of two simultaneous soft errors which appear separately in two distinct redundant logic blocks in the same logic partition; and the denominator is the combination of two simultaneous soft errors appearing in arbitrary regions of the whole TMR design. Then, (1) can be computed and simplified as

$$[P_{\mathrm{E}}]_{\max}=\frac{3m_1^2+3m_2^2+\ldots+3m_n^2}{(3m_1+3m_2+\ldots+3m_n)[(3m_1+3m_2+\ldots+3m_n)-1]/2}$$

$$=\left(3\sum_{i=1}^{n}m_i^2\right)\Bigg/\left[\left(3\sum_{i=1}^{n}m_i\right)\left(3\sum_{i=1}^{n}m_i-1\right)/2\right]. \quad (3)$$

Generally, there is $3\sum_{i=1}^{n}m_i \gg 1$ and then (3) can be expressed approximately as

$$[P_{\mathrm{E}}]_{\max}\cong\frac{2}{3}\left(\sum_{i=1}^{n}m_i^2\right)\Bigg/\left(\sum_{i=1}^{n}m_i\right)^2. \quad (4)$$

All m_i are positive, so there is $\left(\sum_{i=1}^{n}m_i^2\right)\le\left(\sum_{i=1}^{n}m_i\right)^2$ and when n=1, the maximum value of $[P_{\mathrm{E}}]_{\max}$ is 2/3.

If all m_i are equal, i.e., every redundant logic block has the same number of sensitive nodes, then (4) can be expressed as

$$[P_{\mathrm{E}}]_{\max}\cong\frac{2}{3n}. \quad (5)$$

Equation (5) indicates that $[P_{\mathrm{E}}]_{\max}$ only depends on n and is inversely proportional to n, while has nothing to do with m_i if and only if all m_i are equal. That means the maximal number of logic partitions is accompanied with minimal probability of two simultaneous errors in TMR designs when each redundant logic block in every logic partition has the same number of sensitive nodes by chance.

III. Test Circuit Analysis

A dot product of two vectors circuit, which is a heavily used tool in physics, is used as the test case to evaluate the robustness of the TMR design with different logic partitions. The dot product of two vectors $\mathbf{a}=[a_1, a_2, \ldots, a_n]$ and $\mathbf{b}=[b_1, b_2, \ldots, b_n]$ is defined as

$$\mathbf{a}\bullet\mathbf{b}=\sum_{i=1}^{n}a_ib_i=a_1b_1+a_2b_2+\ldots+a_nb_n \quad (6)$$

where n is the dimension of the vectors. In dimension 8, i.e., n=8, the circuit consists of eight separate multipliers, whose outputs are summed to give a final result, as presented in Fig. 3, where a_i and b_i are both 4 bit digital signals.

Four different versions of this design were implemented in Xilinx ISE design tool. The first is the standard one with no SEU mitigation at all, i.e., no utilization of TMR (see Fig. 3).

The second implementation, named "TMR_max", is protected by TMR using the maximum logic partition. In this case, each combinational logic component must be triplicated and majority voters were inserted in their outputs, as presented in Fig. 4. Obviously, there is a total of 15 logic partitions, i.e., n=15, and every logic partition has a majority voter that actually denotes three redundant majority voters. If all multipliers and adders are taken as the minimal logic components, SEUs could only affect those nets between them. If we suppose all buses are single bit digital signals, then each redundant logic part in each logic partition has 3 sensitive nodes (2 input nodes and 1 output node). That means m_i=3 (i=1, 2, ... , 15). According to (5), the maximal probability of two simultaneous errors of this maximum logic partitioning TMR design can be calculated approximately as $[P_{\mathrm{E}}]_{\max}$=4.44%.

The third version "TMR_med" is a TMR design with medium logic partition, as shown in Fig. 5. Every three logic components (two multipliers and one adder or just three adders) are grouped into a logic partition, and they are triplicated and then followed by a TMR voter. There is a total of 5 logic

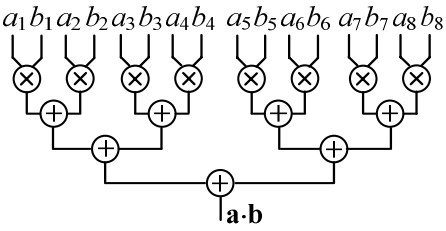

Figure 3. Dot product of two 8-dimension vectors.

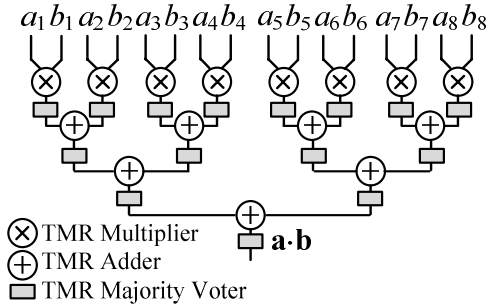

Figure 4. TMR_max: TMR design with maximum logic partition.

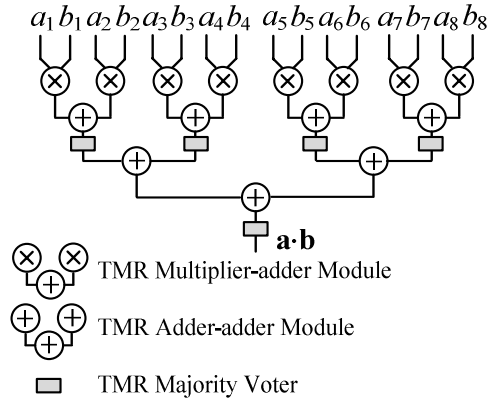

Figure 5. TMR_med: TMR design with medium logic partition.

partitions, i.e., n=5. All multipliers and adders are also taken as the minimal logic components, and all of the buses are taken as 1 bit, so each redundant logic part in each logic partition has 7 sensitive nodes (4 input nodes, 2 internal nodes and 1 output node). That means m_i=7 (i=1, 2, ... , 5). The maximal probability of two simultaneous errors in this case can be demonstrated as $[P_E]_{max}$=13.33%.

The fourth version "TMR_min" is the simplest TMR implementation, where the whole circuit is triplicated and only one TMR majority voter is placed in the outermost output, as presented in Fig. 6. There is just one logic partition, i.e., n=1. That means any two simultaneous errors appearing in any two distinct redundant logic part of three can cause a final fault. Then we can get $[P_E]_{max}$=66.67%.

The main characteristics of these four implemented versions of the dot product of two vectors circuit is compared in Table I, where the "resource utilization" reports the number of the FPGA input and output blocks (IOBs) and slices that those circuits use. Even the maximum TMR logic partitioning design only occupies 839 slices and that is actually a very small portion of area for a FPGA device. Therefore, each of these designs can be mapped into a single FPGA chip. As a matter of fact, it is not the low area utilization but the high pin count of TMR designs (3 times as much as the standard design, i.e., no TMR design) that is the determinant for choosing the destination FPGA device.

A first conclusion drawn from Table I is that all three TMR designs present greater than 3 times area overheads because of their full hardware redundancy, and with the number of logic partitions increasing, area overhead increases substantially. The standard design without TMR mitigation only uses 202 slices,

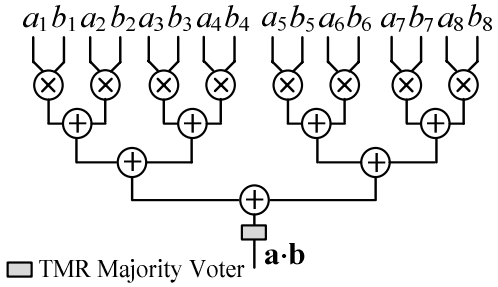

Figure 6. TMR_min: TMR design with minimum logic partition.

TABLE I. COMPARISON BETWEEN DIFFERENT TMR PARTITIONING DESIGNS

Designs	Resource Utilization		Estimated Performance (MHz)	$[P_E]_{max}$ (%)
	# *IOBs*	# *Slices*		
No TMR	75	202	53.9	100
TMR_min	225	623	39.6	66.67
TMR_med	225	683	47.9	13.33
TMR_max	225	839	43.4	4.44

but the number of slices that the minimum, medium and maximum logic partitioning TMR designs use 3.08 times, 3.38 times, and 4.15 times that, respectively. The area overheads of the maximum logic partitioning TMR design even exceed 400%, and that cannot be accepted in space applications where area is at a premium.

Second, the estimated $[P_E]_{max}$ decreases dramatically with the number of logic partitions in the TMR designs. It is reduced from 66.67% for minimum logic partition to 4.44% for maximum logic partition for the test circuit. It is worth nothing that those data are just the estimated maximal probability of two simultaneous errors for the case study circuits, the actual probability will be much less than that. Of course, even the maximum logic partitioning design still cannot completely avoid the possibility of two simultaneous upsets. Apparently, the minimum logic partitioning TMR design cannot apply to any fields because of its high probability of two simultaneous errors.

IV. CONCLUSIONS

Results show that there is a tradeoff between the number of logic partitions (or between the number of voters) and combination property of TMR designs. Placing voters just at the final output is not sufficient to avoid errors. A combination of TMR and additional voters (such as medium partition and maximum partition) may ensure high levels of reliability in the case study circuits. Although the insertion of extra voters can improve the TMR reliability, it does not avoid completely the chance of two simultaneous upsets appearing in two distinct redundant logic parts that are voted by two different voters.

For ground-based systems such as NPPs, where the overhead is insignificant, especially compared to reliability requirements, maximum logic partition is preferred. While in space applications, where area and power are at a premium, medium logic partitioning TMR approach can be the optimal option.

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