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A Highly Reliable Fault-Tolerant Microprocessor System for Industrial Process Control

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***Abstract*—In this paper,researches have been carried out on how to improve microprocessor system reliability using fault - tolerant theory and technique. A kind of Three Module Redundant fault-tolerant microprocessor system structure has been proposed which can mask both transient fault and permanent fault. This fault-tolerant system has been realized in hardware using microcontroller 80c552 as core. The fault-tolerant system consists of three functional modules with the same hardware and a fault-masking network. the three modules are alternative in function and the fault-masking network is used for fault-detection and fault-tolerance. The fault-tolerant microprocessor system has been applied into Robotization Automatic Drilling Machine and as the main control unit which executes key tasks.Its powerful fault-toerance and high reliability have been proved by practice.**

I. INTRODUCTION

At present microprocessor system have been widely used in industrial process control, especially in sequence control. Sequence control plays an important role in industrial process automatic control.It means that with the site input signals the executing mechanism of production equipment and production process works according to scheduled program so as to realize automatic control based on switch valnesmainly. The task is on the basis of technological requirements, logic algorithm, sequence operation and time set and count rule.Fig.1 gives on example of basic form of a typical sequence control system .

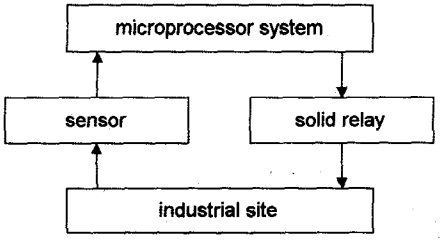

Fig.1 A diagram of sequence control system

The practical application environment of the microprocessor system used for sequence control is industrial site.The condition there is very bad,such as large temperature change,high humidity, serious dust,the influence of vibration and shock,oritical electromagnetic disturbance,bad power supply. All these factors lead to the increase of fault probability of the microprocessor system.Therefore the research on microprocessor system with high reliability used for sequence control becomes an important task inevitably which has to be solved urgently.

Generally speaking, there are two ways to enhance the reliability of microprocessor system.The first one is to avoid fault, i.e.by correct design,optimal choosing of component and device,careful arrangement of circuit, cautious install and reinforcement and other methods to prevent the microprocessor system from the fault.But it is practically impossible to realize the goal absolutely.Fault-avoiding methods can only reduce the probability of fault.When the fault occurs, the system will be in failure.This limits the ability of applying fault-avoiding methods for enhancing the reliability of microprocessor system.The second way is fault-tolerance.It means that the system can still finish a group of program or algorithm, also we can say that the program can't be broken or changed by the fault in the system and the executing result will have no wrong even when some hardware or software faults take place.The basic idea of fault-tolerance is careful design of system structure and fault masking through redundant technique like additional resource.The fault-tolerant method is better than the fault-avoiding method in view of the increase of the reliability of the microprocessor systems. So the study of increasing the reliability of microprocessor system will be carried out by using fault-tolerant theory and method.

II.SYSTEM STRUCTURE OF FAULT-TOLERANT MICROPROCESSOR SYSTEM

According to Fig.1, if the microprocessor system is thought as a black box and only the input and output value considered, the system for sequence control can be expressed as Fig.2.

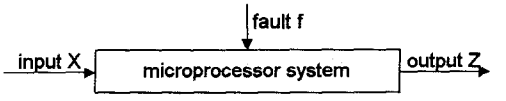

Fig.2 Schematic diagram of sequence control system

In Fig.2,X is the input vector of the system;
Z is the output rector of the system;
f is the fault of the system .

As for the microprocessor system, the output vector Z can be looked as the function of input vector X and fault f,that is: $Z=Z(X,f)$.

If the output of the system can be expressed as $Z=Z(X,\lambda)$

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when there is no fault, the normal output set of the system can be expressed as : $S=\{Z(X,\lambda)|X\in Q\}$,
and fault output set : $S_f=\{Z(X,f)|X\in Q\}$,
where Q stands for normal input set of the microprocessor system.

If all the function and task of the microprocessor system can be undertaken by a circuit module m, Fig.2 can be expressed as Fig.3.

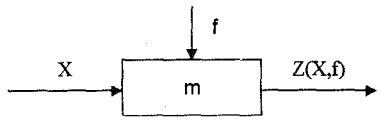

Fig.3 Schematic diagram of sequence control system.

In order to equip the system with fault-tolerant ability, a fault-masking network p must be added to the output level of module m so as to correct Z(X,f) as Z(X, λ) as showing in Fig.4.

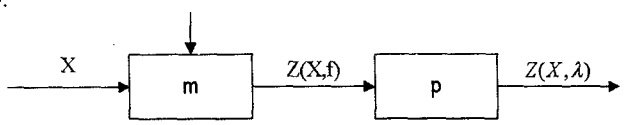

Fig.4 Schematic diagram of sequence control system with fault-masking network

If add extra information, named redundant information and make the fault output set S_f of module m satisfy the following relations:
$Z(X,f)\in S_f$ and $Z(X,\lambda)\in S_f$,
from S_f the fault-masking network can choose Z(X,λ) and mask Z(X,f) so as to realize fault-tolerance .

Because of the parallel output of module m, any fault of m may lead to many bit errors in output. Therefore redundant information must be added for every output bit of module m. This can be achieved only through adding (N-1) modules the same as m to form N times module redundant system simply called NMR system. It is shown in Fig.5.

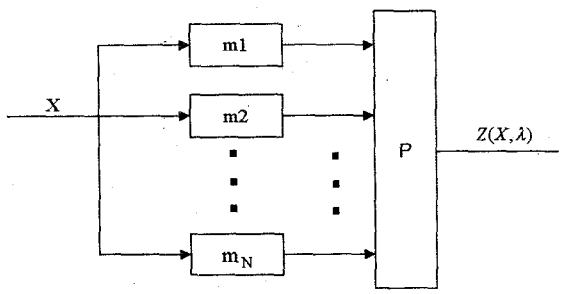

Fig.5 N times module redundant sequence control system

In Fig.5, if the N modules work and produce output simultaneously, the same output bit of each module will form an odd-oven check code $S_f=\{(00...0),(11...1)\}$ (in Fig.5 only showing one output bit of the modules). Then the fault-masking network can choose Z(X,λ) and realize fault-correcting only by comparing and decoding for S_f.

Considering hardware realization and the ratio of performance to price, in this paper we choose N=3, that is to say, use 3 modules to form Three Module Redundant(TMR) system so as to realize fault-tolerant function of microprocessor system. The fault-masking network p adopts XOR gate for comparison function and 3-state gate for choosing function. Such fault-tolerant microprocessor system structure is shown in Fig.6.

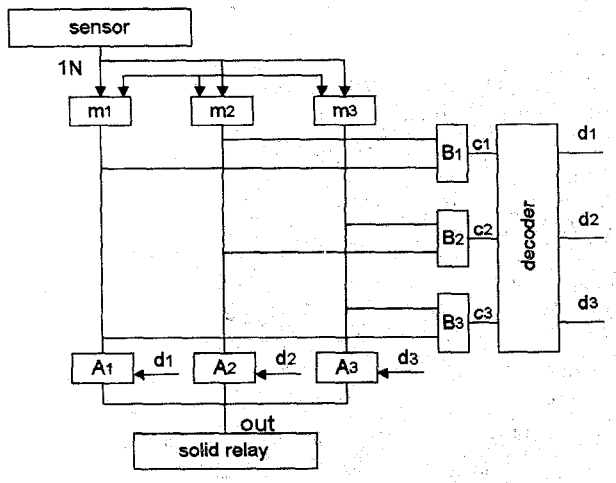

Fig. 6 Fault-tolerant microprocessor system structure I

In Fig.6,

· m_1, m_2 and m_3 are 3 functional modules with the same hardware structure. Each of them can finish all sequence control task alone if there is m fault. Among the 3 modules m_1, m_2 and m_3, only one of them is unnecessary for normal operation and the other two belong to redundant hardware resource. The 3 modules form a TMR system.

· m_1, m_2 and m_3 are interconnected so that data can transmitted within them to fulfill fault-detection.

· Information from sensor is transmitted into the 3 modules simultaneously in order to guarantee their input identical.

· A_1, A_2 and A_3 are 3 3-state gates, and B_1, B_2 and B_3 3 XOR gates. XOR gate is used for comparison Fault-masking network consists of decoder, XOR gate and 3-state gate together.

Further discuss on the design of decoder will be made in the following. At first the decoding principles for decoder are given here.

· If the output of two XOR gates connected with module m is "0", i.e. compared result is the same, the output of decoder will be $d_i=1, d_j=0 (i\neq j)$. Module m_i is chosen to control the solid relay.

· If there is no such module whose two connected XOR gates produce output "0", the module whose one connected XOR

gate output "0" will be chosen to control solid relay.

· If none of the XOR gates produces output "0, the functional module will be decided without restriction. Based on the 3 principles, table 1 shows the corresponding relations between input and output value of the decoder.

Table I .The corresponding relations between input and output of the decoder

module state			output of XOR gate			output of decoder		
m_1	m_2	m_3	c_1	c_2	c_3	d_1	d_2	d_3
0	0	0	0	0	0	0	1	0
0	0	1	0	1	1	0	1	0
0	1	0	1	1	0	0	0	1
0	1	1	1	1	1	0	0	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	1	0	0	1
1	1	0	1	1	1	0	0	1
1	1	1	1	1	1	0	0	1

Note:

If the state of module m_1, m_2 and m_3 is "0", the module is in good condition (without fault).

If the state of module m_1, m_2 and m_3 is "1", the module is wrong.

From Table I we can see

· The output of decoder if always "0", that is to say, the 3-state gate A, from m_1 to system output is always close. Therefore the output of m_1 has no influence on solid relay. Then the 3-state gate A_1 can be omitted.

· The output of decoder is only related to the output C_1 of XOR gate, that is when C_1=0, the output of decoder is $d_1d_2d_3 = 010$, when C_1=1, $d_1d_2d_3 = 001$, and has nothing to do with C_2 and C_3. Then XOR gates B_2 and B_3 can be omitted.

· Among the 8 composing states of the decoder, d_2 and d_3 always satisfy $d_2 = d_3$. Then the decoding function can be replaced by a D-trigger.

In one word, the structure of fault-tolerant microprocessor system can be simplified from Fig.6 to Fig.7.

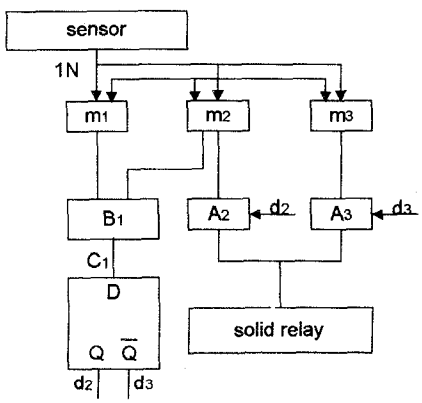

Fig. 7 Fault-tolerant microprocessor system structure II

III. HARDWARE REALIZATION OF FAULT-TOLERANT MICROPROCESSOR SYSTEM

The fault-tolerant microprocessor system shown in Fig.7 can be expressed as Fig.8 in hardware module.

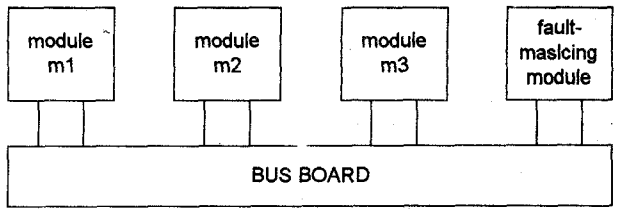

Fig. 8 Hardware structure of fault-tolerant microprocessor system

In Fig.8.

· Module m_1, m_2 and m_3 are the same in hardware. The CPU adapts microcontroller 80c552 made in Philips Company. The communication among them is undertaken by I^2C series bus of 80c552. In addition, there are analog input circuit, switch input circuit and switch output circuit in the modules.

· The components in fault-masking module are XOR gate, 3-state gate and D-trigger only. The XOR gate is 74HC86, 3-state gate 74LS126. In view of low consumption of power 74HC126 should be chosen as 3-state gate. But the 3-state gate is used to drive sold relay directly. Its input part is a light-electricity coupled circuit, which needs 5mA driving current. The maximum inject current of 74HÇ126 is 5mA and 74LS126 ia 8mA. So 74LS126 is fit for this job.

IV. CONCLUSION

In this paper ,as for the high reliability requirement for microprocessor system in industrial process control, based on fault-tolerant theory and technique, a kind of three Module Redundant fault-tolerant microprocessor system structure has been proposed which can mask both transient and permanent fault. This fault-tolerant system has been realized in hardware using microcontroller 80C552 as core. This system has been applied into Robotization Automatic Drilling Machine and as the main control unit which executes key tasks. Industrial tests show that the fault-tolerant microprocessor system can stand the tests of various bad condition in industrial site and has high reliability.

V. REFERENCES

[1]Anderson, T and P.Lee, *Fault-tolerant Principles and Practice*, Pratice-Hall International, 1981.

[2]Serlin.O, "Fault-tolerant Systems in Commercial Applications", Computer, 1984, 19-30.