Radiation tolerance studies using fault injection on the Readout Control FPGA design of the ALICE TPC detector

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Radiation tolerance studies using fault injection on the Readout Control FPGA design of the ALICE TPC detector

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ABSTRACT: Single Event Upsets (SEUs) are a major concern for the TPC Readout Control Unit (RCU) of the ALICE experiment. A SEU is defined as a radiation related bit-flip in a memory cell, and a SEU in the onboard SRAM based FPGA of the RCU may lead to corrupted data or, even worse, a system malfunction. The latter situation will affect the operation of the ALICE detector since it causes a premature end of data taking. Active partial reconfiguration is utilized in a dedicated reconfiguration solution on the RCU, and this makes it possible to implement fault injection. Fault injection means inserting bit flips in the configuration memory of the FPGA in a controlled laboratory environment. This paper presents the results of the fault injection study and shows how this result can be combined with SEU measurements to estimate the functional failure rate as a function of luminosity.

KEYWORDS: Radiation damage to electronic components; Digital electronic circuits; Front-end electronics for detector readout

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1 Introduction

When designing electronic systems that are intended to be used in a radiation environment it is important to know how this kind of environment affects the electronics. In modern electronics, errors that arise as a result of the exposure to radiation are commonly referred to as Single Event Effects (SEE) [1]. SEE are categorized into hard errors and soft errors. Hard errors are considered to be fatal for the electronic device as they lead to short circuits, while soft errors can in most cases be corrected. One type of soft error is a Single Event Upset (SEU). A SEU is caused by a nuclear reaction between an incoming particle and the silicon in the integrated circuit. The reaction is inducing charge in a memory cell with the result that the bit stored in the cell changes value.

SEUs are the main concern for designs using Static Random Access Memory (SRAM) based Field Programmable Gate Arrays (FPGAs) in radiation environments [1], as SEUs might lead to functional failures in the algorithm programmed in the device. An example of a system using commercially graded SRAM based FPGAs is the readout electronics for the Time Projection Chamber (TPC) [2] in the ALICE (A Large Ion Collider Experiment) [3] detector.

Using radiation beams to qualify an FPGA design is both expensive and cumbersome. The fault injection solution presented in this paper runs on actual TPC readout electronics, giving a lab setup that in architecture and functionality is identical to real operation. This implies that the fault

injection test is both a realistic and cost effective way to analyze the impact of the SEUs on the performance of the ALICE detector.

The potential radiation related errors that can be detected during the fault injection test are divided into two categories: (1) reliability faults, and (2) performance faults. Reliability faults cause a system failure that eventually will stop the data taking for the ALICE experiment. These faults have by far the highest severity level since they affect the operation and stability of the complete ALICE detector. Performance faults are faults that affect the data quality. Two subtypes of performance faults are recognized: (1) Loss of data, and (2) corrupted data. These faults are considered to have a lower severity level than the reliability faults since they only have an impact on the actual sub-system where the error occurred.

2 System description

The main physics goal of ALICE [3] is to study the Quark Gluon Plasma, a state of matter that existed for a very short time after the Big Bang. To study this, the Large Hadron Collider (LHC) accelerates lead ions close to the speed of light. The lead ions are collided in the center of the ALICE detector, and simulations of the radiation environment where the ALICE TPC readout electronics is located estimates a flux level of a few hundred high energy hadrons/cm^2/s (E_{kin} >20 MeV) [4]. This is about 10^5 times larger than the terrestrial neutron flux [5].

2.1 ALICE detector

The ALICE detector has an onion-like structure where most of the sub-detectors are stacked radially in layers from the interaction point outwards. The TPC detector [2] is one of the innermost sub-detectors and is a gas filled barrel with 557 568 sensor-pads equally divided between the two ends of the barrel. The two sides are partitioned into 108 readout partitions each, and the sensor-pads for each readout partition are connected to one Front End Electronics (FEE) system. The FEE performs trigger handling, readout and control of the partition. The data readout of the ALICE Experiment is trigger driven [6], i.e. an early trigger controls buffering of data and the last trigger starts the shipping of data to the Data Acquisition (DAQ) system for storage and analysis.

2.2 TPC front end electronics

The FEE [2] consists of up to 25 Front End Cards (FECs) performing analog and digital filtering, shaping, sampling and buffering of the data. The analog to digital conversion and digital signal processing is done by the ALICE TPC Readout Chip (ALTRO) [7] on the FEC. The FECs are connected via two branches of mezzanine backplanes to a Readout Control Unit (RCU) that is in charge of the data readout and control (figure 1). The RCU consists of a motherboard with two additional mezzanine cards attached: the Detector Control System (DCS) Board and the Source Interface Unit (SIU). The DCS board is an embedded computer with an ARM Hardcore CPU embedded in an Altera FPGA [8]. It is a Linux system communicating with the higher layer in the DCS via Ethernet. The main task of the DCS board is to control and monitor the FEE [9]. The SIU card hosts an optical transceiver and is the connection point to the DAQ system.

The RCU motherboard host a Xilinx Virtex-II pro vp7 FPGA [10, 11] that is referred to as the RCU Main FPGA. The RCU Main FPGA connects to all the logical systems of the ALICE

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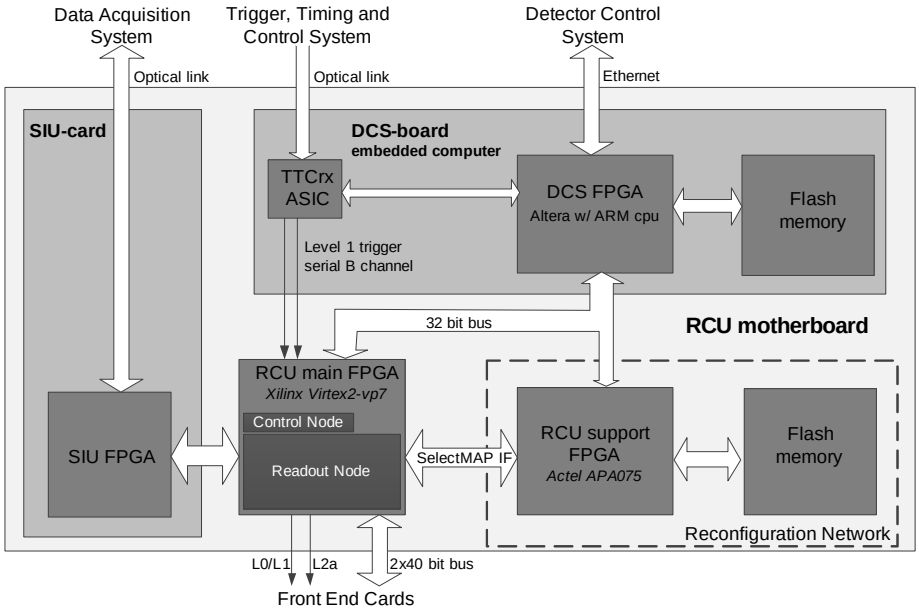

Figure 1. Schematic diagram of the TPC RCU.

detector. It receives and decodes triggers from the trigger system, it controls the data transport from the FECs and ships the data to the DAQ over the SIU. It is also in charge of monitoring the performance of the RCU board and of the FECs.

2.3 RCU main FPGA architecture

The RCU main FPGA [12] has two basic tasks: data readout and detector control. The data readout is handled by the readout node, while the control node handles the low level detector control functionality [13]. The readout node is by far the largest element as it uses more than 92% of the Configurable Logic Blocks (CLBs) and 75% of the Block Random Access Memory (BRAM). In contrast, the control node uses approximately 4% of the CLBs and no BRAM. The remaining 25% of the available BRAM resources on the FPGA cannot be used due to the implementation of the active partial reconfiguration [11].

2.4 Reconfiguration network

To be able to correct the SEUs in the RCU Main FPGA, a reconfiguration network was established [14]. It consists of two radiation tolerant devices; a small ACTEL APA075 Flash based FPGA [15] (labeled the RCU Support FPGA) and a flash memory [16] to hold the configuration files of the FPGA. The smallest addressable unit of the configuration memory in a Xilinx FPGA is called a frame, and one of the tasks of the RCU support FPGA is to do frame by frame readback, verification and correction (FRVC). The configuration files are stored on the flash memory device, making the Reconfiguration Network self contained and independent of the DCS board once running.

FRVC is possible since Xilinx devices allow reading and writing the configuration memory without interfering with the behavior of the algorithm programmed in the FPGA. When running

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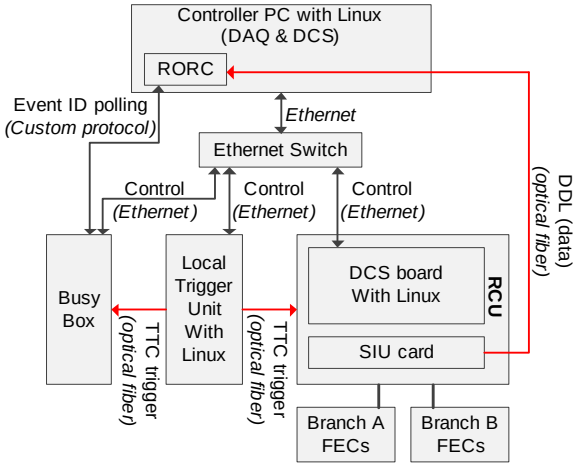

Figure 2. Sketch of the test setup used for the fault injection test.

FRVC, one frame after the other is read back from the RCU main FPGA and verified bit by bit with the same frame stored on the flash memory device. If a difference is found, the complete frame is overwritten and the error is corrected. All frames but BRAM frames can be read and written in such a way [11]. A detailed description of the solution can be found in [4, 14]. The maximum frequency of the FRVC is limited by timing constraints of the RCU flash memory, and runs continuously at about 6.6 Hz. Given an average event rate of about 1 kHz for p-p collisions [2], as much as 130 collisions are expected during the 150 ms it takes to read all frames.

3 Fault injection test

One of the major benefits of the RCU having an embedded Linux system is that it is fairly easy to modify to incorporate additional tasks. The fault injection software is one such application, and is extensively described in [17]. The advantage of running the fault injection tool on a system identical to the one installed in the experiment is the possibility to inject SEUs during operation under close to normal conditions in the laboratory.

3.1 Test setup

The RCU in the laboratory setup (figure 2) is connected to a set of 25 FECs on two sets of back-planes, branch A and branch B. This gives a total number of 3200 channels. The test is controlled by a master script running on a PC with Linux that also includes a Readout Receiver Card (RORC) and software for data readout. Remote login both to the Local Trigger Unit (LTU) and the DCS board gives access to their functionality. The LTU is used to issue Level 2 accept (L2a) trigger sequences, i.e. full valid trigger sequences that will buffer the sampled data and make the RCU ship the data to the RORC. More trigger sequences exist in the real system [6], but they are not needed in the scope of this test, as the L2a sequence activates most functions in the FPGA code, hence gives best coverage of logic.

The RCU and FECs are configured to do data readout via the RORC. This includes filling the pedestal memory of the ALTRO with predefined values taken from actual events gathered from

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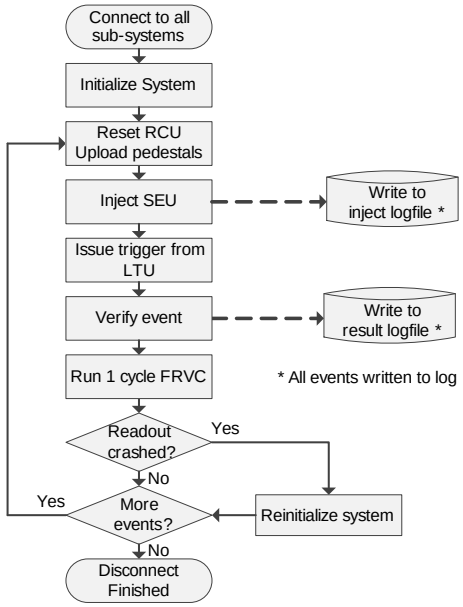

Figure 3. Flowchart showing the different steps in the fault injection test.

the ALICE experiment. This makes it possible to verify that the data received at the DAQ end is equal to the data actually being shipped from the ALTRO upon trigger reception. The remote login to the DCS board is used to control the fault injection tool [17]. A copy of all the individual frame files is stored on a mounted network drive, and the fault injection tool picks a random bit in a random frame and inverts the value. The erroneous frame is then written to the selectMAP interface using the direct selectMAP mode [14]. The injected bit flips are randomly distributed. The fault injection tool is slightly modified to make it fit the external controller script. The inclusion of a Busy Box [2] in the test setup implies that all components needed to replicate the ALICE readout system are present.

3.2 Test description

As shown in figure 3, the test starts with connecting to the DCS board and the LTU from the Linux PC. After that, the system is initialized, i.e. the RCU main FPGA is programmed from the flash memory, before the ALTROs and the RCU are configured and made ready for trigger reception and data readout. Then the LTU is set up to issue triggers. The next step is performed by the fault injection tool. This is started from the script and one single bit flip is injected at a random bit position in a random frame. The SEU number and the location are written to a log file. After the bit flip is injected the script issues a command to the LTU to send an L2a trigger sequence from which an event readout automatically follows.

The shipped event is then verified and the result is logged along with the SEU number. This makes it possible to map the functional faults with the exact location from the logfile of the injected SEU. An FRVC cycle is performed afterwards to correct the injected bit flip. If the injected bit flip causes a crash of the event readout the whole system is reconfigured, since a reliability fault leaves the system in a state where recovery is highly unlikely by only clearing the injected bit flip. If the

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event readout showed no detected errors or only performance faults, the scripts simply moves on and injects another bit flip in the configuration memory until the preselected number of events is reached. The average time for injecting one bit flip, doing a readout, running an FRVC cycle and verifying the result is about 5 seconds.

During the fault injection test a total number of 206 151 bit flips were injected in the configuration memory of the FPGA, of which only 287 are the same bit being flipped more than once. The total number of configuration bits for the Xilinx Virtex-2 vp7 excluding BRAM frames is 3 161 344 [11]. This implies that about 6.5% of the configuration bits were actually tested. A higher coverage would have been preferred, however the need to share the test setup with other activities imposed this limit.

3.3 Benefits of the fault injection test

The only test comparable to fault injection is a full scale irradiation test. Fault injection has two major benefits over an irradiation test, namely cost and simplicity. Given a dedicated test setup it is in general easier to gain better statistics with fault injection as the testing period will not be limited by external factors like cost and available beam time, etc. Fault injection is also more readily available during design and development of the FPGA code. When algorithms are written or modified it is very easy to classify the radiation tolerance of the module prior to a release version. This will naturally improve the quality of the design.

3.4 Limitations of the test

In general, fault injection can only simulate SEUs occuring in the CLB configuration memory of the FPGA, since these are the only memory elements accessible with active partial reconfiguration. This means that SEUs occuring in the BRAM elements, in the configuration interface and in the registers at design level is not possible to simulate. SEUs in the BRAM elements will, in the real system, be a measurable source for performance faults, and the only way to test for this is in a radiation beam.

The occurrences of SEUs in a radiation environment are by definition random, while in the test a bit flip is injected at a predefined time of which the RCU main FPGA is in an idle period. The bit flip stays there throughout the full readout of the event. The injected bit flip is always corrected at the end of each cycle, so the fault injection test does not test for multiple bit upsets. However, given the rate of SEUs that have been measured under running conditions [18], it is highly unlikely that one RCU experiences two SEUs within the FRVC cycle time of 150 ms. Additionally, the trigger rate in real life is normally far higher than the frequency of the FRVC, i.e. when a SEU occurs in the real experiment it will affect more events than one and appear static for most events.

Another limitation is given by the fact that the DCS board is used for running the fault injection tool. This implies that the control node in the RCU main FPGA is not tested. However, this is not critical because of the relatively small size of the control node compared to the readout node. Additionally, since the control node does not lie on the trigger and readout path, it is highly unlikely that an error in this part of the FPGA logic will have a negative effect on the data stream.

The fault injection test reached a configuration bit coverage of about 6.5%, a number that preferably should be higher. However, it is not likely that an irradiation test would provide better

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Table 1. Results from the fault injection test.

Fault type	Num. of Faults	Faults/SEU [%]	SEUPI [SEUs/Fault]
All	10 341	5.02	19.9
Reliability	2 210	1.07	93.5
Performance	8 131	3.94	25.4
Loss of data	*2 499*	*1.21*	*82.6*
Corrupted data	*5 632*	*2.73*	*36.6*

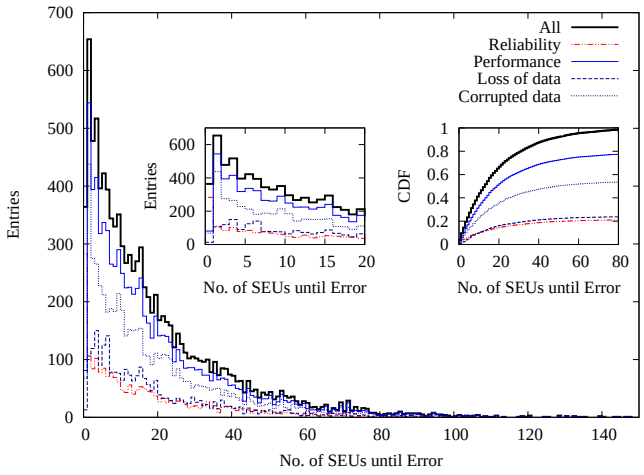

Figure 4. Measured distribution showing the number of SEUs injected until a functional failure occurs. The main graph shows a distribution of the number of SEUs per fault, the left insert highlights the area with the highest counts, and the insert to the right shows a cumulative representation of the distribution.

coverage. Since multiple bit upsets are highly unlikely to occur in the real experient [18], a higher SEU rate than what is provided by the fault injection test is not interesting. This implies that a high intensity beam is not desired. Actually, several SEUs within one event readout would make it difficult to point out which individual SEU was responsible for the detected functional failure.

4 Results

10 341 of the 206 151 injected bit flips resulted in a detectable functional failure, of which 2 210 were reliability faults and 8 131 were performance faults. Table 1 gives an overview of these results.

4.1 Fault injection test results

It is seen (figure 4) that 5 bit flips are sufficient to provoke a functional failure in about 20% of the cases, and that the distribution is similar for the different types of error. This is as expected since 96% of the available resources in the FPGA are used, hence is the number of sensitive bits for the design almost maximized. In addition, no extra mitigation techniques are implemented because of

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the limited number of resources given by the choice of FPGA. The fault injection test gives a SEU Probability Index (SEUPI) of 19.9 SEUs/fault. As a rule of thumb, Xilinx estimates an SEUPI of at least 10 SEUs/fault [19]. Given the fact that the sensitive area for the test is 92% of the logic elements and that the Xilinx SEUPI number is a conservative estimation, this result is in the expected range. Counting only reliability faults, the SEUPI is as high as 93.5 SEUs/fault. This implies that most of the functional faults are not critical for the operation of the ALICE detector, and that the RCU main FPGA will be operating normally when the FRVC corrects the bit flip in the FPGA.

The type of error given by a bit flip in the same topological location was also analyzed. Of the 287 cases where the same configuration bits were flipped more than once, only 2 configuration bits gave inconsistent results such as a reliability fault in one case and a performance fault in the other. This is related to the test being executed using sparse readout mode [13] with actual data recorded by the ALICE detector. In sparse readout mode, only channels of which the data size is non-zero are read out and because of differences in the data for each collision, the active channels change from event to event. This in turn means that different parts of the logic in the FPGA are active during a readout cycle resulting in different types of fault situations for certain configuration bits.

4.2 Functional failures as a function of integrated luminocity

One of the goals of the fault injection test is to get an estimate of the correlation between the rate of functional failures we can expect in the RCU design with respect to the measured SEU rate. The SEU rate is continously monitored by the DCS and the collected data has been analyzed during a period with p-p runs from the beginning of May until the end of August, 2011 [18]. A linear correlation between integrated lumonicity and the SEU count was found with a mean value of 0.49 SEU/nb^{-1} for all 216 RCUs on the TPC detector.

When multiplying this number with the SEUPI found by the fault injection test, the rate of failures is 0.025 faults/nb^{-1}. The rate of reliability faults is 0.005 faults/nb^{-1}. This implies that the expected number of failures related to SEUs in the RCU main FPGA in the same period as [18] is approximately 80, while the expected number of reliability faults in the same period is approximately 16. To analyze the number of failures actually seen in this period not already accounted for is very difficult since there are many potential sources of error in the system. This is especially true for performance faults, so the logbooks from the runs were investigated looking at situations where the readout crashed and left the system in a erroneous state. In a period from 1st May 2011 to 16th June 2011 the total number of error situations found was 39, of which maybe 5 are likely to be caused by radiation related reliability faults in the RCU main FPGA. The other error situations were understood and handled. This means that the daily estimated failure rate is about 0.13 reliability faults per day, while the daily measured rate is about 0.11 reliability faults per day. The statistics in the measured failure rate are very low, but still it is a clear indication that fault injection is a reliable method for testing radiation effects at the design level.

5 Conclusion and outlook

This paper presents the first results from the fault injection test performed on the TPC RCU main FPGA. The tests have shown that the SEUPI of the current design is 19.9 SEUs/functional fault. This is a result which is very hard to improve given the available logic resources of the Xilinx

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Virtex-2 pro. The functional faults are divided into two sub categories: reliability faults and performance faults, of which the former is by far the most severe. A reliability fault will prematurely abort the ongoing data taking, hence affecting the complete ALICE detector. The SEUPI for reliablity faults is 93.5 SEUs/fault. With the current running conditions this implies 0.005 reliability faults/nb^{-1}. Since there is a linear correlation between SEUs and integrated luminosity, the SEU rate can be expected to grow at the same level as the luminosity given otherwise equal conditions. Currently a typical fill with stable beams reaches an integrated luminosity ranging from about 20 to 200 nb^{-1} [20]. If we assume a mean value of 100 nb^{-1} per fill, it means that approximately every other fill experiences an interruption in the ALICE data taking due to a functional failure in the RCU main FPGA. Given that the luminosity will increase by a factor of 10 in the future, it can be expected that the RCU main FPGA will cause at least 5 interruptions per fill on the average. Adding this on top of a potentially increased error rate in other components, it is clear that the efficiency of the ALICE detector will be drastically reduced.

However, upgrades of the ALICE TPC readout electronics are currently being discussed within the Collaboration. The purpose of these upgrades is to remove bottlenecks and increase the data rate, as well as improving the robustness against SEUs. The fault injection study together with the results from [18] emphasizes the importance of the latter. If it is decided to use SRAM based FPGAs in the FEE of a possible future ALICE upgrade, it should be considered to also implement a solution for fault injection. Given the latest development in FPGA technology it is possible to do this without additional circuitry [21], and, as emphasized in this paper, fault injection has proven to be an excellent tool for analyzing and improving the radiation tolerance at design level for a SRAM based FPGA.

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