Broadband FPGA Payload Processing in a Harsh Radiation Environment

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***Abstract*—In this paper, we propose a concept for broadband *Digital Signal Processing* under consideration of mitigation schemes to increase the reliability. We take *Single Event Upsets* into account to guarantee a reliable operation during a *In-Orbit-Verification*. It will be performed on the *Fraunhofer On-Board Processor*, which is a dynamically reconfigurable *On-Board Processor* platform based on two space-grade *Virtex-5QV* FPGAs. A master and slave FPGA concept enables broadband *Digital Signal Processing* experiments, which are controlled and monitored by the high reliable master FPGA. Each FPGA processes a separated signal path of the *Fraunhofer On-Board Processor*. The first FPGA executes scrubbing of both FPGAs, measures the current radiation and observes the whole system with a fault management. The second FPGA realizes only the broadband *Digital Signal Processing*, which results in more usable resources. We analyze the impact of the radiation to point out the influence to the FPGAs.**

A case study demonstrates a *Digital Down Converter* for broadband *Digital Signal Processing*. This hardware verification evaluates a 306 Mbit/s broadband signal, modulated with *Quadrature Phase-Shift Keying*. It results in a *Signal-to-Noise Ratio* of 19.29 dB. Due to separation of mitigation schemes and broadband *Digital Signal Processing* the system operates reliable and the resources are used efficient.

I. Introduction

Today's FPGAs play a major role in many *Digital Signal Processing* (DSP) application areas like telecommunication, radar, video, audio and image processing. Due to their success, FPGAs are also used in space applications, like the *Fraunhofer On-Board Processor* (FOBP). The FOBP is part of the scientific payload of the *Heinrich Hertz* communication satellite. This satellite is planned to be launched into a *Geostationary Earth Orbit* (GEO) in 2018 followed by an operation of 15 years. The orbit position will be 17.6 ° East.

During the in-orbit verification the *Fraunhofer IIS* will perform various communication experiments with the FOBP. Here, FPGAs offer significant competitive advantages with respect to *Application-Specific Integrated Circuits* (ASICs). Since FPGAs are in-field reconfigurable, it is possible to change the hardware structure of the FPGA after the satellite has launched into orbit. New features can be added to extend or renew the set of services the implemented application offers and to prolong the useful lifetime of the satellite. We chose to leverage the FPGAs capability to be reconfigured for various tasks. Thereby it is possible to save space, reduce weight and enable the use of future communications protocols. Unfortunately, the reconfiguration capability comes at a price. *Static Random-Access Memory* (SRAM)-based FPGAs are highly susceptible to so-called *Single Event Effects* (SEEs) when operating in a harsh radiation environment like space. We have done a radiation analysis (see Section IV) to predict and mitigate these effects.

In order to proof our concept we built an *Elegant Bread Board* (EBB) of the FOBP. Since the tests with this model were performed successfully, we are developing an *Engineering Model* (EM). This EM is currently in the layout. After manufacturing and functional tests of the EM we will manufacture a *Engineering and Qualification Model* (EQM), which is our on-ground reference, and a *Proto-Flight Model* (PFM), which will actually be integrated in the satellite. Before conducting our communication experiments we have to reconfigure the FPGAs with a adapted firmware. A initial-configuration, stored in a non-volatile *Magnetoresistive Random-Access Memory* (MRAM), ensures the fail-safe reconfiguration of the FPGAs [1]. Each FPGA is able to reconfigure itself due to partial reconfiguration (reconfiguration time t_{Cfg} depends on the partition size) and can reconfigure the other one completely (reconfiguration time $t_{\mathrm{Cfg}} = 120\,\mathrm{ms}$ with 51 MHz configuration clock).

Our experiments cover applications like on-board processing for broadband communication, single-hop connection, communication for mobile users and a digital radiation monitor. In this paper we will focus on the on-board broadband processing and the radiation effects to calculate the reliability of such a system.

The remainder of this paper is structured as follows: Section II reviews the related work. Section III gives an overview of our system. Section IV points out the expected SEU rates for the used *Xilinx Virtex-5QV* FPGA in a GEO. The firmware concept and details of our system implementation are discussed in Section V. Section VI finally applies our radiation results to a *Quadrature Phase-Shift Keying* (QPSK) modulated *Digital Down Converter*.

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II. Related Work

The option to adapt in-flight the implementation of on-board digital processors is becoming an issue for modern satellite systems. Due to enhanced mission lifetimes and new technologies it is in favor to investigate architectures that supports reconfigurable implementation. Previous work, done by [2] describes a regenerative *On-Board Processor* (OBP) architecture adapted from the SRAM-based FPGA technology to enable a fully reconfigurable platform.

We facilitate a regenerative transponder due to our multi FPGA platform. By using a *virtual Telemetry/Telecommand* (vTC/TM) link it is therefore possible to reconfigure the FPGAs remote in-orbit. The impact of charged particles on electronic devices and their triggered malfunction has also been analyzed a lot in the recent years. Even though the focus of this paper is not on mitigation techniques for radiation effects, we still want to mention the potential of *Block Random-Access Memories* (BRAMs) or other FPGA primitives to serve as a radiation particle sensor. We modeled a self-adaptive mitigation concept, which is able to calculate the current radiation environment by detecting the injected upsets in the stored BRAM and adjust the mitigation level to the actual requirements [3]. On-orbit SEU results of the configuration SRAM and BRAM in XQVR1000 FPGAs are presented in [4]. In [4] is also stated that the SEU upset rate is lower than the best case estimate and much lower than any worst-case conditions.

In comparison to other broadband communication on satellite platforms or on-board *Software Defined Radios* (SDRs) [5] with 100 Mbit/s we achieve with our proposed system 306 Mbit/s.

III. System Overview

The FOBP contains four main hardware modules. The *Radio Frequency Card* (RFC) consists of an analog front-end receiver, a analog front-end transmitter and a clock distribution. The *Power Supply Unit* (PSU) connects the satellite power to the FOBP, prepares and distributes the power for the other cards. Furthermore, the PSU implements a connection to the satellite bus via *High Power Commands* (HPC) and *Bi-level Switch Monitors* (BSM) which allows to control and monitor high priority signals. Two DSP cards performs the signal processing of the OBP with space grade *Xilinx Virtex-5QV* FPGAs. Each DSP card consists of an *Analog-to-Digital-Converter* (ADC), an FPGA and a *Digital-to-Analog-Converter* (DAC) and realizes one of the two processing paths. Fig. 1 shows the structure of the FOBP with these two paths.

The used ADC has a resolution of 10 bit and a maximum sampling frequency of 1.5 GS/s. Both paths interface inputs (*I1* and *I2*) at an *Intermediate Frequency* (IF) of 1530 MHz. Path one has a *Bandwidth* (BW) of 36 MHz (following narrowband) and path two a BW of 450 MHz (following broadband). We use direct sampling to convert the IF carrier from the L-band to a lower IF. With this direct conversion the analog signal processing on the RFC is simplified by using only amplifiers and filters. The receiver bandpass filter reduces the bandwidth to avoid aliasing effects and the transmitter bandpass filter attenuates replications of the DAC spectrum.

Important for the direct conversion and high-speed signal processing is a precise clock with a high stability characteristic. To achieve these preferences we use a *Oven Controlled Crystal Oscillator* (OCXO) which provides a global clock supply for all components. The OCXO has a center frequency of 120 MHz, a stability of ± 120 ppb and a phase noise ground of -165 dBc/Hz. *Phase-Locked Loop* (PLL) synthesizers derivate the sampling clock for the ADC and DAC from this OCXO reference. This clock supply and distribution enables a constant phase relation and consequently a high precision sampling.

The sample frequency f_s will be calculated with the following equation which is defined by the frequency domain. The left border of a specified Nyquist region is expressed by two terms, which are set equal in Equ. 1 (f_{IF} is the intermediate frequency):

$$f_{IF} - \frac{fs}{4} = (Nyquist - 1) \cdot \frac{f_s}{2} \tag{1}$$

Dissolving Equ. 1 for f_S we get the following equation:

$$f_s = \frac{2 \cdot f_{IF}}{Nyquist - 0,5} \tag{2}$$

For the final calculation of f_s three further conditions are necessary:

1) Nyquist-Shannon sampling theorem (here for BW 450 MHz): $f_s > 2 \cdot BW = 900\,\mathrm{MHz}$
2) Maximum f_s of the ADC: $f_s < 1500\,\mathrm{MHz}$
3) Optionally: $f_s \in \mathbb{N}_{\mathrm{MHz}}$

According to these conditions we have to use the third Nyquist for the broadband path. This results in f_s of 1224 MHz (see Equ. 2). The sampling for the narrowband path is more relaxed because the condition one allows a smaller f_s. Hence, we use the fifth Nyquist with a f_s of 680 MHz (this is limited to the maximum Nyquist of the DAC).

IV. Radiation Analysis

The reliability of electronic components, circuits and systems is essential in space applications. Due to the shrinking size of electronic devices they become more vulnerable in terms of damaging interaction with radiation. The primary short-term radiation effect is called *Single Event Effect* (SEE) [6]. SEEs occur when a charged particle penetrates sensitive nodes within electronic devices. A sensitive node usually combines a voltage level with an information bit. Due to altering the electrical potential of electrical charge it possible to regulate the node. If the charge collected by an ionizing particle at one junction reaches a certain value, defined as critical charge, the particle will upset or affect the circuit. The charged particles mainly compounds of *Electrons, Neutrons, Protons* (P) and *Heavy Ions* (HI) that are emitted directly from the sun or accrue from outer space as *Galactic Cosmic Rays* (GCR).

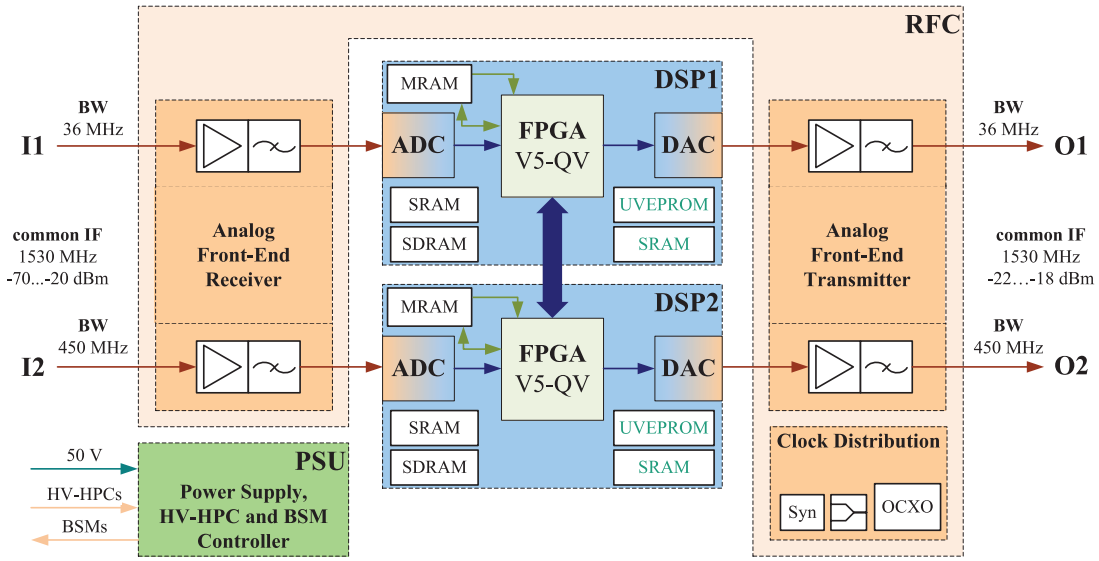

Fig. 1: Overview of the FOBP: *Power Supply Unit* (PSU), *Radio Frequency Card* (RFC) and two DSP cards

SEEs can be classified into three main groups: Destructive errors, hard errors and soft errors. Destructive errors cause physical damage and hard errors resulting in a permanent change of the function. The corruption of a stored information is a soft error, which is temporary and non-destructive. They can be eliminated by resetting the system or rewriting the stored data in the affected memory cell. Soft errors can be subdivided into *Single Event Functional Interrupts* (SEFIs), *Single Event Transients* (SETs) and *Single Event Upsets* (SEUs). In this paper, we will focus on SEUs only, because SEFIs are at least three orders of magnitude less then SEUs for the used *Virtex-5QV*.

In order to predict SEUs during a space mission, one has to be conscious about the key parameters. The initial point for SEU calculations is usually measured and delivered by the manufacture of the device and are called the *Weibull-Parameters*. The probability for an SEE to occur in a certain device is given in terms of a *Cross Section* (CS). It is a function of the energy that is transferred from a crossing ionizing particle to the device per unit path length and is usually given as *Linear Energy Transfer* (LET). The amount of collected charge in a *Sensitive Volume* (SV) depends strongly on the LET. Among a characteristic value, called *LET Onset* (LET_{on}) no upsets will occur because the charge collection is too low. Increasing the LET implicates a larger size of the CS. This gain of the CS with respect to the LET is continuing until the *Saturation Cross Section* (CS_{sat}) is reached. It defines the upper limit for SEEs, due to the fact, that an ion injecting more charge in SV will not increase the SEE probability anymore.

In addition to the *Weibull-Parameters*, mission specific values, like trajectory, shielding and solar conditions have a large impact on SEU calculations. Depending on the mission orbit and the shift of the solar activity during the traverse of a solar cycle, the particle flux is not uniform. These circumstances are considered in the widely accepted tool *Cosmic Ray Effects on Micro-Electronics* (CREME96). Tab. 1 shows the SEU rate calculations for primitives of the *Virtex-5QV*. We assumed a shield thickness of 7 mm aluminum (6.5 mm due to OBP box shielding and additional 0.5 mm due to the satellite *Kapton* envelope) in GEO. The average flux of particles was calculated for five different solar conditions: *Solar Minimum* (lowest solar activity during a solar cycle), *Solar Maximum* (highest solar activity during a solar cycle), *Worst Week* (averaged over 180 hours during the worst week observed in the last two solar cycles), *Worst Day* (averaged over 18 hours during largest flux enhancement in the worst week) and *Peak 5 Minutes* (averaged fluxes observed on *GOES* in October 1989) [7]. Notice that the solar wind during periods of high solar activity reduces the *galactic cosmic ray* flux. Thus, the minimum in GCR flux occurs during *Solar Maximum*, and the maximum in GCR flux occurs during *Solar Minimum*. Due to this behavior the SEU rates at the *Solar Minimum* conditions are higher than the rate during *Solar Maximum*. The overall upset rate results in the addition of the *Heavy Ion* and *Proton* upset rates at the given solar conditions. [8]

Fig. 2 depicts the overall upset rates of used FPGA resources in this paper. Here the DSP slices are most vulnerable FPGA primitives for the proposed broadband DSP. The curves are presented separately for *Heavy Ions* and *Protons*. The first left marker of all curves represents the upset rate at the *Onset* of the *Solar Maximum*. From this point, the next points right represents the radiation conditions *Solar Minimum, Worst Week, Worst Day* and *Peak 5 Minutes*. In order to mitigate SEUs in the BRAM an *Error Detection and Correction* (EDAC) code is implemented. The *Configuration Controller, Configuration Memory* (Cfg.) and *Flip Flops* (FFs) are radiation hardened by design. Additional the FFs include a filter that can be activated to attenuate *Single Event Transients* (SETs). Relating to *DSP-Registers* no radiation protection was applied. As shown by the SEU rates listed in Tab. 1 the embedded BRAM is the

TABLE I: Overall upset rates μ of the *Virtex-5QV* in GEO with a 7 mm aluminum shielding

Resource Type / Device	Count	*Solar Min.* (Upsets/s/device)	*Solar Max.* (Upsets/s/device)	*Worst Week* (Upsets/s/device)	*Worst Day* (Upsets/s/device)	*Peak 5 Min.* (Upsets/s/device)
Configuration Memory	34,087,072 Bit	2.02×10^{-8}	3.88×10^{-9}	6.99×10^{-7}	1.69×10^{-6}	6.10×10^{-6}
BRAM Primitive 512×72 Bit	298	3.98×10^{-5}	1.29×10^{-5}	2.70×10^{-3}	9.93×10^{-3}	3.61×10^{-2}
FF SET Filter off	81,920	3.50×10^{-8}	8.59×10^{-9}	1.77×10^{-6}	5.70×10^{-6}	2.07×10^{-5}
FF SET Filter on	81,920	1.23×10^{-9}	2.38×10^{-10}	1.15×10^{-7}	3.87×10^{-7}	1.41×10^{-6}
DSP M-Register	320	1.41×10^{-6}	5.03×10^{-7}	1.01×10^{-3}	3.77×10^{-3}	1.37×10^{-2}
DSP other Register	1,280	3.13×10^{-6}	1.11×10^{-6}	2.22×10^{-3}	8.25×10^{-3}	3.00×10^{-2}
Configuration Controller	4	4.06×10^{-12}	1.14×10^{-12}	4.13×10^{-10}	1.45×10^{-9}	5.27×10^{-9}

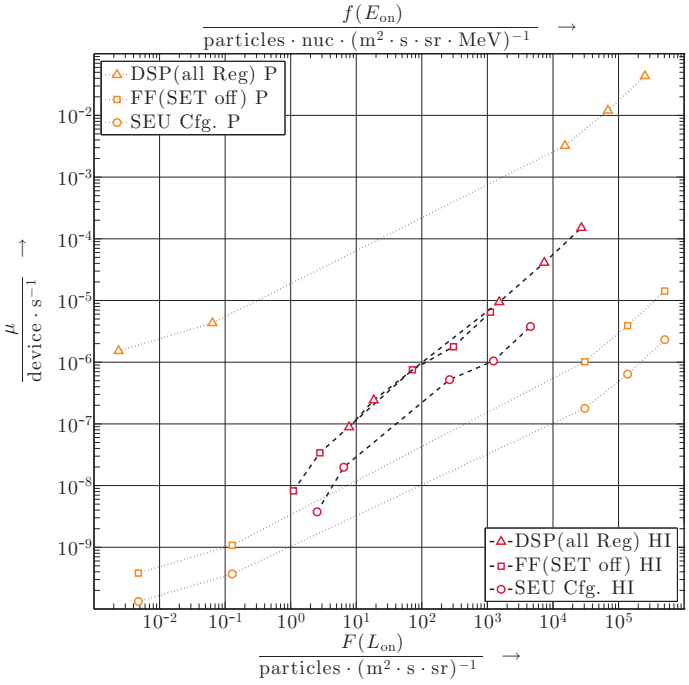

Fig. 2: *Heavy Ion* (HI) upset rate as function of the integral flux $F(L_{\text{on}})$ and *Proton* (P) upset rate as function of the differential flux $f(E_{\text{on}})$ for selected resource types of the *Virtex-5QV*

most sensitive type of resource. This enables the BRAM as a sensor to detect SEUs for space missions. By means of measuring upsets it is possible to determine the corresponding flux, respectively the solar conditions. Latter information can be used to adjust on board mitigation sequences according to the current radiation pollution [3].

There are several approaches to mitigate the upset rates in electronic devices. *Hardening by Design* (logic structures are modified to achieve the SEU immunity) and *Hardening by System* (modifications in the software and duplication in the logic modules are performed) are two possible solutions that are based on techniques like *Triple Modular Redundancy* (TMR) or an EDAC code (*Hamming Code*). Using special fabrication processes for instance *Silicon on Insulator* (SOI) is generally known as *Hardening by Technology*. [9]

V. Firmware Concept

This section presents a firmware concept for the high reliable DSP platform, which allows the processing of broadband channels. We introduce a system architecture consisting of a combination of a reliable control part and broadband processing part.

A. System Architecture

The following subsection focuses the architecture of both *Virtex-5QV* FPGAs. To achieve a high reliability as well as a broadband DSP we demand a system concept which separate both requirements. On the one hand we need a high reliable FOBP on-board control and on the other a high-speed DSP for broadband communication, which requires many FPGA resources. As mentioned in Section III the FOBP consists of two DSP cards for the signal processing. This enables an approach which separates the different operations to the different FPGAs. The first FPGA complies the FOBP control master role to archive a high reliability for both FPGAs. The second FPGA focuses on the broadband DSP and acts as slave device. Fig. 3 shows the system architecture with both DSP cards and FPGAs.

B. FOBP Control

An important feature to increase the reliability is an initial configuration, which enables a self-reconfiguration or the full reconfiguration of the other FPGA. After a power up of the FOBP both FPGAs are configured with the initial configuration, stored in the non-volatile MRAM. The content of this initial configuration is similar for both FPGAs and enables a reconfiguration of a dynamically reconfigurable part (see Fig. 3). A *System-On-Chip* (SoC) is able to perform a partial reconfiguration of its own dynamically reconfigurable regions (via the *Internal Configuration Access Port* (ICAP) interface). If both FPGAs are signaling a successful start up, one FPGA can be completly reconfigured (via the *Select Map* interface). For the broadband signaling experiments the first FPGA receives a dedicated firmware and configures the second FPGA with this new bit file. The first FPGA keeps its initial configuration, which includes also the FOBP control functionality. Fig. 3 includes the configuration of the FPGAs. These initial configuration concept to ensure the FPGA reconfiguration in space increases the reconfiguration reliability significant [1].

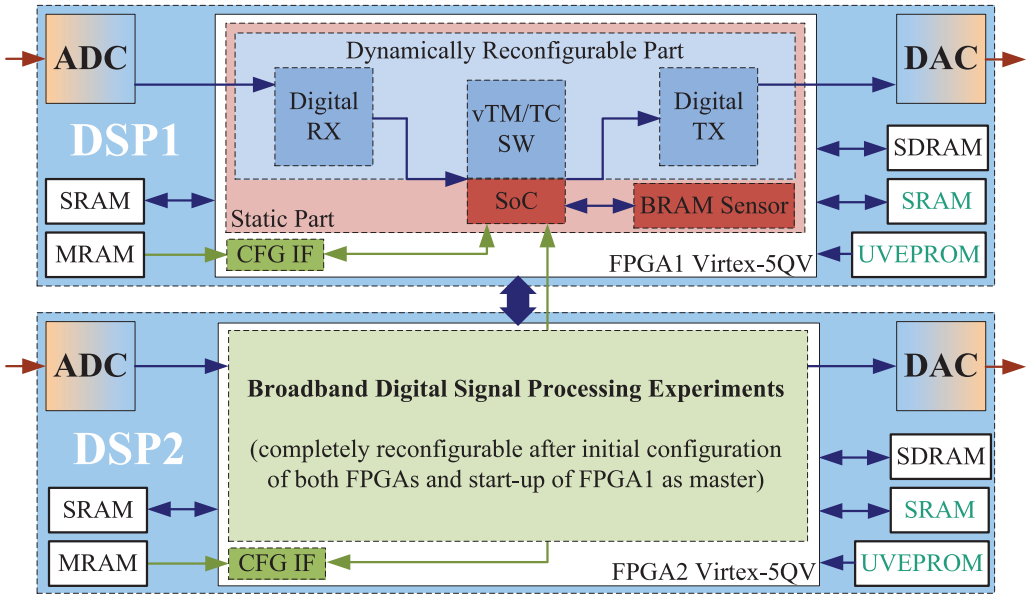

Fig. 3: System architecture with two DSP cards with *Virtex-5QV* FPGA. The first FPGA realizes the FOBP control part (equal to the initial configuration) and the second FPGA the broadband DSP. CFG IF is the configuration interface.

The SoC is located in the static part of the initial-configuration and is based on a 32-bit microprocessor. Most likely we will use the *LEON3FT* from *Aeroflex Gaisler* built on top of the GRLIB platform [10]. The hardware and the boot code of the SoC is part of the static area in the initial-configuration and is therefore unchangeable. Nevertheless, it is possible to update the application software (e.g. the vTM/TC processing code). The four main tasks of the SoC can be described as follows:

(1) Reconfiguration (as mentioned before) and scrubbing is the first task. A *Error-Correcting Code* (ECC) read-back scrubbing corrects configuration SEUs of both FPGAs. The access to the configuration memory is equal to the mentioned reconfiguration.

(2) The SoC performs *Fault Detection, Isolation and Recovery Correction* (FDIR). This includes a fault detection of different components inside (e.g. the demodulator) or outside (e.g. the ADC) the FPGA. All status signals are combined and evaluated with a *Fault Management Unit* (FMU), which choose a suitable error handling strategy if a fault is detected. The broadband DSP firmware includes a resource efficient error detector, which is connected to the FDIR system and allows an error detection of the second FPGA. If an error is not recoverable, the FMU initiates a reset or a reconfiguration via the *Select Map* interface (see task (1)).

(3) A *virtual Telemetry/Telecommand* (vTC/TM) channel provides the controlling and monitoring of the FOBP. The uplink of the first path (*I1* to *O1* in Fig. 1) includes the vTM/TC signal, which is demultiplexed respectively multiplexed with the normal user uplink. The received signal contains bit files, software files or control parameter for the firmware. We transmit status information periodically over the downlink to signal the ground station the FOBP status. These information include also calculated *Bit Error Rates* (BERs) or *Signal-to-Noise Ratios* (SNRs) of the broadband DSP experiment as a feedback for a adaptive coding and modulation. Furthermore, it enables the possibility to debug the firmware in space.

(4) The radiation measurement provides radiation values for the system. According to Section IV the internal BRAM can be used to determine the current radiation. With this measurement the SoC calculates a redundancy for an adaptive mitigation depending on the current SEU rate.

A possible mitigation scheme for the broadband DSP in terms of redundancy like *Dual Modular Redundancy* (DMR) or *Triple Modular Redundancy* (TMR) is not applicable cause of the extensive resource consumption. So errors will occur and we will accept them as part of the experiment. Nevertheless, it is important that faults are detected and repaired as soon as possible. We implemented the broadband signaling processing without any feedback loops, so SEUs on the logic layer and corrected SEUs of the configuration are temporary. Configuration SEUs of the second FPGA will scrubbed by the SoC of the first FPGA.

C. Broadband Digital Signal Processing

This section presents the firmware part for the broadband DSP (see second FPGA in Fig.3). To receive the digital data with the sampling frequency calculated in Eq. 2 we use the quad-demultiplexing of the ADC output. The input of the FPGA have to process these four data buses each with 306 MHz. Therefore a *Digital Down Converter* (DDC) is necessary, which combines these buses and extracts the different sub-bands of the input signal. Focus of the proposed broadband DSP is one broadband channel with the maximum possible bandwidth. A further narrowband signal within the 450 MHz analog band is multiplexed in the frequency domain.

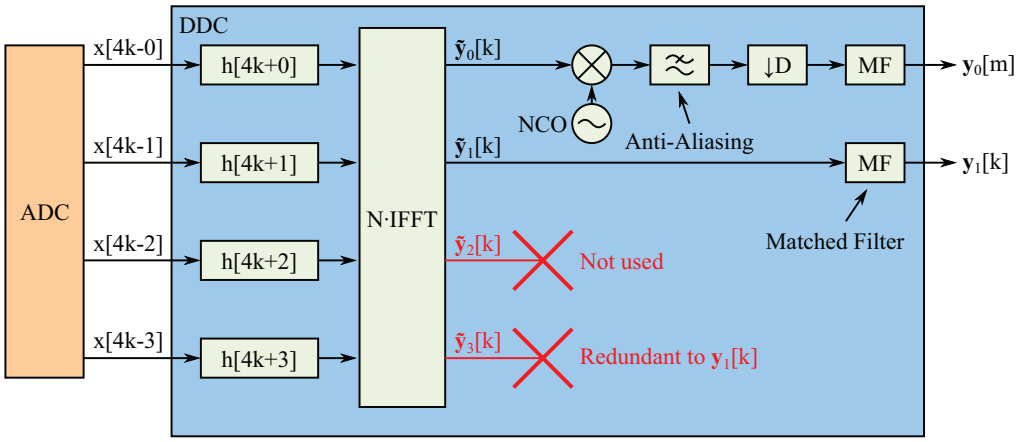

Fig. 4: Structure of the *Digital Down Converter* (DDC) for the extraction of narrowband signal $y_0[m]$ (additional mixing) and broadband signal $y_1[k]$

Fig. 4 presents the principle of our DDC approach.

The left side of the figure depicts the ADC with quad-demultiplex-outputs and the right side visualizes the DDC in the FPGA. We use a polyphase filter bank. The general filter of the filter bank will be modulated with an N-fold *Inverse Fast Fourier Transformation* (IFFT) and results in prototype filters $h[N \cdot k+n]$. These prototype filters can be implemented more efficient and save resources.

Outputs of the filter bank are four IQ-channels. The channel $\tilde{y_3}[k]$ is redundant to $\tilde{y_1}[k]$, which includes a 306 MHz BW baseband signal with a sample rate of 306 MHz. This signal determines the broadband signal and can be used directly without frequency conversion.

Channel $\tilde{y_0}[k]$ and $\tilde{y_2}[k]$ can use a maximum BW of 153 MHz. Further quadrature mixers enable the frequency conversion of signals, which are not located on the baseband frequency, into the baseband. Additionally, anti-aliasing filter with decimation and the matched filter allow to treat narrowband signals or signals, which does not requires a high sampling frequency. We choose the channel $\tilde{y_0}[k]$ for the narrowband signal and discard $\tilde{y_2}[k]$ channel.

For a broadband DSP chain a *Digital Up Converter* (DUC) is necessary to provide the baseband signal to the DAC. The structure for the DUC is equal to the DDC and will be mirrored from the DDC of Fig. 4.

A design challenge of the DDC or DUC is the maximal frequency of 360 MHz [11] for the *Virtex-5QV* FPGA, which is close to the processing clock of 306 MHz. This critical timing needs special methods for broadband DSP. To relax this timing for narrowband processing we developed a concept which is capable of changing the sample rate dynamically. If a path with smaller sub-band is used, the sampling frequency can be lower, for example 680 MHz for the fifth Nyquist region (see Eq.1). As mentioned in Section III the FOBP contains two signal processing paths, which also demands a dynamical adaption between both paths.

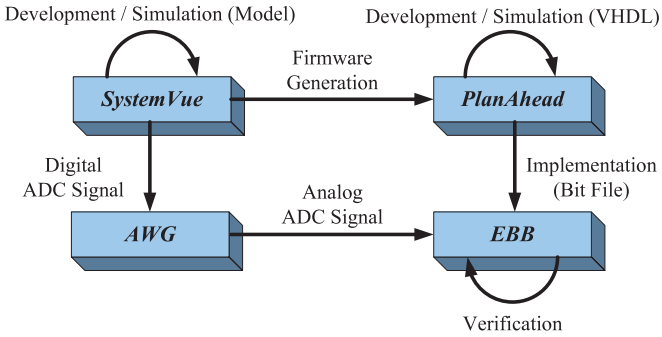

Fig. 5: Design and verification process for the DDC concept

VI. Case Study

In order to proof the concept we performed a case study to verify the broadband DSP. Section V-C has presented the approach to process the narrow- and broadband signal as a combined input signal of the ADC. The software tool *SystemVue* from *Agilent Technologies* enables a model-based design process for the DDC. Furthermore it is possible to simulate the design and generate synthesizable *Very High Speed Integrated Circuit Hardware Description Language* (VHDL)-code. We implement this DDC-code together with the additional application specific VHDL-code and the framework using *Xilinx PlanAhead*. The additional application specific VHDL-code includes a *ChipScope Pro* instance, a module to parametrize the PLL via *Serial Peripheral Interface* (SPI) and a procedure for the initial start up of the firmware. The PLL provides the sampling clock for the ADC, which is derived from the OCXO clock (Section III). An *Arbitrary Waveform Generator* (AWG) generates the analog input signal for the ADC and obtains this signal from *SystemVue*. Fig. 5 depicts the design and verification process.

To achieve a successful timing we use physical block and timing constraints for the *PlanAhead* design and allow a higher effort for the implementation tools. We implemented the design on the space-grade FPGA, the *XQR5VFX130*,

and on the equivalent *Commercial Off-The-Shelf* (COTS) FPGA, the *XC5VFX130T*. Both FPGAs are speedgrade -1. Tab. II summaries the resources consumption and the essential configuration bits for the *Virtex5-COTS* and the *Virtex5-QV* implementation.

Both implementations were successful. The *Virtex5-COTS* finishes without timing errors and the *Virtex5-QV* with timing errors (*Xilinx Timing Score: 9387 ps*) as a result of the more critical timing requirements for the space-grade FPGA.

The *Elegant Bread Board* (EBB), a proof of concept model for the FOBP, use a *Clock Distribution Card* (includes the PLL for the sampling clock), a *e2V-ADC Card* and a *DSP Card* to verify the design. The used AWG is the *AWG7122B* from *Tektronix*, which performs a direct sampling up to 24 GS/s. Our L-band signal (1530 MHz carrier) is created with quintuple oversampling on 18.36 GS/s. The sub-band modulation is QPSK for each sub-band. This results in a symbol rate of 153 MBd (306 Mbit/s) for the broadband and 1 MBd (2 Mbit/s) for the narrowband.

The 450 MHz input of the ADC is separated in the broadband and narrowband signal. Fig. 6 shows the IF signal of the ADC. The broadband signal is centered to 306 MHz and the narrowband to 135 MHz. The amplitude is scaled to full scale (FS) cause of the digital signal representation. The channel power of each sub-band is equal. A *Root-Raised-Cosine* (RCC)-filter with a roll-off factor $\alpha = 0.5$ performs the pulse shaping. The used BW for the broadband signal is 229.5 MHz and for the narrowband signal 1.5 MHz.

A *ChipScope Pro Integrated Logic Analyzer* provides snapshots of the received and processed signal from a BRAM via JTAG interface. Such a snapshot of the IQ-Signal is fed to a *Matlab*-based evaluation program, which calculates the phase offset and the QPSK demodulation. We determine the *Signal-to-Noise Ratio* (SNR) and the *Error-Vector-Magnitude* (EVM) to qualify the design. Tab. III shows the values of the broadband DSP in comparison to the VHDL simulation results.

The VHDL simulation and hardware results are quite similar. The focus of the case study was the evaluation of the broadband DSP part. Due to this the results for the narrowband processing are not mentioned. To conclude the case study we discuss the SEU rates for the broadband DSP. The following equation accumulates all SEUs from the used resources inside the FPGA.

TABLE II: Resource consumption and essential configuration bits of the implemented DDC. The table includes the resources for the framework, *ChipScope* and the PLL parametrization via SPI. In comparison *Virtex5-COTS* and *Virtex5-QV* implementation.

Resource Type	Available	*Virtex5-COTS*	*Virtex5-QV*
Flip Flops	81,920	4,538 (5.5 %)	4,555 (5.6 %)
LUTs	81,920	3,152 (3.8 %)	3,171 (3.9 %)
DSP-Slices	320	95 (29.7 %)	95 (29.7 %)
BRAM	298	11 (3.7 %)	11 (3.7 %)
Essent. CfgBits	34,087,072	862,576 (2.5 %)	885,131 (2.6 %)

TABLE III: Comparison of the simulation and hardware verification results for the broadband DSP.

	SNR	EVM
Simulation	21.17 dB	6.71 %
Hardware	19.29 dB	9.62 %

$$\mu_{\mathrm{DDC}} = \sum_{n} \left(\mu_n \cdot \frac{n_{\mathrm{Design}}}{n_{\mathrm{Available}}} \right) \tag{3}$$

$$= \mu_{\mathrm{Cfg}} \cdot \frac{\mathrm{CfgBits}_{\mathrm{Essential}}}{\mathrm{CfgBits}_{\mathrm{Available}}} + \mu_{\mathrm{DSP}} \cdot \frac{\mathrm{DSP}_{\mathrm{DDC}}}{\mathrm{DSP}_{\mathrm{Available}}} + \mu_{\mathrm{FF}} \cdot \frac{\mathrm{FF}_{\mathrm{DDC}}}{\mathrm{FF}_{\mathrm{Available}}} + \mu_{\mathrm{BRAM}} \cdot \frac{\mathrm{BRAM}_{\mathrm{DDC}}}{\mathrm{BRAM}_{\mathrm{Available}}} \tag{4}$$

The calculation includes the BRAM, which mainly used by the *ChipScope* module. Furthermore, the BRAM can be protected with ECCs to reach better upset rates. We have calculated the results for this three radiation scenarios:

- *Solar Minimum*: 0.24 upsets/s
- *Worst Week*: 91.47 upsets/s
- *Peak 5 Minutes*: 1.23 x 10^3 upsets/s

This facilitate an operation for the *Solar Minimum*. Communication algorithms like error correction on the baseband signal are needed to ensure an error-free source signal. A more complex algorithm have to be used during the *Worst Week* radiation scenario. An operation within the *Peak 5 Minutes* is complicated. We can detect the different radiations scenarios with our *BRAM Radiation Sensor* and apply an adaptive mitigation [3].

VII. Conclusion

In this paper, we proposed a FPGA-based *Digital Signal Processing* in the satellite as regenerative transponder. Due to the harsh environment the radiation effects, especially SEUs,

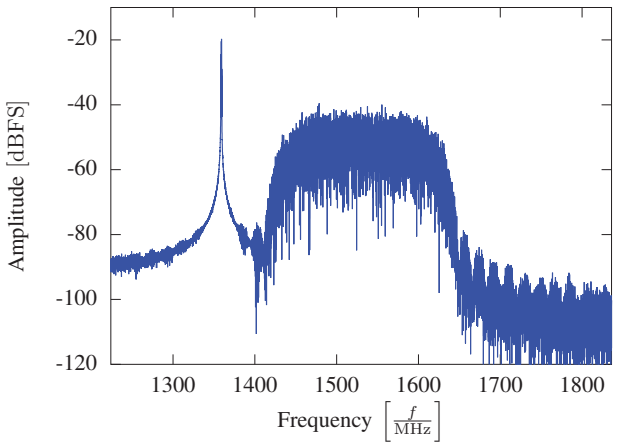

Fig. 6: Spectrum of the ADC input signal. A 1.5 MHz narrowband channel and a 229.5 MHz broadband channel.

were taken into account. We implemented a DDC, as part of the digital receiver, in our case study. The bandwidth of one broadband channel is 229.5 MHz and the symbol rate is 153 MBd at a QPSK modulation. The implementation results in 29.7 % DSP slice and 5.6 % logic occupation of one *Virtex-5QV*. The mean time to upset for this implementation is 4.11 s for the *Solar Minimum* and 0.01 s the *Worst Week* for this non-hardened design. Whereby an SEU does not create an error if a non-relevant bit is affected (e.g. SEU in a noisy bit). These are the first implementation results for the *Virtex-5QV*. We achieve an SNR of 19.29 dB with our hardware.

For future work, we want to solve the few timing errors in space-grade FPGA. We will integrate the DUC and implement a channel coding, frequency and phase synchronization for this broadband DSP. Also appropriate mitigation schemes will be implemented like *Algorithm-Based Fault Tolerance* (ABFT) for the DSPs, TMR for critical logic in the control path and EDAC for BRAM to improve the overall upset rate of the design. Of course this mitigation have to be resource and timing efficient.

With our master and slave FPGA concept we enable broadband DSP experiments, which are controlled and monitored by the high reliable master FPGA.

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