Gandhi Puvvada

Steps to run compxlib to compile Xilinx libraries in Modelsim PE Student Edition 10.0a for USC Students (EE201L/EE560)

1 Finish installing Xilinx Webpack 13.1 and ModelSim PE Student Edition 10.0a/10.0b

1.1 We assume that you have successfully installed and tested the above two tools. Make sure that we have *not* selected compatibility mode for the modelsim tool if you are a Windows 7 user. See Modelsim installation instructions.

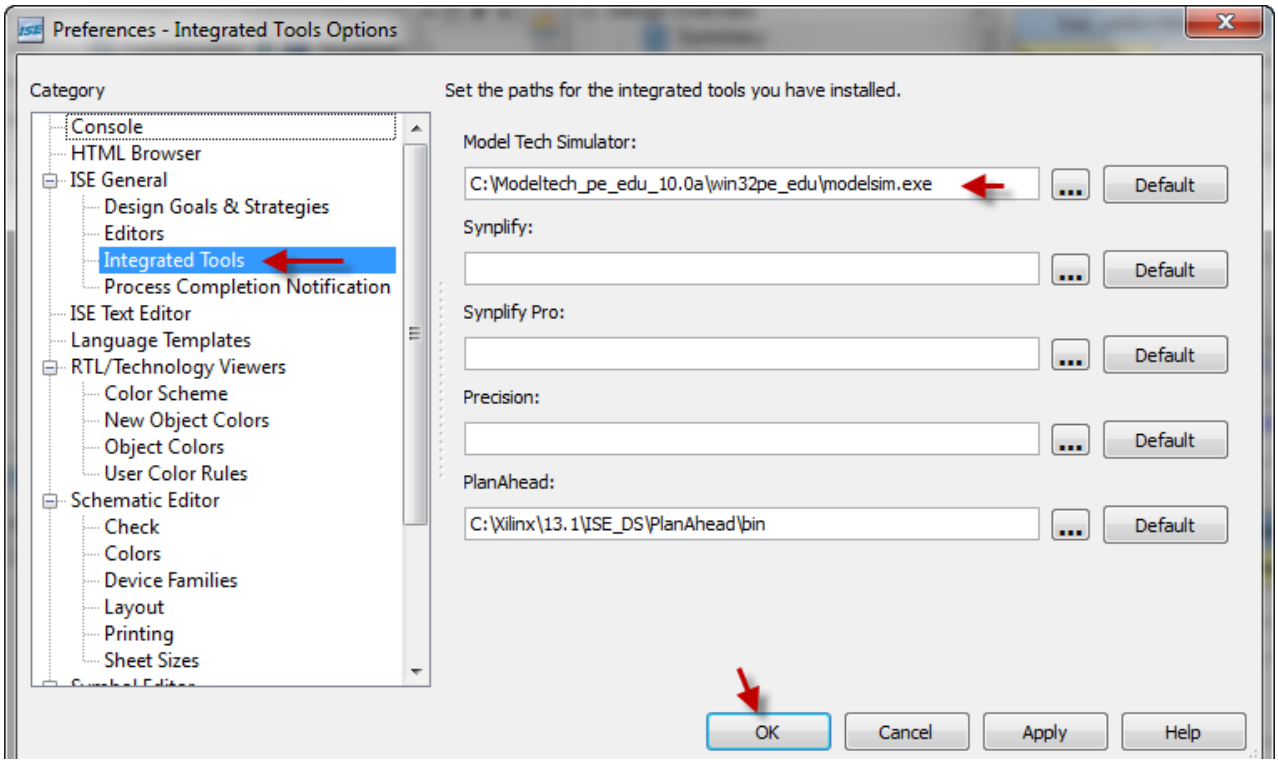
1.2 This procedure (of compiling Xilinx libraries in Modelsim using compxlib utility) is needed only if we need to perform timing simulation of designs implemented in Xilinx using Modelsim. It is needed in EE201L and in EE560. The EE201L students may be able to skip this if they finish doing the simulation on the school computers.

2 compxlib

2.1 The procedure is a little murky as we need to circumvent a bug in xilinx tools.

2.2 I have provided you a design "adder4bit_post_route_simulation". Place this design in C:\Xilinx_projects folder. Invoke Xilinx Webpack navigator and open this project.

2.2.1 Set Modelsim as the default simulator. Go to Edit => Preferences and bring up the screen below and specify the Model Tech Simulator location.



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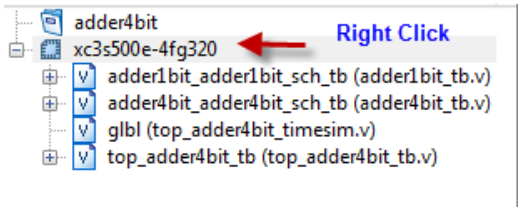
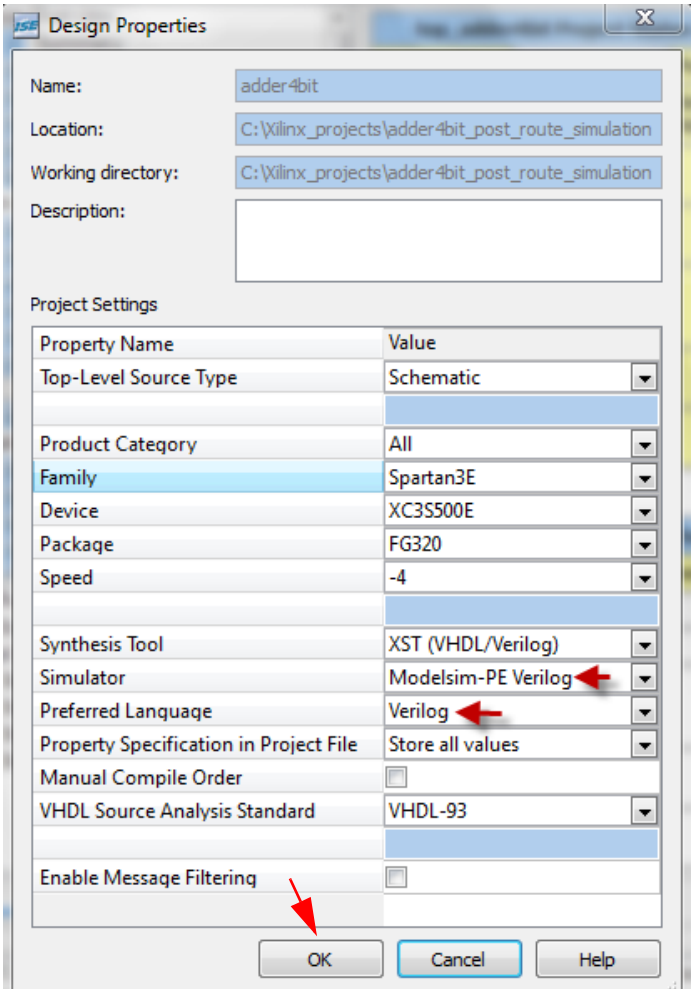
2.2.2 Also for the project, in the design properties, you can set Modelsim as the simulator of your choice.

In the implementation view, right click as shown below and select Design properties.





2.3 Open the command line window on your PC. Start => All Programs => Accessories => Command Prompt
In the command window change directory and invoke compxlib. Note: If your system is a 32-bit system, you would change directory to nt instead of nt64.

2.4 **If the gui in the next section does not let you select ModelSim PE simulator, then close the GUI and go back to the command prompt and type exactly as given below at the above prompt.** (Note: you can type compxlib - help and it displays what switches means what.)

```
compxlib -s mti_pe -p C:\Modeltech_pe_edu_10.0a\win32pe_edu -l all -arch
spartan3e -arch spartan6 -arch spartan6l -lib all -w -verbose
```

The above replaces the next 5 GUI screens. The 6th GUI screen choices are default anyways.

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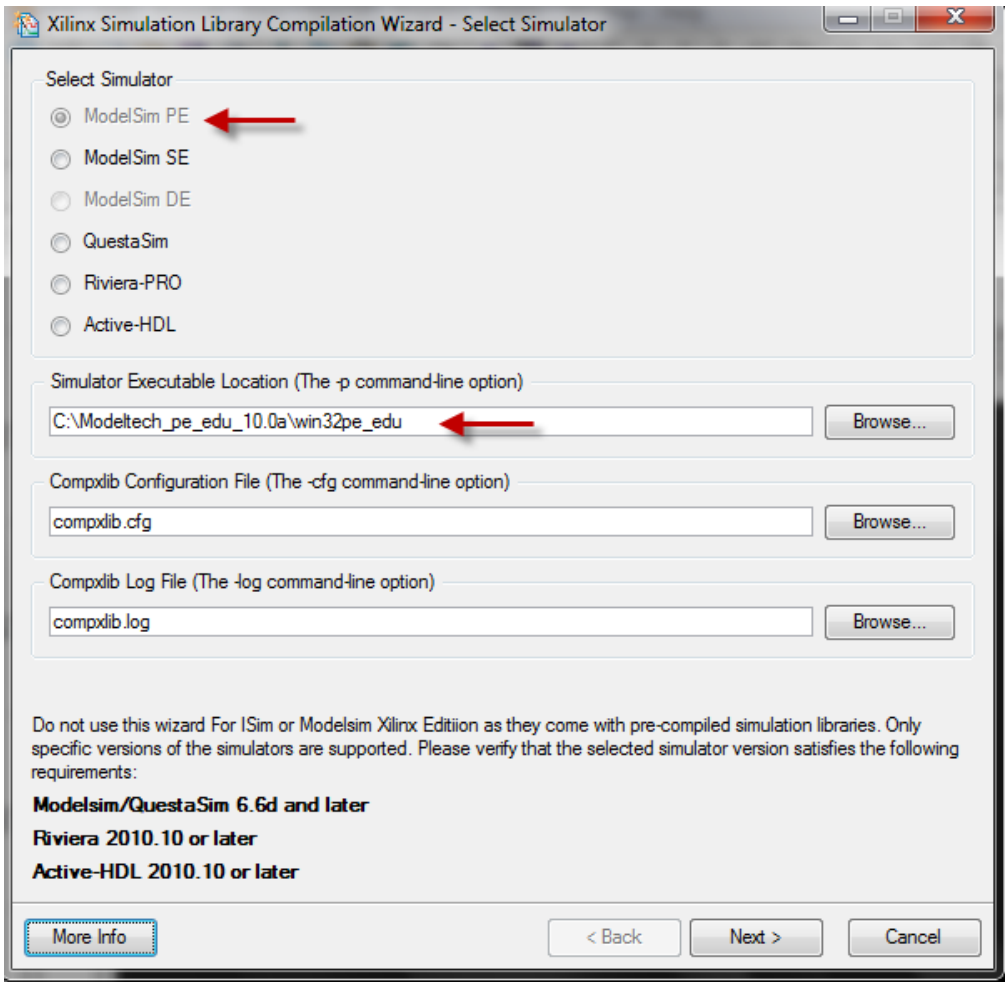
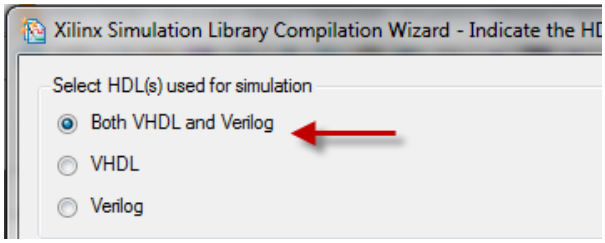
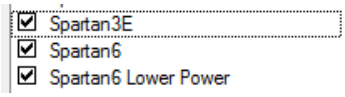
2.5



2.6



2.7



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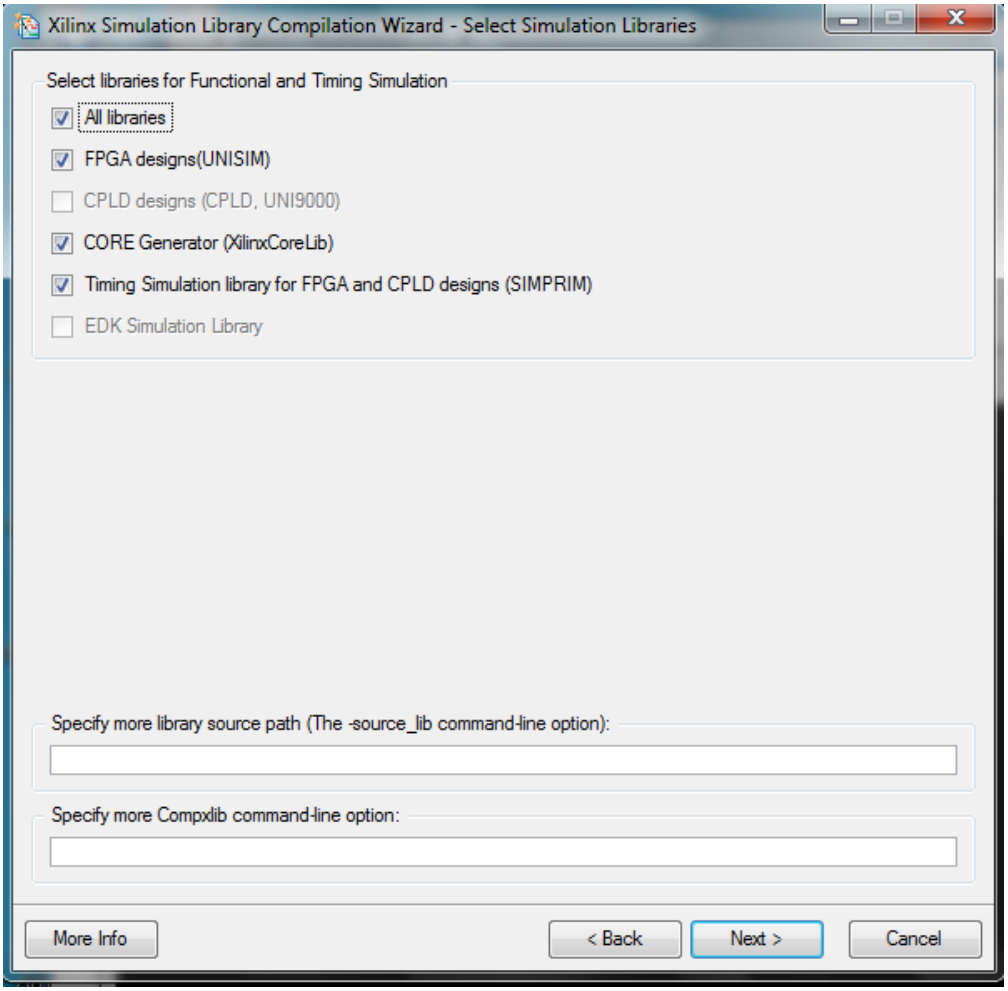
2.8



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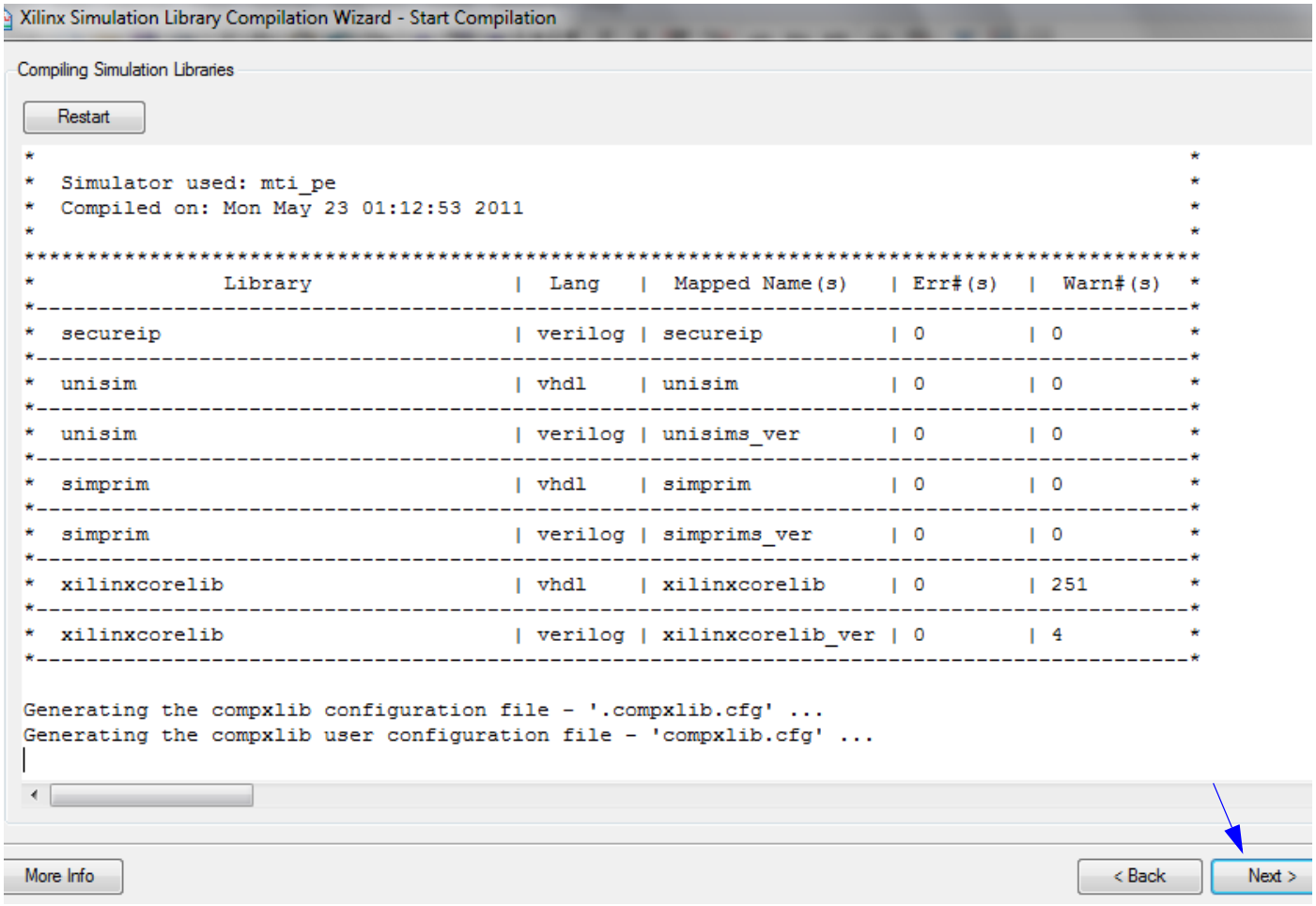
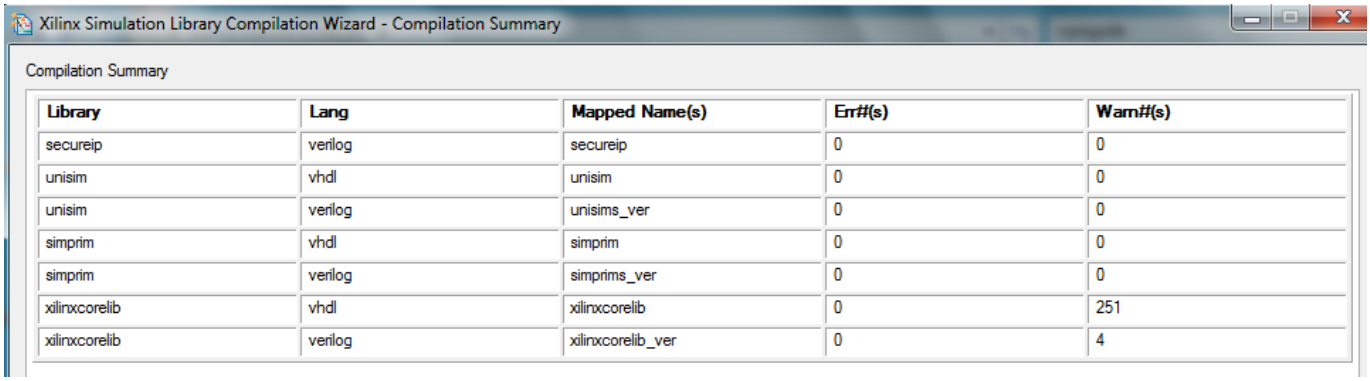
2.9



2.10 Click Finish.



2.11 You can use Windows explorer to see that several files are produced under each of these two directories

C:\Xilinx\13.1\ISE_DS\ISE\verilog\mti_pe\10.0a\nt64\
C:\Xilinx\13.1\ISE_DS\ISE\vhdl\mti_pe\10.0a\nt64\

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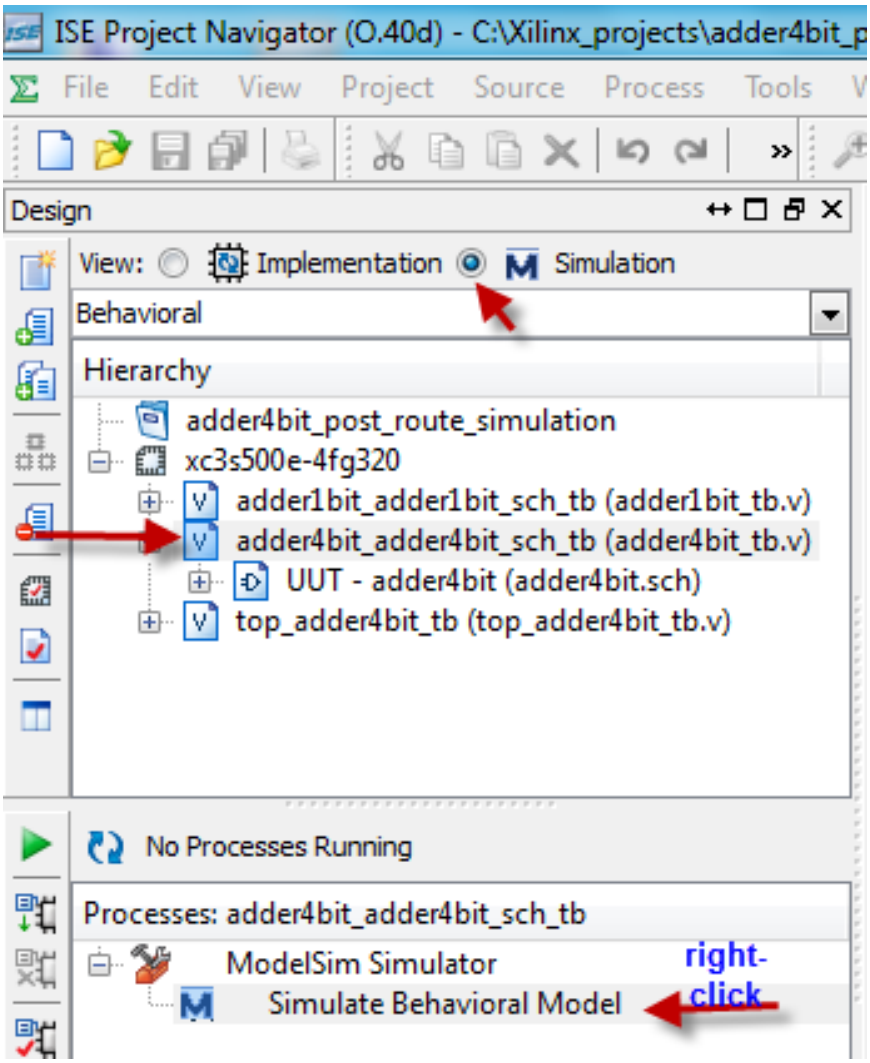
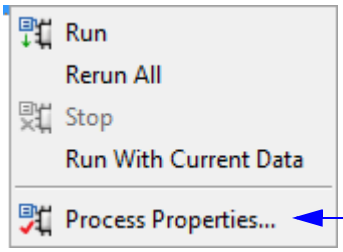
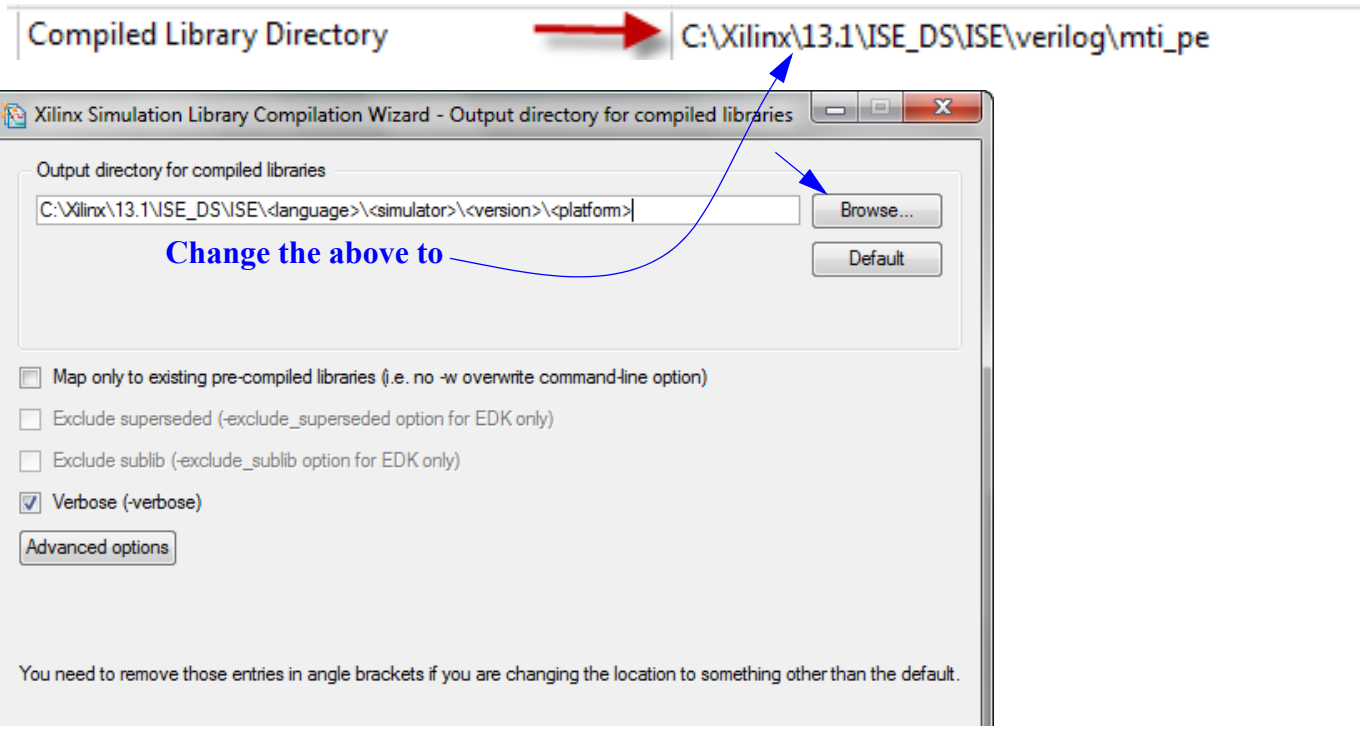
2.12







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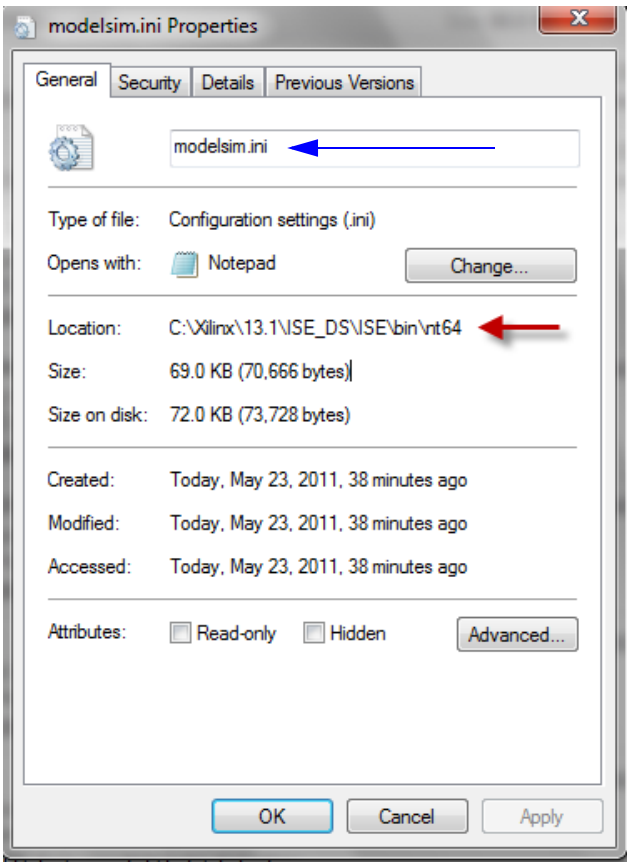
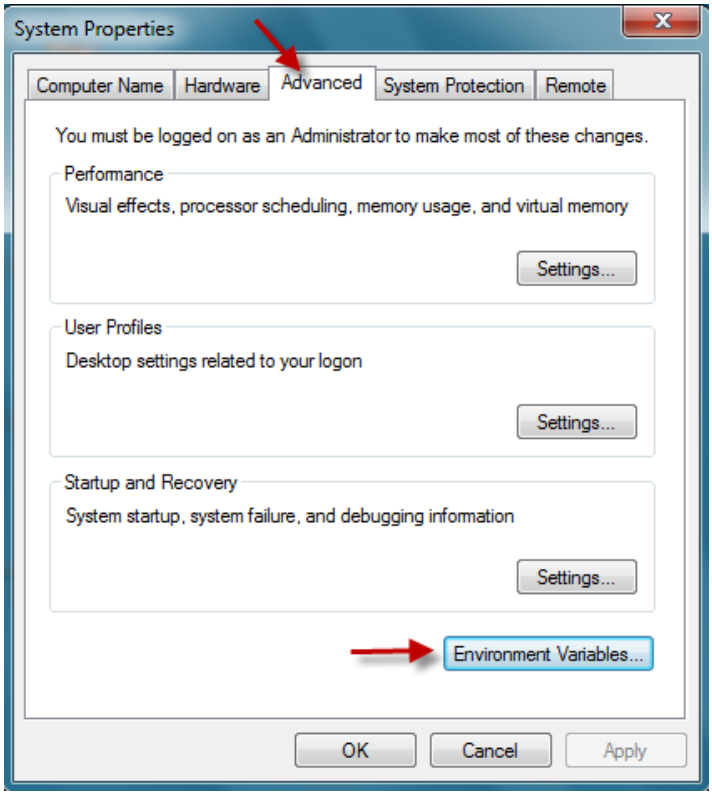
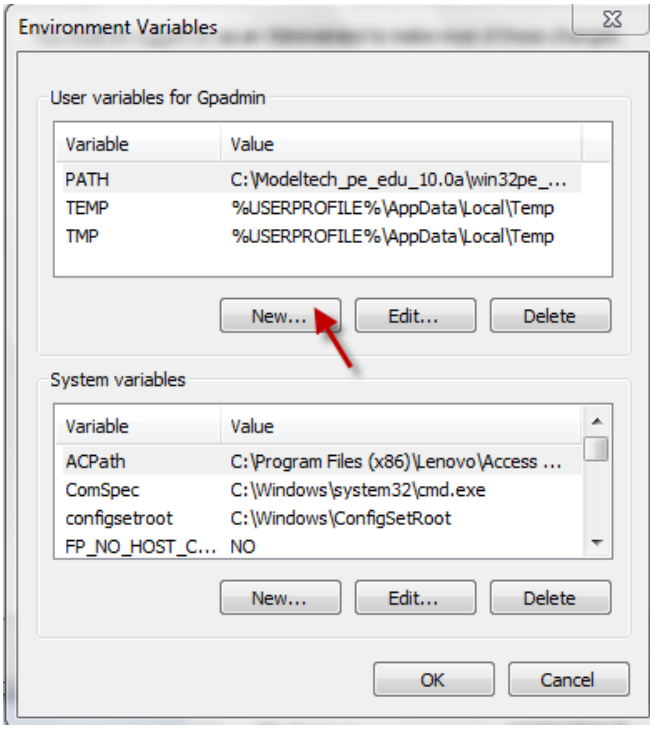
2.13 Search for modelsim.ini under C:\Xilinx and you find it



2.14





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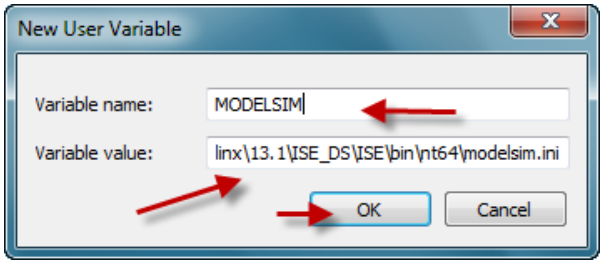
2.15



2.16 try simulating it.

```
Started : "Simulate Behavioral Model".

Creating automatic do files...
 ------------------------------------------------------------------------
 * udo file already exist (divider_tb.udo). It will not be re-generated.
 * creating main do file (divider_tb.fdo) for Behavioral Simulation...
   > executing 'C:/Modeltech_pe_edu_10.0a/win32pe_edu/vsim.exe -version' to get the mti_pe version...
   > mti_pe version is Edition
 * determining pre-compiled simulation library path information...
  > using mapping file set by MODELSIM env (C:\Xilinx\13.1\ISE_DS\ISE\bin\nt64\modelsim.ini)...
  > extracting library mapping information from 'C:\Xilinx\13.1\ISE_DS\ISE\bin\nt64\modelsim.ini'...
    > Compilation info: secureip
     ******************************************************
     + Source Library    : C:/Xilinx/13.1/ISE_DS/ISE/secureip/mti
     + Compilation Time  : Mon May 23 01:12:53 2011
     + Platform          : nt64
     + Simulator         : mti_pe
     + Simulator Version : 10.0a
     ERROR: Simulator version mismatch!
          The simulation libraries were compiled for the 'MTI_PE 10.0a' version, but
          the selected simulator is 'MTI_PE Edition'. Please recompile the libraries for
          the selected simulator version or change the simulator selection.

     + Xilinx Version    : 13.1
     + Number of Errors  : 0
     + Number of Warnings: 0
     ******************************************************

ERROR: Error(s) encountered while extracting pre-compiled simulation library information.
       Please check the log above for more details.

INFO: Simulation process aborted!
```

Good!

unfortunate!
Xilinx is yet to fix this

2.17 We found this fix.

http://forums.xilinx.com/t5/Simulation-and-Verification/webpack-13-1-config-to-run-modelsim10-0a-PE-student-ed-from-proj/td-p/134336

As per this advice change 10.0a in the line SimulatorVersion = 10.0a in 4 .rpt files in the vhdl directory and

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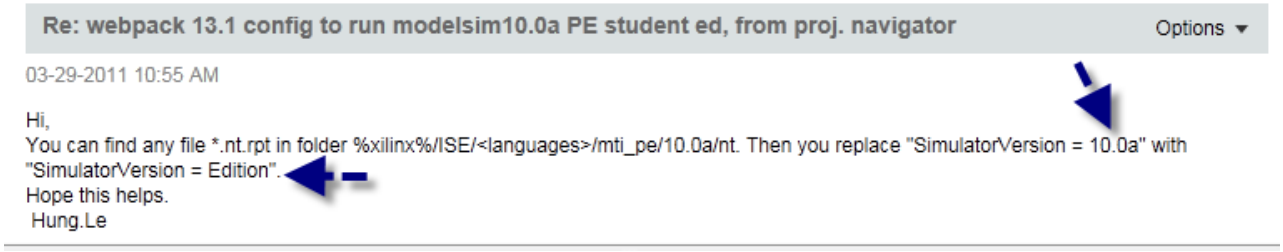
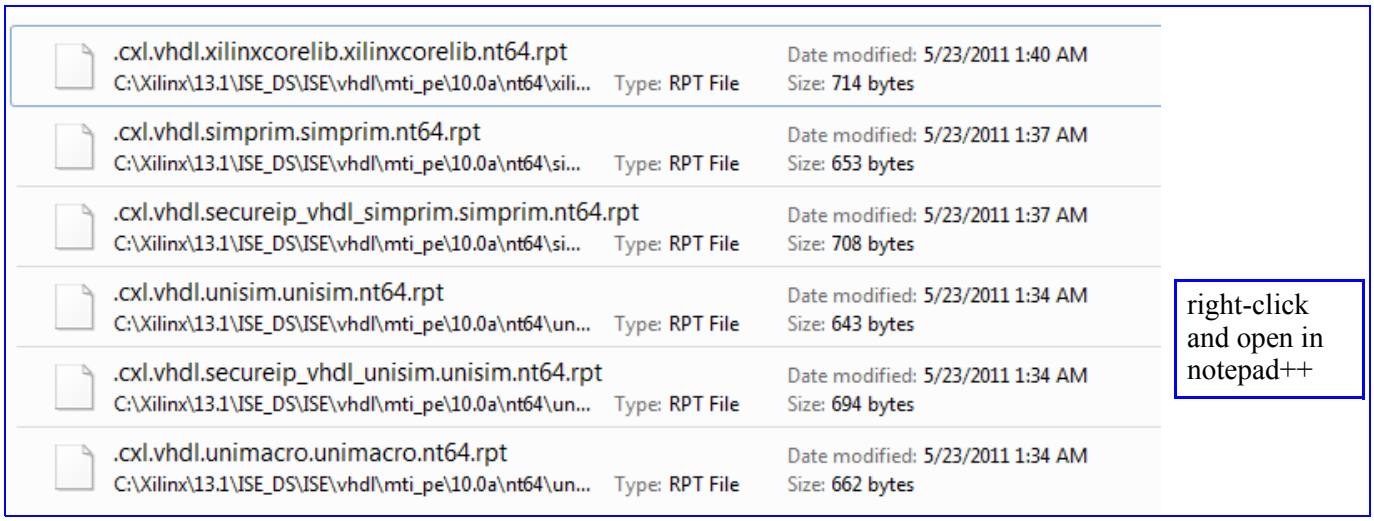
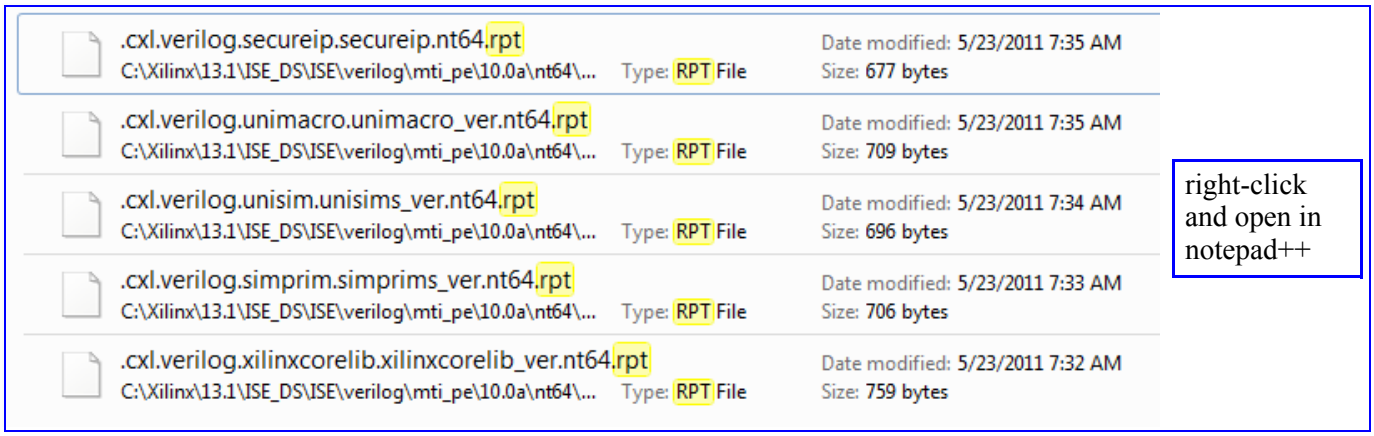
4 .rpt files in the verilog directory.



2.18 Go to the vhdl directory: C:\Xilinx\13.1\ISE_DS\ISE\vhdl
Search for .rpt files (as shown below). Open each one in notepad++ and change only one place in each of these.
Repeat the same for the verilog directory: C:\Xilinx\13.1\ISE_DS\ISE\verilog
6 .rpt file under the vhdl directory



5 .rpt file under the verilog directory



3 Now verify by performing a Post- Place & Route simulation in ISE.

3.1 Now, in ISE Project Navigator, go to Project => Cleanup Project Files .... Cleanup the files and try to perform post-route (timing) simulation. It will resynthesize, place and route the design

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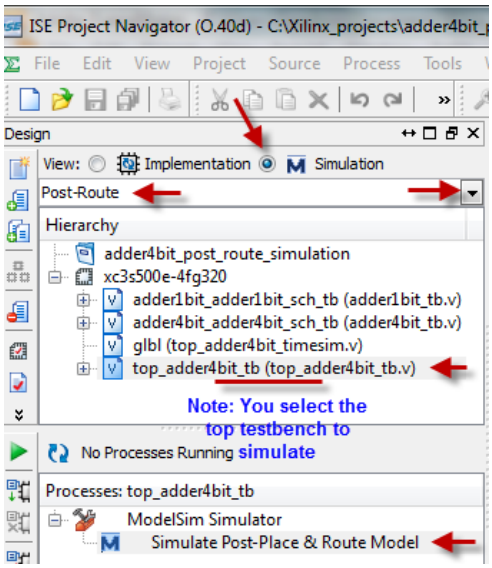
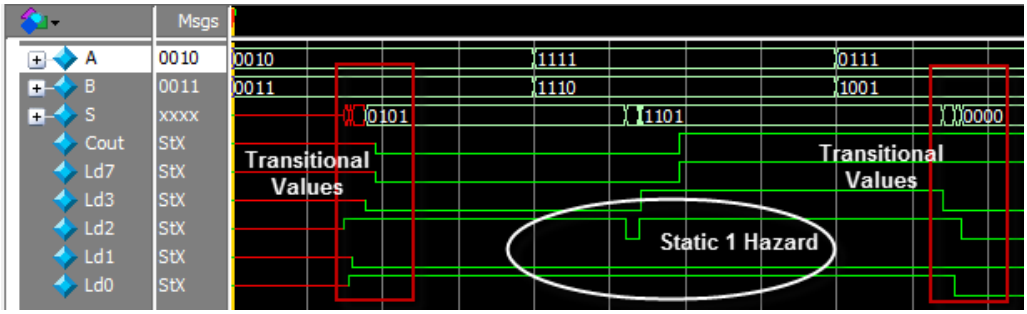
3.2



3.3 A selected portion of the waveform. Notice the actual delays of the gates and interconnect causing transitional values in the waveform



4 Celebrate your successful completion of compiling xilinx libraries using modelsim PE.

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