Electron-Induced Single-Event Upsets in Static Random Access Memory

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***Abstract*—We present experimental evidence of single-event upsets in 28 and 45 nm CMOS SRAMs produced by single energetic electrons. Upsets are observed within 10% of nominal supply voltage for devices built in the 28 nm technology node. Simulation results provide supporting evidence that upsets are produced by energetic electrons generated by incident X-rays. The observed errors are shown not to be the result of "weak bits" or photocurrents resulting from the collective energy deposition from X-rays. Experimental results are consistent with the bias sensitivity of critical charge for direct ionization effects caused by low-energy protons and muons in these technologies. Monte Carlo simulations show that the contributions of electron-induced SEU to error rates in the GEO environment depend exponentially on critical charge.**

***Index Terms*—Energetic electron, error rate, single-event effects (SEEs), single-event upset (SEU), static random access memory (SRAM).**

I. Introduction

THE semiconductor industry continues to scale complementary metal–oxide–semiconductor (CMOS) technologies to smaller feature sizes with reduced operating voltages in pursuit of performance and density goals. Continuing decreases in device dimension and operating voltage reduce the critical charge required to produce a single-event upset (SEU), significantly affecting the reliability of modern technologies in space and terrestrial environments. Decreasing critical charge has led to the emergence of SEUs induced by lightly ionizing particles, such as low-energy protons and muons [1], [2]. Traditionally, the primary radiation effects caused by energetic electrons in the trapped radiation environments of Earth and Jupiter were considered to be total-ionizing dose (TID), displacement damage, and spacecraft charging [3], [4]. However, in recent years, interest has emerged regarding effects related to the spatial distribution of charge produced by lightly ionizing particles, including high-energy secondary electrons [5]–[11]. These secondary electrons, also called δ-rays, lose their kinetic energy through ionization, producing electron–hole pairs that may cause SEUs. Various studies [5]–[11] have obtained conflicting results in attempts to quantify, primarily via modeling and simulation, the contributions of energetic electrons to the overall upset rate in memories fabricated at advanced technology nodes. Despite extensive efforts, lack of experimental data has left the role of energetic electrons in the SEU response of modern SRAMs an open question.

In this work, a low-energy X-ray source is used to generate energetic, nearly ballistic electrons to evaluate the susceptibility of CMOS SRAMs fabricated in the 28 and 45 nm technology nodes to electron-induced SEUs. Throughout this paper, "electron-induced SEUs" refer to events in which the initiating particle is a high-energy electron (δ-ray); the eventual upsets are produced by thermalized electron–hole pairs generated as the δ-rays lose their energy through ionization. Upsets are observed within 10% of nominal supply voltage for the 28 nm technology node. That these memory upsets are indeed electron-induced SEUs is supported by Monte Carlo radiation transport simulations, which show that single energetic electrons deposit sufficient ionizing energy to generate charge in the sensitive volume of the device that is well in excess of estimated critical charge values. The relative importance of electron-induced SEUs is compared to other physical processes, such as direct ionization from low-energy protons [1], [12]–[14] and muon-induced upsets [2], [15] in determining error rates in 28 and 45 nm technology generations. The impact of electron-induced SEU on scaling of feature size and voltage in modern CMOS processes, ultra-low power applications, and error rates in the space radiation environment is discussed in detail.

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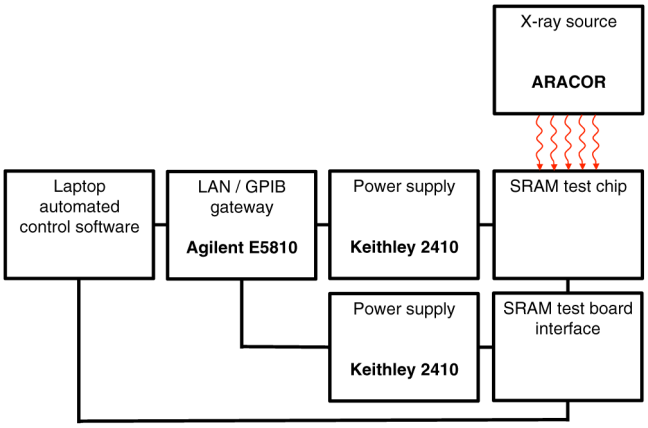

Fig. 1. An automated test system allows independent control of two Keithley 2410 SourceMeters for the SRAM test chip and test board interface through a LAN/GPIB gateway. Control commands are transmitted to the SRAM test board through a USB connection from a laptop. This system allows the supply voltage of the SRAM to be modulated *in situ*. The device under test is exposed to energetic X-rays under varied supply voltage conditions.

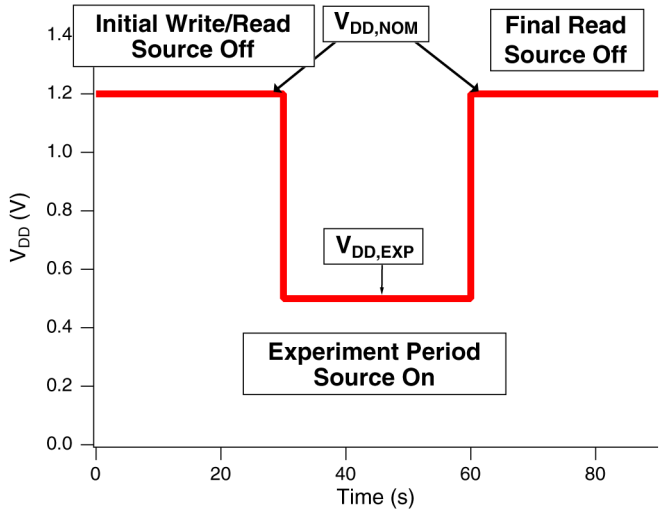

Fig. 2. Example timing diagram for measuring upsets at reduced bias. Read and write operations are performed under nominal bias condition, V_{DDNOM}. During exposure the rail is reduced to a value, V_{DDEXP}, for the duration of the experiment. Upon conclusion of the exposure, the nominal rail is restored, a final read operation is performed, and any errors recorded.

II. Electron-Induced SEUs in SRAM

The sensitivity of 28 and 45 nm bulk SRAMs to energetic electrons produced by X-rays with an ARACOR 4100 X-ray irradiator is investigated. In addition, simulations using Monte-Carlo Radiative Energy Deposition (MRED) [16] are used to quantify the contribution of energetic electrons to upset rates and to estimate error rates for trapped electrons at geosynchronous orbit.

A. Experimental Setup

A diagram of the experimental setup used to investigate electron-induced SEUs is shown in Fig. 1. An automated test system was developed to allow independent control of two Keithley 2410 SourceMeters for the SRAM test chip and SRAM test board through a GPIB/LAN gateway while sending control commands to the SRAM test board through a USB connection. This configuration allows remote control of the SRAM supply voltage and allows the power supply current to be monitored while performing parametric testing of the SRAM test chip.

Reduced supply voltage conditions are employed in this study to help determine the susceptibility of the SRAM to singly charged particles and compare the bias dependence of electron-induced upset rates to that of upsets known to be caused by low-energy protons and muons [1], [2]. Low-voltage operation has practical significance, since it is common for SRAMs in standby mode to operate at 70%–80% of the nominal supply voltage to reduce power consumption [17], [18]. Low-power applications, mobile communications, mobile computing, and medical devices also frequently employ power-saving techniques that include reducing V_{DD} during standby and idle modes of operation, making this a relevant testing approach.

Fig. 2 shows the applied bias as a function of time for a representative testing sequence employed in this study. An initial write and read, using either checkerboard or all-zero pattern, is performed at nominal bias conditions prior to X-ray exposure of the device under test (DUT). The supply voltage is then lowered while the DUT is irradiated. In the case of Fig. 2, the total exposure time was 30 s. In other experiments, the total exposure time was varied from 30 s to several minutes. Once the X-ray source was turned off, the supply voltage was returned to nominal conditions and the final state of the memory was read. The final and initial states of the memory were compared to identify any errors that may have occurred, noting the address and data patterns of observed errors for postprocessing.

During the experimental period, the range of supply voltages used in this study varies from 0.35–1.0 V. The SRAM test chips used in this work are commercial parts *designed* to operate and remain stable between 0.5–1.0 V. In functionality and parametric bench testing, the test chips were confirmed to be stable down to 0.35 V during a one-hour testing period, which is much longer than typical X-ray exposure times. Extensive testing was done prior to irradiation to demonstrate that no bit flips occurred under any bias conditions, indicating the memory was written properly and held valid information through the timing sequence shown in Fig. 2 and in all other cases shown in this work. Functionality and parametric testing was performed before and after each radiation exposure for equivalent time periods to ensure the integrity of the SRAM under all bias conditions. This procedure verifies that the data remain intact and stable at all supply voltage conditions and that no degradation due to TID has occurred during or after each X-ray exposure.

Irradiation was performed with a beam current of 1 mA and beam voltage of 50 kV. The X-ray spectra produced under these conditions are shown in Fig. 3 [19], [20]. For the unattenuated spectrum in Fig. 3, 10 keV is the average energy, and 50 keV is the endpoint bremsstrahlung energy. The interaction between X-rays in this energy range and electrons is dominated by the photoelectric effect. The generated photoelectrons are emitted omnidirectionally. The energy transferred to the generated photoelectron is described by

$$E_{e^-} = \hbar\omega - E_b \tag{1}$$

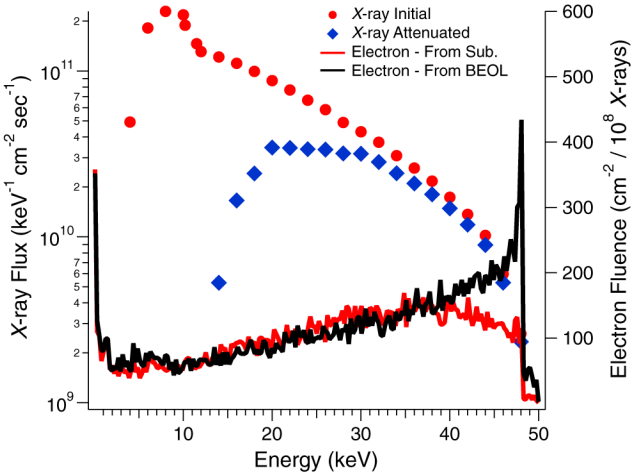

Fig. 3. X-ray and electron spectra produced by the ARACOR 4100 X-ray irradiator. The average energy is 10 keV and the maximum energy is 50 keV, corresponding to the endpoint bremsstrahlung energy [19], [20]. For the error rate testing in this study, the spectrum is modified by a 1 mm aluminum attenuator, which reduces the flux of low-energy X-rays incident onto the DUT. The electron fluences corresponding to monoenergetic 50 keV X-rays interacting with the active silicon region in the "forward" (scattering events in the active device overlayer materials, denoted BEOL) and "reverse" (scattering events in the device substrate) beam directions are shown on the right.

where $\hbar\omega$ is the incident X-ray energy, and E_b is the binding energy of the photoelectron in its initial shell. For highly energetic photons (where $\hbar\omega \gg E_b$), most of the absorbed photon energy is transferred to the photoelectron.

A 1 mm aluminum attenuator was placed above the DUT with an air gap of 3.5 cm between the attenuator and the test chip. The attenuator filters the low-energy X-ray spectrum, passing the more energetic X-rays that are more likely to produce observable electron-induced effects. This reduces the dose-rate and TID effects. Attenuation of the initial spectrum by the 1 mm layer of aluminum is calculated using the Beer–Lambert law and plotted in Fig. 3. The prominent 10 keV X-ray peak is absent from the attenuated spectrum; only the high energy tail of the X-ray distribution is capable of transporting through the attenuator and interacting with the DUT. The majority of photoelectrons generated in the attenuator are reabsorbed before leaving the Al.

Fig. 4 shows the transport of maximal energy, 50 keV, photoelectrons generated at the Al-to-air interface. The Al is on top, and the air gap is the large rectangle. The DUT is very thin and on the bottom of the figure. Photoelectrons have random trajectories. The few electrons that transport through the air gap to the DUT stop within the first few micrometers of the back end of line (BEOL) materials (metallization and dielectric layers) [21]. Therefore, only X-rays absorbed within the DUT itself generate photoelectrons that can interact with the device material in the sensitive volume of the device. An example of this type of interaction is shown in Fig. 5 where the absorption of an incident 10 keV X-ray leads to the generation of an initially free, nearly ballistic electron that deposits 9.3 keV of energy when it scatters within the sensitive volume of a 45 nm SRAM.

The electron fluence spectrum corresponding to a monoenergetic beam of 50 keV X-rays in the "forward" and "reverse" beam direction is plotted on the right-hand side of Fig. 3. The most frequent energy corresponds to the incident X-ray energy in the forward direction, which corresponds to photoelectrons generated in the BEOL materials and the active silicon region. In the reverse beam direction, corresponding to electrons generated in the substrate that transport back to the active silicon, the situation is more complicated due to the random trajectory of the generated photoelectrons. This demonstrates the random nature, in energy and trajectory, of the electron environment local to the sensitive volume.

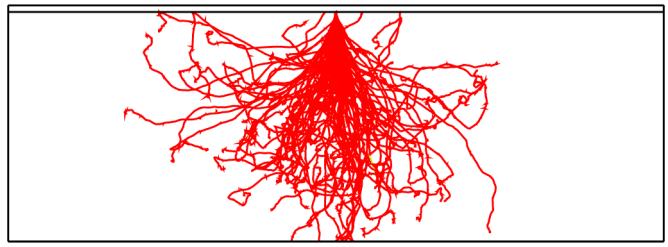

Fig. 4. 50 keV photoelectrons exiting the aluminum attenuator have insufficient energy to transport through the 3.5 cm air gap and back-end-of-line (BEOL) materials to reach the active silicon. Only photoelectrons generated in the DUT itself can interact with the device material in the sensitive silicon region.

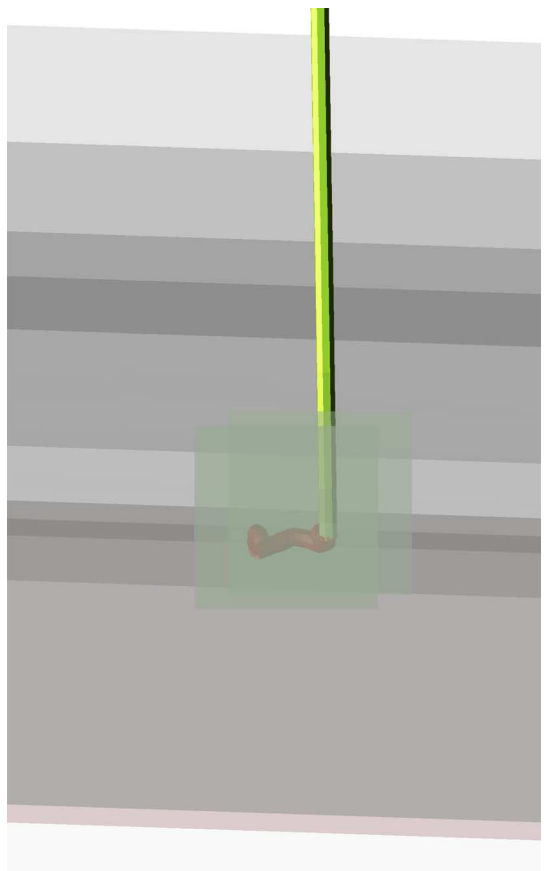

Fig. 5. A 10 keV X-ray is normally incident on the simulated device structure of a 45 nm SRAM. It subsequently undergoes photoabsorption resulting in the generation of a energetic electron. The resulting electron then transports through the device material, depositing energy in excess of 9.3 keV within the sensitive volume of the SRAM.

Following the method used in [20], flatband voltage, V_{FB}, shifts were measured with MOS capacitors to calibrate the

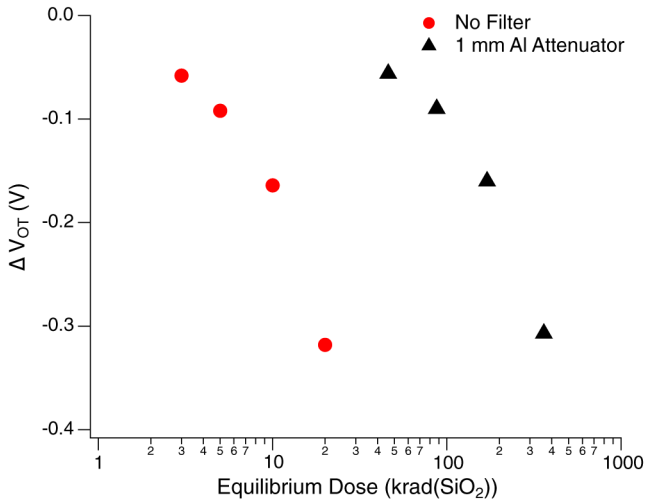

Fig. 6. ΔV_{OT} as a function of equilibrium dose for MOS capacitors irradiated with beam current and voltage of 1 mA and 50 kV, respectively. Devices were biased with 10 V on the gate during irradiation. The use of a 1 mm Al attenuator causes an increase in equilibrium dose required to achieve equivalent shifts in ΔV_{OT} by a factor of 17, indicating the nominal dose rate of 1.7 krad (SiO_2)/min is reduced to 100 rad (SiO_2)/min.

dose-rate. The devices were fabricated and packaged at Sandia National Laboratories; lids were removed for the X-ray irradiations. The calibration devices were n-type substrate MOS capacitors featuring aluminum dot gates with an area of 0.01 cm^2 and SiO_2 gate-oxide thickness of 101 nm [22]. The dose-rate calibration data are plotted in Fig. 6, which shows the change in oxide-trapped charge as determined by shifts in C–V characteristics. The equilibrium dose shown in Fig. 6 represents the nominal, unattenuated dose from the X-ray source. The measured dose-rate incident on the MOS capacitor is reduced by a factor of 17 when compared with the nominal dose rate [20]. The attenuated dose rate is 100 rad $(SiO_2)/\mathrm{min}$.

The X-ray flux is calculated by integrating over the attenuated energy spectrum in Fig. 3 and can be calculated as

$$\phi_{\mathrm{total}} = \sum_{i=0}^{\infty} \phi(E_i) \tag{2}$$

where $\phi(E_i)$ is the flux of photons with energy E_i, and ϕ_{total} represents a cumulative photon flux. Evaluating (2) with the attenuated photon spectrum yields a cumulative photon flux of 1.5×10^{12} cm^{-2} s^{-1}. Similarly, the electron flux corresponding to 50 keV X-rays is calculated to be 1.16×10^{6} cm^{-2} s^{-1}.

B. Experimental Results

Using the methods described above, several experiments exposing SRAMs to energetic X-rays were performed to investigate the plausibility of electron-induced upset events. Four types of devices were used: Test Chips A and B are 28 nm SRAMs with a capacity of 23 Mbit and nominal operating voltage of 0.9 V in triple-well (TW) and dual-well (DW) processes, respectively; Test Chip C is a 28 nm SRAM with a capacity of 32 Mbit and nominal operating voltage of 1.0 V; and Test Chip D is a 45 nm SRAM with a capacity of 4 Mbit and nominal operating voltage of 1.1 V. Normalized cross sections are obtained for each applied bias condition using the following relationship:

TABLE I
X-RAY SUPPLY VOLTAGE, EXPOSURE TIME, AND FLUENCE

	Test Chip A		Test Chip B	
V_{DD} (V)	Time (s)	Fluence (cm^{-2})	Time (s)	Fluence (cm^{-2})
0.35	40	6×10^{13}	40	6×10^{13}
0.4	130	1.95×10^{14}	120	1.8×10^{14}
0.5	310	4.65×10^{14}	300	4.5×10^{14}
0.6	620	9.3×10^{14}	630	9.45×10^{14}
0.7			1260	1.89×10^{15}
0.8			630	9.45×10^{14}
	Test Chip C		Test Chip D	
V_{DD} (V)	Time (s)	Fluence (cm^{-2})	Time (s)	Fluence (cm^{-2})
0.45	90	1.35×10^{14}	270	4.05×10^{14}
0.5	180	2.7×10^{14}	30	4.5×10^{13}
0.55	180	2.7×10^{14}	360	5.4×10^{14}
0.6	540	8.1×10^{14}	860	1.29×10^{15}
0.65	300	4.5×10^{14}	1080	1.62×10^{15}
0.7	600	9×10^{14}	528	7.92×10^{14}

$$\sigma(\mathrm{V_{DD}}) = \frac{N}{A_{\mathrm{cell}}\Phi} \tag{3}$$

where N is the number of observed errors, A_{cell} is the cell area of the SRAM being tested, and Φ is the photon fluence. Error bars are shown at the one-sigma confidence interval in all experimental and simulated cross sections. Table I shows the experimental supply voltage conditions, exposure time, and corresponding X-ray fluence for measurements on each test chip.

Fig. 7 plots the normalized cross section, as described in (3), as a function of supply voltage for SRAM test chips exposed to X-rays. Fig. 7 shows that errors are observed when these devices are biased between 0.35 V and 0.8 V while exposed to X-rays. The resulting upset cross section of all test chips exhibits an exponential dependence on applied bias because of the voltage dependence on critical charge. This is consistent with well-established test procedures used for assessing the single-event error rates for protons and muons [1], [2]. In the case of Test Chip B, upsets were observed within 10% of the nominal supply voltage of 0.9 V, which is within the designed operating voltage range for the SRAM. Each of the SRAM test chips exhibits a cross section less than the total cell area at all supply voltages, resulting in normalized cross sections less than unity. All observed errors had unique memory addresses, strongly suggesting that errors occurred randomly within the memory array during experiments and were not caused by repeated bit-flips in "weak" cells. Again, we note that no bit-flips occurred due to reduced bias conditions during functionality and parametric tests before and after X-ray irradiation of all test chips under all bias conditions, indicating the memory operated under stable conditions during experiments.

Photocurrents produced by the overall photon flux are generated as the result of X-ray irradiation. The generated photocurrent produced by the collective effect of the X-ray source can be calculated as

$$I_{\mathrm{PC}} = qV\dot{D}_{\mathrm{SiO_2}}\dot{R}_{\mathrm{SiO_2}} \tag{4}$$

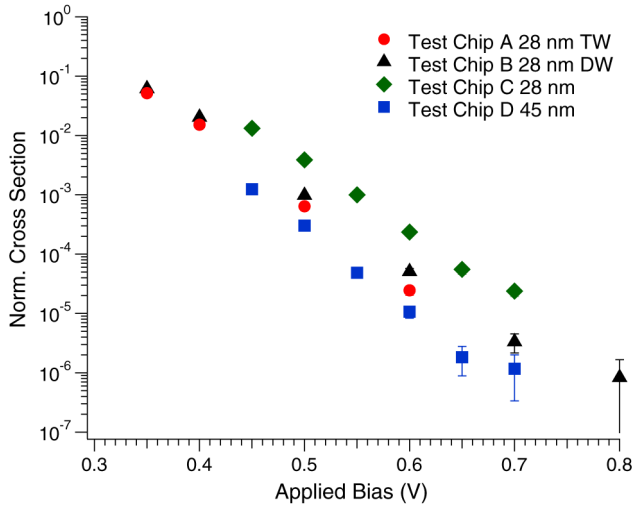

Fig. 7. Experimental errors induced during irradiation with X-rays in an ARACOR 4100 X-ray irradiator. The bias sensitivity of critical charge in SRAMs provides strong evidence of energetic electron-induced upsets in modern SRAMs.

where q is elementary charge, V is the volume of an SRAM cell, $\dot{D}_{SiO_2}$ is the dose rate in SiO_2, and $\dot{R}_{SiO_2}$ is the density of electron–hole pairs generated per rad(SiO_2). The generated collective photocurrent in an individual SRAM cell is calculated with (4) to be approximately 1 fA. SPICE simulations were performed for 28 nm SRAM Test Chips A and B for each experimental bias condition. The simulation results indicate restoring currents are greater than 100 nA at the lowest experimental supply voltage, 0.35 V. Hence, as expected, collective photocurrents generated in X-ray experiments are significantly smaller than the restoring current of SRAM cells and are incapable of causing the observed errors. Furthermore, the probability of coincident photon events contributing to the error rate can be calculated as

$$Pr(X_1 \| X_2) = (\phi A_{\text{cell}} \tau)^2 \tag{5}$$

where ϕ is the incident photon flux, A_{cell} is the cell area, and τ is the characteristic time for an upset event (in this work, this is assumed to be 10 ns). Evaluation of (5) for the 28 nm and 45 nm SRAMs results in probabilities of 6.45×10^{-10} and 1.9×10^{-9}, respectively, of coincident photons contributing a single upset to the experimental results. The contribution of coincident photons to the observed upsets on the time scale considered in this work is therefore negligible.

Lastly, it is important to monitor the TID accumulated by the test chip, since this can lead to degradation of the memory and result in a loss of functionality [23]. The dose accumulated in the experiments for the triple-well 28 nm bulk SRAM, Test Chip A, was less than 1.9 krad(SiO_2). The dual-well SRAM, Test Chip B, accumulated 5 krad(SiO_2) during the experiments. Test chip C, a 28 nm SRAM, accumulated a dose of 5.4 krad(SiO_2), and Test Chip D, a 45 nm SRAM, accumulated a total dose of 11.1 krad(SiO_2). Test chip C, a 28 nm, 32 Mbit bulk SRAM, underwent the largest change in power supply current based on measurements before and after irradiation, where the pre- and postirradiation power supply currents were 82.7 mA and 81.5 mA, respectively. This is a decrease in power supply current of less than 1.5%. Similarly, none of the other devices discussed in this work accumulated sufficient dose to compromise memory operation or cell integrity.

The above results and analysis demonstrate that, for the experimental conditions considered here, single energetic electrons produced by X-ray irradiation are by far the most likely cause of the observed errors within the SRAMs.

C. Simulation of X-ray Energy Deposition in SRAMs

Radiation transport simulations were performed with MRED [16], a Geant4-based code (version 9.6p2) [24] with Fortran extensions that include PENELOPE 2008 [25], to evaluate the potential impact of electrons produced by energetic X-rays on the device SEU response. PENELOPE 2008 extends the low-energy range for electromagnetic processes from 250 eV down to approximately 100 eV and also tracks electrons with greater spatial resolution. These refinements produce increased fidelity of energy deposition estimates in the small sensitive volumes of interest in this work.

High-energy protons cause single-event effects primarily through secondary ions produced in nuclear reactions [1], [12], [13], [26]. For a given proton energy, experimental cross sections are expressed with reference to the primary proton flux, regardless of the upset mechanism. In this sense, the case of single-event effects caused by secondary electrons is analogous. Results in this work are therefore plotted as a function of the incident X-ray fluence, which provides the most consistent reference for analyzing single-event effects caused by secondary electrons. The X-ray energy used in the simulations, 50 keV, is representative of the end-point bremsstrahlung within the X-ray spectrum and results in the generation of the most energetic and ionizing secondary electrons. We simulate a 4 kbit SRAM array using a sensitive volume structure consistent with a 45 nm bulk SRAM using MRED. Energy deposition is calculated for individual X-rays on an event-by-event basis. The sensitive volume geometry used was 0.22 μm^2 $\times$ 500 nm, which is representative of 45 nm processes in the ITRS roadmap [27]. In addition, the simulated structure includes the 1 mm aluminum attenuator and appropriate BEOL thickness with 15 μm of oxide and metallization. The SRAM was simulated to a total 50 keV photon fluence of 2×10^9 cm^{-2}. This fluence was found to be sufficient to determine the energy deposited and ultimately estimate the resulting error rate with adequate precision to compare with the experimental data. The vertical black lines in Fig. 8 represent estimates of critical charge for 45 nm SRAMs as in [9] for supply voltages of 0.55 V and 1.1 V, which correspond to 0.19 fC and 0.38 fC of generated charge, respectively, and are used to indicate the charge generation required to upset cells.

Simulated integral cross sections are shown in Fig. 8, indicating that secondary electrons generated by the incident X-rays are capable of depositing sufficient energy to exceed the critical charge estimate of a 45 nm SRAM. The eventual upsets result from collection of thermalized electron–hole pairs generated by the high-energy electrons. These results, suggesting energetic electrons are capable of depositing sufficient ionizing energy to exceed the critical charge of 45 nm SRAMs operating

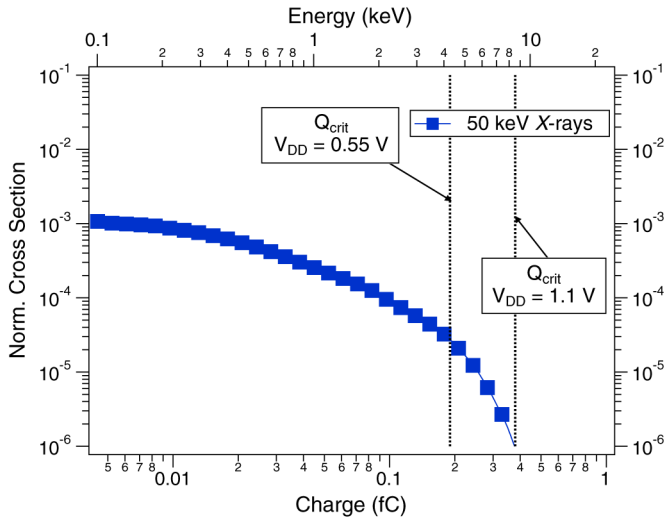

Fig. 8. MRED simulation results of mono-energetic, 50 keV X-rays normally incident on a 45 nm bulk SRAM structure. The vertical black lines represent the lower limit estimates of critical charge for a 45 nm SRAM. The results provide supporting evidence suggesting that energetic electrons generated by incident X-rays are capable of depositing sufficient energy to exceed the estimated upset threshold.

under reduced supply voltage, are consistent with previous computational results reported in [9] and [10]. The normalized cross section in Fig. 8 at a supply voltage of 0.55 V agrees with experimental test results from Test Chip D in Fig. 7 within a factor of two. These results suggest that the 45 nm SRAM is relatively insensitive to single-electron SEU at nominal supply voltage, consistent with the SEU data in Fig. 7. These simulation results confirm that energy deposition from energetic electrons generated in photoabsorption events is the most likely explanation for the experimentally observed upsets in Fig. 7.

D. Comparison to Low-Energy Proton and Muon SEUs

With the observation of electron-induced SEU, it is quite useful to quantify the significance of this effect relative to other well-understood phenomena. To this purpose, we compare the data set presented in Fig. 7 to SEU data sets obtained with low-energy protons and muons.

Low-energy proton experiments were performed in the Pelletron facility at Vanderbilt University. Experiments were performed under vacuum with a monoenergetic proton beam at an energy of 3 MeV normally incident on Test Chip B and 1 MeV normally incident on Test Chip D. The sensitivity of the 28 nm SRAM test chip was investigated for supply voltage in the range of 0.35–1.0 V. The 45 nm SRAM test chip was investigated for applied biases of 0.8–1.2 V. The timing sequence for applied bias during experiments with low-energy protons is identical to that of Fig. 2. Parts were tested to a fluence of 10^{12} cm^{-2}

Muon experiments were performed at TRIUMF using the M15 beam line. Low-energy positively charged muons with a known energy distribution were normally incident on Test Chips A and B, 28 nm bulk SRAM, and Test Chip D, a 45 nm SRAM. The muon beam energy characterization at TRIUMF is described in [2]. The incident muon energy was varied by means of a tunable momentum filter [2], [15]. The timing sequence for applied bias during experiments with low-energy muons is identical to that of Fig. 2. Parts were exposed to a total fluence of 6.2×10^8 cm^{-2}. A normalized upset cross section is obtained for muons and low-energy proton experiments from (3).

Fig. 9(a) and (b) show SEU data from low-energy proton and muon experiments plotted alongside electron-induced SEU data from Fig. 7 for 28 nm and 45 nm test chips. Data shown in Fig. 9 are normalized to error rates observed during X-ray irradiation at 0.35 V for Test Chips A and B, and 0.45 V for Test Chip D. All test chip samples exhibit exponential SEU cross-section dependence on applied bias, consistent with previous results [1], [2]. Electron sensitivity is observed within 10% of nominal bias conditions for Test Chip B, indicating that SEUs initiated by high energy electrons may be observable in more sensitive present-generation ICs, and at nominal supply voltages for future technology nodes. We note that, under nominal bias conditions, Test Chips A, B, and D exhibit sensitivity to muons and protons, while no events initiated by single high-energy electrons are observed. This indicates that high-energy electrons are much less important than protons and muons for SRAMs from these technology nodes, operating at or near nominal bias conditions.

As the applied bias is reduced, electron-induced SEUs exhibit a larger dependence on supply voltage (a larger slope) than muons and protons in the 28 nm and 45 nm technology nodes.

E. Electron-Induced SEU Event Rates

Comparing the experimental cross sections in Fig. 9 indicates the sensitivity of SRAMs to protons, muons, and X-rays, but event rates depend on the flux of these particles for different environments. Trapped electrons form two different belts in the near Earth radiation environment, each with distinct characteristics [3], [4].

We have evaluated SEU event rates for trapped electrons at geosynchronous orbit during solar maximum with 150 mils of aluminum shielding using spectra obtained from the AE-8 model. The differential flux spectrum of incident electrons through 150 mils of aluminum shielding is plotted in Fig. 10(a). The trapped electron environment described in Fig. 10(a) is much more energetic than the generated electron spectrum used in our X-ray experiments. The most energetic electrons at geosynchronous orbit during solar maximum have energy of approximately 5 MeV, which would require 500 mils of aluminum shielding to attenuate completely. MRED was used to model the interaction of the electron particle spectrum with the semiconductor materials. The material structure is identical to the structure from Fig. 8, corresponding to a 45 nm bulk SRAM.

Fig. 10(b) shows the resulting simulated event rates (left axis) as a function of generated charge (bottom axis) within the sensitive volume of a single SRAM cell. Electron energy deposition events rarely exceed 10 keV, which is consistent with Fig. 8 and [9], [10]. Fig. 10(b) demonstrates the rare nature of electron-induced SEU events in the space radiation environment, indicating that many years of flight time may elapse before the observation of such an event is expected for a typical 45 nm bulk SRAM operating under nominal bias conditions. Fig. 10(b)

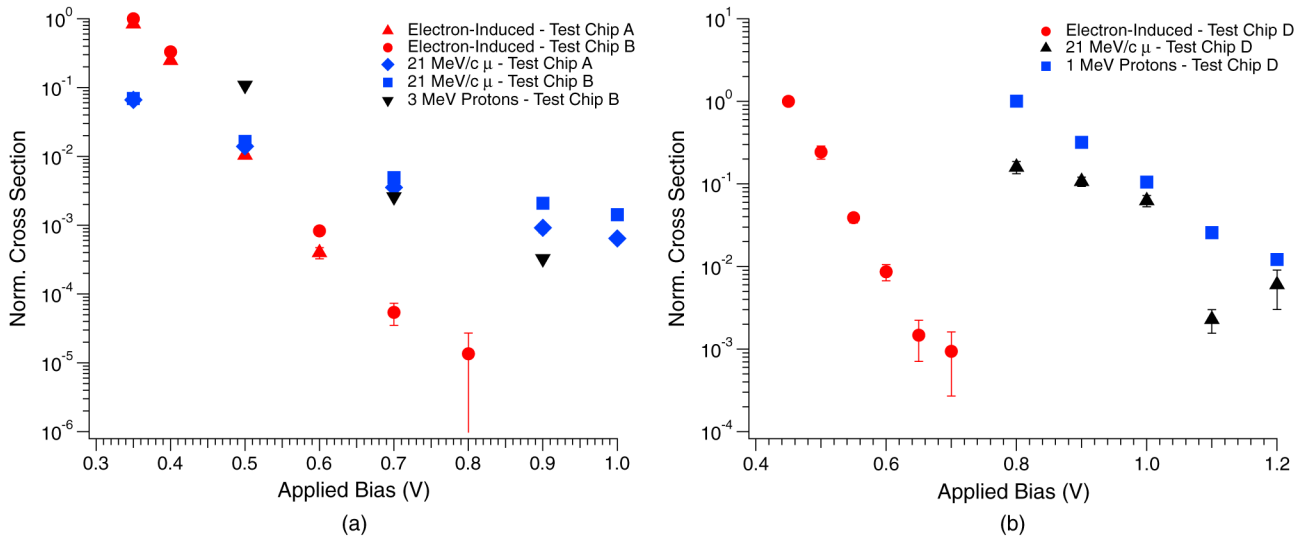

Fig. 9. SEU cross-section dependence on supply voltage for electron-induced SEU cross sections observed during X-ray irradiation, compared with low-energy protons and muons in (a) 28 nm and (b) 45 nm SRAMs. Data shown are normalized to X-ray data at 0.35 V for Test Chips A and B, and 0.45 V for Test Chip D. Results show that, under nominal bias conditions, protons and muons are capable of inducing upsets in 28 nm and 45 nm SRAM while this sensitivity is absent for energetic X-ray electrons generated during X-ray exposure. Under reduced bias conditions, electron-induced SEUs exhibit a larger dependence on supply voltage than muons and protons in the 28 nm and 45 nm technology nodes.

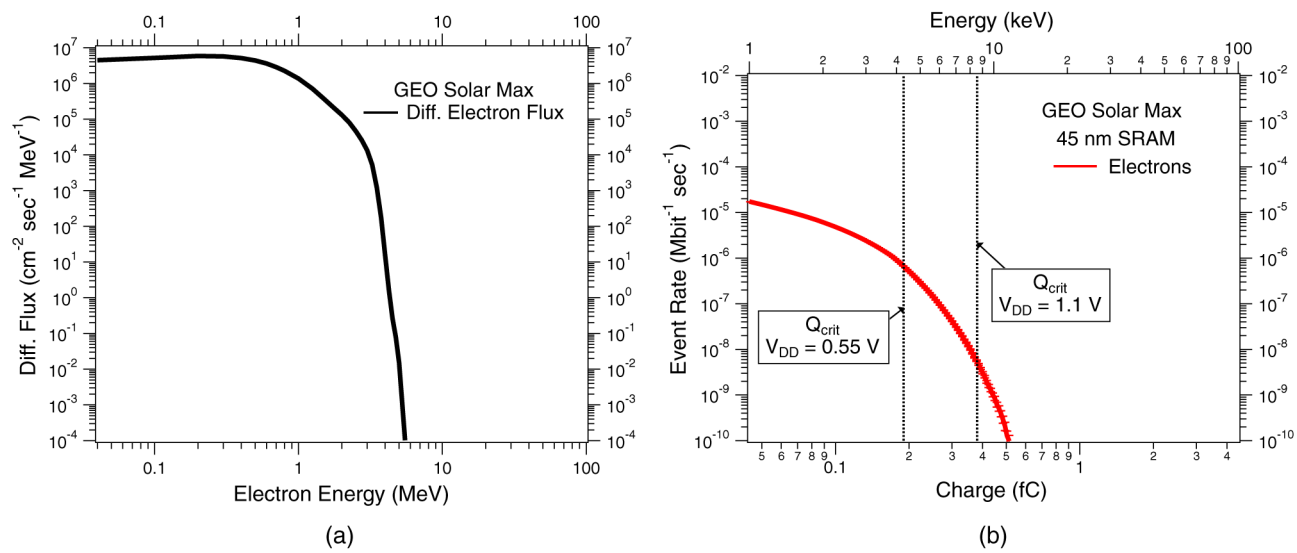

Fig. 10. MRED simulations performed on the 45 nm structure from Fig. 8 using the AE-8 description of the electron environment, at geosynchronous orbit during solar maximum with 150 mils aluminum shielding. The differential flux spectrum of incident electrons is plotted in (a). Simulation results show that the event rate of electrons is small for devices operated under nominal supply voltage, as seen in (b). However, more sensitive devices will experience a significant increase in single electron events. These results suggest that operating SRAMs under reduced bias conditions will result in a dramatic increase in single electron events.

shows that the event rate depends strongly on the critical charge of the SRAM; a reduction of critical charge from 0.4 fC to 0.2 fC results in a change in event rate of approximately two orders of magnitude. Employing more sensitive SRAM technologies or operating at reduced supply voltage conditions has a direct and significant impact on SRAM error rates. In contrast, total error rate predictions for a 65 nm SRAM at geosynchronous orbit in the solar minimum environment are on the order of 2.4×10^{-6} Mbit^{-1} s^{-1} [14]. At geosynchronous orbit in "worst-day" conditions, error rates for the same 65 nm SRAM are as high as 3.6×10^{-3} Mbit^{-1} s^{-1} [14]. This indicates that the error rates at geosynchronous orbit of larger technology nodes with higher critical charge are roughly 2.5–5 orders of magnitude higher than our estimates of electron-induced error rates at nominal bias conditions.

III. Summary and Conclusion

Evidence of single electron-induced SEU in 28 and 45 nm CMOS SRAMs is presented. Energetic electrons are generated by exposure of the SRAMs to an X-ray source and an Al attenuator. The experimental SEU cross-sections depend exponentially on applied bias, consistent with previous experimental results obtained with muons and low-energy protons. No errors were observed in functionality and parametric testing before and after irradiation of all test chips under all applied bias conditions. This demonstrates that test chips remained stable during

X-ray irradiation. Thus, errors are not due to "weak bits" or photocurrents resulting from the collective energy deposition of the X-rays. Instead, our results and analysis strongly suggest that the observed errors are the result of single energetic electron scattering events within SRAM cells. The event rate of electron-induced SEU is low at geosynchronous orbits for the devices we have evaluated. Moreover, electron-induced upsets only occur at measurable rates under reduced bias conditions for present generation technology. This suggests that the overall contribution of energetic electrons to error rates is small in present-generation technology. We conclude that electronics designed to operate with ultra-low power likely will exhibit higher relative sensitivity to energetic electron induced upsets. This represents an additional design concern for both space and terrestrial environments, to avoid unexpectedly high upset rates from lightly ionizing particles.

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