Optimized Robust Digital Voter in TMR Designs

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***Abstract*—Nanoelectronic systems are now more and more prone to faults and defects. Redundancy techniques are implemented widely to increase the reliability. However, many researches are based on the assumption that the voter is perfect while this is not true. This paper proposed a fault-tolerant and simple majority voter structure for TMR. Experimental results show its optimization over the formers.**

I. Introduction

Redundancy techniques such as N-tuple modular redundancy (NMR) is now widely used to correct faulty behavior and achieve high reliability [1], [2]. NMR consists of $N+1$ components: N replicas of the module **M** and a voter **MAJ**.

NMR systems require a voter in order to decide the final output. There are several voting strategies such as majority, median or plurality [3]. The majority voter implements more efficiently at the low redundancy factors ($N < 7$) [4]. Most of the former research works are based on the assumption that the voter is hardened structured [1], [2]. However, voter circuit also introduces new locations where faults may occur.

This work presents a fault-tolerant majority voter for TMR designs. Section II presents some preliminaries of NMR. Section III introduces the proposed majority voter. In section IV, performances of the proposed voter are compared. Finally, section V outlines some conclusions.

II. Reliability Analysis of TMR Strategy

The reliability of a NMR system based on majority voter can be given by the expression (1).

$$R_{NMR-IV} = R_{MAJ} \times \sum_{i=\lceil N/2 \rceil}^{N} \binom{N}{i} q_M^i \left(1-q_M\right)^{N-i} \quad (1)$$

Notice that q_M gives the probability that a module generates correct outputs and $\binom{N}{i}$ represents the amount of possible combinations with i correct modules and $N-i$ faulty modules. Here we consider that voter may fail, which is a more realistic hypothesis, the probability of correctness at the output will decrease according to the reliability R_{MAJ}.

Figure 1 shows the impact of the voter's reliability on the global reliability of a TMR system. It supposes $q_{MAJ} = q_M$.

III. Majority voter structures in TMR

TMR is designed under the hypothesis of single-fault models which is also considered in this work.

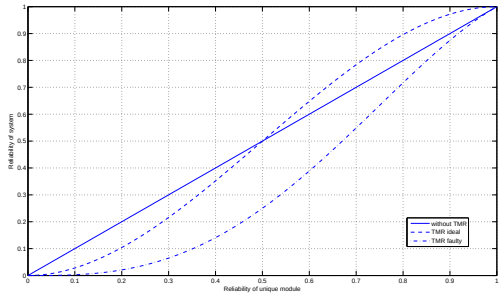

Fig. 1. Reliability curves for TMR with ideal and faulty voter.

A. Classic voter

The scheme of classic voter as shown in Figure 2 derives directly from the canonic boolean expression in (3). However, this structure masks the single-fault only if it occurs on one module **M**. If **AND** or **OR** gates in the voter fail, it is possible to output an incorrect value. For example, if $A = B = C = 0$ and there is an unique fault in $S1$, the output will be $V = 1$ which is an incorrect value.

$$V = ABC + AB\overline{C} + \overline{A}BC + A\overline{B}C \quad (2)$$
$$= AB + BC + AC \quad (3)$$

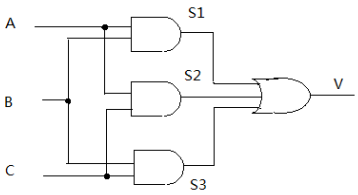

Fig. 2. Conventionall scheme for the majority voter.

In [5], a fault-tolerant voter named *NFTVC* is proposed as shown in Figure 3. The circuit contains a priority encoder designed to output a selecting signal for the multiplexer. With $A = B = C = 0$, if any of the nodes in the voter, i.e. either $S1$ or $S2$ is stuck to 1, the circuit will still produce the correct output as 0. This voter structure is fault-tolerant but not succinct.

- if $I1 = 0$, then $sel = 0$ and A (equals to B) is going to be selected as the output;

- if $I2 = 0$, then $sel = 1$ and C (equals to B) is the selected output.

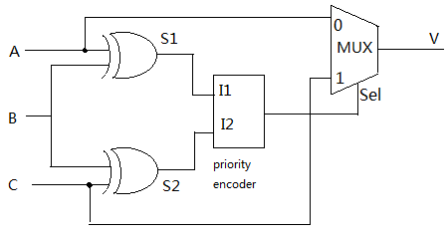

Fig. 3. Kshirasgar's scheme for the majority voter (NFTVC).

B. A simple fault-tolerant voter

In this work we propose an alternative scheme for majority voting presented in Figure 4. We can see that this structure is fault-tolerant following the analysis below:

a) A fault occurs on the voter: It means that the unique internal node S is stuck to a fault. Due to the single-fault model, the output is correct, independent of the value S ($A = B = C$)

b) A fault occurs on one of the modules M:

- Case 1 (C is faulty): the logic signals A and B are the same and $S = A \oplus B = 0$. So, the multiplexer's output will be signal B which represents the majority value.
- Case 2 (A or B is faulty): the logic signals A and B are different and the majority must be the logic value given by $AC + BC$, which corresponds to logic value C. According to the scheme, this relation is respected because $S = A \oplus B = 1$.

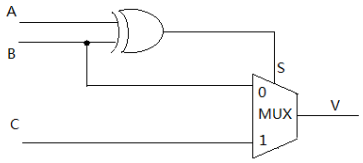

Fig. 4. Proposed scheme for the majority voter.

IV. Results and Analysis

This section gives some comparison results based on adders with TMR and different voters. The results are given in Table I and Table II.

TABLE I
RESULTS SYNTHESIZED IN XILINIX'S FPGA.

Comparison	None	Classic	NFTVC	Proposed
Instances	9	22	21	15
Delay ns	7.5	11.5	9.5	8
IO pads	5	11	11	11
LUTs	2	9	7.5	7.5
CLBs	1	5	4	4

TABLE II
RESULTS SYNTHESIZED IN ASIC (RTL COMPLIER).

Comparison	Classic	NFTVC	Proposed
Instances	25	31	25
Area	31	40	32
Power μw	2.35	3.75	2.85

We also utilize the SPRA algorithm described in [6] to extract the reliability of the architectures as shown in Figure 5. Unlike the classical voter, the proposed voter is robust. Furthermore, it produces low delay and is cost-effective.

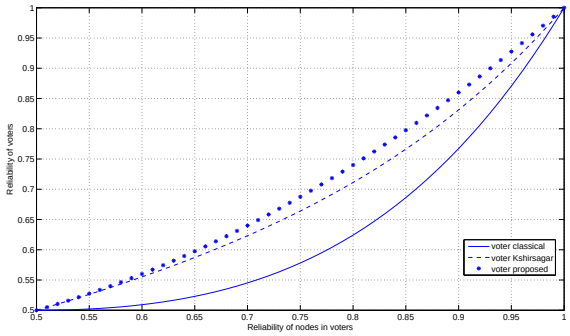

Fig. 5. Reliability curves for conventional (continuos line), NFTVC (dashed line) and the proposed voter (dotted line).

V. Conclusion

In this paper, we presented an alternative architecture for majority voter to be used in TMR schemes. The proposed solution is robust to single fault and exceeds those previous ones in terms of reliability. Furthermore, it saves area, power dissipation and propagation delays.

References

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