Study of Single Event Upsets in different Double Gate FinFET based SRAM Topologies

[1]K.Srikanth, [2]N.Vinodhkumar, [3]K.K.Nagarajan, *Member, IEEE* , [4]Dr.R.Srinivasan
[1]PG Scholar, ECE Dept., [2]JRF, IT Dept., [3]Assistant Professor, MCA Dept, [4] Professor, IT Department
SSN College of Engineering, Chennai, India
srikanth.kanaga@gmail.com, vinodhkumar.cc@gmail.com

***Abstract*—Soft errors also known as Single Event Upsets (SEU) is a term that defines the non-permanent errors caused in microelectronic circuits when high energy particles strike at the sensitive regions of the devices. In this paper, independently driven double gate (IDDG) FinFET and simultaneously driven double gate (SDDG) FinFET based 6T-SRAM cells are studied for their soft error performance. Ten different topologies, nine IDDG based topologies namely Flex-V_{TH}, Flex PG, PG-SN, PG-OSN, Flex PD, Flex PU, Flex-cell, Flex PUPG, Flex PDPG and one SDDG based topology are studied to find out the minimum dose required to flip the value stored in the SRAM cell using TSPICE simulations with 45 nm PTM model. Flex-PG and PG-OSN are having better immunity to radiation and a critical dose value of 1.18 MeV-cm^2/ mg.**

***Key words*— 6T SRAM, DG FinFET, SEU, TSPICE**

I. INTRODUCTION

Radiation-induced single event upsets (SEU) have a large impact on the reliability of devices in the deep sub-micron technology. In particular, ultra-scaled memory integrated circuits are more sensitive to SEU and pose a major challenge for the design of memories. The most commonly used memory cell design uses six transistors (6T-SRAM) to store a bit. SRAM is by far the dominant form of embedded memory found in today's Integrated Circuits (ICs) occupying as much as 60-70% of the total chip area and about 75%-85% of the transistor count in some IC products

Single event effects are the result of the interaction of highly energetic particles, such as protons, neutrons, alpha articles or heavy ions with sensitive regions of a microelectronic device or circuit[1]. A SEU is a change of state caused by a radiation particle that strikes a sensitive node in a microelectronic device such as those in Static Random Access Memory (SRAM). If a strike occurs near a sensitive node in a circuit, the resulting drift and diffusion carrier action will create a large current and a voltage transient spike. The amount of charge (generated by a particle strike) required to cause flip in the values stored in the memory cell is referred as critical charge.

CMOS technology scaling dramatically increases the sensitivity of integrated circuits to radiation [2]. MOSFET scaling also has encountered significant limitations due to short channel effects. Alternative solutions to replace the conventional planar bulk MOSFET architecture have been proposed and studied in the recent literature [3], [4], [5]. Double gate FinFET structures (DG-FinFETs) are presently considered as one of the best possible alternative for replacing the bulk devices in the nanometer regime [6]. FinFET based 6T-SRAMs have been investigated extensively in literature. FinFET based 6-T SRAM circuit is shown in Figure2.1. DG-FinFETs can be simultaneously driven double gate (SDDG) FinFETs or independently driven double (IDDG) gate FinFETs. A SDDG FinFET can be easily converted into IDDG FinFET through a single process step chemical mechanical polishing. IDDG FinFETs has two independent gates and can be biased separately. It is this interesting feature of IDDG FinFET that gives the circuit designer the option to design and achieve 6T-SRAM operation with different circuit topologies. In this work 10 different SRAM circuit topologies are constructed and their SEU or soft error performance is studied. Radiation in devices is modeled as current source in TSPICE simulator. Minimum radiation dose value required to flip the cell is found out by performing transient simulations in TSPICE and different circuit topologies are compared for their soft error performance. In the next section, TSPICE simulator and the simulation methodology have been discussed. Simulation results are discussed in the section 3. Finally, section 5 gives the conclusion.

II. SIMULATOR AND SIMULATION METHODOLOGY

A. Simulator

Tanner T-Spice Circuit Simulator from Tanner EDA is used to perform all the simulations. This simulator has many modules and the following are used in this study.

- TSpice: To edit circuit's netlist, setting up and running up of simulations and probing the results

- W-Edit: To provide an intuitive multiple window, multiple chart interface for easy viewing of waveforms

B. Simulation methodology

Basic parts of a 6T SRAM are Pull up (PU), Pull down (PD), Passgate (PG). DG-FinFET consist of front gate and back gate.The back gate biasing of the PU, PD and PG leads to ten different topologies[7,8] .They are described as follows

978-1-4673-5036-5/13/$31.00 ©

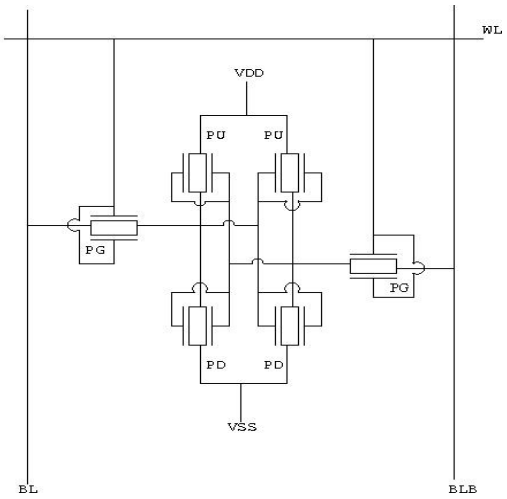

Fig 2.1.DG-FINFET based 6T SRAM

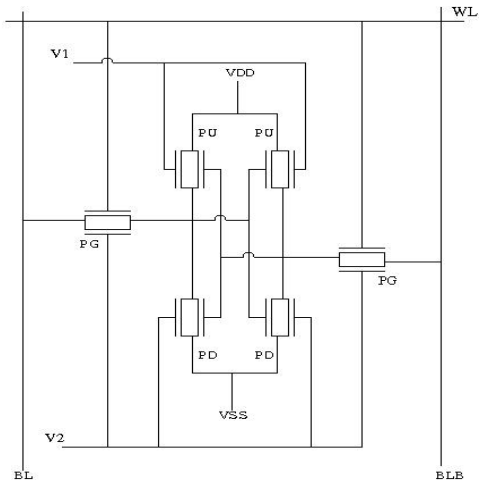

Fig 2.2 FLEX-V_{th}

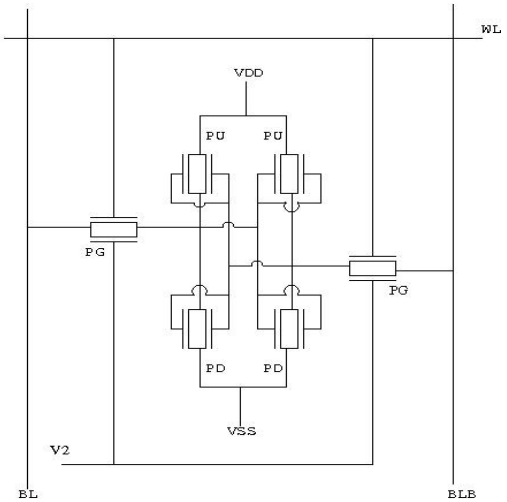

Fig 2.3FLEX- PG

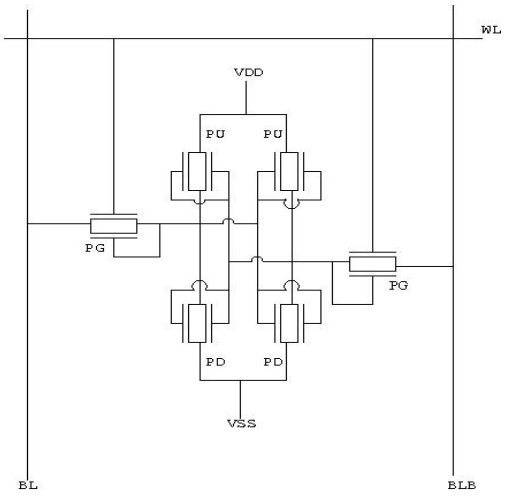

Fig 2.4 PG-SN

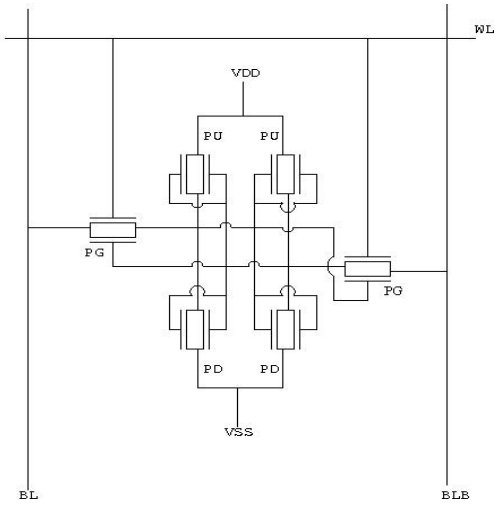

Fig 2.5 PG-OSN

TABLE 2.1 FIVE NEW TOPOLOGIES PROPOSED IN THIS WORK

Topology	PU	PD	PG
FLEX-PUPD	**I**	**I**	**S**
FLEX-PU	**I**	**S**	**S**
FLEX-PD	**S**	**I**	**S**
FLEX-PUPG	**I**	**S**	**I**
FLEX-PDPG	**S**	**I**	**I**

Key:

I→ Independently driven.

S→Simultaneously driven.

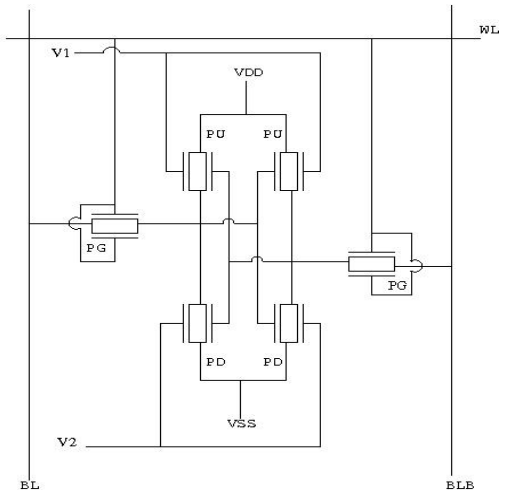

Fig 2.6 FLEX-PUPD

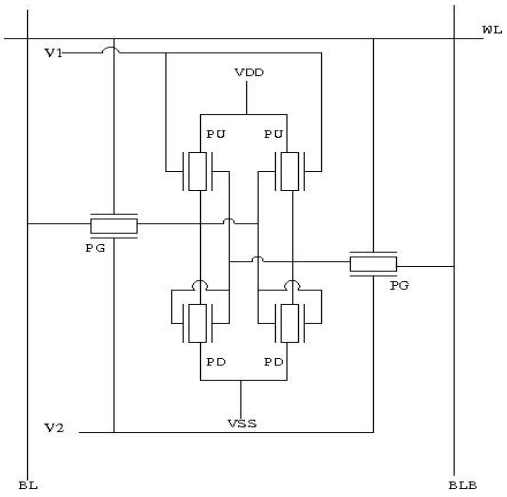

Fig 2.9 PUPG

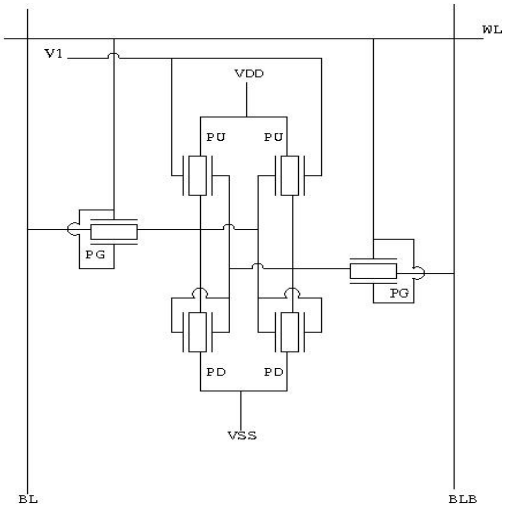

Fig 2.7 FLEX-PU

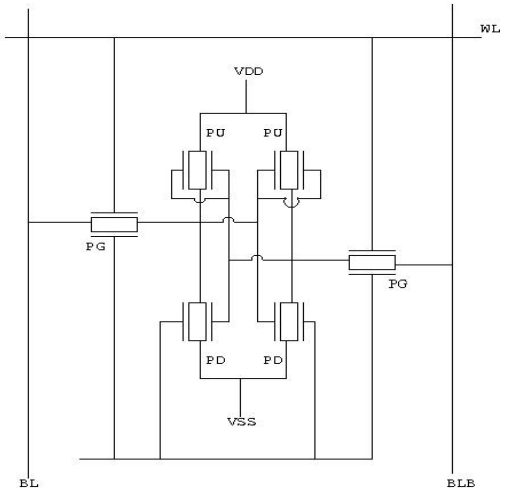

Fig 2.10 FLEX-PDPG

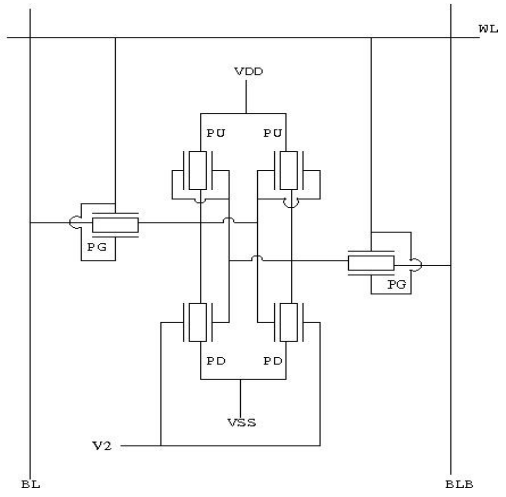

Fig 2.8 FLEX-PD

B.1 Modeling of radiation as current source **:**

The methodology commonly used to study transient effects as SEU couples SPICE simulations with current injection. The current pulse is extracted from other kind of simulations or more often modeled. Then this current is injected as current source by passing the drain and bulk electrodes of the sensitive transistor of the SPICE-modeled SRAM. Radiation dose produces electron hole pairs which due to drift and diffusion upset the device. This nature of the dose is represented by current source in double exponential form with rapid rise time (t_r) and gradual fall time (t_f) connected at the sensitive node. Let Q_{inj} be the total charge deposited by the current pulse, K is the charge deposited along a unit length of ionizing particle track, L_c is the charge collection depth and LET is the linear energy transfer in (Mev-cm^2)/mg.[9]

$I_{inj}(t) = Q_{inj} * T_W$ ……....(2.1)

$Q_{inj} = K * L_c * LET$ ……(2.2)

$TW = [e^{(-t/tf)} – e^{(-t/tr)}]/(t_f-t_r)$….(2.3)

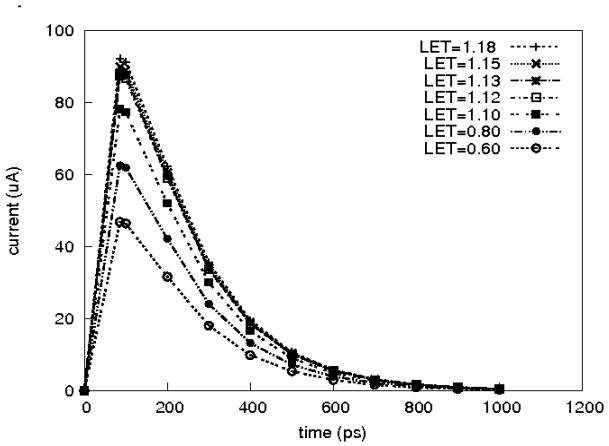

Fig.2.11 Modeling Current Source

Normally $t_r << t_f$ due to the slow decay of ion track and has a typical value of ~200ps. Injected current variation for different LET values for t_r =50ps , t_f=164ps , K=10.8, L_c=2µm and T_w a constant current pulse width.

The modelled current source is connected to the circuit as shown in figure 2.12.

III. RADIATION STUDY ON DIFFERENT FINFET BASED SRAM

The single event induced charge is modeled in T-Spice using double exponential current source connected at sensitive node. Simulation output of the FLEX-PG is shown in the Fig.3.1.From the simulation results it is clear that during the access period the content of the cell changes according to the input. This new value is supposed to be stored in the cell till the next access occurs . But at the point of current strike the cell contents are flipped and retains the same value till the next access occurs. As soon as the access occurs the cell retains its original value stating that the upset is temporary hence called soft error.

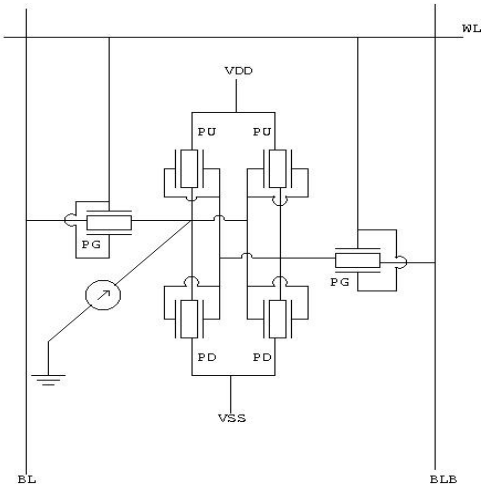

Fig 2.12 Modeling Radiation Using Current Source

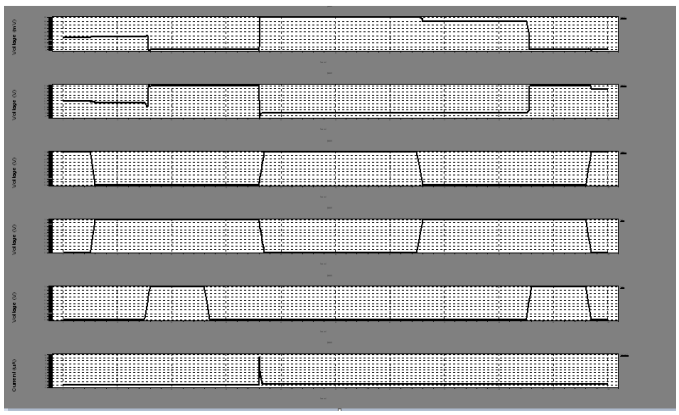

Fig. 3.1 Simulation output for FLEX-PG

The results of ten topologies of DG-FinFET are shown in Table 3.1 .The table shows the comparison of ten different topologies of DG-FinFET 6T SRAM with respect to their behavior on radiation strike. The critical dose for which the upset occurs is observed and the corresponding current values are shown. Among all the topologies listed above flexible pass gate (FLEX-PG) and pass gate-opposite storage node (PG-OSN) shows better performance due to their capability to withstand high dose i.e LET=1.18(Mev-cm2)/mg. The drivability of pull down to pass gate transistors which corresponds to the β ratio is thus flexibly controlled by the bias voltage (V2) for pass Gate. The back gate bias provided to the access transistor enhances the control of gate over the channel due to which it can withstand high radiation dose. In case of PG-OSN the effect of connecting the back gate to opposite storage node enhances the coupling and leads to same results as provided by FLEX-PG. Pass gate-storage node (PG-SN) with LET=1.13 performs slightly less compared to PG-OSN.

FLEX-PG, PG-OSN, PG-SN have independent dual gate FinFET (IDG FinFETs) used only for PG and other transistors are composed of dual gate FinFET (DG-FinFET). This makes them to perform better over flexible Vth (FLEX-Vth) which is a composed of IDG FinFETS. FinFET based 6T SRAM which is composed of DG-FinFETs produces upset at LET=1.15(Mev-cm2)/mg, simultaneously driven gate property of this configuration is responsible for its performance. Apart from the above configurations which were proposed earlier five new topologies produced interesting results [Table 2.1 and 3.1]. Out of these five topologies the FLEX-PDPG with pull up part simultaneously driven , pull down and access part independently withstands LET=1.12(Mev-cm2)/mg almost similar to FLEX-PG and FLEX-OSN. FLEX-PD topology with pull up and access simultaneously driven, pull down independently driven withstands a dose of LET=1(Mev-cm2)/mg .

TABLE 3.1 COMPARISON OF CRITICAL CHARGE FOR 10 DIFFERENT DG-FINFET BASED 6T SRAM TOPOLOGIES

s/n	Topology	Cell		Access (v)	Upset Observed	
		Pull up (v)	Pull Down (v)		Critical Dose (Mev-cm^2)/mg	Current (μA)
1	FINFET	--	--	--	1.15	89
2	PG-SN	--	--	--	1.13	88
3	PG-OSN	--	--	--	1.18	92
4	FLEX - PG	--	--	0.36	1.18	92
		--	--	0.1	1.15	90
		--	--	-0.04	1.15	90
5	FLEX-PU	0.3	--	--	0.4	31.29
		0.5	--	--	0.34	26.54
		0.6	--	--	0.31	24.54
6	FLEX-PD	--	0.36	--	0.8	62.58
		--	0.1	--	1	78
		--	-0.04	--	1	78
7	FLEX-PDPG	--	0.36	0.3	0.8	62.58
		--	0.1	0.5	1.12	87
		--	-0.04	0.6	1.12	87
8	FLEX-PUPG	0.3	--	0.36	0.52	40.67
		0.5	--	0.1	0.34	26.5
		0.6	--	-0.04	0.31	24.5
9	FLEX-PUPD	0.3	0.36	--	0.52	40.67
		0.5	0.1	--	0.68	53
		0.6	-0.04	--	0.6	47
10	FLEX – V_{th}	0.3	0.36	0.36	0.5	43.36
		0.5	0.1	0.1	0.68	53
		0.6	-0.04	-0.04	0.6	47

IV. ACKNOWLEDGEMENT

This work is supported by Defense Research and Development Organisation , Government of India.

V. CONCLUSION

We have compared ten different topologies of DG-FinFET based 6T-SRAM . The comparison proved that FLEX –PG and FLEX-OSN are the best topologies which can withstand a high dose of radiation when compared to other topologies. They can withstand an LET of 1.18 (Mev-cm^2)/mg i.e(92 uA) which is the critical dose value where the device behavior is lost and below which the device operates normally. The BAR graph (Fig 5.1) shows the comparison for all the 10 different topologies.

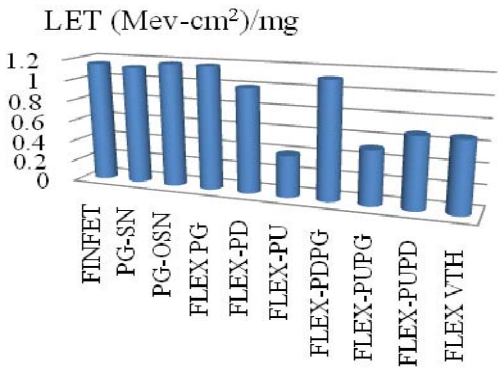

Fig 5.1 Bar graph comparing LETs of ten different topologies.

REFERENCES

[1] Fan Wang, Vishwani D. Agrawal (2008), "Soft Error Rate Determination for Nanometer CMOS VLSI Circuits", 40th Southeastern Symposium on System Theory University of New Orleans New Orleans, LA, USA, March 16-18, 2008 **pp:** 324 – 328.

[2] E.L. Petersen, P. Shapiro, J.H. Adams, E.A. Burke, Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Devices, IEEE Trans. Nucl. Sci. 29 (6) (1982) 2055–2063.

[3] "International Technology Roadmap for Semiconductors." Available: http://public.itrs.net

[4] Y. Taur, D. Buchanan, W. Chen, D. Frank, K. Ismail, S.-H. Lo, G.Sai-Halasz, R. Viswanathan, H.-J. C.Wann, S.Wind, and H.-S.Wong, "CMOS scaling into the nanometer regime," *Proc. IEEE*, vol. 85, no. 4, pp. 486–504, Apr. 1997.

[5] J. T. Park and J. P. Colinge, "Multiple-gate SOI MOSFETs: Device design guidelines," *IEEE Trans. Electron Dev.*, vol. 49, pp. 2222–2229, Dec. 2002.

[6] T. Hiramoto, M. Saitoh, and G. Tsutsui, "Emerging nanoscale silicon devices taking advantage of nanostructure physics," *IBM J. Res. Develop.*, vol. 50, no. 4/5, pp. 411–418, 2006.

[7] Kazuhiko Endo et.al (2008), "Enhancing SRAM cell performance by using Independent Double Gate FinFET", Electron Devices Meeting, *IEDM*.2008, IEEE International.

[8] V.N.Ramakrishnan, R.Srinivasan, "Soft error study in double gated FinFET-based SRAM cells with simultaneous and independent driven gates". Microelectronics Journal 43 (11) (2012) 888-893.

[9] Fan Wang, Vishwani D. Agrawal," Single Event Upset: An Embedded Tutorial fan wang". VLSI Design, VLSID 2008.21ST International Conference ;**pp**:429 – 434.

[10] "NASA Thesauras and Infomation." NASA, 2007. http://www.sti.nasa.gov/thesfrm1.htm