FULL TEMPERATURE SINGLE EVENT UPSET CHARACTERIZATION OF TWO MICROPROCESSOR TECHNOLOGIES

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Abstract

Data for the Fairchild 9450 I^3L bipolar microprocessor and the Harris 80C86 CMOS/epi (vintage 1985) microprocessor are presented, showing single event soft errors for the full mil-spec temperature range of -55 deg. C. to 125 deg. C. These data show for the first time that the soft error cross sections continue to decrease with decreasing temperature as we test at subzero temperatures. The temperature dependence of the two parts, however, is very different.

Introduction

Several workers (1, 2, 3) have explored the response of integrated circuits to single event phenomena at elevated temperatures and observed an increase in device sensitivity: an enhanced soft error or latchup cross section in some situations and/or a decreased value of the threshold linear energy transfer (LET) for soft errors and for latchup. This study expands on that work by measuring soft error cross sections at subzero temperatures. In order to make the conclusions more general, two complex devices (microprocessors) of different technologies were tested.

The data given here show a markedly different response to temperature of the soft error cross sections for each part type. However, in both cases, the cross section remains essentially constant or decreases monotonically with decreasing temperature (within typical SEU data scatter), suggesting that the SEU response at subzero temperature presents no inherent sensitivity. Special situations can be expected to occur in different device types, so the parts user must maintain his vigilance.

Instrumentation and Test Method

The tests were carried out at the Lawrence Berkeley Laboratory (LBL) 88-inch cyclotron, using 186 MeV argon [LET = 13 MeV/(mg/cm^2)], 107 MeV neon [LET = 4.8 MeV/(mg/cm^2)] and 77 MeV nitrogen ions [LET = 2.55 MeV/(mg/cm^2)], impinging at normal incidence and at an angle of 60 degrees with respect to the normal. One device of each type was tested at each angle for a series of different temperatures ranging between -55 deg. C. and 125 deg. C.

The general approach to SEU testing is now quite standard and has been described elsewhere (4). However, JPL has installed a new permanent vacuum chamber at LBL (Figure 1) which offers improvements in beam fluence measurements and temperature control (3). The testing at high temperature is described in detail in Ref. (3)--it involves installation of nichrome-wire heaters at each socket in combination with a controller and thermocouple (and occasionally also a precalibrated remote IR sensor). For this test, a new liquid nitrogen cooling system was also installed.

The cooling system used cold nitrogen gas flowing through a heat exchanger block to remove heat. The cooler was installed in the vacuum system on a DUT positioner mechanism. The tubes carrying the nitrogen gas to and from the heat exchanger were made of "Bellows" type copper tubing with stainless steel AN flared type fittings on both ends. These fittings used a disposable copper "nose seal" to make a vacuum-tight seal that will reliably reseal after removal and reinstallation.

As seen in Figure 2, a 180 liter Dewar was used to supply liquid nitrogen (LN_2) which was routed through the throttle valve and on to the copper helix where the LN_2 changes phase to a gas. The gas was fed to the supply side of the DUT exchanger block where it exits through an N_2 vent on the exhaust side. Control of this system was accomplished by adjusting the throttling valve while observing the temperature via thermocouple TC-1. The actual DUT temperature (silicon die face) was also monitored by an infrared temperature sensor.* A temperature differential of 2 degrees C. was noted between the silicon chip face and the heat exchanger block. The DUT temperature was maintained at $\pm$5 degrees for each selected temperature level.

The tester approach for the microprocessors was selective--not exhaustive. In general, the test for both microprocessors had the following elements in common:

1) Examination of many (but not all) of the component elements, such as the AX-register, Program Interrupt Register (PIR), and many others.

2) The AX-register and PIR are 16-bit registers that were each tested with all ones and all zeros to check for any bit state preference. When no state preference was evidenced, checkerboard patterns were used thereafter to expedite the test.

3) The dynamic test software algorithm loops endlessly through a reset cycle, register conditioning, and checking phase, until an error condition is detected that indicates the register has undergone some change. Each algorithm was tailored to match the disciplines of the individual registers, loading a known pattern for later comparison, the checking phase, such that errors could be uniquely determined.

*Unfortunately, the remote IR technique has several pitfalls. For one, it appears necessary to calibrate a new emissivity factor for each device type at each temperature. Furthermore, it is not obvious just what portions of the chip that the IR is sensing; the thin oxide, the dopant-dependent semiconductor, substrate and support material may each be contributing to an overall (but not necessarily meaningful) temperature. Hence, in practice, the thermocouple read-out is taken as standard.

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For the 9450, the bus status signals were monitored by peripheral hardware throughout each loop of the software to negate any error count should some anomaly cast doubt on the source of an error. The combination of no anomaly and a register error constituted a single event upset.

Result

One each of two device types was tested: the Fairchild 9450 bipolar I^3L 8-bit microprocessor and the Harris 80C86 CMOS/epi (Mask No. 1750, vintage 1985) 16-bit microprocessor. Soft error cross sections (calculated as the number of upsets divided by the projected fluence) vs temperature for each device is given in Table 1, for the maximum effective LET ion--186 MeV argon at a 60 degree beam angle. The 80C86 data set is limited to the AX-Register, and the 9450 data set is limited to the Program Interrupt Register (PIR).

Table 1 - SEU Cross Sections (cm^2) vs Temperature - Argon at 60 deg Angle

Temp. (deg C)	Fairchild 9450 (PIR)	Harris 80C86 (AX-Register)
-55	$5.3\pm4\times10^{-6}$*	$1.5\pm.2\times10^{-4}$
-30	$8.8\pm.5\times10^{-6}$	$1.6\pm.1\times10^{-4}$
Room T	$1.0\pm.1\times10^{-5}$	$2.0\pm.1\times10^{-4}$
60	$1.9\pm.1\times10^{-5}$	$2.0\pm.1\times10^{-4}$
95	$4.1\pm.2\times10^{-5}$	$2.2\pm.2\times10^{-4}$
125	$8.0\pm.2\times10^{-5}$	----------

*In general, data scatter is worst at the lowest temperature. Upset rates are smaller and variations in temperature control are greatest there.

The data for the bipolar device (9450 program interrupt register) show a greater than ten-fold monotonic increase in cross section with increasing temperature over the tested temperature range, but most of that increase occurs at temperatures above room T (20 deg C.).

The data for the CMOS/epi device (80C86 AX-register), on the other hand, show a small change in the soft error cross section with temperature over the entire mil-spec range. One might conclude, erroneously, that this fact was simply consistent with the idea that the argon ion had such a high effective LET = 26 MeV/(mg/cm^2) that the measured upset cross section at any temperature was simply equal to the constant geometric cross section. However, data obtained with lower LET ions given in Tables 2 & 3 for this part (80C86 AX-register) show the same insensitivity to temperature. The lower LET cross sections are much smaller than that for Ar and therefore clearly not geometrically limited. Hence, for the lower LET ions at least, the temperature insensitivity of SEUs requires a more extensive analysis.

One cannot, however, attribute this insensitivity to the CMOS/epi technology. Published data (1) on soft error cross sections of CMOS devices show a strong increase in SEU rates with temperature, which at higher LET may simplify to a temperature-independent cross section in the limit of geometric saturation. Latchup thresholds (Ref. 3) of CMOS/epi devices also show a strong increase in single event effects with increase in temperature. Clearly, insensitivity to temperature is not a universal property of CMOS devices. Generalizations (if any can be forthcoming) will require a larger experimental base, including both simple and complex parts data.

Table 2 - 80C86 Soft Error Cross Sections* (cm^2) vs Temperature-Neon

Temp. (deg C)	Beam Angle (0 deg.)	Beam Angle (60 deg.)
-55	$1.6\pm.2\times10^{-5}$	$5.1\pm.8\times10^{-5}$
-30	$2.3\pm.2\times10^{-5}$	$4.6\pm.2\times10^{-5}$
Room T	$1.9\pm.1\times10^{-5}$	$4.8\pm.3\times10^{-5}$
60	$1.9\pm.1\times10^{-5}$	$4.0\pm.2\times10^{-5}$
95	$1.8\pm.3\times10^{-5}$	$5.2\pm.2\times10^{-5}$

*AX-Register only

Table 3 - 80C86 Soft Error Cross Sections* (cm^2) vs. Temperature-Nitrogen

Temp. (deg. C.)	Beam Angle (0 deg.)	Beam Angle (60 deg.)
-55	$4\pm3\times10^{-6}$	$2.6\pm.1\times10^{-5}$
-30	$2\pm.5\times10^{-6}$**	$1.0\pm.3\times10^{-5}$**
Room T	$5.8\pm1\times10^{-6}$	$1.7\pm.2\times10^{-5}$
60	$5.7\pm3\times10^{-6}$	$2.0\pm.5\times10^{-5}$
95	$5.6\pm3\times10^{-6}$	$1.2\pm.3\times10^{-5}$
125	$6.2\pm2\times10^{-6}$	$2.0\pm.8\times10^{-5}$

*AX-Register only
**The authors presume an undetermined systematic error occurs here.

Conclusion

The data for the two silicon microprocessors, representing the two major technology groups, show that subzero temperature conditions within the mil spec range (-55 deg C to 125) did not greatly affect the SEU sensitivity of these devices. The same data did show substantially different changes in the overall temperature sensitivity (-55 deg C to 125 deg C) for each of the two parts. The possibility remains that other part types, such as those utilizing temperature-dependent resistors, may respond very differently, even at subzero temperatures.

Much future work remains with regard to analyzing heavy-ion-induced latchup in devices at room temperature and as a function of temperature. More experimental data of the type given here as well as data for simpler device structures is desirable. The intrepid theoretical physicist will most likely require detailed parts information, such as that pertaining to the circuit structure of the latches, as well as an adequate (and original) computer program.

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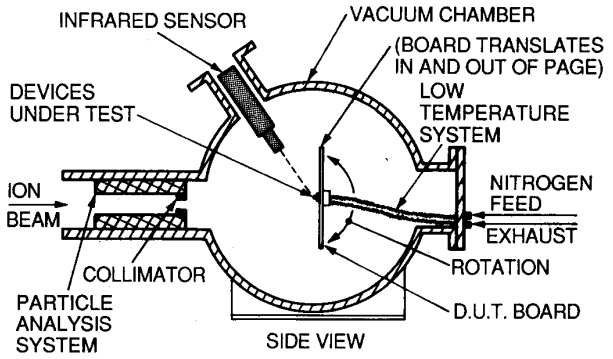

Figure 1. Vacuum Chamber

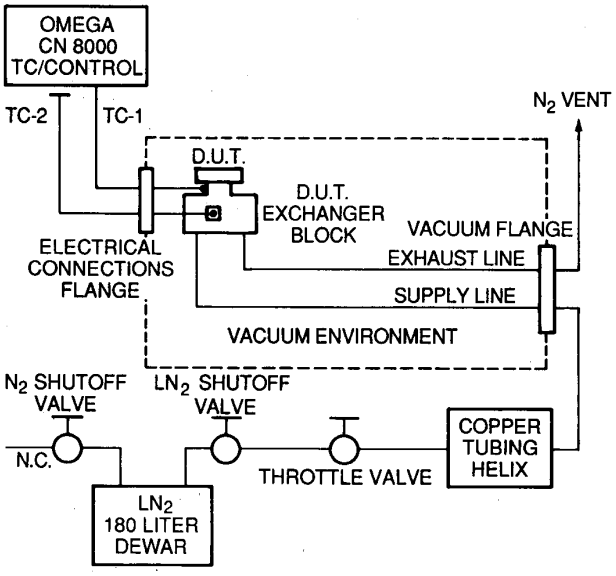

Figure 2. Cooling System - Notes: 1) TC-2 Unconnected, used only as spare; 2) Supply and Exhaust Lines are Flex Bellows Copper Tubing; 3) Copper Tubing Helix is Composed of (4) Loops of 1/4" Copper Tubing Looped in a 18" Diameter Configuration; 4) All Lines Beyond LN_2 Shutoff Valve are 1/4" Tubing, 5) All Thermocouples are Copper/ Constantan Type (T).

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