

**Fault Tolerant Design Implementation on
Radiation Hardened By Design SRAM-Based
FPGAs**

by

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B.S., Electrical Engineering (2011)

United States Air Force Academy

Submitted to the Department of Aeronautics and Astronautics

in partial fulfillment of the requirements for the degree of

Master of Science in Aeronautics and Astronautics

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2013

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Abstract

SRAM-based FPGAs are highly attractive for space applications due to their in-flight reconfigurability, decreased development time and cost, and increased design and testing flexibility. The Xilinx Virtex-5QV is the first commercially available Radiation Hardened By Design (RHBD) SRAM-based FPGA; however, not all of its internal components are hardened against radiation-induced errors. This thesis examines and quantifies the additional considerations and techniques designers should employ with a RHBD SRAM-based FPGA in a space-based processing system to achieve high operational reliability. Additionally, this work presents the application of some of these techniques to the embedded avionics design of the REXIS imaging payload on the OSIRIS-REx asteroid sample return mission.

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Acknowledgments

I would like to thank the Air Force and the MIT Space Systems Laboratory for the opportunity to attend graduate school and learn so much about space avionics design and systems engineering.

Thanks to Mark, Kevin, Harrison, Eric, Niraj, and Matt—the dedicated members of the REXIS team—for the many hours of questions and discussions they endured concerning the interaction between their subsystems and the avionics subsystem. You guys were a lot of fun to work with, and I will look back with a smile!

Additionally, I would like to thank Joel Villasenor, Gregory Prigozhin, Rick Foster, Steve Kissel, and Beverly Lamarr from the Kavli Institute and John Doty of Noqsi Aerospace for their patience and willingness to teach and share their valuable experience. I also would like to thank Dmitriy Bekarr, Brian Franklin, Paula Pin-gree, and Charles Norton of JPL for sharing their experience with COVE. At NASA GSFC, I specifically thank James Dailey for his constant support of, and critical eye on, REXIS FSW development, and Dave Petrick for sharing his invaluable experience with the SpaceCube project and his many reviews of the MEB schematics. I would also like to thank Sara Haugh, Tom Jackson, Dave Harmon, Ray Ladbury, Dave Sheppard, and Tom Flatley at NASA GSFC.

I am extremely grateful to Shuyi Chen for the many hours he poured into making the REXIS frame grabber work and then in improving it during his time as a UROP in the early days of the project. He taught me everything I know about Verilog, and his diligent and tireless efforts are the sole reason the REXIS SXM functions as designed. I have complete confidence in him as the future REXIS avionics lead.

Special thanks Bruno Alvisio for consistently reminding me there is never enough time to do everything we might want to in life, and therefore we should find what we are passionate about and pursue it with a smile, while never forgetting the people who helped us on the way.

I gratefully thank my family for their constant support, encouragement, and love. Without them, I would not have accomplished this work.

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List of Acronyms and Initialisms

FPGA - Field Programmable Gate Array
REXIS - REgolith X-ray Imaging Spectrometer
BRAM - Block Random Access Memory
SRAM - Static Random Access Memory
ECC - Error Correcting Code
FSW - Flight Software
SEU - Single Event Upset
SXM - Solar X-ray Monitor
CCD - Charge Coupled Device
RHBD - Radiation Hardened By Design
OR - logical OR
CCID - Lincoln Lab CCD model designator
DCM - Digital Clock Manager
SEFI - Single Event Functional Interrupt
SDD - Silicon Drift Diode
PLL - Phase Lock Loop
DE - Detector Electronics
XRTC - Xilinx Radiation Test Consortium
TMR - Triple Modular Redundancy
CRC - Cyclic Redundancy Check
LET - Linear Energy Transfer
SDRAM - Synchronous Dynamic Random Access Memory
LMB - Local Memory Bus
ADC - Analog-Digital Converter
IP - Intellectual Property
TESS - Transiting Exoplanet Survey Satellite
TID - Total Ionizing Dose
ASCA - Advanced Satellite for Cosmology and Astrophysics
OSIRIS - Origins-Spectral Interpretation-Resource Identification-Security-Regolith Explorer
ETU - Engineering Test Unit
MPMC - Multi-Port Memory Controller
DC - Direct Current
WDT - Watchdog Timer
SEE - Single Event Effects
ICAP - Internal Configuration Access Port
ACIS - Advanced CCID Imaging Spectrometer

MGT - Multi-Gigabit Transceiver
DSP - Digital Signal Processor
PCB - Printed Circuit Board
CNV - Convert
TEC - Thermoelectric Cooler
UART - Universal Asynchronous Receiver/Transmitter
RG - Reset Gate
LSE - programming language
BYU - Brigham Young University
IA - Imaging Array
FS - Framestore
SEL - Single Event Latchup
NASA - National Aeronautics and Space Administration
MIT - Massachusetts Institute of Technology
RAM - Random Access Memory
NICER - Neutron Star Interior Composition Explorer
MEB - Main Electronics Board
MB - MicroBlaze
CLB - Configurable Logic Block
SECDED - Single Error Correct Double Error Detect
OTP - One-Time Programmable
MCU - Microcontroller Unit
GPIO - General Purpose Input/Output
EDAC - Error Detect And Correct
PWM - Pulse Width Modulation
PLB - Processor Local Bus
MIG - Memory Interface Generator
LVAL - Line Valid
LUT - Look Up Table
FVAL - Frame Valid
FAR - Frame Address Register
DRP - Dynamic Reconfiguration Port
NOR - logical not OR
MSB - Most Significant Bytes, Most Significant Bit
CREME - Cosmic Ray Effects on Micro-Electronics
CMOS - Complimentary Metal Oxide Semiconductor
TXEL - True X-ray Events List
ST - Split Threshold
SET - Single Event Transient
RPP - Rectangular Parallel Piped
MOSFET - Metal Oxide Semiconductor Field Effect Transistor
MAC - Media Access Control
GTX - Gigabit Transmitter
SEUXSE - Singel Event Upset Xilinx Sandia Experiment
PXEL - Possible Events List
POR - Power-On Reset
MTTU - Mean Time To Upset

MISSE - Materials International Space Station Experiment
ITAR - International Traffic in Arms Regulations
ISS - International Space Station
FIFO - First In First Out
EDK - Embedded Development Kit
CDH - Command and Data Handler
CAD - Computer Aided Drafting
XPS - Xilinx Platform Studio
STP - Space Test Program
STS - Space Transportation System
SPI - Serial Peripheral Interface
SMAP - SelectMAP
SIS - Solid-state Imaging Spectrometers
PMAD - Power Management and Distribution
MOS - Metal Oxide Semiconductor
MIPS - Million Instructions Per Second
JPL - Jet Propulsion Laboratory
HETE - High Energy Transient Explorer
GSFC - Goddard Space Flight Center
EM - Engineering Model
DVAL - Data Valid
DDR - Double Data Rate
CXO - Chandra X-ray Observatory
COVE - Cubesat On-board processing Validation Experiment
BPI - Byte Peripheral Interface
ASIC - Application Specific Integrated Circuit
VHSIC - Very-High-Speed Integrated Circuit
VHDL - VHSIC Hardware Description Language
TBD - To Be Determined
SXC - Soft X-ray Camera
STAT - Status
SR - Serial Register
SEGR - Single Event Gate Rupture
SEB - Single Event Burnout
RHBP - Radiation Hardened By Process
PSRM - Processor System Reset Module
PROG - Program
PLD - Programmable Logic Device
NAND - Logical Not AND
MPU - Measurement/Power Unit
LVDS - Low Voltage Differential Signaling
JFET - Junction Gate Field Effect Transistor
JAXA - Japan Aerospace Exploration Agency
IO - Input/Output
FM - Flight Model
FF - Flip Flop
EMI - Electromagnetic Interference

EMAC - Ethernet Media Access Control
DUT - Device Under Test
DAC - Digital-Analog Converter
BER - Bit Error Rate
XTMR - Xilinx Triple Modular Redundancy
XRF - Remote X-ray Fluorescence
VDC - Volts Direct Current
UV - Ultraviolet
UROP - Undergraduate Research Opportunities
TVAC - Thermal Vacuum Chamber
TPOR - Power-On Reset Time
TLD - Trakimas-Larosa-Doty
TANSTAAFL - There Ain't No Such Thing As A Free Lunch
SOI - Silicon on Insulator
SMA - Safety and Mission Assurance
SBU - Single Bit Upset
RISC - Reduced Instruction Set Computer
NSEU - Neutron Single Event Upset
MUSES - series of mission launched by the MU class rocket, C stands for third of series
MRM - Mission Response Module
MDM - MicroBlaze Debug Module
LOL - Loss Of Link
JSC - Johnson Space Center
GOES - Geostationary Operational Environmental Satellites
FI - Front Illuminated
ET - Event Threshold
ISAS - Institute of Space and Astronautical Science
ESA - European Space Agency
EEPROM - Electrically Erasable Programmable Read Only Memory
DPST - Double Pole Single Throw
DCE - Domain Crossing Error
CTE - Charge Transfer Efficiency
CCE - Charge Collection Efficiency
BSP - Board Support Package
BI - Back Illuminated
BAE - British Aerospace Electronic Systems
AND - logical AND

Chapter 1

Introduction

1.1 Motivation

Since the late 1990s, reconfigurable, static random-access memory (SRAM) based field programmable gate arrays (FPGAs) have become increasingly attractive to designers of space-based systems due to their on-orbit reconfigurability, low development cost, and flexible design flow. FPGAs are well-suited to space-based digital signal processing tasks, providing the possibility for orders of magnitude increases in performance over processor-based implementations. Unfortunately, the technology making SRAM-based FPGAs reconfigurable also leaves them especially vulnerable to radiation-induced errors in the space environment when compared to traditional non-reconfigurable FPGA designs for space applications.

The recent advent of radiation-hardened by design (RHBD) SRAM-based FPGAs, such as the Xilinx Virtex-5QV, has provided dramatically decreased estimated radiation-induced error rates. However, not all of the components of the Virtex-5QV are RHBD, meaning these components are identical to the components used in the commercial grade Virtex-5 FPGA. Each of the non-RHBD components have specific radiation-induced error vulnerabilities, and some of these components require additional design implementations to decrease the frequency of errors while operating in high radiation environments such as space. These additional design implementations result in design constraints that would likely not exist in terrestrial design with a

commercial SRAM-based FPGA. This thesis enumerates and quantifies some of the additional design techniques and considerations for an embedded system in a high radiation environment using a RHBD SRAM-based FPGA and assesses the design impact of these techniques.

1.2 Overview

An FPGA is a configurable integrated circuit containing a regular structure of logic cells and special function hardware modules. Designers may customize the interconnection of these logic cells and hardware modules to create user logic designs that perform specific functions, such as demodulation of a radio frequency signal to extract the information contained in the signal. The large number of logic cells internal to FPGAs makes massive parallelization of processing possible, ideally suiting FPGAs to space-based computation tasks, which usually involve high frequency digital signal processing.

Traditionally, designers of space-based FPGA systems have employed one time programmable (OTP) FPGAs, which historically have proven less sensitive to radiation-induced errors than SRAM-based FPGAs. However, designers may program the internal logic of OTP FPGAs only once, thus limiting the design process flow and eliminating the possibility of reconfigurability. Designers may program SRAM-based FPGAs thousands of times, thus creating a more open logic design flow, facilitating increased hardware testing, and allowing reconfigurability of the design. At the same time, SRAM-based FPGAs are inherently vulnerable to errors resulting from ionizing radiation present in the form of charged particles in the space environment. These vulnerabilities have discouraged their use in many mission critical applications. Despite these limitations, commercial grade SRAM-based FPGAs have flown on many space missions, in both earth orbit [27] [25] [73] and interplanetary missions [75]. Avionics systems flying commercial SRAM-based FPGAs typically employ configuration bitstream management and triple modular redundancy (TMR) techniques to reduce the radiation-induced error rate.

Of primary concern to system designers is the vulnerability of the configuration cells in SRAM-based FPGAs. The configuration cells control the user logic design implemented on the FPGA, and thus an error in the configuration cells can cause malfunctions in, and possibly failure of, the logic design. To increase the reliability of SRAM-based FPGAs in high radiation environments such as space, Xilinx applied Radiation Hardened By Design (RHBD) techniques to produce the space grade Virtex-5QV. The design effort focused on hardening the configuration cells against radiation-induced Single Event Upsets (SEUs), as well as increasing the robustness of the logic cells to radiation-induced Single Event Transients (SETs). The RHBD Virtex-5QV is shown in Figure 1-1.

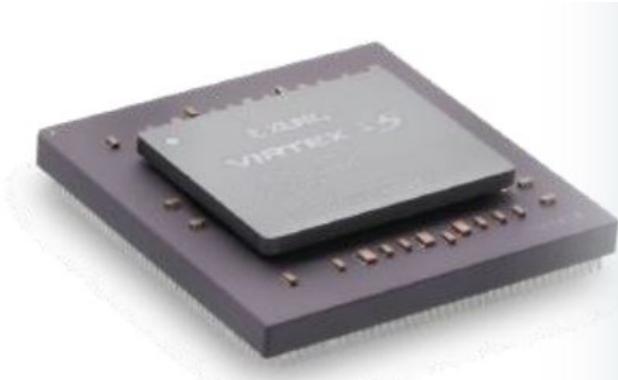


Figure 1-1: Xilinx Virtex-5QV RHBD SRAM-based FPGA [28]

To verify the effectiveness of the RHBD efforts, the Xilinx Radiation Test Consortium (XRTC) has performed substantial radiation testing on the Virtex-5QV to characterize its response to high energy charged particles. The XRTC brings together experts from industry, government, and academia with the purpose of characterizing radiation effects and mitigation techniques for reconfigurable FPGAs [40]. The XRTC members have performed static and dynamic radiation tests on almost all of the non-RHBD features and published the results in various journals, at conferences, and in technical reports. As the XRTC's ongoing radiation test campaigns of the Virtex-5QV have shown, the design efforts have been particularly successful in decreasing the error rate in the configuration and logic cells.

1.3 Focus

The focus of this work is to enumerate and quantify the cost of the additional design implementations used to apply fault tolerance to the non-RHBD elements of the RHBD SRAM-based Virtex-5QV. These techniques are especially applicable to the use of soft core processors in SRAM-based FPGAs (commercial or RHBD), interest in which continues to rise [35] [64]. The additional design factors include system clock frequency effects and user memory storage space, in addition to system design trades on required external components, interface complexity, power consumption, and cost. A prime example of an additional design factor is fault mitigation in the block random access memory (BRAM) hardware units used to store user design data in Xilinx FPGAs. Since the BRAM units are not RHBD in the Virtex-5QV, the designer may activate built-in error detect and correct (EDAC) circuitry (which is Single Error Correct Double Error Detect (SECDED) in the Xilinx implementation) to mitigate radiation-induced errors. Adding the EDAC circuitry to the BRAM modules in the FPGA fabric results in timing constraints on the speed at which the clock network can operate, as well as power and area increases in the user design. Designers must be cognizant of the effects and limitations of additional fault tolerance and factor the implications into system design with the RHBD SRAM-based Virtex-5QV.

The additional design techniques for RHBD SRAM-based FPGAs identified in this thesis have been applied as fundamental avionics design elements for the the RE-golith X-ray Imaging Spectrometer (REXIS), which is a student payload on NASA's Origins Spectral Interpretation Resource Identification Security Regolith Explorer (OSIRIS-REx) asteroid sample return mission. The REXIS avionics system is based on a MicroBlaze softcore processor running on a Virtex-5QV along with supporting external power, memory, and interface circuitry. The REXIS flight avionics system serves as a prime case study of how applying additional fault tolerance techniques to an SRAM-based RHBD FPGA system affects a real world system.

Although the Virtex-5QV is International Traffic in Arms Regulations-controlled (ITAR-controlled), Xilinx planned to provide designers the option of using the com-

mercial grade Virtex-5FX130T as a development platform for the space grade Virtex-5QV. This scheme allows designers to prototype logic designs and printed circuit board (PCB) configuration and layouts with the commercial Virtex-5FX130T, thus reducing cost and removing ITAR restrictions from initial design work. All estimates of FPGA logic utilization and power consumption in this work were performed on either the commercial grade Virtex-5FX70T FPGA on the Xilinx ML507 development board or the commercial grade Virtex-5FX130T FPGA on the Xilinx ML510 development board using Xilinx software designed for the commercial Virtex-5 FPGA family. No ITAR-controlled software was used to produce results for this work, and all research data presented is publicly available.

1.4 Thesis Overview

This thesis begins with a literature review of the deleterious effects of radiation on SRAM-based FPGAs, FPGA radiation testing and effects prediction, and the Virtex-5QV FPGA in Chapter 2. Chapter 3 follows the literature review with the identification and analysis of the additional design techniques for FPGA systems implemented on RHBD SRAM-based FPGAs . In Chapter 4, the design techniques are applied to the REXIS avionics system to demonstrate their impact on a real world satellite payload system. This work concludes with further research possibilities of the additional RHBD SRAM-based FPGA design techniques and future testing of the REXIS system in Chapter 5.

Chapter 2

Radition Effects on FPGAs, FPGA Radiation Testing, and the RHBD Virtex-5QV

This chapter provides a brief background on the effects of total ionizing dose (TID) and single event effects (SEE) on electronics and then details particular radiation effects on FPGAs, specifically SRAM-based FPGAs, including single event functional interrupt (SEFI) types and multi-bit upsets (MBUs). Traditional methods of FPGA SEU testing are presented, along with estimation techniques for on-orbit single event upset (SEU) error rates. The chapter closes with an overview of the Xilinx RHBD SRAM-based Virtex-5QV FPGA and radiation testing of the Virtex-5QV.

2.1 Radiation Effects on Electronics

Radiation effects on electronics generally are classified into two types: total dose effects, typically known as total ionizing dose (TID), and single event effects (SEE). TID describes the cumulative effects of charged particles on the doping levels of substrate materials within electronics, specifically silicon. SEE refer to altered circuit functionality as a result of a single charged particle interacting with the internal material of an electronic component. The contributions of this work focus primarily

on additional design techniques to mitigate errors resulting from SEE in SRAM-based FPGAs.

2.1.1 Total Ionizing Dose

Total ionizing dose (TID) in electronics is a cumulative, long-term degradation mechanism due to mainly protons and electrons depositing charge in electronic components, while a smaller contribution occurs from secondary particles arising from interactions between the primary particles and spacecraft electronics [76]. As a result of the slow accumulation of charge in transistor's oxide regions (Figure 2-1), TID causes threshold shifts in transistor gate voltage, increased transistor leakage current, and timing skews [65]. Initially, TID effects appear as parametric degradation of the device and ultimately results in functional failure.

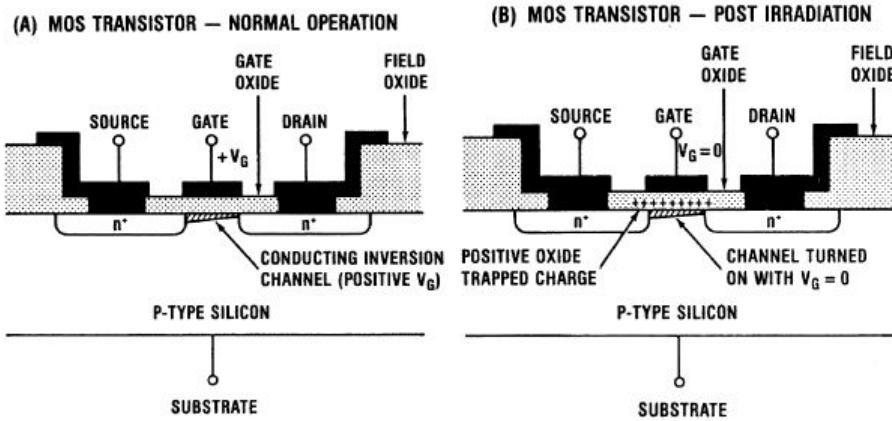


Figure 2-1: Radiation-induced charging of gate oxide in n-channel MOSFET: (a) normal operation (b) post-irradiation [69]

TID is specified in units of rad, where a rad is defined as radiation absorbed dose. A rad is the measure of the amount of energy deposited in the material and is equal to 100 ergs (6.24E4 eV or 10 nJ) of energy deposited per gram of material. The energy deposited in a device must be specified for the material of interest. Thus, for a metal oxide semiconductor (MOS) transistor, total dose is measured in units of rad(Si) or rad(SiO_2). Ability to withstand TID in Radiation Hardened (RadHard) components is also specified in units of rads, or more typically in krads. [53]

Mitigating TID effects is typically accomplished using radiation hardened by process (RHBP) techniques and/or shielding. RHBP techniques involve modifying the standard wafer fabrication process and include inserting an oxide layer in the transistor substrate, thinning MOS transistor gate oxides, and growing an epitaxial layer under regions of high doping density [65]. Placing shielding material (such as aluminum) around sensitive electronics can reduce TID by absorbing most electrons and lower energy protons. As shielding is increased, however, shielding effectiveness decreases because of the difficulty in slowing down higher energy protons [76].

2.1.2 Single Event Effects

Single event effects (SEE) are the electrical disturbances caused by an energetic charged particle's ionization of a silicon lattice in an electronic device [26]. The passage of a single charged particle through a device or a sensitive region of a microcircuit can induce SEE. Figure 2-2 shows a representation of a charged particle depositing charge as it passes through the physical structure of a transistor.

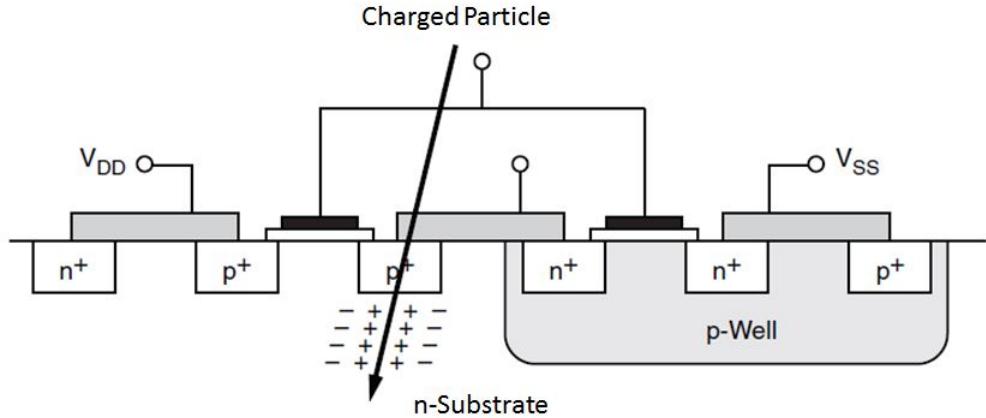


Figure 2-2: Charge deposition by charged particle into the substrate of a transistor [26]

In order for a charge particle (heavy ion or proton) to affect the operation of a circuit, it must transfer sufficient charge to a transistor gate such that the transistor's output state changes. The minimum amount of charge required is usually referred to as Q_{crit} , as shown below in

$$Q_{crit} = C_{node} \times V_{node} \quad (2.1)$$

where C_{node} is the capacitance between transistor nodes and V_{node} is the transistor operating voltage. Thus as transistor process sizes shrink (resulting in decreased capacitance) and transistor operational voltage decreases, Q_{crit} decreases [65], and the charged particle energy necessary for upset is also decreased. In a latching circuit with memory elements, a single event effect can cause the wrong value to be stored and thus produce an error lasting until the value in memory is corrected/modified, while a single event effect in a combinatorial circuit can create a transient error in a current operation. These errors can propagate through the device's logic stream and lead to errors such as a pin outputting an incorrect value or a circuit element latching incorrect data [65]. SEE can manifest in several forms:

Single Event Upset (SEU)

Single events upsets occur when a single charged particle causes one or more memory cells or configuration cell within the device to change state. If only a single memory or configuration cell changes state, the SEU is referred to as a single bit upset (SBU). If multiple memory or configuration cells change state, the SEU is called a multi-bit upset (MBU).

Single Event Transient

A single event transient (SET) occurs when a single charged particle causes a temporary voltage/current spike. If the pulse width of this spike is sufficiently large, and occurs at the right time, it can be latched in a flip-flop and propagate through the circuit [80]. The probability of an error being latched increases with increasing clock frequency [36].

Single Event Latchup

Single event latchup (SEL) is the high current state of a bi-stable parasitic four-layer PNPN structure inherent in complimentary metal oxide semiconductor (CMOS) where a short circuit sustains itself through positive feedback. It may

be triggered by single-event charge deposition or electrical noise, but the only way to remove latchup is to cycle power. [83] Traditionally in radiation testing, any sudden high current mode that requires a power cycle of the component to recover functionality and nominal current qualifies as a latchup. [83] Depending on the duration and amplitude of the high current condition, a SEL may cause permanent damage to a device [65]. Vertical thyristors in CMOS technology cause SEL. [47].

Single Event Functional Interrupt

A single event functional interrupt (SEFI) is an upset of an internal memory element or a circuit which causes a loss in the device's functionality[65]. Traditionally, to recover an FPGA-based system from a device SEFI, the FPGA must be re-configured via pulsing the PROG pin or cycling power, which involves a minimum outage of some tens or hundreds of milliseconds [83].

Single Event Gate Rupture

Single event gate ruptures (SEGR) primarily affect metal oxide semiconductor field effect transistors (MOSFETs) when operating in the OFF condition (no current is flowing between drain to source). However, MOSFETs in the ON state still are susceptible to over current conditions caused by charged particle interaction.

Heavy ions (galactic cosmic rays and solar heavy ions) usually cause single event effects by direct deposit of charge. This effect is measured by the ion's linear energy transfer (LET), which is the energy lost by the ion per unit length in the material of interest normalized by the particular material's density [76]. LET has units of MeV-mg/cm². Not every heavy ion strike will deposit enough charge to upset a node, given that different paths through a region surrounding a sensitive node will require different amounts of time to pass through the region, which results in different amounts of charge deposited in the sensitive region.

The region surrounding a sensitive node in an electronic device from which charge from an ion strike is collected is known as the sensitive volume (sometimes referred to

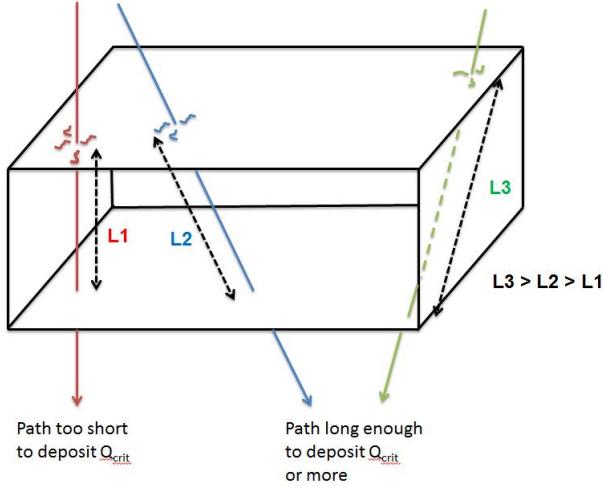


Figure 2-3: Different chord lengths of charge particles passing through sensitive region of an electronic device [36]

as the collection volume). The critical charge (Q_{crit}) is the amount of charge that must collect in the sensitive volume to cause an upset in the device. To correlate the SEU rate with the direction dependencies of a given device, the sensitive volume is often taken to be a rectangular parallel piped (RPP), a 3D volume roughly corresponding to the depletion region of a pn-junction. However, this approach only is useful as a mathematical or conceptual model and must not be interpreted as an accurate physical model. An ion's entry angle into the sensitive volume will determine the length of the path, or chord length, for that ion through the sensitive volume, as shown in Figure 2-3. Some particle chord lengths will be long enough for a particular ion to deposit Q_{crit} required for an upset, and others will deposit a smaller amount of charge that, although collected, will not cause an upset condition. [36]

Protons can also induce SEE in electronics. Typically, protons do not generate sufficient ionization to produce the charge necessary for SEE. Instead, protons cause SEE via nuclear interactions with secondary particles (spallation and fractionation products) [36]. Proton energy (more so than LET) is significant in the production of secondary particles that can cause SEE, therefore device sensitivity to these particles usually is expressed as a function of incident proton energy [76]. If a proton strike causes nuclear reaction within a sensitive region of a node, an upset will occur [36].

2.2 Radiation Effects on FPGAs

An FPGA is a configurable integrated circuit based on a high logic density regular structure, made up of an array of logic blocks and interconnections customizable by programmable switches. The user can customize the logic blocks and interconnections to realize various designs for different applications [21]. Currently, antifuse-based, SRAM-based, and flash-based technologies are the main methods used to implement the programmables switches in FPGA devices. Many NASA systems have used FPGAs that employ antifuse technology, in which permanent connections are programmed by high-current pulses that change the state of small regions in the gate array, making circuit connections to implement the user design [21]. Anti-fuse FPGAs are one time programmable (OTP), meaning the user may program the interconnections between logic blocks only once. Actel and Aeroflex are the primary manufacturers of antifuse FPGAs.

In SRAM FPGAs, the programmable switch is usually a pass transistor or multiplexer controlled by the state of a Static Random Access Memory (SRAM) bit [21]. Thus, SRAM-based FPGAs are reconfigurable, allowing users to reprogram them thousands of times. Antifuse technology has several inherent limitations that make SRAM-based FPGAs more attractive. First, once an antifuse device is programmed, it cannot be changed; additional devices have to be programmed and physically replace the installed devices. Second, available antifuse gate arrays are considerably smaller in gate count than SRAM configurable gate arrays. [21] However, SRAM-based FPGAs customizations are volatile, resulting in the FPGA losing its configuration when the device is powered off. Thus, SRAM-based FPGAs must be programmed with the desired interconnections each time they are powered on. Atmel and Xilinx are the primary manufacturers of SRAM-based FPGAs for space applications.

Flash-based FPGAs, in which the programmable switch is a floating gate transistor that can be turned off by injecting charge onto the floating gate [21], are also a design option for space-based systems. Although flash-based switches are non-volatile and will survive power cycling, TID is a problem for Flash-based technology [47].

Table 2.1: TID rating and SEL immunity for various space grade FPGAs

Manufacturer	Model	Technology	TID Rating (krad)	Latchup Immunity (MeV-cm ² /mg)
Aeroflex	UT6325 Eclipse[17]	Antifuse	300	120
Microsemi	RT3PE600L[16]	Flash	25 - 55	96.5
Microsemi	RTAX-S[4]	Antifuse	200 - 300	117
Xilinx	XQR4V[9]	SRAM	300	125
Xilinx	XQR5VFX130[95]	SRAM	1000	125

Flash-based memories require a charge pump to facilitate writing and erasing, and charged particle interaction degrades the charge pumps [85]. Radiation testing also has shown NAND-based architectures to be inherently more sensitive to TID damage than NOR-based architectures [85]. Actel is the primary manufacturer of Flash-based FPGAs, such as the RT3P series [16]. Table 2.1 lists the advertised TID and SEL ratings of several space-grade FPGAs.

Traditionally, Altera reconfigurable FPGAs have not been considered for space applications due to their tendency to latchup in radiation testing with low LET (cite Single Event Effects Test Results for Advanced Field Programmable Gate Arrays, 2006) [22]. However, recent testing of the Altera Stratix-IV indicated that the device was latchup immune up to an effective LET of 145.5 MeV-cm²/mg [42]. Thus Altera devices may be suited for space applications, pending further SEL, static, and dynamic testing in conjunction with fault tolerance mitigation characterization.

2.2.1 Xilinx SRAM-based FPGAs

This thesis focuses on fault mitigation strategies and techniques in SRAM-based FPGAs, specifically Xilinx FPGAs. Xilinx FPGAs consist of an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by an array of routing switches (general routing matrix (GRM)) located at the intersections of horizontal and vertical routing channels. Each CLB has a set of look-up tables (LUT), multiplexers, and flip-flops, which are divided into slices. A

LUT is a logic structure able to implement a Boolean function as a truth table. The CLBs provide the functional elements for constructing logic while the IOBs provide the interface between the package pins and the CLBs. The FPGA matrix also has dedicated memory blocks called BRAMs, clock delay-locked loops (DLLs) for clock distribution delay compensation, clock domain control phase lock loops (PLL) for frequency multiplication and clock network de-skew, and other components that vary according to the FPGA family. Figure 2-4 shows a generic representation of the Xilinx FPGA architecture. [21]

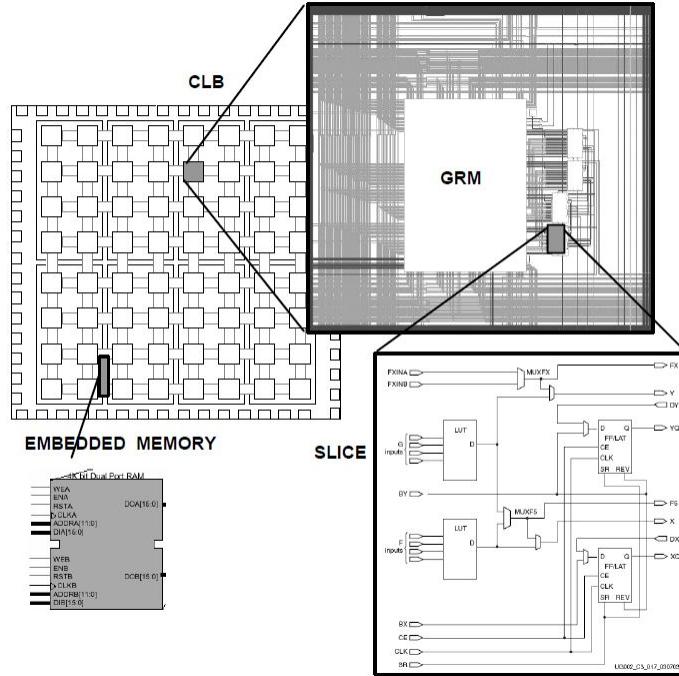
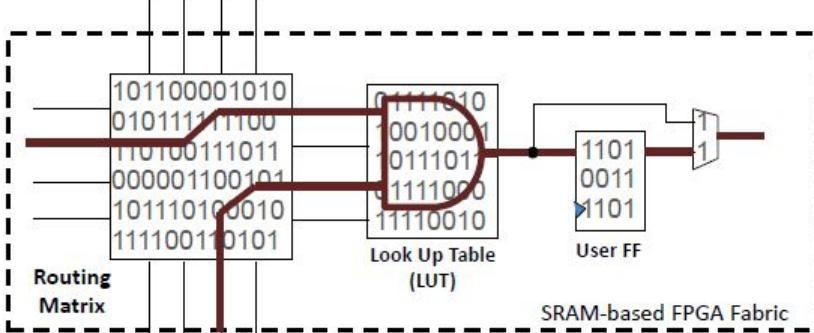


Figure 2-4: Xilinx SRAM-based FPGA Architecture [21]

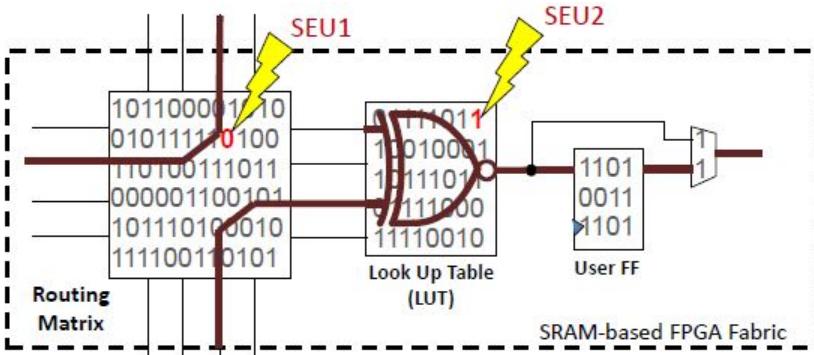
2.2.2 SEE in SRAM-based FPGAs

In an SRAM-based FPGA, configuration memory cells control the routing and logic of a user design on the device. Thus, upsetting an SRAM cell in the configuration memory can change the behavior of the user design until proper value is restored to the SRAM cell [80]. Figure 2-5a shows the correct operation of a user design a routing, LUT, and flip flop configuration intended to implement a logical AND with the series of 1's

and 0's representing the individual configuration cells that control the function of the routing and logic elements. Figure 2-5b then illustrates how SEU-induced changes (sometimes known as bit flips) to values stored in the configuration memory cells could cause an unintended signal rerouting and change in the logical function of the design.



(a) User design operating correctly



(b) Error in user design resulting from SEU-induced configuration cell bit flip

Figure 2-5: SEU effects in SRAM-based FPGA logic fabric [68]

Unlike most electronic components, in which SEU-induced errors either temporarily change the behavior of a circuit (such as in the case of an SET), or permanently damage the circuit (in the case of a SEL, SEB, or SEGR), SEU-induced configuration cell changes in SRAM-based FPGAs can cause errors that take on the characteristics of both transient errors and permanent errors [80]. As a result of this dual set of radiation effects vulnerabilities, researchers usually distinguish between static and dynamic radiation effects in SRAM-based FPGAs. Static effects are errors caused

by radiation-induced upsets to the bit-value stored in any storage element (e.g. configuration cells, user flip-flops, BRAM cells, etc.) [78]. Dynamic effects are upsets resulting from inadvertent latching of transitory effects (SETs) in the control, clocking and access circuitry of a storage cell. The unpredictable nature of permanent changes to user designs has traditionally been a roadblock to the use of SRAM-based FPGAs in space systems and has motivated the importance of protecting configuration memory in SRAM-based FPGA designs for space missions.

It is important to note a static upset a configuration memory cell is not synonymous with a functional error because a given configuration cell upset might have no effect on user design functionality. [29]. In Xilinx FPGAs, approximately one of every eight configuration bits is a routing bit, and less than 40% of routing bits are in use in a fully utilized FPGA [26]. Additionally, because less than 20%, and typically less than 10%, of the configuration cells have any significance to a design implementation, a high probability exists that any given configuration bit flip will have little or no effect on the design. For example, the programmable interconnect has many possibilities, but only a few of those possible connections are used in a particular design, meaning an SEU causing the connection of an unused segment of interconnect to another unused segment has no effect on a given design [34]. Also, an SEU affecting device unused hardware resources (such as unused CLBs, I/O, DCMs, BRAMs, etc.) will not affect the design [33].

2.2.3 Multi-Bit Upsets in SRAM-based FPGAs

Multi-bit upsets (MBUs) can introduce more than one error into a system at any given time. Thus, MBUs in SRAM-based FPGAs are of significant concern because their effects break the underlying assumptions for systems using triple modular redundancy (TMR) fault mitigation techniques, which rely on no more than one error occurring in the system at any one time.

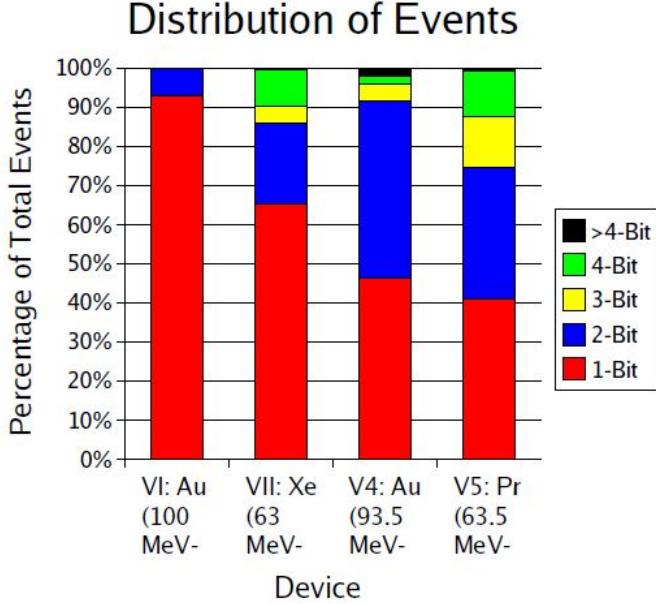


Figure 2-6: Distribution of single bit and multi-bit upsets in accelerator testing of Xilinx Virtex FPGA family [48]

MBUs can manifest as multiple independent errors or span redundant circuit copies [48]. When an error in two or more redundant copies (domains) of a circuit implemented with TMR causes the voter to select the wrong value, a domain crossing error (DCE) occurs [74].

As shown in Figure 2-7, radiation testing of Xilinx FPGAs has shown that each successive Virtex family has been more susceptible to MBUs than previous generations [48] [74]. Figure 2-6 shows a breakdown of single bit and multi-bit upsets as a percentage of total upsets observed during testing.

2.2.4 SRAM-Based FPGA SEFI

SEUs that affect the values stored in an SRAM-based FPGA's control logic elements can cause a SEFI to occur [43]. When a SEFI occurs in an SRAM-based FPGA, a complete reconfiguration or power-cycle of the device is required before the design returns to normal functionality [83]. A list of SEFIs observed in XRTC radiation testing of the Virtex-5QV follows below [83].

POR SEFI

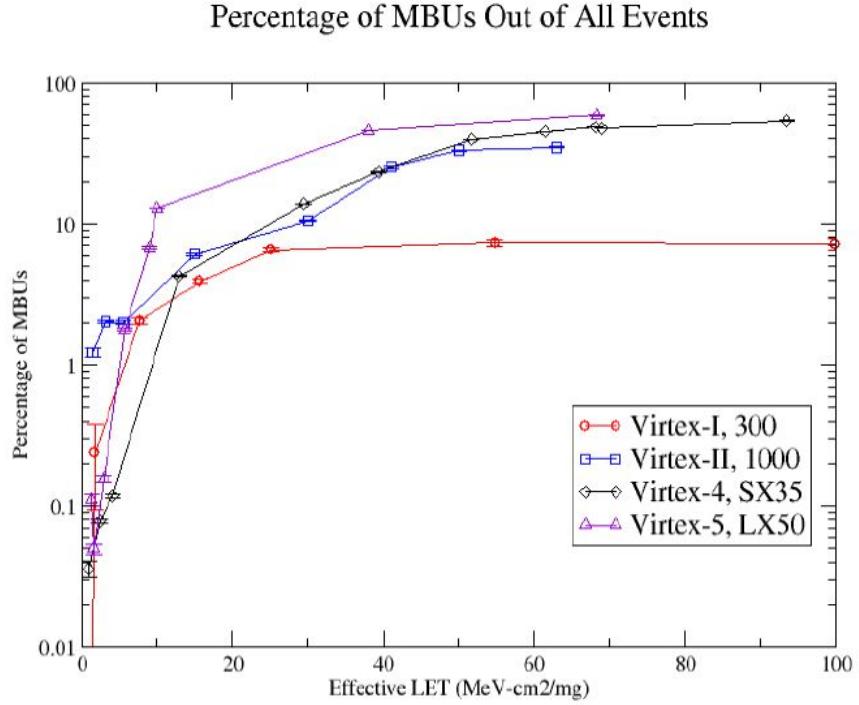


Figure 2-7: Percentage of observed radiation-induced errors that were MBUs at various particle energies for Xilinx Virtex FPGA family [48]

The Power-On-Reset (POR) SEFI results in the loss of all program and state data and reset of all internal storage cells. This SEFI is evidenced by the DONE pin dropping low, a sudden drop in the FPGA current consumption to its pre-configuration value, and the loss of all configuration functions. After a POR SEFI, attempts to readback the configuration bitstream will result in an unusually large number of readback errors.

SMAP SEFI

SelectMAP (SMAP) SEFIs result in loss of capability to read or write through the SelectMAP port of the FPGA. The SelectMAP port provides access to the the FPGA's configuration memory for bitstream readback and modification. The inability to refresh data or the retrieval of only meaningless data over the SelectMAP interface indicates this SEFI has occurred.

FAR SEFI

The frame address register (FAR) SEFI results in the continuous incrementing

of the FAR in an uncontrollable fashion. The FAR holds the configuration frame address for access into the FPGA’s configuration memory. This SEFI is evidenced by the loss of capability to read and write control values to the FAR while other aspects of the SelectMAP port remain fully functional.

Global Signal SEFI

The Global Signal SEFI includes assertion of the Global Set/Reset (GSR), Global Write Enable (GWE), Global Drive High (GHIGH_B), and others. A user design can observe all of these signals via the status register (STAT) or one of the control registers (CTLx).

Although so-called “scrub SEFIs” were observed in radiation testing of the Virtex-4QV [43], XRTC testers have not observed them in testing of the Virtex-5QV [83]. SEFI testing usually involves exposing the FPGA to a significantly higher flux of highly energetic particles than are observed in worst case space environments. SEFIs are typically low in occurrence and rarely occur on-orbit¹. However, in test environments where test engineers hugely accelerate event rates to obtain statistical significance and accurate measurements of upset conditions with negligible event cross sections, SEFIs may occur [43].

2.2.5 Terrestrial Radiation Effects

Surface-based (terrestrial) upsets are of interest to systems that must be highly reliable and highly available despite being very sensitive to radiation. High altitude military and commercial aircraft systems encounter over 300 times the amount of neutron radiation than systems operating at sea-level. FPGAs are vulnerable to radiation effects at high altitudes, and are also vulnerable to radiation-induced upsets on the earth’s surface [72]. Among other considerations, this is due to the scaling (or shrinking) of the microscopic transistors and other electronic components of devices. As discussed previously, the smaller the device size, the easier it is for a low energy particle to cause an error. Thus, as technology continues to improve and shrink,

¹See Quinn et. al.[73] for discussion of an observed Virtex-4 SEFI on-orbit

systems will experience more and more undesirable effects due to radiation on earth [36].

Table 2.2: Neutron cross section per bit for several Xilinx FPGA families [97]

FPGA Family	Configuration Memory	Block RAM	Error
Virtex-II Pro	2.74×10^{-14}	3.91×10^{-14}	+/- 10%
Virtex-4	1.55×10^{-14}	2.74×10^{-14}	+/- 10%
Virtex-5	6.70×10^{-15}	3.96×10^{-14}	+/- 10%

The Rosetta neutron single event upset (NSEU) test is an ongoing Xilinx effort to characterize the effects of neutron induced errors from 60,000 feet of altitude down to sea level [62]. Xilinx has placed test systems at various locations world wide—an example of such a test system for Virtex-II devices appears in Figure 2-8 and contains 100 XC2V6000 chips arranged in a ten by ten matrix for a total of nearly two billion configuration bits under observation. Much of Xilinx's reliability data for FPGA functionality and hardware module reliability [97] is based on testing with the Rosetta modules.

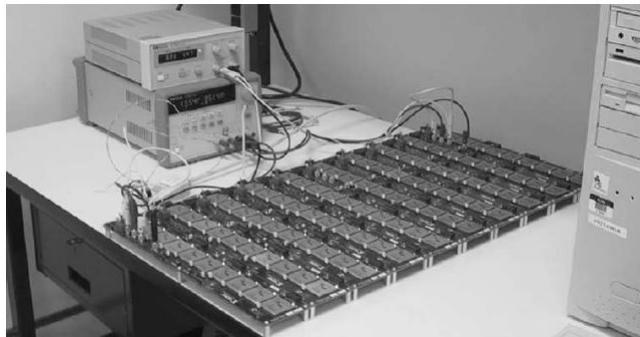


Figure 2-8: Rosetta experiment array of 100 Virtex devices [62]

2.3 FPGA Radiation Effects Prediction and Testing

Modeling radiation effects on a particular FPGA requires physical characterization of the FPGA and characterization of the planned orbit the FPGA will encounter in

space. Bombarding the FPGA with ionized particles in a particle accelerator chamber and monitoring the effects provides physical characterization of the FPGA’s radiation response, while characterizing the planned orbit typically consists of using established software tools to obtain estimates of charged particle flux in the planned orbit. Once researchers and designers accomplish both of these steps, they can then calculate an estimate for the number of radiation-induced upsets the FPGA will experience on-orbit [36].

2.3.1 Device Cross Section

As described in this section, static cross section is used to measure the static vulnerability of an FPGA to radiation effects. Researchers determine an FPGA’s static cross section by observing the number of static upsets induced in the device by a given fluence of radiation during particle accelerator testing. The static cross section of a device, σ , is calculated by dividing the number of upsets observed by the fluence of particles, as shown below in Equation 2.2 [36].

$$\sigma = \frac{\#errors}{particle\,fluence} = \frac{\#errors}{\#(particles/cm^2)} = (cm^2) \quad (2.2)$$

This static cross section corresponds to the sensitive or SEU vulnerable area of the device to radiation at a particular energy. To determine an overall static per-bit cross section, researchers repeat experimental testing at a range of particle energy levels and fit the resulting data points to a distribution for analysis (the Weibull distribution is commonly used, as discussed below). In addition, testers repeat experimental device characterization for both protons and heavy ions, facilitating static cross section estimates for each type of radiation. [36]

Several complicating factors may arise in determining a device’s static cross section, one of which is many particle accelerators are limited in the energy level of particles they can generate for testing. In these cases, researchers may tilt the device with respect to the particle accelerator beam to increase the effective LET. As was discussed previously, providing a longer path through sensitive regions allows

charged particles more time to deposit charge and thus upset the node (see Figure 2-3). Multiplying the denominator of Equation 2.2 by the cosine of the particle angle of incidence (theta) accounts for the increase in effective LET and angle of incidence, as shown in Equation 2.3 [36].

$$\sigma = \frac{\#errors}{particle fluence \times \cos(\theta)} = \frac{\#errors}{\#(particles/cm^2) \times \cos(\theta)} = (cm^2) \quad (2.3)$$

2.3.2 Weibull Curves

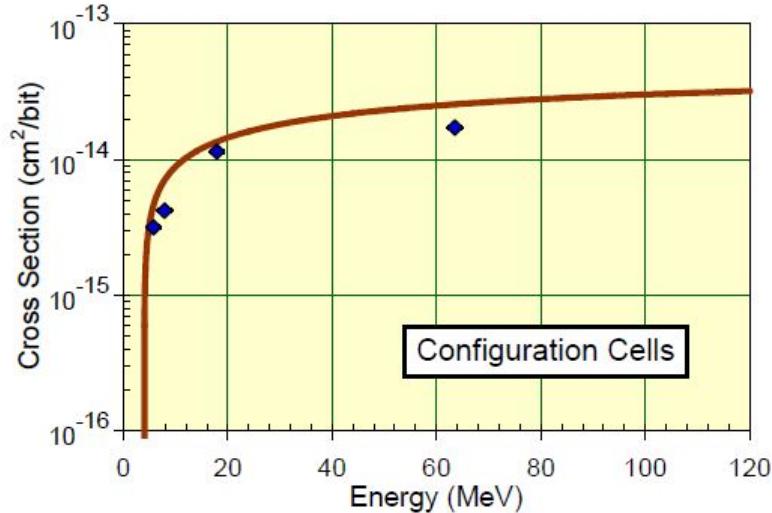


Figure 2-9: Weibull curve for Virtex-4QVSX55 configuration cell upset susceptibilities to protons [43]

Weibull curves are typically used to represent the vulnerability of an FPGA (and other microelectronics) to charged particles, via fitting the cross section data obtained during testing. The curves show the per bit cross section vulnerability of a given device to different charged particle energies. Equation 2.4 gives the Weibull distribution for protons [36].

$$\sigma(energy) = \sigma_{sat}(1 - e^{-[(x-x_o)/W]^s}) \quad (2.4)$$

where σ_{sat} is the limiting or plateau cross section of the device in cm^2 , x is the proton energy in MeV , x_o is the upset threshold energy in MeV , W is the dimensionless width parameter, and s is the dimensionless exponent parameter of the Weibull fit. An example of a proton Weibull curve fit to test results of the Virtex-4QV SX55 FPGA's static cross section for configuration cells appears in Figure 2-9.

Weibull curves for heavy ion cross sections are calculated slightly differently to account for the effective LET of the heavy ions. Equation 2.5 gives the heavy ion Weibull distribution [43].

$$\sigma(LET) = \sigma_{sat}(1 - e^{-(L-L_{thresh})/W]^s}) \quad (2.5)$$

where σ_{sat} is the limiting or plateau cross section of the device in cm^2 , L is the effective LET in $MeV \times cm^2/mg$, L_{thresh} is the upset threshold LET in $MeV \times cm^2/mg$, W is the dimensionless width parameter, and s is the dimensionless exponent parameter of the Weibull fit.

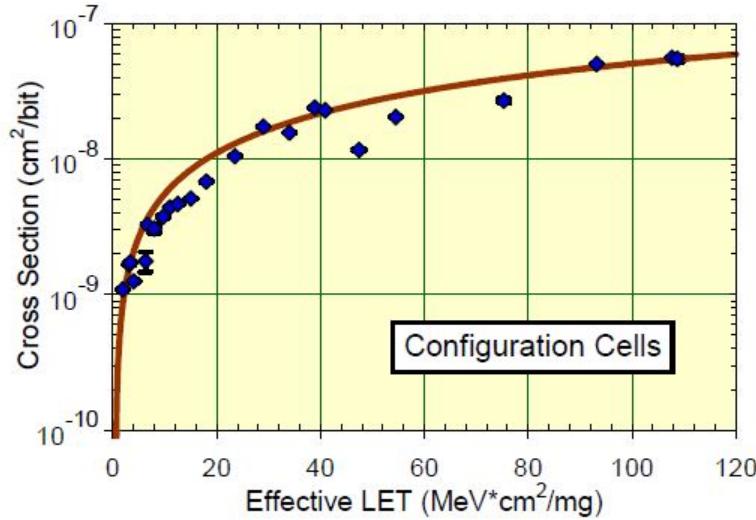


Figure 2-10: Weibull curve for Virtex-4QV SX55 configuration upset susceptibilities to heavy ions [43]

An example of a heavy ion Weibull curve fit to test result's of the Virtex-4QV's configuration cell static cross section testing results appears in Figure 2-10.

For SRAM-based FPGAs, SEFI device cross sections sometimes appear to be

on the same scale as the SEU bit cross sections, but in reality when the SEU cross sections are scaled to device cross sections, the SEU cross sections are several orders of magnitude larger than the SEFI device cross sections. While the SEU bit cross-section is very small, each device has millions of configuration bits. The SEFI device cross section reflects the accurate reasoning that only 10-1000 bits usually are responsible for each SEFI state [49].

2.3.3 CREME96

The Naval Research Laboratory first developed the Cosmic Ray Effects on Micro-Electronics (CREME) modeling and simulation tool in 1981, and CREME has since become the industry standard for predicting upset rates in electronics due to ionizing radiation [36].

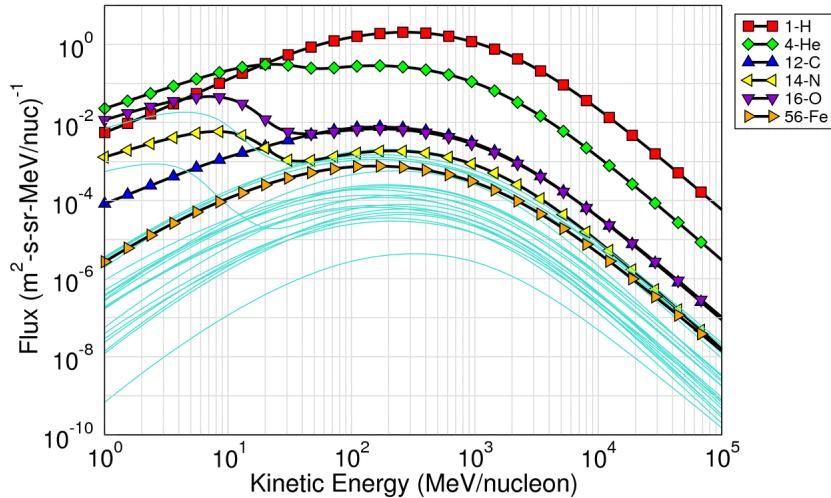


Figure 2-11: CREME96-generated predictions for various charged particle flux for interplanetary/geosynchronous orbit during solar minimum

CREME creates numerical models of the near-Earth space radiation environment and evaluates the expected error rates from radiation effects on the electronic device given user-supplied device cross section data. CREME can predict upset rates for a given device from both proton and heavy ion interaction. Seven different solar

conditions for flux of particles in the near earth radiation environment are available: solar minimum, solar maximum, solar minimum trapped proton peak, solar maximum trapped proton peak, worst week, worst day, and worst 5 minute peak. Engle et. al. provide a concise review of the CREME96 calculation process [36]. Figure 2-11 is an example CREME output for charged particle flux in interplanetary/geosynchronous orbit during solar minimum, and Figure 2-12 is an example CREME96 output for heavy ion LET flux in interplanetary/geosynchronous orbit during solar minimum.

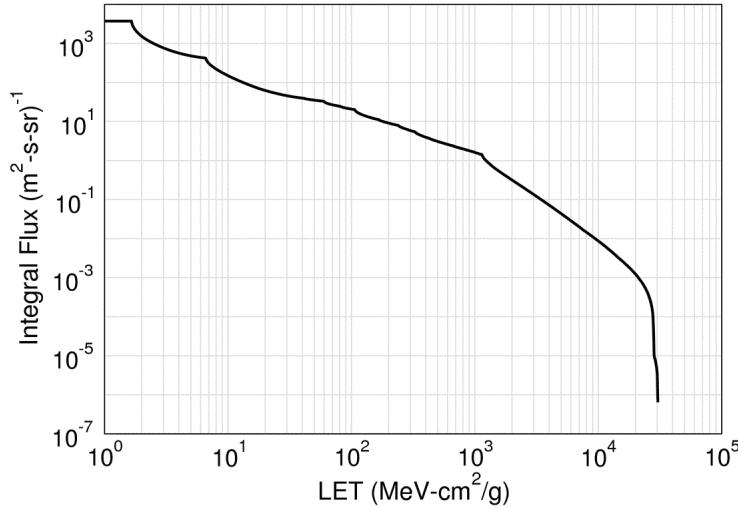


Figure 2-12: CREME96-generated predictions for integral LET spectrum for interplanetary/geosynchronous orbit during solar minimum

2.3.4 Upset Rate Prediction

Using estimates of the charged particle flux from software tools like CREME and measured device sensitivity to radiation effects in the form of device cross sections, researchers and designers can estimate device error rates for a given orbit. The calculations are different for proton error rates and heavy ion rates due to the angular dependence of heavy ion effects. To estimate the expected upset rate due to protons, one integrates the product of the device proton cross section and the flux of protons with energy larger than some E over all E , as shown in Equation 2.6 [36].

$$UpsetRate = \int_0^{\infty} \sigma(E)f(E) dE. \quad (2.6)$$

where $\sigma(E)$ is the device proton cross section as a function of energy E and $f(E)$ is the differential flux of particles with energy $>E$.

To estimate the error rate due to heavy ions, one essentially multiplies the device heavy ion cross section for each LET value with the predicted heavy ion flux at the LET value and then integrates over the entire LET spectrum of interest. However, as mentioned previously, only ions of a particular LET with sufficient chord length to deposit Q_{crit} will cause an upset. Thus a term to account for the percentage of particles P at a specific LET α that will deposit at least Q_{crit} is introduced into the calculation. Equation 2.7 shows the simplified calculation. [36]

$$UpsetRate = \int_0^{\infty} \sigma(\alpha)P(\alpha)F(\alpha)d\alpha. \quad (2.7)$$

where α is the LET in MeV-mg/cm², $\sigma(\alpha)$ is the heavy ion cross section as a function of α , $P(\alpha)$ is the differential of path lengths in the sensitive volume that can deposit Q_{crit} with a LET of α , $F(\alpha)$ is the integral flux of heavy ions with LET $>\alpha$.

2.3.5 Fault Injection

Fault injection involves inserting faults into particular targets in a device at a determined time in the operating process and monitoring the results to determine the design's fault response behavior [63]. In SRAM-based FPGAs, fault injection takes the form of intentionally corrupting configuration bits in the device and observing the effects on the user design [37]. Due to its high flexibility in terms of spatial and temporal information, fault injection is an attractive technique for the evaluation of design characteristics such as reliability, safety, and fault coverage. Additionally, it also offers reduced turnaround time and evaluation cost compared to traditional radiation ground testing with particle accelerators, aiding designers in developing SEU-hardened systems [63].

Radiation testing with a particle accelerator is used in many cases to validate fault

injection analyses and results [80] [63] [57]. The limitations of fault injection methods include inability to alter the state of flip flops in the FPGA [57] and inability to simulate errors in the logic that controls the configuration process (bitstream loading) [31]. If possible, a combined characterization strategy including both particle accelerator testing and fault injection testing provides a comprehensive set of fault modes and error conditions, which designers may use to develop higher fidelity radiation effects models.

2.4 Traditional Mitigation Techniques

A large amount of research and testing has identified techniques for mitigating the effects of radiation-induced upsets in electronics, specifically in FPGA designs [49] [47]. Configuration scrubbing, Triple Modular Redundancy (TMR), and error correcting codes (ECC) are among the most popular. Additionally, in an SRAM-based FPGA design using BRAM to store data (such as the instruction and data memory of a softcore processor), designers should employ techniques to protect user design memory.

2.4.1 Configuration Bitstream Scrubbing

Because upsetting an SRAM cell in the configuration memory can change the behavior of a user design in an SRAM-based FPGA, constantly monitoring the configuration bitstream to avoid fault accumulation is necessary [21]. The process of detecting upsets in configuration memory is known as configuration bitstream monitoring, while correcting upsets in configuration memory is known as configuration bitstream scrubbing. While the user design runs on an SRAM-based FPGA, a scrubbing unit continually checks for upsets in the configuration memory. Scrubbing allows a system to repair bit-flips in the configuration memory without disrupting the user design operation, including the memory cells controlling the CLB, LUT, and routing configurations. Configuration scrubbing prevents the build-up of multiple configuration errors and reduces the time in which an invalid circuit configuration is allowed to

operate within the user design. In Xilinx FPGAs, scrubbing does not refresh the contents of CLB flip-flops, BRAMs, or Dynamic Reconfiguration Ports (DRP), as these bits are not accessible through bitstream readback [21]. However, the configuration bits occupy significantly more memory cells in an SRAM-based FPGA than the flip flops, BRAMs, and DRP bits, as shown in Table 2.3.

Table 2.3: Configuration and user memory bit percentages for the Xilinx Virtex-4 FX60 FPGA [80]

Memory Type	Bits	Percentage of Total
Configuration Bits	20,960,512	81.0%
User BRAM Bits	4,870,144	18.8%
User Flip-Flop Bits	50,560	0.2%

Designers may apply a power cycling scheme as the simplest form of scrubbing because it causes FPGA reconfiguration, which eliminates any accumulated errors [26] (assuming the memory device storing the configuration bitstream does not suffer any radiation-induced upsets). At the very least, an external device is required to remove power from the FPGA and then reapply power to the FPGA to start configuration with an error-free bitstream. However, a power cycle only scheme provides no visibility into the nature of the configuration errors and allows errors to persist until configuration occurs after power-up, both of which are significant drawbacks.

Most mitigation approaches use either a monitoring and scrubbing unit external to the FPGA or an internal monitor and scrubber implemented on the FPGA with a combination of custom logic and dedicated hardware modules. If the scrubber is external, it typically is implemented on a separate RadHard processor, FPGA, application specific integrated circuit (ASIC), or programmable logic device (PLD). An external scrubber also may read the contents of the FPGA configuration bitstream and compare it for errors against a “golden” (un-irradiated and correct) copy of the configuration bitstream, which usually is stored in radiation-hardened non-volatile memory. If the scrubber is internal, it may use hardware modules to calculate Cyclic Redundancy Check (CRC) values of frames of the configuration bitstream and com-

pare them to the known CRC values for each frame [80] [33], or rely on Hamming codes for SECDED error mitigation [31].

For Xilinx FPGAs, external scrubbing usually is performed through the SelectMAP interface. In an external scrubbing scheme, the configuration controller must be able to perform three of the four key functionalities listed below, with readback/error detection optional under specific circumstances [87]:

- FPGA configuration
- SEFI detection and handling
- Active partial reconfiguration (scrubbing)
- Readback/error detection

External “blind” configuration scrubbing typically performs constant rewrites of configuration memory values whether or not upsets have occurred in the memory cells [51]. If no upsets have occurred, the scrubber will simply write the same configuration data into the FPGA that is already present for each pass over the bitstream. If upsets have occurred, scrubbing will overwrite the upset configuration bits with correct values [51]. In the past, this so called ”blind” scrubbing (i.e., without configuration readback) was done more frequently. Through the years, however, the logic and registers necessary for scrubbing have grown larger and SEUs in these areas during scrubbing have been observed to cause high current latchup states [49].

Readback scrubbing with correction is a variation of blind scrubbing. In this mode, an external scrubber reads back the FPGA internal configuration memory and compares it with a golden bitstream. If the scrubber finds a difference between the bitstreams, the scrubber overwrites the erroneous configuration frame with the correct values from the golden bitstream [51]. The external scrubber may calculate a CRC value for each configuration frame prior to beginning scrubbing, thus allowing rapid comparison of each frame’s CRC to the corresponding golden frame’s CRC during scrubbing. Because the device bitstream is not scrubbed top-to-bottom, SEUs in the configuration circuitry only should have a localized effect [49].

2.4.2 Triple Modular Redundancy

TMR is the classic and most commonly used error mitigation technique for SRAM-based FPGAs [79] [49]. TMR provides fault tolerance by triplicating a user design and instantiating a voter to vote on the outputs of the three modules. If a fault occurs in one of the triplicated versions of the design, the other two modules will out-vote the faulty module, ensuring the overall output remains correct. The circuits must operate in lockstep for the voter to atomically compare their outputs [65]. However, since the configuration bits controlling logic and routing in an SRAM-based FPGA are susceptible to SEUs, the voter itself and all routing also must be triplicated to prevent errors due to a fault in the voter [79]. Implementing TMR in a design can incur power and area costs of up to 3 times more than what a non-triplicated design would require [26].

Much of the FPGA design process depends on synthesis tools designed to minimize the area and maximize the speed of the user design in the FPGA fabric [49]. Despite a designer's intentions, synthesis tools may remove some or all of the redundant circuit modules meant to implement TMR in a circuit in order to optimize a circuit for performance (speed) and minimal hardware area consumption [47]. This issue is especially salient when inputs and outputs are single sourced in a design [47]. As shown in Figure 2-13, the synthesized circuit that will be programmed into the FPGA is not protected by TMR, and the remaining voters increase the sensitive cross-section of the design [47]. To combat over-zealous synthesis tools, industry and researchers have developed specialized synthesis tools, such as the Xilinx TMRTTool [14] [47] and BYU BL-TMR Tool [47] [73], to maintain TMR implementations.

2.4.3 User Memory Protection

Since most designs make use of internal BRAM for data storage, providing fault tolerance and reliability techniques to BRAM is of prime importance in FPGA systems. For softcore processors in particular, upsets in the user memories must be detected and corrected [80]. Additionally, because BRAM cells switch quickly between states

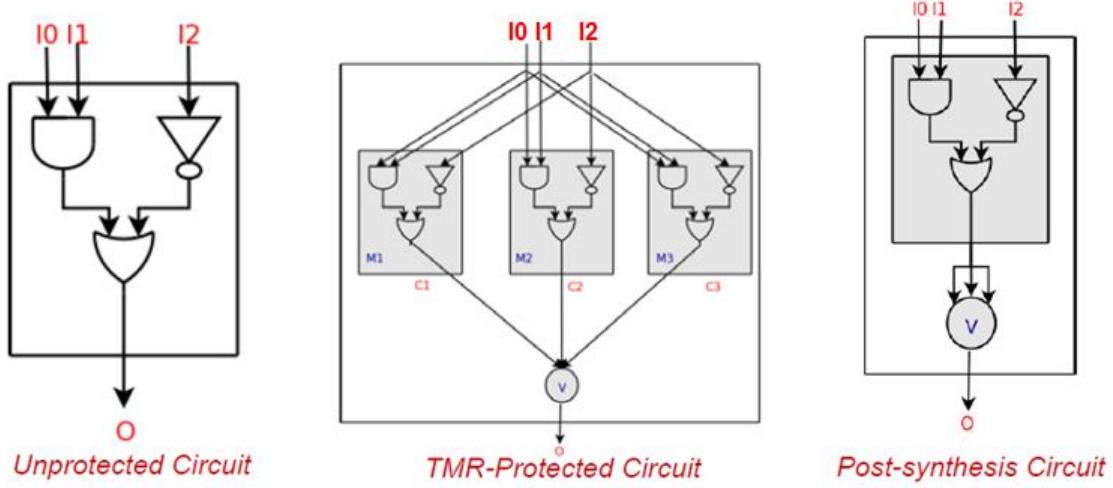


Figure 2-13: Example of FPGA synthesis tool removing redundant modules to optimize circuit for speed and area [47]

during operation, they are more susceptible to SEUs than configuration cells, which remain static during most (if not all) of operation [33]. As noted previously in this section, configuration bitstream scrubbing does not access the memory bits stored in BRAM and is therefore not useful for correcting radiation-induced errors in BRAM. Error correcting codes (ECC) and memory scrubbing are the primary methods of mitigating errors in user memory.

SECDED Methods

Error correcting codes (ECC), which consist of adding extra bits to a memory array to indicate the status of the data stored in the memory array, are traditionally the method of choice for memory protection. Hamming code, a relatively simple yet powerful ECC code, provides single error correction and double error detection (SECDED). It involves transmitting data with multiple check bits (parity bits) and decoding the associated check bits when receiving data to detect errors. The check bits are parallel parity bits generated from the logical XORing of certain bits in the original data word. If bit error(s) are introduced in the codeword, several check bits show parity errors after decoding the retrieved codeword. The combination of these check bit errors display the nature of the error, and the position of any single bit

error is identified from the check bits. [81]

SECDED provided by ECC is an efficient method to correct the effects of an SEU in a memory word and detect when two errors occur in a memory word. When more than two errors are present in a memory word, one of three results occur. Either the erroneous word is an incorrect but valid code word (thus no correction or detection occurs and the output is incorrect), or a single error is falsely corrected (and the output is incorrect), or a double error is detected. If a double error is reported when there are more than two upsets, the upsets will be caught, otherwise SECDED fails.

[79]

SECDED Hamming code implementations in BRAM are available for SRAM-based FPGAs [81], but since the ECC logic and routing is itself sensitive to upsets, measures must be taken to prevent faults caused by upsets in either user memory content, or upsets in the logic and routing protecting the memory [80]. Additionally, employing SECDED ECC in an SRAM-based FPGA has power and performance implications, which this work will address.

Memory Scrubbing

Another reliable method to mitigate errors in BRAM is to constantly refresh the BRAM contents (scrubbing). Since Virtex-5 BRAM modules are dual port memories, one of the ports could be dedicated to error detection and correction. But this also means the BRAM is available only as a single port memory to the rest of the user logic.

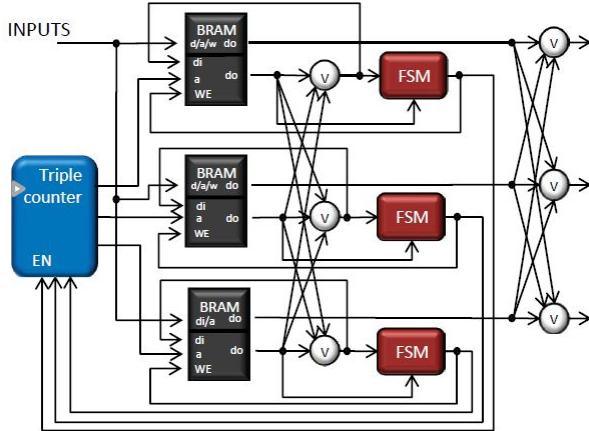


Figure 2-14: BRAM protected by TMR with memory scrubbing [79]

To refresh the memory contents, a counter is used to cycle through the memory addresses, incrementing the address once every established number of clock cycles. For each address, voters choose the correct (voted correct) data to write back into the memory [63].

Fault injection and radiation testing of various protection strategies for BRAM on Xilinx FPGAs have shown full TMR and memory scrubbing can eliminate essentially all SEU-induced errors in a BRAM or in the logic and routing leading to a BRAM, provided at least one redundant BRAM is used for effective scrubbing [80]. Figure 2-14 shows an implementation of triplicated BRAMs with memory scrubbing.

2.4.4 Combined Mitigation Approaches

The possibility of combining various fault mitigation techniques for different mission requirements and mission environments creates a trade space for system designers. Figure 2-15 shows the Xilinx overview for SEU-induced error mitigation scheme selection based on the system requirements and radiation environment [26].

Data Criticality		Low → High		
Error Persistence		No	Yes	
SEU Rate High ↓	Operating Window Low	Minutes	No Mitigation	XTMR
		Days	Scrubbing	
		Months	Scrubbing XTMR	
		Continuous	Redundant Devices	

Figure 2-15: Xilinx radiation-induced error mitigation trade space matrix [26]

In the least stringent case, when the SEU rate in the mission environment is low, the operating window is minimal, and the importance of the FPGA data production is low, a system with no added mitigation may suffice. However, as SEU rate, operating window, and data criticality increase, more mitigation techniques should be applied to the system to increase reliability, including configuration scrubbing and TMR (XTMR represents application of the Xilinx TMRTTool, which appears later in this work). In the most stringent case in which SEU rate, operating window, and data criticality are high, redundant FPGAs may be employed to achieve the highest level of reliability.

The matrix in Figure 2-15 does not account for power consumption considerations, area cost, or performance impact of the various options presented. As more mitigation techniques are added, power consumption will almost certainly increase, likely by a factor of three for TMR implementation, and possibly by a factor of two for configuration scrubbing, depending on the scrubber implementation. A designer must carefully weigh the associated cost of added mitigation techniques to ensure the mitigated system still meets power, area, and performance requirements.

2.5 Xilinx RHBD XQR5VFX130 FPGA

As the first RHBD SRAM-based FPGA, the Xilinx XQR5VFX130 (Virtex-5QV) offers radiation hardness as well as reconfigurability, making it particularly attractive

for space-based systems. This section provides a brief background of SRAM-based FPGAs in space, an overview of the Xilinx Virtex-5QV FPGA and its radiation-hardened features, and radiation test results for the Virtex-5QV.

2.5.1 SRAM-based FPGA Space Flight Heritage

A brief survey of several publicly announced space missions using SRAM-based FPGAs appears in this section to provide a background on SRAM-based FPGA space flight heritage and resources for examining past system designs, fault tolerance methods, and radiation-induced error rates. This summary is not exhaustive, but represents an attempt to locate and document published records of SRAM-based FPGAs in space.

4000 Series and Virtex

In 2003, the Virtex XQR4062XL, part of the XC4000XL series, flew on the Australian FedSat mission [25] [80]. In 2007, Los Alamos National Laboratory launched CFESat, which used three Virtex XQVR1000 FPGAs as the data processors for its reconfigurable computer experiments [27]. Two Virtex XQVR1000s were the main controllers of all brushed DC and stepper motors on the Discovery and Spirit rovers of the Mars Exploration Rover Mission, and four XQR4062XL devices controlled the Mars lander pyrotechnics [75]. Interestingly, the Xilinx FPGAs on the Mars rover mission were left powered on during the seven month cruise from Earth to Mars, and during that time the Jet Propulsion Laboratory (JPL) collected upset rate data [75].

Virtex-4 and Virtex-5

The Materials International Space Station Experiment (MISSE) is a series of experiments focused on testing the effects of a space environment on materials and computing elements. One of the MISSE-7 experiments is the Single Event Upset Xilinx-Sandia Experiment(SEUXSE) [66], which contains the space grade grade Virtex-4QVFX60 and the commercial grade Virtex-5LX330T [38]. Along with other

payloads on STS-129, SEUXSE launched to the ISS on November 16, 2009, where astronauts deployed the experiment on November 23, 2009.

On the MISSE-8, Xilinx, Sandia National Laboratories, and other partners placed the SEUXSE II experiment, which contains a Virtex-4QV and a Virtex-5QV [80]. SEUXSE II launched as a payload on STS-134, arriving at the ISS on May 16, 2011, where astronauts deployed it for operation on May 20, 2011. STS-134 also returned the MISSE-7 experiment back to earth.

The SpaceCube project at NASA Goddard Space Flight Center (GSFC) has focused on high performance reconfigurable science data processing based on Xilinx Virtex FPGAs, resulting in several successful missions. The project launched two commercial grade Virtex-4 FPGAs as part of Hubble Servicing Mission 4 in May 2009 and a commercial Virtex-5 on a sounding rocket flight in 2011. The SpaceCube team is set to launch three additional commercial grade Virtex-5QV FPGAs on the STP-H4 Department of Defense Space Test Program experiment bound for the International Space Station (ISS) and also plans to fly the Virtex-5QV in a CubeSat form factor. [86]

Another set of experiment carrying the Virtex-4 are the two Los Alamos Experimental Units (LEUs) on the Mission Response Module (MRM) experimental payload on a Department of Defense satellite, each containing one space grade XQR4VLX200 (Virtex-4QVLX200) and one space grade XQR4VSX55 (Virtex-4QVSX55) [73]. The LEUs are exposed to particularly harsh radiation environment due to their orbit profile, making for an interesting study of SEU prediction rates vs. observed error rates and the effects of shielding [73].

JPL’s Cubesat On-board processing Validation Experiment (COVE) payload, which flew on the University of Michigan’s M-cubed CubeSat mission in 2011, is based on the Virtex-5QV for high performance processing [70] [23]. At the time of this writing, ground control operators were unable to send commands to the M-cubed satellite, due to magnetic coupling of M-cubed with another nanosatellite onboard the launch vehicle following the release of the nanosatellites from the launcher. However, a reflight of the COVE payload is scheduled for late 2013.

To provide some context for comparing the radiation-hardness of the Xilinx FPGAs listed in this section, Table 2.4 shows the specified TID hardness and minimum latchup immunity for the different Xilinx space grade SRAM-based FPGA families.

Table 2.4: TID rating and SEL immunity for various space-grade Xilinx FPGAs

Manufacturer	Family	TID Rating (krad)	Latchup Immunity (MeV-cm ² /mg)
Xilinx	QPro XQR4000XL[88]	60	100
Xilinx	QPro Virtex[90]	100	125
Xilinx	QPro Virtex-II[89]	200	160
Xilinx	Virtex-4QV[9]	300	125
Xilinx	Virtex-5QV[95]	1000	125

2.5.2 Virtex-5QV RHBD Features

For Xilinx, the Virtex-5QV is the first product with extensive RHBD features; Virtex-4QV and earlier space-grade FPGAs use(d) exactly the same mask and circuitry as a particular revision of their commercial counterpart [83]. Dual-node configuration cells, 12 transistor flip flops, and epitaxial CMOS process technology provide RHBD protection for the Virtex-5QV. The Virtex-5QV is manufactured on a 65-nm process size.

Each RHBD configuration cell in the Virtex-5QV consists of two distinct nodes with internal redundancy to prevent any single node collecting charge from upsetting the configuration bit, although a brief transient on the cell output is possible [83]. Unless two nodes collect at least the minimum charges Q_{crit1} and Q_{crit2} , the cell will not upset after an SEE interaction [61]. The pairs of nodes that can induce upset by simultaneously collecting charge are intentionally spaced a certain distance apart. This results in an upset susceptibility for a given ion that varies a few orders of magnitude depending on an ion's entry angle into the device, with the vector aligned with the straight line between the two nodes being the most sensitive direction [83].

The Virtex-5QV uses Xilinx's 12 transistor (12T) flip flop design with SET filters to lower SET effects [83], as shown in Figure 2-16. The flip flops (registers) require

dual inputs that must agree to alter register state. This dual input design facilitates temporal filtering on the flip flops [28].

The use of epitaxial CMOS process technology has made Virtex Single Event latch-up immune to a LET threshold greater than 120 MeV/mg. The epitaxial layer eliminates the capacitive build up that occurs between the doped regions and the substrate, significantly attenuating the ability for excess charge from a charged particle interaction to build up and cause a transistor's state to switch [65].

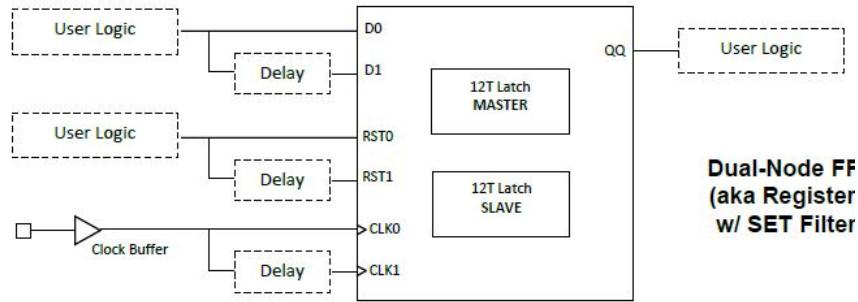


Figure 2-16: Dual node flip flops with SET filters implemented in Virtex-5QV [84]

2.5.3 Virtex-5QV Hardened and UnHardened Components

The primary focus of radiation hardening in design of the Virtex-5QV was to maximize hardness against configuration bit errors. Thus, some of the special function hardware modules in the device remain equivalent to those in the commercial Virtex-5 and are not hardened against radiation-induced effects. Table 2.5 provides a listing of the RHBD features of the Virtex-5QV and the unhardened features.

Table 2.5: XQR5VFX130 Feature Set [83]

Functional Block	Available Resources	SEU Mitigation
Logic Cells	131,072	RHBD
6-Input LUTs, CLB-FFs	81,920	RHBD
Distributed RAM (kBit)	1,580	RHBD
BRAM Blocks (36kBit)	298	EDAC
Total BRAM (kBit)	10,368	EDAC
Clock Tiles	6 (4 PLL, 2 DCM)	None
DSP48E ² Slices	320	None
MGT ³ Channels	18	None
PCIe Blocks ⁴	3	None
EMACs ⁵	6	None
User IO (MGT)	836 (18)	None

2.5.4 Xilinx TMRTTool

To support design with the Virtex-4QV and Virtex-5QV, Xilinx developed a specialized synthesis software package called TMRTTool. Traditional TMR does not protect against SEUs in voting logic or against SETs, nor does it easily support the reconfigurability of Xilinx FPGAs [14]. TMRTTool specifically addresses these issues and ensures the final logic programmed into the FPGA correctly implements TMR. To achieve these goals, the Xilinx TMR approach involves [14]:

1. Triplication of all inputs, including clocks and throughput (combinational) logic
2. Triplication of feedback logic and insertion of majority voters on feedback paths
3. Triplication of all outputs, using minority voters to detect and disable incorrect output paths

TMRTTool is available from Xilinx but is ITAR-controlled. Thus this work does not analyze design or implementation with TMRTTool.

²Digital Signal Processor

³Multi-Gigabit Transceivers

⁴Peripheral Component Interconnect Express

⁵Ethernet Media Access Control

2.5.5 Virtex-5QV Radiation Testing

The XRTC has performed hundreds of hours of heavy ion and proton testing of the Virtex-5QV to measure the radiation susceptibility of the configuration memory, logic cells, and special function hardware modules. For almost all tests, the XRTC motherboard with appropriate daughter DUT (shown in Figure 2-17) is exposed to either heavy ions or protons, depending on the test, and monitored for SEFI conditions and SEU errors.

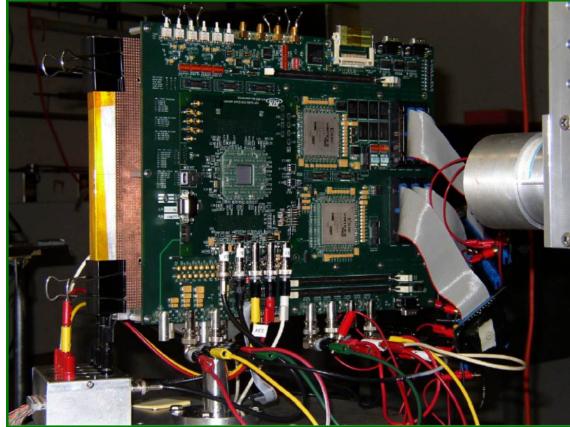


Figure 2-17: XRTC Motherboard test apparatus with supporting circuitry and interconnections used for radiation effects testing [45].

Because Virtex-5 devices are offered only in flip-chip packaging, irradiation is done through the backside of the silicon substrate. To allow charged particles from the particle accelerator to reach the active layer at the bottom of the chip with sufficiently high-LET, the backside of the silicon must be thinned to less than 100 micrometers, as shown in Figure 2-18. In Figure 2-18, the device on the left has been thinned to approximately 100 micrometers, while the device on the right is un-thinned [42].

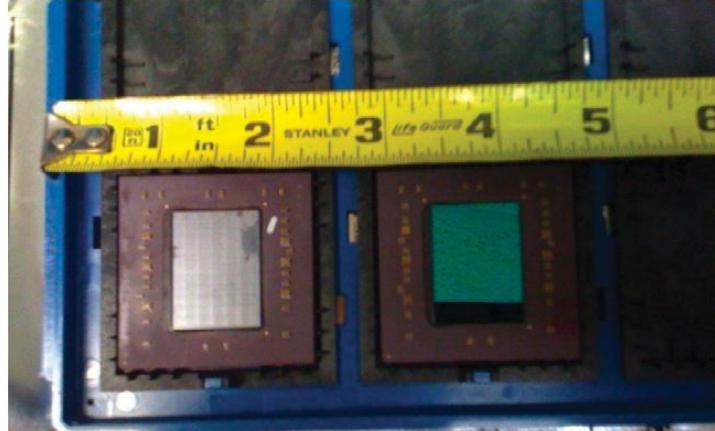


Figure 2-18: Two FX-1 series Virtex-5QV devices used for XRTC test campaigns [42]

Latchup Testing

For latchup testing, the device junction temperature, internal voltage, I/O voltage, and auxiliary voltage are held as close as possible to the maximum rated values. XRTC testers used high energy particles with an effective LET greater than 104 MeV-mg/cm^2 , and observed no latchups during bombardment. [83]

SEFI Testing

Observed Virtex-5QV SEFIs are placed into two main categories: Design-intrusive, and Visibility intrusive. In the design-intrusive category are the Power-On-Reset-like (POR) and the Global Signal (GSIG) SEFIs. The visibility-intrusive category includes the malfunctions of the SelectMap Port (SMAP) or the Frame Address Register (FAR). [83]

Static Testing

As mentioned previously, static effects are errors caused by radiation-induced upsets to the bit-value stored in any storage element, such as configuration cells, user flip flops, or BRAM. A summary of static radiation testing of the Virtex-5QV performed by various members of the XRTC appears in Table 2.6.

Table 2.6: Static radiation test results summary for Virtex-5QV [84]

XQR5VFX130	MTTU	Units	Details
SEFIs	9,930	years/Device	Mean Time to SEFI
CLB-Flip Flop (filters on)	3	upsets/century	all 81,920 bits
CLB-Flip Flop (filters off)	1-2	upsets/year	all 81,920 bits
Configuration Bits	5	upsets/year	all 34.1 million bits
Block Memory (EDAC off)	13	upsets/day	all 10.9 million bits

Dynamic Testing

As described previously in this chapter, dynamic effects are upsets that result from inadvertent latching of transitory or SETs in the control, clocking and access circuitry of a storage cell. A summary of dynamic radiation test results performed by various members of the XRTC appears in Table 2.7.

Table 2.7: Dynamic radiation test results summary for Virtex-5QV [84]

XQR5VFX130	MTTU⁶	Units	Upset and Op Details
DCM, PLL	130	years / DCM or PLL	Glitch, 12 DCMs + 6 PLLs
MGTs	20	years/GTX	LOL ⁷ 18 GTX's, 3.125 GHz
Block Memory (EDAC on)	12	years/Device	all 10.9 million bits
CLB-FF (filters on)	2.5	years/Device	all 81,920 bits, 200 MHz
CLB-FF (filters off)	2	months/Device	all 81,920 bits, 200 MHz
DSP48E	5	years/DSP	320 DSPs in Device
IODELAY	32	years/bit	836 IO's in Device
EMAC	TBD	—	—
PCIe	TBD	—	—

The static and dynamic radiation test results demonstrate the effectiveness of RHBD techniques employed in the design and fabrication of the Virtex-5QV. The BRAM with EDAC off (estimated 13 upsets per day) and CLB flip flops with filters

⁶mean-time-to-upset

⁷loss-of-link

off (estimated 6 errors/year) are the only components with a predicted error rate more frequent than once every few years. Table 2.8 shows the dramatic improvement in radiation hardness of the Virtex-5QV as compared to the space grade Virtex-II Pro and space grade Virtex-4QV.

Table 2.8: Estimated upset rates in geosynchronous orbit for Xilinx Virtex space-grade FPGAs

FPGA	Configuration Memory (upsets/device-day)	BRAM (upsets/device-day)	SEFI (device-years/event)
XQR2V6000[26]	13.3	2.03	181
XQR4VFX60[43]	4.4	3.26	103
XQR5VFX130T[84]	0.014	0.0023 ⁸	9930

2.6 Conclusion

SRAM-based FPGAs offer significant design flexibility and impressive processing capability for space-based missions, at the cost of increased radiation-induced error vulnerabilities as compared to RadHard antifuse FPGAs. By understanding and analyzing the expected mission radiation environment, performing fault injection, and characterizing the radiation effects response of an FPGA through particle accelerator testing, designers can choose appropriate mitigation techniques to increase the reliability of an FPGA-based system on orbit. These mitigation techniques come at the cost of increased power consumption, increased cost, and in some cases limited performance ranges.

⁸with EDAC enabled

Chapter 3

Fault Tolerant Design on RHBD SRAM-based FPGAs

The primary focus of this work is to identify the additional design considerations and factors recommended for designing with a RHBD SRAM-based FPGA in a space-based embedded system as well as to characterize the system design space resulting from applying the additional design techniques. The Xilinx Virtex-5QV FPGA is the RHBD SRAM-based FPGA analyzed in this work, as at the time of this writing it is the only such FPGA in commercial production. The additional considerations in fault tolerant system design with a RHBD SRAM-based FPGA are implementation of configuration bitstream management and scrubbing, protection of unhardened, special purpose hardware blocks through fault tolerance and redundancy, and softcore processor fault tolerance and watchdog application.

The analysis presented in this work assumes TMR is not necessary for logic modules implemented with LUTs and flip flops in the Virtex-5QV due to the inherent design effort to harden most of the internal components of the FPGA. Thus this work does not analyze the additional costs of applying TMR to user logic designs on the Virtex-5QV. However, this work does consider redundancy techniques for the special function hardware modules of the Virtex-5QV.

3.1 Configuration Bitstream Scrubbing

The reliability of the configuration bitstream is essential to SRAM-based FPGA operation. If the bitstream stored in non-volatile memory is unintentionally altered (e.g. by an SEU) before loading onto the FPGA, then the user design represented by the bitstream could operate incorrectly or fail entirely. If the FPGA configuration programmed by the bitstream is altered while the user design is operating on the FPGA, it could cause errors in the design operation or failure of the design.

As noted previously, because less than ten percent of configuration cells have a direct effect on a typical user design, nine out of ten configuration SEUs will have no effect on the user design [33]. However, if an SEU flips a critical bit in the design (the bit controlling the global reset for example) then it does not matter that the previous nine SEU-induced bit flips had no effect on the design's operation, because the design has suffered a major fault from the critical bit flip. Thus taking design steps to mitigate the effects of SEUs in the configuration memory is essential to reliable SRAM-based FPGA in the space environment.

As outlined in Chapter 2, both external and internal approaches exist to configuration management and bitstream scrubbing. External scrubbing usually involves a RadHard ASIC or OTP FPGA [21], such as an Actel RTAX or Aeroflex Eclipse. An internal scrubbing design typically uses internal hardware modules and supporting user logic to detect single and double bit errors and correct single bit errors, and an internal design should at least include an external watchdog timer or circuit of some kind[21]. A trade space exists when making a design choice between adding an external device versus relying on internal hardware modules for configuration management and scrubbing. Although external scrubbers are more reliable than internal self-scrubbers, external scrubbers consume more power and board area and require additional design effort to implement [51].

3.1.1 Virtex-5 Bitstream Considerations

Table 3.1 shows the bitstream sizes for the Virtex-5FX70T and the Virtex-5FX130T, both of which are used in this work to estimate design resource use and power consumption. The Virtex-5 configuration bitstream is divided into configuration frames of 1,312 bits each (41 words of 32-bits each) [13]. Additionally, each configuration frame contains 12 built-in ECC bits (bits 640 to 651) and 16 unused bits (bits 656 to 671). Figure 3-1 shows the position of the 12 ECC bits and 16 unused bits in each configuration frame for the Virtex-5 family. For use in estimating design cross section and error rates, Table 3.2 shows the approximate number of configuration bits controlling the primary device components and hardware modules of the Virtex-5 family.

Table 3.1: Virtex-5 FX70T and FX130T configuration bitstream sizes [13]

Device	Configuration Bits
XC5VFX70T	27,025,408
XC5VFX130T	49,234,944

Any SEU-induced change to the ECC bits has no change on the active design. Although less obvious, invariably eight to 13% of the bits in the configuration memory are immune to SEU-induced alteration and can be subtracted from the total configuration size when calculating the device cross section [33]. Additionally, although routing control bits account for over 60% of the configuration bits, a typical user design only uses approximately 10 to 20% of the available routing resources [30].

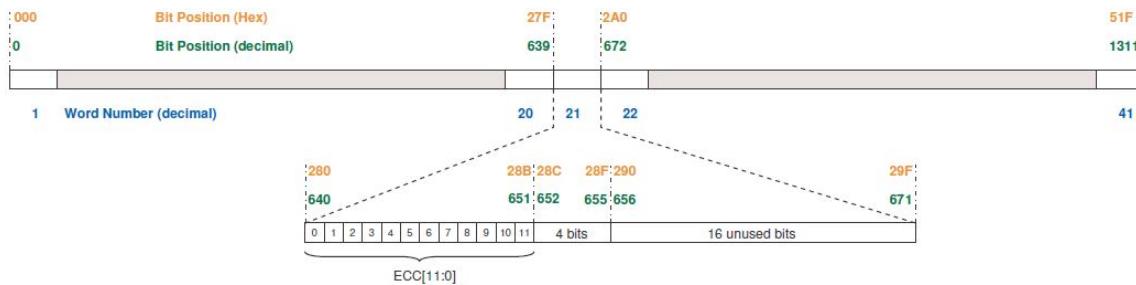


Figure 3-1: Position of ECC bits and unused bits in a single Virtex-5 configuration frame [32]

Table 3.2: Approximate number of configuration bits associated with most common Virtex-5 device features [33]

Device Feature	Appoximate Number of Configuration Bits
1 logic slice	1,181
1 BRAM (36 kbits)	1,170
1 BRAM (18 kbits)	585
1 I/O block	2657
1 DSP48E slice	4,592

Dynamic Reconfiguration Port Bits

Dynamic reconfiguration port (DRP) bits allow a user design to change certain conditions in hardware functional blocks (clock management tiles and gigabit transceivers) while the blocks are operational [13]. XRTC radiation testing has shown certain DRP bits appear as “stuck bits” to an external scrubber, or show readback differences an external configuration manager cannot correct through scrubbing [87]. The number of DRP bits in the Virtex-5QV FPGA per hardware module is:

1. DCM: 369 bits/instance (4,428 total in the device)
2. PLL: 496 bits/instance (2,976 total in the device)
3. GTX: 1,280 bits/GTX_DUAL tile (12,800 total in the device)

A total of 13,665 DRP bits exist in the Virtex-5QV FPGA. However, 13,665 is a conservative count because many DRP bits are unassigned memory cells that do not control any functionality. Thus, these unassigned bits may be subtracted from the total. [87]

3.1.2 External Scrubbing

In an external scrubbing scheme, the external scrubber is generally a space qualified FPGA (typically OTP), PLD, or ASIC. For example, commercially available Virtex-5 based processing boards use RadHard Actel FPGAs and older generation Xilinx Radiation-Tolerant FPGAs to provide configuration management and bitstream

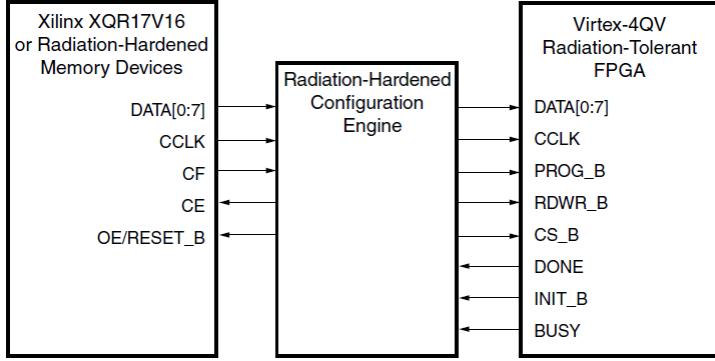


Figure 3-2: External configuration manager interface to non-volatile memory and SelectMAP interface to Virtex-4QV FPGA [31]

scrubbing [3] [19]. The XRTC test apparatus for Virtex-5QV radiation testing has employed both the Virtex II Pro and additional Virtex-5QVs as external configuration managers [87].

In the setup shown in Figure 3-2, the external configuration manager accesses the FPGA (a Virtex-4QV in this case) via the SelectMAP interface, which is the most efficient and comprehensive device access for configuration and mitigation [31]. The configuration manager has control of the data lines to the FPGA’s configuration, as well as capability to read the control signals that provide the configuration status of the FPGA.

Upon system power up, the configuration manager starts programming the FPGA as soon as the INIT pin is taken high or after the power on time (TPOR) requirement specified in the device data sheet. Once power up and configuration is successfully completed, the configuration manager enters the SEE mitigation process, which consists of SEFI checking and active partial reconfiguration. SEFI checking steps through frame address register (FAR), status register (STAT), and Control register (CTL) to verify the status and functionality of each register. Figure 3-3 provides a flow chart for external configuration management and bitstream scrubbing, and the reader may examine Carmichael and Tseng’s application note [31] for details on the SelectMAP command and data sequence for register test, register readback, and scrubbing.

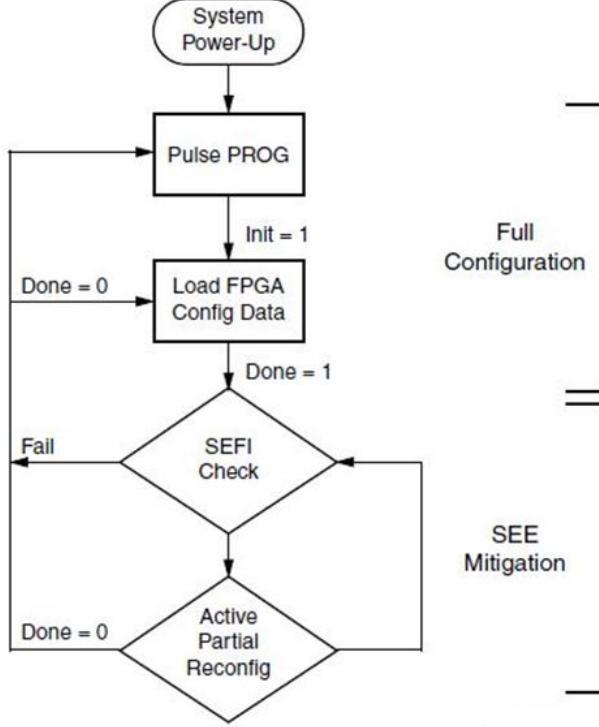


Figure 3-3: Flow chart for external configuration management and bitstream scrubbing [31]

Advantages of External Scrubbing

External scrubbing provides the opportunity to compare the active bitstream values to a golden copy of the bitstream stored in external non-volatile memory. Also, external scrubbers have the ability to correct any number of configuration errors because they are not constrained to relying on SECDED methods to detect and correct errors [24]. Additionally, external scrubbing provides the opportunity to deal with non-configuration bit upsets via use of a mask file [87], which can eliminate false positive configuration bit upset detection.

Disadvantages of External Scrubbing

The disadvantages of an external configuration manager and scrubber are increased cost, increased power consumption, increased board area, increased design complexity, and decreased design flow flexibility. In external scrubbing schemes, the configuration monitors are usually radiation hardened devices that are often OTP, meaning a design

error or a desired modification to the configuration management algorithm frequently results in an additional device burn or even an entire board re-spin, resulting in additional system cost and possible delay of design release/system implementation [30].

3.1.3 Internal Scrubbing

Internal bitstream monitoring and scrubbing techniques for the Virtex family of FPGAs typically use a combination of the Internal Configuration Access Port (ICAP), Frame ECC, and Readback CRC internal hardware modules (also known as user primitives). The ICAP and Frame ECC are available in the Virtex-II, Virtex-4, and Virtex-5 families, while the Readback CRC only is available in the Virtex-5 family. A brief description of each of the hardware modules appears below.

ICAP

The ICAP hardware module allows user designs to access configuration registers, readback configuration data, or partially reconfigure the FPGA after configuration is complete [13]. The interface of the ICAP resembles the interface used by the traditional SelectMap [50], with a selectable data width of 8-bits, 16-bits, or 32-bits [13].

Frame ECC

The Frame ECC logic is designed to detect single-bit and double-bit errors and in each configuration frame of the FPGA using the 12 ECC bits built into each frame as SECDED Hamming code parity values [13]. The Frame ECC module does not repair erroneous bits in a configuration frame; a user design is required to recognize errors in syndrome values and then correct altered bits [13].

Readback CRC

The Readback CRC module continuously scans (reads) the configuration cells of the device in the background while a user design is in operation. Initially, the readback CRC calculates a golden CRC value for each frame, to which

subsequent rounds of readback CRC values are compared. If the CRC value computed by a scan differs from the goldenCRC value, a change to the configuration has occurred [33], which the readback CRC indicates by driving the CRC error pin of the Frame ECC primitive high and driving the INIT_B pin low [13]. LUT-based memory storage, BRAM content, and Dynamic Reconfiguration Port memories are masked during background readback by the Readback CRC module [13].

Internal configuration bitstream scrubbing has been the subject of several university research efforts, as well as Xilinx development efforts. This section presents three internal configuration schemes: two provided by Xilinx, and one published by researchers at BYU. Finally, the advantages and disadvantages of internal scrubbing are presented and analyzed.

SelectMAP Internal Configuration Manager

As shown in Figure 3-4, designers can implement an internal configuration monitor using Master SelectMAP Mode. In this Xilinx-based design [30], the “self-hosting configuration management core” can perform bitstream readback, scrubbing, SEFI detection, and other specialized configuration management as required [29].

The external watchdog and oscillator shown in Figure 3-4 provide a fallback mechanism in the event of a configuration failure or SEFI. If the configuration management core detects a SEFI, it then asserts the SEFI signal to the watchdog so the watchdog will reset the FPGA. The configuration core periodically should pat the watchdog with a reset signal to reset the watchdog’s counter. If the configuration manager fails to assert the reset signal, then the watchdog should pulse the PROG pin on the FPGA to trigger a full reconfiguration of the FPGA. [29]

The two primary disadvantages to the internal SelectMAP scheme described above are the number of additional I/O pins required and the possibility of a radiation-induced error causing the internal configuration monitor to write erroneous values to the bitstream stored in the non-volatile memory array.

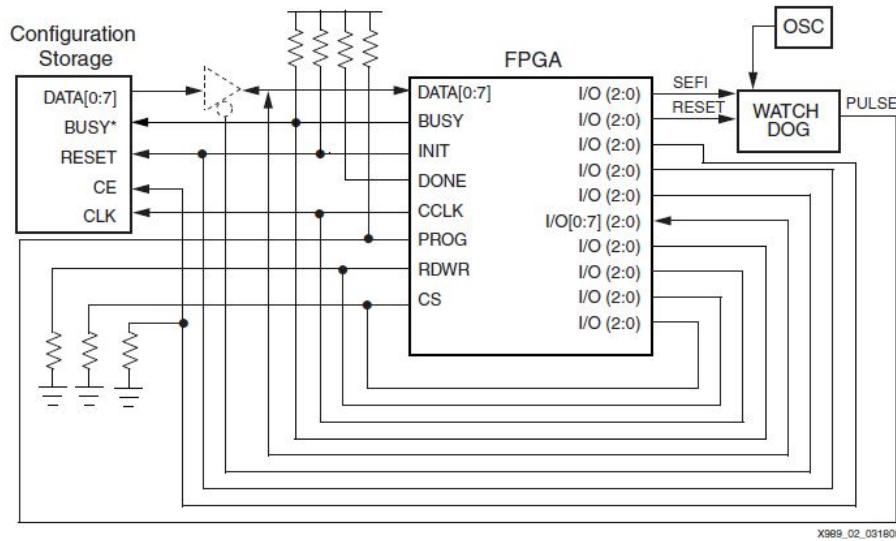


Figure 3-4: Block diagram of single FPGA in Master SelectMAP Mode implementing a triplicated configuration management scheme [30]

BYU Virtex-4 Internal Scrubber

Researchers at BYU developed an internal bitstream scrubber using the internal ICAP and Frame ECC hardware modules to implement SECDED [50], with process control implemented on a Xilinx PicoBlaze softcore microprocessor. Figure 3-5 shows a block diagram of the BYU internal scrubber system. Using instruction memory stored in BRAM, the PicoBlaze accesses the ICAP module to correct single-bit errors in the configuration memory. Since the internal scrubbing design is vulnerable to SEUs during operation, the BYU team added TMR and BRAM scrubbing to the design to increase its reliability, as shown in Figure 3-6.

Testing of the BYU design with the Avnet Virtex-4LX25 evaluation board at the Crocker Cyclotron demonstrated the triplicated scrubber achieved a fluence to failure 3.6 times larger than the unmitigated scrubber [50]. As one might expect, additional reliability and fault tolerance came at a price: the utilization numbers in Table 3.3 demonstrate how applying TMR to the design doubled the logic utilization and tripled the BRAM usage.

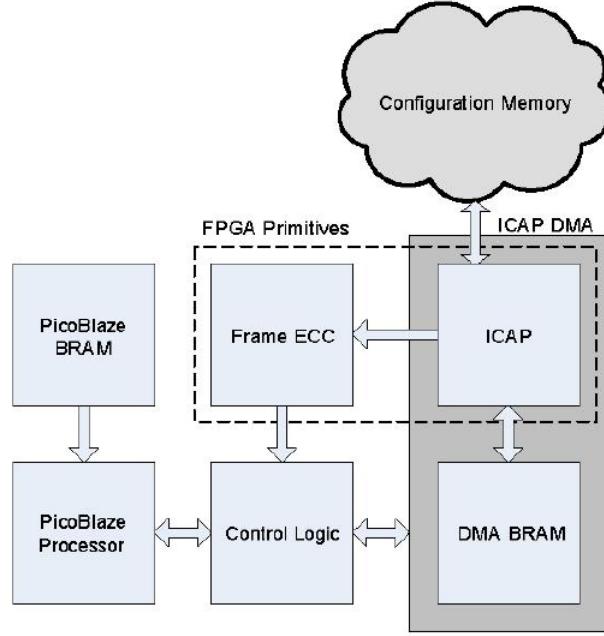


Figure 3-5: Block diagram of hardware modules and custom logic in BYU’s ICAP-based internal scrubber [50]

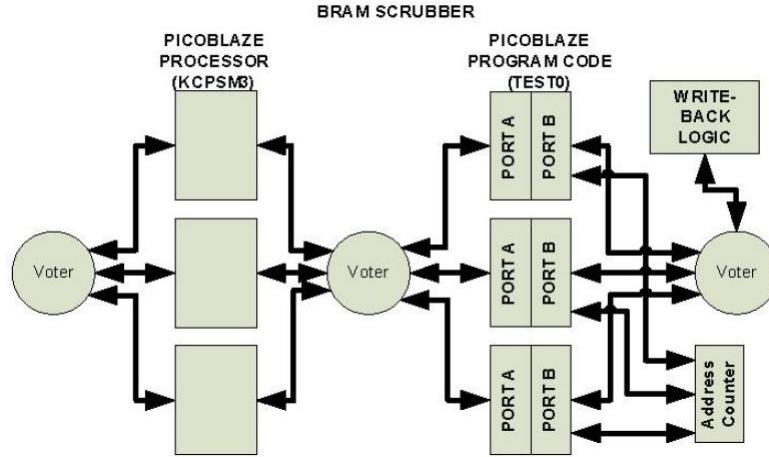


Figure 3-6: PicoBlaze processor BRAM memory protected with TMR and scrubbing [50]

Xilinx Virtex-5 Internal SEU Controller

In a similar fashion to the BYU Virtex-4 internal scrubber, the Xilinx Virtex-5 SEU Controller uses the ICAP and Frame ECC hardware modules within the Virtex-5 family along with a PicoBlaze processor to provide internal SECDED bitstream

Table 3.3: Resource Utilization for BYU internal scrubber, shown with and without TMR on the Virtex-4LX25 [50]

Resource	Non-TMR	TMR
Flip Flops	680 (3%)	1082 (5%)
Slices	736 (6%)	1308 (12%)
BRAM	2	6

scrubbing. The primary difference between the two designs is the use of the Virtex-5's built-in readback CRC hardware module in the SEU controller; the Virtex-4 family does not contain a readback CRC. When a frame containing an error is scanned, the SEU controller detects the resulting syndrome ECC error and triggers the correction procedure immediately [33].

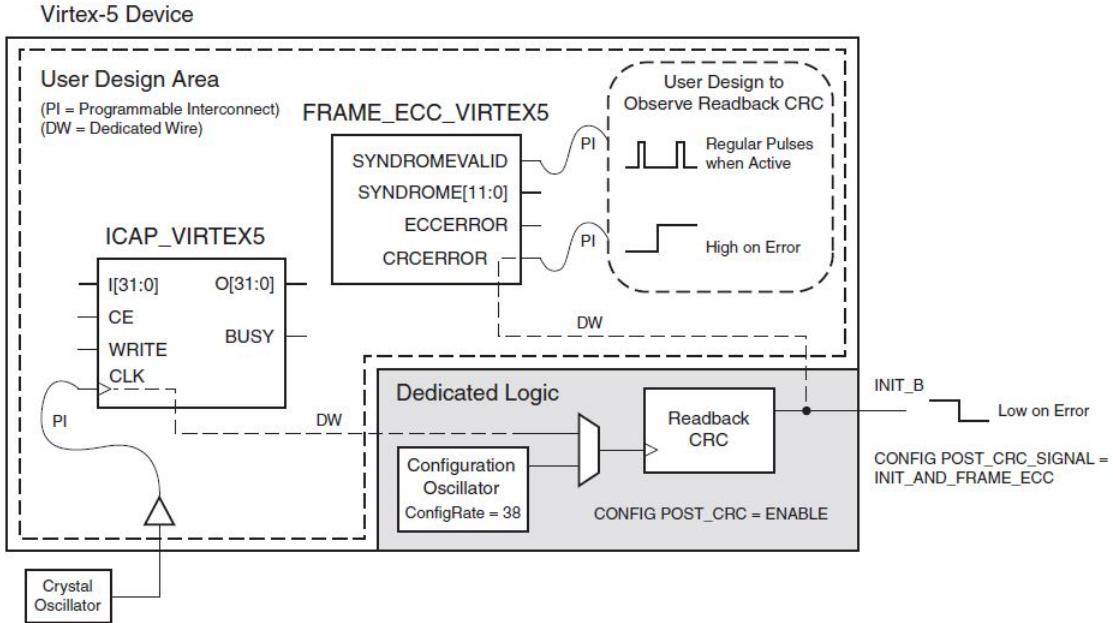


Figure 3-7: Readback CRC block diagram for internal scrubbing of FPGA bitstream [33]

Table 3.4 gives time required for each readback CRC scan of the Virtex-5 bitstream. The worst case time for the SEU controller to detect and repair a bitstream error is the time to complete a full scan. Following error correction, the effects the error had on operational states and data might continue and a localized reset to circuits might be appropriate [33].

For comparison to the other internal bitstream scrubbing designs, build results

Table 3.4: Readback CRC clock cycle and scan times for Virtex-5 SEU Controller [33]

Device	Clock Cycles per Readback CRC Scan	Readback CRC Scan Time at 60 MHz	Longest Readback CRC using ConfigRate = 38
XC5VFX70T	611,686	10.19	32.19
XC5VFX130T	1,100,816	18.35	57.94

for the SEU controller on the Virtex-5FX70T using the ML507 development board appear in Table 3.5, and power consumption estimates are shown in Table 3.6.

Table 3.5: Resource Utilization for Virtex-5 SEU Controller Macro on Virtex-5FX70T

Hardware Resource	Used	Available	Utilization
Slice Register	329	44800	1%
Slice LUT	343	44800	1%
Block RAM (18 kB)	1	148	1%
ICAP	1	2	50%

As with most internal scrubbing designs, one disadvantage of this approach is vulnerability of the scrubbing components themselves to SEU-induced configuration upsets and SETs. For example, the 12 internal ECC bits in a configuration frame themselves might also be flipped by an SEU. This would not cause a change to the user design, but could cause the SEU controller to incorrectly detect an error in the configuration bitstream and alter the bitstream. If higher reliability of the SEU controller is necessary, the BRAM storing the instruction memory of the PicoBlaze could be triplicated, as was done in the BYU ICAP-based scrubber design.

Table 3.6: Power consumption estimate for Xilinx Virtex-5 SEU controller implemented on Virtex-5FX70T

Parameter	Quiescent	Dynamic	Total
Supply Power (W)	1.057	0.055	1.112

Internal Configuration Scrubbing and Partial Reconfiguration

Since most published internal scrubbing schemes use an ICAP hardware module to access the configuration bitstream of the FPGA, concern exists when designing for partial reconfiguration in a system using internal scrubbing. Although each device in the Virtex-5 family contains two ICAP modules, only one may be active at any one time. Research has indicated partial reconfiguration and configuration bitstream scrubbing can be integrated into a single design [51].

Advantages of Internal Scrubbing

The advantages of an internal configuration monitor revolve around independence of an additional external device, which reduces cost, power, and board area. Additionally, an internal scrubbing scheme is free of the limited design flow typically associated with an external OTP configuration monitor. Since the scrubbing is implemented on a reconfigurable SRAM-based FPGA, internal configuration monitoring and scrubbing designs offer reduced hardware cost and more design flow flexibility at the cost of increased SEU cross section associated with increased use of internal hardware modules and supporting internal logic.

Disadvantages of Internal Scrubbing

Internal scrubbers are limited to either CRC-based or SECDED (dependence on syndrome length) error correction due to the lack of direct access to a golden configuration bitstream for comparing current bitstream values with intended bitstream values [24]. Another disadvantage is the vulnerability is the ICAP, frame ECC, and readback CRC hardware modules themselves, which are used to calculate the CRC or syndrome of each frame in the configuration memory. These modules are susceptible to radiation-induced errors.

3.1.4 SEFI Detection

After SEL, SEFIs represent the second most detrimental radiation induced effect in an SRAM-based FPGA (assuming SEB and SEGR do not occur). Therefore, a fault tolerant design should provide a mechanism for detecting and, if possible, correcting SEFI conditions. The most direct way to detect SEFIs in an SRAM-based FPGA is to monitor the FPGA's internal configuration registers [87]. In an external scheme, directly monitoring the DONE and INIT pins provides insight into the status of the configuration. In an internal configuration monitoring scheme, the user design could periodically read the configuration registers (via the ICAP hardware module) and check for incorrect values. If an incorrect configuration register value is detected, a variety of responses are possible, and designers should tailor a solution to the specific application and user design.

3.1.5 Configuration Scrubbing Summary

Table 3.7 presents a comparison of the advantages and disadvantages of internal scrubbing and external scrubbing schemes.

Table 3.7: Comparison of external and internal scrubbing schemes

Parameter	External Scrubber	Internal Scrubber
Error Detection	More Capable	Less Capable
Error Correction	More Capable	Less Capable
Design Flexibility	Lower	Higher
Design Complexity	Higher	Lower
Power Consumption	Higher	Lower
Cost	Higher	Lower

3.2 Hardware Modules for Redundancy

This section examines additional mitigation techniques and considerations for the non-RHBD special function hardware modules in the Virtex-5QV. With the exception of BRAM, XRTC upset rate estimates are low for the unhardened hardware modules

(see Tables 2.6 and 2.7); however, the error rates resulting from radiation testing do not predict error arrival times [73]. Therefore, designers should be aware of the additional mitigation techniques and consider applying them to better protect user designs in the space radiation environment.

3.2.1 Block RAM and FIFO

For designs requiring internal memory storage (most designs use a large proportion of available BRAM [33]), protecting user memory is essential for reliable design operation. Since BRAM cells switch quickly between states during operation, they are more susceptible to SEUs than configuration cells, which are required to remain static during most (if not all) of operation [33]. First In First Out (FIFO) storage elements also are implemented using Block RAM in the Virtex-5 family. Radiation testing of the Virtex-5QV has demonstrated the BRAM is the most vulnerable of the unhardened special function blocks within the Virtex-5QV, with an estimated 13 upsets/day due to radiation effects in a geostationary orbit (see Table 2.6) with error correcting code (ECC) functionality disabled. Enabling ECC significantly reduces the upset rate to 12 years/device (see Table 2.7). Although ECC is quite effective at protecting BRAM cells from SEUs, implementing it comes at a cost. As this section will quantify, enabling ECC constrains the maximum clock frequency at which a user design may operate.

Each of the Virtex-5QV's 298 BRAM blocks are configurable as 512 x 64-bit RAM with eight ECC bits for every 64-bit word. When ECC is enabled, the 8-bit parity checksum is used during every read operation to detect and correct single-bit errors, and to detect (but not correct) double-bit errors. During a write, the parity checksum is generated and stored. For every word read, the 72-bits are fed into an ECC decoder that generates status bits indicating: no error, single-bit error detected and corrected, or double-bit error detected [18]. The BRAM words are implemented with an interleaved bit separation scheme such that every bit in the word is in a separate BRAM block [44]. This interleaving decreases the likelihood of a multi-bit upset causing a double bit or larger error the SECDED ECC system cannot correct.

As shown in Table 3.8, taken from the Virtex-5QV DC Switching User Guide [11], 260 MHz is the maximum frequency at which a design may use BRAM in ECC mode. If the writeback mode of the ECC is enabled, the maximum frequency for BRAM further decreases to 180 MHz. Comparing the maximum frequencies available in the Virtex-5QV, using ECC with BRAM can half the maximum possible BRAM access frequency, which significantly reduces maximum design speed available.

Table 3.8: BRAM maximum operating frequencies for Virtex-5QV [11]

BRAM Use Case	Virtex-5QV Max Frequency(MHz)
Block RAM in all modes	360
Block RAM in Cascade mode	320
FIFO in all modes	360
Block RAM in ECC mode	260
Block RAM in ECC mode with writeback enabled	180

A small power increase results from adding ECC to BRAM in a user design; however, as shown in Table 3.9, the increase in power required to implement ECC on BRAM is not significant. Thus the power cost associated with implementing ECC on BRAM modules is likely acceptable in most systems. BRAM power consumption estimates in Table 3.9 were calculated for the Virtex-5FX70T at an ambient temperature of 25° Celsius using the Xilinx XPower Analyzer tool and include power consumption of the I/O blocks used for the address and data lines of the BRAMs.

Table 3.9: Resource utilization and estimated power consumption for BRAM with and without ECC

Number of BRAMs	BRAM Type	ECC	Power (W)
1	Single Port	None	1.012
2	Single Port	None	1.031
3	Single Port	None	1.048
1	Simple Dual Port	None	1.016
2	Simple Dual Port	None	1.035
3	Simple Dual Port	None	1.053
1	Simple Dual Port	ECC	1.022
2	Simple Dual Port	ECC	1.048
3	Simple Dual Port	ECC	1.065

MIG and MPMC

The Xilinx Memory Interface Generator (MIG) implements memory controllers for interfacing internal user logic to external memory devices (such as SDRAM) and typically employs BRAMs to pass data between the user design and the external memory component. The Multi-Port Memory Controller (MPMC) IP core uses MIG to implement memory interfaces between external memories and internal hardcore processors (PowerPC) and softcore processors (MicroBlaze) on the Virtex-5 [93]. The MIG uses standard Virtex-5 BRAMs, which are not radiation hardened but do include ECC options. Although data may not remain in the BRAMs used by the MIG for lengthy periods of time, subject to the use case of the design, the data still is vulnerable to upset while stored there. The cost of adding ECC to the MIG and MPMC BRAMs is additional FPGA resource utilization and increased power consumption.

Softcore Processor Memory in BRAM

For softcore processor applications, designers may choose to locate the instruction and data memory in internal BRAM, rather than solely in external electrically erasable programmable read only memory (EEPROM) and/or SRAM, or to employ BRAM instruction and data caches for externally stored memory. Several studies of softcore processors on FPGAs have demonstrated the significant performance speedups achievable by relying solely on BRAM for instruction/data memory storage or using BRAM for instruction/data caches, as compared to external instruction/data memory storage [35] [64]. Mitigation techniques for the unhardened BRAMs in the MicroBlaze softcore processor appear later in this chapter, along with the design trades associated with their use.

3.2.2 DCM and PLL Blocks

The possibility of SEU-induced clock signal failures poses significant risk to synchronous mission-critical embedded systems. The Digital Clock Manager (DCM) and

Phase Locked Loop (PLL) hardware modules that provide clock frequency synthesis (output frequency increase or decrease via multiplication of an input frequency) and de-skew are not RHBD in the Virtex-5QV. Thus the addition of mitigation techniques to the non-RadHard DCM/PLL blocks can become key to ensuring reliable clock signal generation for correct system functionality.

If, for example, a design employs a DCM to generate a multiplication or division of the input clock frequency, and a charged particle interaction induces a change in the configuration memory controlling the DCM, the effects could be severe. If the SEE causes the DCM to lower the output frequency from that which the design originally intended, then the design may under-perform. This under performance might result in decreased payload functionality and/or degraded communication rates with other systems onboard the spacecraft or with ground control. In the case of precision attitude control, a significant decrease in clock speed could cause a catastrophic failure in the system's ability to control the spacecraft's position and orientation. As another example, if the SEE causes the DCM to unintentionally increase its output frequency, the higher clock speed could result in the design no longer meeting timing constraints, which could produce a multitude of error and failures. From a payload perspective, if the clock frequency controlling the interface to the spacecraft bus/primary avionics is altered, it could result in inability of the payload to communicate with the spacecraft, thus eliminating any payload data production and the possibility of diagnosing the issues from the ground.

The Xilinx-recommended solution is to bring in the clock signal directly from an external clock source (such as an oscillator) to a clock buffer, without passing it through a DCM or PLL [33], as shown in Figure 3-8. This reduces the risk of relying on a DCM or PLL to produce the system clock for an entire user design. Including a DCM or PLL and interconnect logic in the clock path results in additional configuration bits being used in the design, which increases (by a small amount) the chance of SEU upset [32]. If system design requires on-chip clock multiplication in the form of DCM or PLL, then a PLL provides slightly higher reliability than a DCM because it requires fewer configuration bits than a DCM, which decreases its

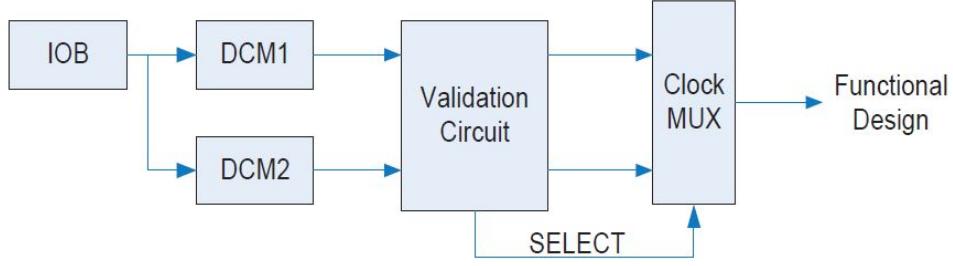


Figure 3-9: Mitigated design for DCM and/or PLL which adds redundancy into the clock network [42]

cross-section to SEUs [32].

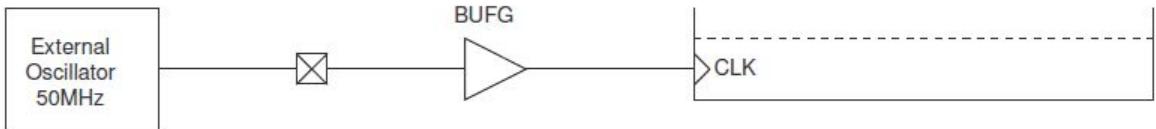


Figure 3-8: Direct connection of clock signal from external oscillator to logical block within user design [33]

Adding Redundant Clock modules

As listed in Chapter 2, the XRTC has produced radiation-induced upset estimates for the Virtex-5QV DCM and PLL modules in geosynchronous orbit. In radiation testing campaigns of the DCM and PLL blocks in 2011, the XRTC used a mitigated design to increase the area of the device under test (DUT) and evaluate a possible mitigation technique [42]. This mitigated design, shown in Figure 3-9, also could provide redundancy against SEU errors, at the cost of additional hardware utilization.

The arrangement shown in Figure 3-9 did not use triple modular redundancy during radiation testing. Instead, the validation circuit compared the output of the primary DCM (DCM1) to an expected value, and counted each clock cycle as valid if that value was correct. If the validation circuit determined the primary DCM's output was incorrect, it switched to the secondary DCM's (DCM2) output until the primary DCM recovered. Observed error signatures in the DCM and PLL blocks during radiation testing by the XRTC were altered frequency, clock glitches, or completely

Table 3.10: Logic and power consumption costs of multiple DCMs on Virtex-5FX70T, input clock of 100 MHz, output clock of 125 MHz

DCMs	Slices Used	Estimated Power Consumption (W)
1	1	1.101
2	2	1.207
3	3	1.312
4	4	1.422
5	5	1.517

Table 3.11: Logic and power consumption costs of multiple PLLs on the Virtex-5FX70T, input clock of 100 MHz, output clock of 133 MHz

PLLs	Slices Used	Estimated Power Consumption (W)
1	0	1.148
2	0	1.298
3	0	1.453
4	0	1.601
5	0	1.752
6	0	1.903

arrested functionality. Recovery from the arrested functionality error consisted of a reset to the Clock Management Tile and configuration bitstream scrub [42].

Using the design shown in Figure 3-9 as a baseline, a designer could add additional redundancy to the DCM/PLL system by adding a third DCM to the system. Table 3.10 provides an estimate of the logic resource and power consumption costs associated with adding additional DCMs to a Virtex-5 design. Power consumption estimates were calculated for the Virtex-5FX70T at 25° Celsius ambient temperature using the Xilinx XPower Analyzer tool.

The numbers presented in Table 3.10 are for reference because they were generated without any additional logic corresponding to a user design implemented on the FPGA. The build results indicate adding additional DCMs comes at the cost of about 1 logic slice and 100 mW per DCM, although adding redundant DCMs in an actual user design could involve more logic and power resources due to the specific requirements of the design.

Estimates for employing additional PLLs appear in Table 3.11, calculated for the Virtex-5FX70T. As with the DCM resource use estimates, the PLL resource estimates

are provided for reference; they do not include additional user logic that would appear in a design and use the output of the PLL(s) for operation. The build results indicate adding an additional PLL requires about 150 mW. It is important to note the PLL hardware modules in the Virtex-5 family are capable of providing more clock outputs than the DCMs, and the PLLs are separated by physical location either on the top or bottom of the Virtex-5 device. PLLs on the top half of the device are driven only by global clock pins in I/O Bank 3, while PLLs on the bottom half of the device are driven only by global clock pins in I/O Bank 4 [18].

Monitoring Clock Module Errors

A simpler option for adding fault tolerance to system design with PLL and/or DCM modules is to provide a method of monitoring the clock module output(s) for errors. An error monitoring logic design might detect DCM/PLL output errors and signal a controlling logic element, which could then reset the malfunctioning clock module. A block diagram for such an error monitoring scheme appears in Figure 3-10. The primary clock signal to the error monitor would be the base clock frequency passed through from an external oscillator, while the other input would be the adjusted (multiplied up or down) output frequency of the DCM/PLL. The "output error" signal from the error monitor would connect to a controlling logic unit, which might be a softcore processor. These connections would allow the controller unit to reset the clock module and clear any error conditions if the error monitor detects an error in the clock module output.

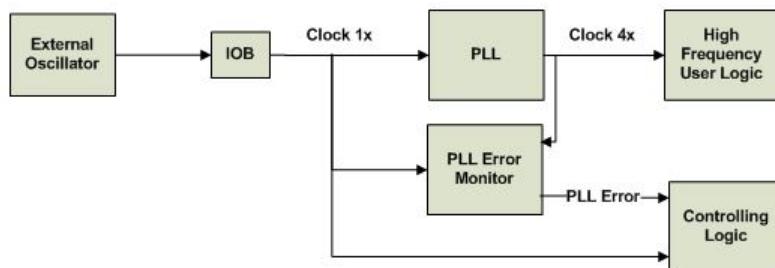


Figure 3-10: PLL error detection scheme

A designer could apply error monitoring functionality to a DCM/PLL-generated clock signal feeding a non-critical component of the user logic such as an image processing block. This would allow the controlling logic module to operate from the more reliable base clock frequency and reset both the DCM/PLL and the non-critical user logic component if an error occurs.

3.2.3 Digital Signal Processor Blocks

The DSP blocks in the Virtex-5 family are intended to perform high speed mathematical operations and are optimized for such operations. DSPs may operate at frequencies up to 550 MHz [78] in the Virtex-5 family. On the Virtex-5QV, the DSP blocks are not hardened against radiation-induced errors.

XRTC SEU effects testing on the DSP48E blocks in the Virtex-5QV took place in 2009 at the Texas A&M Cyclotron and in 2009 at the Lawrence-Berkeley Cyclotron [78]. Figure 3-11 shows the approximate locations on the Virtex-5QV die of the DSP blocks tested.

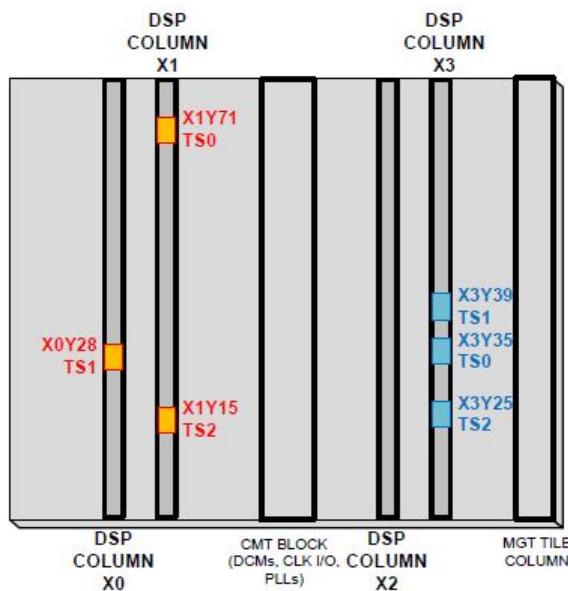


Figure 3-11: Virtex-5QV die diagram showing approximate locations of DSP48E blocks used in XRTC testing [78]

Analysis of the test results of the Virtex-5QV's DSP48E blocks predicts a mean

time to upset (MTTU) per DSP block as low as 15 years/upset for multiplication operations, 17.5 years/upset for add/subtract operations, and 72.5 years/upset for accumulate operations, at the tested clock frequencies of 25.0 MHz, 12.5 MHz, and 6.25 MHz [78]. When the test results are extrapolated to operation using a 450 MHz clock, the MTTU decreases to five years per DSP in a geosynchronous orbit(see Table 2.7). Given the low frequency of upset occurrence, the overall response may be considered acceptable for many missions, especially since DSPs are usually employed as high through-put structures [78], meaning a temporary error in the output of a DSP block likely only would impact the particular calculation at the time and not result in high impact system faults or failures.

Although most applications may tolerate occasional DSP output errors, other applications may have more stringent reliability requirements. Unlike ECC on BRAM, no default error mitigation techniques are built into the DSP blocks of the Virtex-5 family. If a design requires a DSP to meet processing requirements, a designer might apply a TMR-like approach using multiple DSPs to perform the same calculations, with a voter to ensure the majority output is passed on to the next circuit element. Such a scheme appears in Figure 3-12.

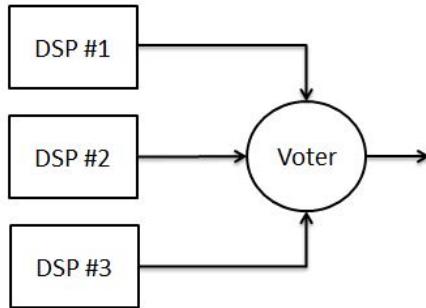


Figure 3-12: DSP triplication for additional fault tolerance

As Table 3.12 indicates, the cost of adding additional DSPs to a design can be quite small, and the Virtex-5QV contains 320 DSP hardware modules [95]. The results listed in Table 3.12 were generated for the Virtex-5FX70T at an ambient temperature of 25° Celsius using Xilinx XPower Analyzer, with each DSP configured as a 17-bit x 17-bit unsigned multiplier, with a 35-bit output and 100 MHz input clock. Indeed,

triplicating each DSP in a design and adding a voter circuit to arbitrate the outputs of all three DSPs could be feasible without incurring a significant power consumption increase. However, as with all reliability methods involving hardware redundancy, the designer should weigh the increased cross sectional area resulting from adding additional DSPs and arbitration circuitry.

Table 3.12: Logic and power consumption costs of multiple DSP blocks on Virtex-5FX70T

DSPs	Slices LUTs	Estimated Power Consumption (W)
1	8	0.997
2	12	1.001
3	18	1.002

3.2.4 Other Hardware Modules

The other special function hardware modules in the Virtex-5QV (as well as the Virtex-5 family) are the Mutli-Gigabit Transceivers (MGTs), Peripheral Component Interconnect Express (PCIe), and Ethernet Media Access Control (MAC) blocks. XRTC testing of the MGT blocks predicts error rates as low as 20 years per transceiver (see Table 2.7) and the communication channel's resynchronization protocol can correct most errors resulting from SEUs [67]. The XRTC has not performed (or has not yet released the results) radiation testing on the PCIe and Ethernet MAC hardware modules. Thus, this work considers additional fault tolerance on the MGT, PCIe, and Ethernet MAC blocks only minimally.

Mutli-Gigabit Transceivers (MGTs)

The MGT blocks implemented in the Virtex-5 FPGA family are used to transmit high rate serial data to and from the FPGA, as depicted in Figure 3-13. On the Virtex-5QV, the MGT blocks are unhardened and are equivalent to the commercial MGT blocks in the rest of the Virtex-5 family, making them vulnerable to SEU-induced data loss and bandwidth reduction.

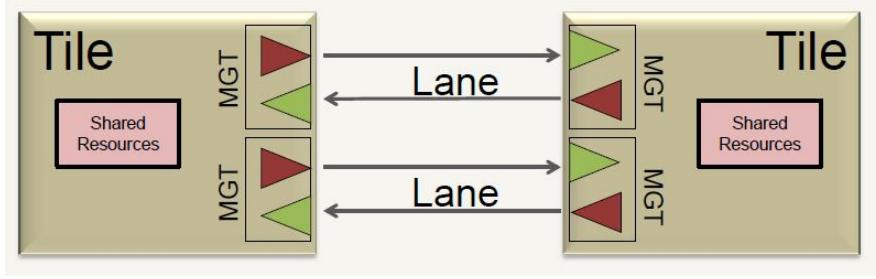


Figure 3-13: Block diagram of MGT implementation between two FPGAs [59]

To protect the functionality and reliability of high speed data transfer using the MGT blocks, a designer may implement a protocol on top of the basic MGT functionality. One example is Xilinx's Aurora protocol, on which XRTC members have performed radiation tests to determine its effectiveness at mitigating SEU-induced errors [59]. Aurora is available as an IP Core and only requires approximately 500 logic slices for implementation in the FPGA fabric [59].

As shown previously (see Table 2.7), XRTC estimated error rates are 20 years per GTX in radiation testing of the unhardened MGT blocks in the Virtex-5QV. Radiation testing of the MGT blocks on the Virtex-5QV using the Aurora protocol determined the Aurora protocol can recover from 97% of SEU induced errors. Manual recovery was required for 2.5% of SEU events and 0.12% of SEU induced errors required reconfiguration of the device under test [59]. Thus, in a space-based system utilizing the MGT blocks within the Virtex-5QV, addition of the Aurora protocol can protect the unhardened MGT blocks from most SEE-induced errors.

PCIe and Ethernet MAC Blocks

The XRTC has yet to complete testing on the PCIe hardware blocks or the EMAC hardware blocks of the Virtex-5QV. This thesis does not present fault tolerance techniques for the PCIe or Ethernet MAC blocks in the Virtex-5QV.

3.3 Softcore Processor Trades

Softcore processors implemented on FPGAs offer space system designers many benefits as compared to RadHard hardcore processors such as the BAE RAD750. Reconfigurability is a primary benefit of softcore processors since operators can change their characteristics on-orbit. Additionally, softcore processors allow designers to study trades in internal resource utilization and architectures affecting system performance, reliability, power consumption, and cost. Softcore processors also can offer decreased system development time as well as flexibility to address changing design requirements during the development process.

This work analyzes implementation with the Xilinx MicroBlaze softcore processor on the Virtex-5FX70T and Virtex-5FX130T. Studies of the Leon and MicroBlaze reconfigurable softcore processors implemented on the commercial grade Virtex-4 and Virtex-5 at Sandia National Laboratories have shown both perform similarly when using caches [35] [64]. This section first briefly describes the MicroBlaze fault tolerant hardware and software features provided by Xilinx and then quantifies the resource and performance costs of implementing the features in a MicroBlaze processor system. All Virtex-5 design build results presented were generated using Xilinx Platform Studio (XPS) version 13.4.

3.3.1 MicroBlaze System Architecture

The MicroBlaze is a 32-bit reduced instruction set computer (RISC), implemented in the Harvard architecture, and optimized for implementation in Xilinx FPGAs. Xilinx provides MicroBlaze as an Intellectual Property (IP) core in its Embedded Processor Development Kit (EDK). The MicroBlaze is highly configurable, supporting a wide array of optional features and interfaces to external peripherals as well as allowing the designer to choose a three stage pipeline for area optimization or a five stage pipeline for performance optimization. [96]

RadHard CLBs are the building blocks of the MicroBlaze in the Virtex-5QV, but the BRAM modules used as either primary instruction/data memory storage or in-

struction/data memory caches remain unhardened and the most vulnerable hardware module in the Virtex-5QV. Thus the facet of MicroBlaze architecture of primary interest to this work is the memory subsystem. A BRAM memory subsystem for the MicroBlaze is comprised of the Local Memory Bus (LMB), LMB interface controller, and the BRAM peripheral [92] as shown in Figure 3-14. The Local Memory Bus(LMB) is a synchronous bus primarily used to access internal BRAM [94], and the LMB BRAM Interface Controller provides the interface between the LMB and the BRAM peripheral unit(s) [92].

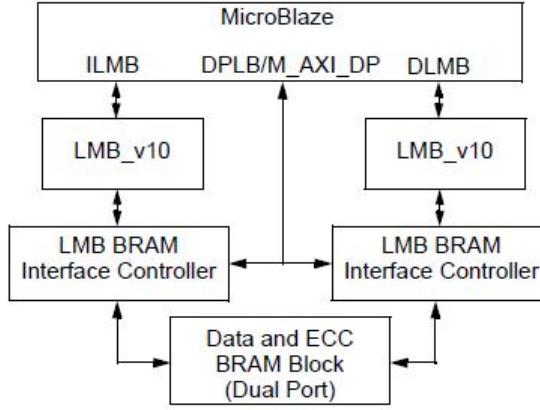


Figure 3-14: MicroBlaze system with LMB and ECC on LMB controllers [92]

3.3.2 Fault Tolerance Use Cases

To mitigate the effect of SEUs in BRAM storing instruction and data memory, a designer can configure the LMB BRAM Controller to use ECC functionality. The controller generates ECC bits ((32,7) Hamming code) and stores them with data whenever the user program writes data to memory. When reading from BRAM, the controller uses the ECC bits to correct all single bit errors in the data it passes to the MicroBlaze and detect all double bit errors in the data read. The controller does not automatically correct the erroneous memory bits stored in BRAM [34]. If the controller detects any errors, it signals MicroBlaze via either the PLB, an interrupt signal through an interrupt controller IP core, or throwing an exception, depending on the fault tolerance use case selected. The reader may view Table 1 of the LMB

BRAM datasheet [92] for the coding definition of the (32,7) Hamming code.

The Xilinx EDK provides four different fault tolerance use cases: minimal, small, typical, and full. A brief description of each use case follows below:

Minimal

In the minimal fault tolerance use case, the ECC logic corrects single bit errors in data words before the LMB interface controller passes them to the MicroBlaze. When the ECC logic detects an uncorrectable error in a data word, it sets an error signal, which generates an exception in the MicroBlaze system. The minimal system is suitable when area constraints are high and/or no need exists for testing of the ECC function or analyzing the error frequency and location. [96]

Small

The small fault tolerance use case is a minimal system with a register added to record the number of single bit errors (correctable errors). Thus, the small system provides the capability to monitor error frequency but no capability for testing of the ECC function. [96]

Typical

The typical fault tolerance use case provides the capabilities to monitor error frequency and generate an interrupt to immediately correct a single bit error through user software. It is a small system with a status register and a first failing address register added. A single bit error latches the address for the access into the first failing address register and then generates an interrupt triggering the MicroBlaze to read the failing address and then perform a read followed by a write on the failing address. The read-read-write sequence will remove the single bit error from the BRAM. The typical use case does not provide support for testing of the ECC function. [96]

Full

The full fault tolerance use case employs all of the features provided by the LMB

BRAM Interface Controller, including enabling full error injection capability, error monitoring, and interrupt generation. It is a typical system with fault injection registers and first uncorrectable error address registers added. [96]

3.3.3 Fault Tolerance Implementation Cost and Overhead

BRAM ECC Overhead

Including seven Hamming code bits used by the ECC logic of the LMB interface controllers for each data word in memory increases the BRAM use for a user design. The percentage increase in required BRAM size varies by FPGA family, as shown in Table 3.13.

Table 3.13: BRAM Overhead for implementing ECC [92]

BRAM Data Size	Virtex-4 Family	Virtex-5 Family
2 kBytes	100%	N/A
4 kBytes	50%	100%
8 kBytes	25%	50%
16 kBytes and larger	25%	25%

Resource Utilization

To quantify the effects of applying fault tolerance use cases to a MicroBlaze system, Table 3.14 shows the resource utilization increase associated with implementing the four levels of fault tolerance in a basic MicroBlaze design. The resources are based on an XPS MicroBlaze project with 32 kB BRAM instruction/data memory system, Universal Asynchronous Receive Transmit (UART), MicroBlaze Debug Module (MDM), and Processor System Reset Module (PSRM) IP core peripherals connected to the MicroBlaze through the Processor Local Bus (PLB), clocked at 100 MHz with a Clock Manager peripheral (DCM), as shown in Figure 3-15. The full use case implementation requires a 66 % increase in logic utilization as compared to the standard MicroBlaze utilization. No interrupt controller or exception handling capability was added to the typical and full fault tolerance use cases project builds in order to

provide a baseline for additional hardware modules necessary for fault tolerance.

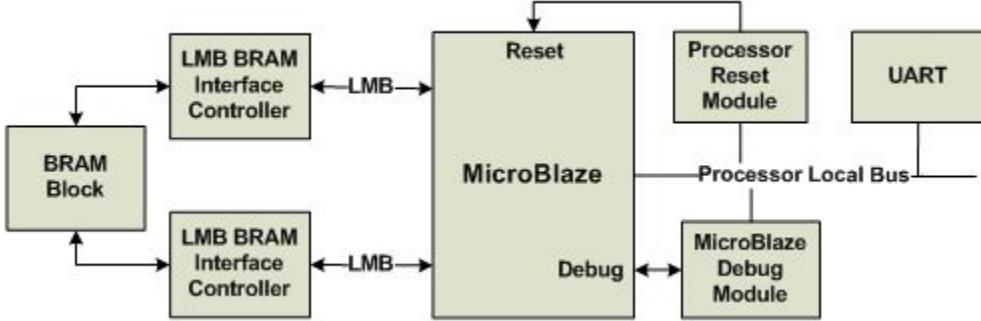


Figure 3-15: MicroBlaze system used to measure resource use of fault tolerance use cases

Table 3.14: Resource utilization for MicroBlaze fault tolerance use cases

Resource	Fault Tolerance Use Case				
	None	Minimal	Small	Typical	Full
Slice Registers	1528(1.00x)	1884(1.23x)	1884(1.23x)	2251(1.47x)	2539(1.66x)
Slice LUTs	1823(1.00x)	2198(1.21x)	2198(1.21x)	2539(1.39x)	2946(1.62x)
BRAMs	8(1.00x)	10(1.25x)	10(1.25x)	10(1.25x)	10(1.25x)
DSPs	3(1.00x)	3(1.00x)	3(1.00x)	3(1.00x)	3(1.00x)

As with most fault tolerance techniques, there ain't no such thing as a free lunch (TANSTAAFL): implementing fault tolerance via ECC in the MicroBlaze BRAM controllers constrains the design space. Table 3.15 shows timing closure status for the same basic MicroBlaze system built with different instruction/data BRAM sizes and system clock speeds. At the maximum selectable system clock frequency available in XPS for the MicroBlaze system of 125 MHz, no successful timing closure is possible for any BRAM equal to or above 32 kBytes in size. In Table 3.15, “Pass” indicates a successful timing closure for the design, while “Fail” indicates failure to meet timing constraints for the design.

The results shown in Table 3.15 illustrate a primary consideration designers should take into account when designing with a softcore processor on an SRAM-based FPGA: incorporating fault tolerance features limits the maximum frequency at which, and the internal instruction/data memory space with which, a user design may operate.

Table 3.15: Timing closure results for various instruction/data memory BRAM sizes with fault tolerance enabled and processor system clock frequencies

		Block RAM Size (kBytes)			
		32	64	128	256
Processor Clock Speed (MHz)	50	Pass	Pass	Pass	Pass
	75	Pass	Pass	Pass	Fail
	100	Pass	Pass	Fail	Fail
	125	Fail	Fail	Fail	Fail

Execution Time Costs with Fault Tolerance

Normally, the Xilinx Data2MEM software program initializes the ECC bits in the configuration bitstream before loading onto the FPGA. However, user software can also initialize the ECC bits by reading and writing back the whole contents of the BRAM data while ECC checking is suppressed and then enabling it by writing a '1' to the ECC On/Off Register. [96]

While imposing a timing constraint on system design, implementing fault tolerance on the MicroBlaze BRAM memory system also incurs some costs in program execution times. Table 3.16 below shows the results of running the Drystone program on non-fault tolerant (minimal) MicroBlaze and fault tolerant MicroBlaze builds.

Table 3.16: Execution times of 500 Dhystone loops on MicroBlaze processor with and without fault tolerance (ECC) enabled on BRAM instruction and data memory

Clock Speed (MHz)	No Fault Tolerance Execution Time (ms)	Fault Tolerance Execution Time (ms)	% Slow Down
50	13.251	13.631	2.87
75	8.834	9.087	2.86
100	6.625	6.815	2.87
125	10.600	N/A	N/A

The fault tolerant execution slow down is not large, but designers must consider it when calculating algorithm execution time on fault tolerant MicroBlaze systems,

especially if the program is pushing the limit of the MicroBlaze’s throughput at a given operating frequency. Execution time for a clock speed of 125 MHz with fault tolerance enabled was not measured because successful timing closure with any fault tolerance use case was not achieved at 125 MHz.

3.3.4 Software Scrubbing

To ensure bit errors do not accumulate in BRAMs, Xilinx recommends periodic memory scrubbing. The Xilinx standalone Board Support Package (BSP) provides the function `microblaze_scrub()` to perform scrubbing of the entire LMB BRAM and all MicroBlaze internal BRAMs used in a particular configuration. This function is intended to be called periodically from a timer interrupt routine. During a scrub, software cyclically reads and writes all addresses, thus correcting any single bit errors in memory at each address. [96]

Calculating Scrubbing Rate

Xilinx provides an approximate equation for determining the frequency at which the `microblaze_scrub()` function should be called to scrub memory, as shown in Equation 3.1[96].

$$P_W = 760 \left(\frac{BER^2}{SR^2} \right) \quad (3.1)$$

where P_W is the probability of an uncorrectable error occurring in a memory word, BER is the soft error rate for a single BRAM memory bit, and SR is the scrubbing rate [96].

3.3.5 Processor Watchdog

To provide a fallback mechanism in case the softcore processor hangs during operation, the designer may add a watchdog timer module to the processor system. Xilinx provides such a hardware IP core in the form of a 32-bit peripheral providing a 32-bit free-running timebase and watchdog timer (WDT) [91]. This watchdog timer IP core

is distinct from the Virtex-5 configuration watchdog timer hardware module, which restarts the FPGA configuration process in the event of configuration failure [13].

The Xilinx WDT peripheral uses a dual-expiration architecture, as depicted in Figure 3-16. After one expiration of the timeout interval, the WDT generates an interrupt to an interrupt controller module and sets the WDT state bit to ‘1’ in the status register. If user software does not clear the state bit before the next expiration of the timeout interval, the WDT triggers a processor system reset. The WDT peripheral also has a single bit in its control register to indicate whether or not a watchdog reset signal was asserted. A system reset does not clear this bit, enabling user software to read it after a processor system reset and determine if a WDT timeout caused the reset. The user software can then write a ‘1’ to the WDT state bit to clear the reset status. User software only can disable the WDT by writing to two distinct addresses, reducing the possibility of inadvertently disabling the WDT in the application code. [91]

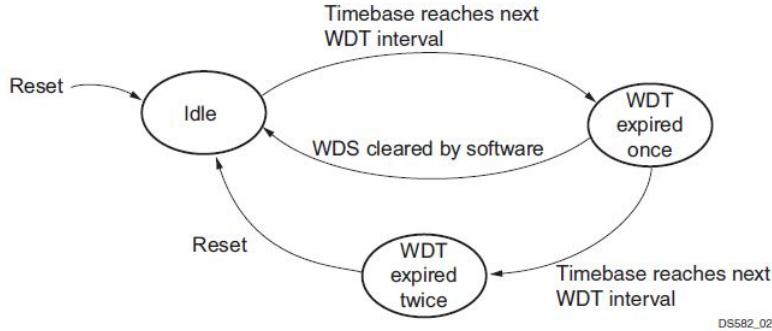


Figure 3-16: Processor system watchdog timer state transition diagram [91]

A general strategy for applying the processor system WDT to a space-based embedded system would design user software to read the reset status bit of the watchdog timer after each reset of the processor system. Following the read, software may generate a telemetry packet including the status of the reset bit, which is useful for ground debugging purposes and tracking radiation effects.

Adding a WDT IP core to a MicroBlaze system requires connecting its reset output to the PSRM IP core, as shown in Figure 3-17. To utilize the interrupts the WDT offers, an interrupt controller is added to the system. Table 3.17 provides

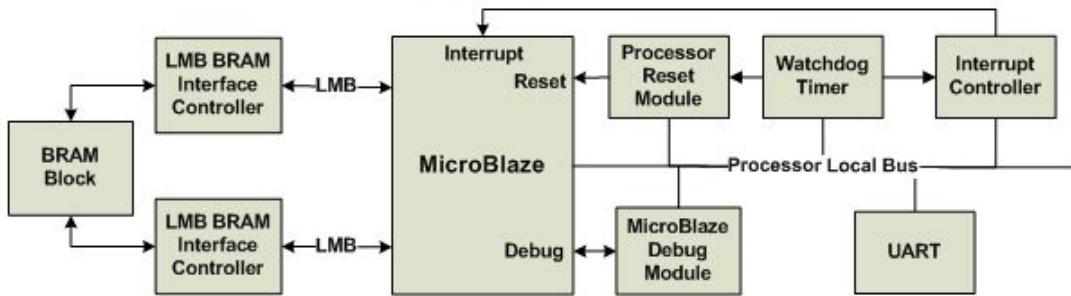


Figure 3-17: MicroBlaze system used to measure resource use of watchdog timer

measurements of the resource and power utilization for different MicroBlaze system build and fault tolerance options when including WDT and Interrupt Controller IP cores. The results in Table 3.17 indicate the addition of a WDT with Interrupt Controller costs few flip flops and LUTs and results in a nearly insignificant increase in estimated power consumption.

Table 3.17: Resource utilization comparison for MicroBlaze with and without watchdog timer and interrupt controller

Resource	Fault Tolerance Use Case			
	None	None	None	Minimal
WDT Present	No	Yes	Yes	Yes
Interrupt Controller Present	No	No	Yes	Yes
Slice Registers	1528(1.00x)	1714(1.12x)	1824(1.19x)	2182(1.43)
Slice LUTs	1822(1.00x)	1974(1.08x)	2115(1.16x)	2513(1.38)
BRAMs	8(1.00x)	8(1.00x)	8(1.00x)	10(1.25x)
DSPs	3(1.00x)	3(1.00x)	3(1.00x)	3(1.00x)
Total Power (W) ¹	1.622(1.00x)	1.631(1.01)	1.623(1.00)	1.645(1.01)

3.3.6 Multiple MicroBlaze

An additional fault tolerant scheme offered by the versatility and size of SRAM-based FPGAs is the implementation of multiple softcore processors in a single user design. Table 3.18 shows resource utilizations for multiple MicroBlaze processors (without

¹Power estimated with ambient temperature of 50° Celsius

any fault tolerance) built in single design. The area cost increases by a factor of approximately 1 for each processor added to the user design. The estimated power consumption, however, scales by significantly less than a factor of 1 for each processor added. Table 3.19 shows the additional resource utilization of adding fault tolerance to the BRAM controllers of the multiple MicroBlaze systems.

Table 3.18: Resource utilization comparison for implementing multiple MicroBlaze processors in a single design

Resource	Number of MicroBlazes			
	1	2	3	4
Slice Registers	1528(1.00x)	2903(1.90x)	4238(2.77x)	5573(3.65x)
Slice LUTs	1823(1.00x)	3501(1.92x)	5049(2.77x)	6596(3.62x)
Power Consumption (W)	1.175(1.00x)	1.219(1.04x)	1.267(1.08x)	1.322(1.13x)

Table 3.19: Resource utilization comparison for implementing multiple MicroBlaze processors with Minimal fault tolerance in a single design

Resource	Number of MicroBlazes			
	1	2	3	4
Slice Registers	1884(1.00x)	3573(1.90x)	5304(2.82x)	6993(3.71x)
Slice LUTs	2198(1.00x)	4120(1.87x)	6173(2.81x)	8093(3.68x)
Power Consumption (W)	1.195(1.00x)	1.265(1.06x)	1.316(1.10x)	1.376(1.15x)

Given the the power consumption increase is small for each added MicroBlaze, designing a system with multiple MicroBlazes could prove an attractive option for robustness and redundancy against radiation-induced errors [60]. Such a system design would allow designers to experiment with a synthesis of hardware and software fault tolerance techniques to achieve higher reliability [65].

3.4 Summary and Recommendations

As analyzed and presented in this chapter, space-based system design with RHBD SRAM-based FPGAs strongly suggests additional design considerations and techniques that are not required for the significant majority of terrestrial designs. These

considerations include actively monitoring and correcting configuration memory, protecting user memory with fault tolerant techniques, and adding redundant modules for non-RadHard modules within the FPGA. Although these additional techniques and considerations constrain the design space for systems on SRAM-based FPGAs, considering their implementation is key to designing high reliability embedded systems for space applications.

For configuration bitstream management and scrubbing, this work recommends implementation of bitstream scrubbing and SEFI detection, whether in an external or internal scrubbing scheme. A system designer must weigh the advantages and disadvantages of each scheme against the required reliability of the FPGA-based system and the available system resources. If sufficient power, budget, board area, and design time are available and the criticality of the system is high, an external configuration manager will provide more functionality for SEU detection and correction and higher fidelity SEFI monitoring and correction. If the design space is constrained and/or the system functionality is less critical, internal scrubbing may be employed to reduce design complexity, power consumption, and board space, while sacrificing error detection and correction capability.

The recommendations of this work for BRAM use in a design are to include ECC on each BRAM in the system. Additionally, if the correctness of the data is crucial, triplication of each BRAM block along with memory scrubbing should be implemented. The designer must then factor in the decrease in maximum BRAM frequency and increase in area and power cost associated with increased reliability.

For designs requiring clock frequencies in addition to those provided by external oscillators, which PLLs and DCMs are typically used to generate, this work recommends adding an error monitoring unit to each DCM and PLL or adding redundant PLLs and DCMs to support each DCM and PLL used in a design. If the output of the clock module must remain constantly accurate, then designers should add redundant clock modules. If, however, the system can tolerate a reset of the clock module and affected user logic when errors occur in the clock module (e.g. in typical image processing applications), then an error monitoring scheme may suffice. The

designer must factor in the additional power consumption increase associated with adding DCMs and PLLs, as well as the location constraints of the DCM and PLL blocks on the FPGA die.

For designs using a MicroBlaze softcore processor, this work recommends applying a fault tolerance use case to the BRAM instruction/data memory system, along with a processor WDT peripheral. A designer should enable either typical or full fault tolerant use case and include interrupt controller to facilitate rapid correction of single bit errors once the LMB BRAM controller detects them. The cost of MicroBlaze fault tolerance use case implementation is constrained processor system clock speed and decreased execution time, along with increased flip flop and LUT use in the FPGA logic structure. Designers must be aware of these limitations and scope the processing requirements of a MicroBlaze system accordingly.

Chapter 4

Implementation of Additional Fault Tolerance on REXIS Instrument

This chapter presents the hardware and software design of the REXIS avionics system based around a Virtex-5 FPGA, along with the application of several of the fault tolerant design techniques presented in the previous chapter to the REXIS avionics system.

4.1 REXIS

The REgolith X-ray Imaging Spectrometer (REXIS) is a student payload on board NASA’s Origins-Spectral Interpretation-Resource Identification-Security-Regolith Explorer (OSIRIS-REx) asteroid sample return mission, scheduled for launch in September of 2016. The REXIS project is a collaboration between the MIT Space Systems Laboratory, the MIT Kavli Institute for Astrophysics and Space Research, and the Harvard College Observatory. A CAD rendering of the REXIS instrument appears in Figure 4-2.

4.1.1 OSIRIS-REx

The OSIRIS-REx asteroid sample return mission is the third planetary science mission selected as part of NASA’s New Frontiers Program. The mission is planned to launch in September 2016 and encounter the asteroid Bennu (formerly 1999 RQ36) in October 2018. Using a variety of imaging payloads, OSIRIS-REx will study Bennu for up to 505 days in order to globally map the asteroid’s surface from a distance of five kilometers to a distance of 0.7 kilometers. The primary science goal is to obtain at least 60 grams of pristine regolith and a surface material sample. Following collection, the sample will return to Earth in September 2023 in a Stardust-heritage sample return capsule. The samples will be delivered to the NASA Johnson Space Center (JSC) curation facility for analysis and world-wide distribution. [2]

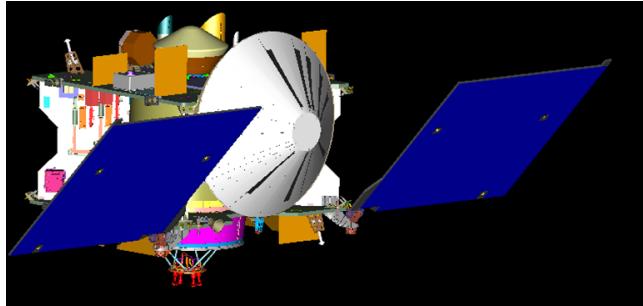


Figure 4-1: CAD rendering of OSIRIS-REx spacecraft in the nominal observing and communication configuration

4.1.2 REXIS Science Mission

REXIS is an x-ray spectrometer designed to use a 2x2 array of charged-coupled devices (CCDs, totaling four megapixels) to characterize the surface of the Bennu asteroid both globally and spatially. The CCD-based coded aperture telescope performs remote X-ray Fluorescence (XRF) spectrometry in the soft x-ray band (0.3 keV - 7.5 keV). Elements on the surface of the asteroid absorb x-rays emitted from the sun and then re-emit, or fluoresce, the x-rays at specific energy levels corresponding to the element type. The re-emitted x-rays pass through the coded aperture mask of REXIS and strike the CCDs, from which a combination of analog and digital electron-

ics measure the charge of each x-ray event. Additionally, REXIS supports a X-ray Monitor (SXM) subsystem to monitor solar activity during instrument observation of the asteroid, which provides context for each set of x-ray event measurements.

REXIS contributes to the OSIRIS-REx mission with two science products: (1) globally measuring the elemental abundances of the asteroid Bennu to classify it among the major asteroid subgroups, and (2) generating a spatial elemental abundance map of the asteroid's surface. REXIS science data can provide context to the sample site selection process to ensure the sample collected is representative of the entire asteroid surface.

REXIS will achieve the first coded-aperture, wide field imaging for fluorescent line composition mapping of an asteroid. The Japan Aerospace Exploration Agency's (JAXA) Hayabusa (MUSES-C) asteroid sample return mission was non-imaging. A focusing, but smaller field of view, fluorescent mapping instrument will fly on the joint European Space Agency (ESA) - JAXA BepiColumbo mission to map Mercury.

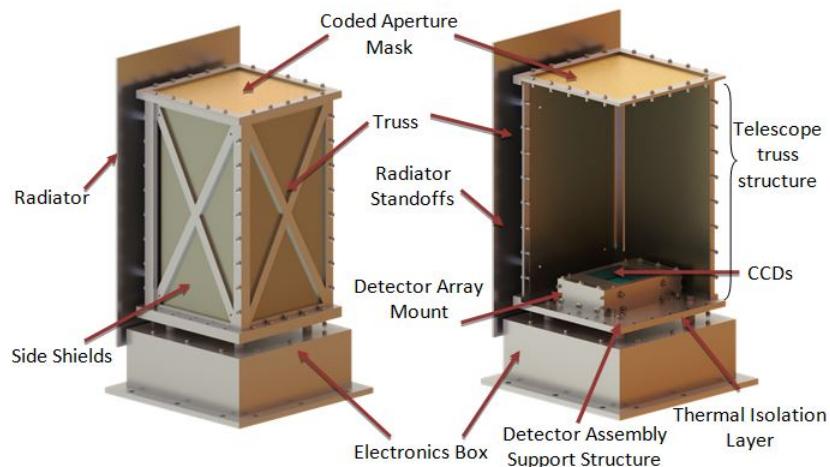


Figure 4-2: CAD rendering of REXIS instrument, without (left) and with (right) side shields removed (radiation cover and thermal strap not shown)

4.2 Requirements and Design Factors

This section discusses the high level driving requirements of the REXIS avionics system. These requirements, trades, and considerations led to selection of the Xilinx

Virtex-5QV SRAM-based FPGA as the heart of the REXIS flight avionics system along with the supporting power management components, memory units, and interface devices.

4.2.1 Requirements

Onboard Image Processing

OSIRIS-REx project requirements specify a 1.5 gigabyte limit on the amount of science data REXIS may transmit to the spacecraft for downlink to earth. This limit prevents the REXIS system from sending complete four megapixel frames to the spacecraft, as each frame would consist of eight megabytes, limiting the total number of frames downlinked to less than 200, which is not sufficient for REXIS to produce an adequate global map of elemental abundance on the asteroid. Thus the REXIS system must perform some onboard image processing of the pixel data collected from the CCDs to generate appropriately-sized science data for downlink to earth.

Additionally, science requirements dictate the integration time of collected charge on the CCID-41s be no more than four seconds to avoid pile up of x-ray events. Pile up occurs when more than one x-ray event strikes the same pixel on the detector array, making it difficult to determine if the charge measured for the pixel resulted from a single x-ray event or multiple x-ray events. Thus, the total time for REXIS avionics to read a frame from the detector array, process the frame for x-ray events, and transmit the resulting x-ray event list to the OSIRIS-REx spacecraft must be less than the four second integration time. Additionally, sufficient slack time must exist to allow flight software (FSW) to read data from the SXM, perform periodic housekeeping functions, and process commands from the spacecraft.

Detector Electronics

The MIT Kavli Institute for Astrophysics and Space Research provides the Detector Electronics (DE) that control the readout of the CCID-41 detectors. The DE implements a Camera Link interface to output the voltage measured on each pixel

of the CCDs, which operates at a base frequency of 30 MHz and a “7x clock” (bit frequency) of 210 MHz, facilitating data transfer at up to 686 MBytes/sec. A detailed description of the Detector Electronics interface appears in Appendix A. An FPGA provides the most straightforward solution to read in the pixel data from CCDs through the Detector Electronics and then store the pixel values in memory for future image processing.

Based on REXIS science goals and mission operating constraints the REXIS avionics system high level requirements are:

- provide digital interface to spacecraft for command processing and telemetry transmission
- provide control and measurement of the CCID-41 detectors
- provide control and measurement of the SXM
- provide onboard image processing of x-ray events
- maintain functionality in interplanetary radiation environment
- meet power, mass, cost, and radiation hardness requirements

4.2.2 Selection of Virtex-5QV

Interface and image processing requirements led the REXIS team to choose an FPGA for the avionics system. Because SRAM-based FPGAs are reconfigurable instead of OTP, they offer a less restrictive and more forgiving design flow, which is ideal for a student team. A reconfigurable FPGA also provides a versatile testbed for evaluating different logic designs and softcore processor implementations, including different system and subsystem clock speeds, different memory sizes, and power consumption. The flexibility of design flow is a primary reason the REXIS team chose an SRAM-based FPGA for the avionics system. SRAM-based FPGAs also provide the option of on-orbit reconfigurability, which was a desired feature of the REXIS avionics system.

Radiation-hardness requirements from the OSIRIS-REx project motivated the REXIS team to limit the possible FPGA choices to space grade FPGAs. The two currently available space grade SRAM-based FPGAs are the Xilinx Virtex-4QV and the Virtex-5QV. The Virtex-4QV is classified as radiation tolerant [9], and uses the same mask and circuitry as a particular revision of the commercial Virtex-4 [83]. The Virtex-5QV, however, uses extensive RHBD features, as listed in Table 2.5, and testing has shown these features to be much more effective at mitigating radiation-induced effects than the older Virtex-IIQV and Virtex-4QV (see Table 2.8). The combination of the need for an FPGA, project-level radiation-hardness requirements, and the RHBD nature of the Virtex-5QV led the REXIS team to the Virtex-5QV for the avionics subsystem.

4.2.3 Development Process

The REXIS instrument development and testing process is separated into the engineering model (EM) phase and flight the model (FM) phase. The REXIS team has designed the Engineering Model to be as flight-like as possible to facilitate high fidelity science data collection testing, spacecraft interface testing, thermal cycle testing, and mechanical/structural integrity and vibration testing. This chapter primarily documents the avionics Engineering Model system, which is designed to use prototype, engineering, or industrial versions of the RadHard electrical components that will serve on the REXIS Flight Model. The Engineering Model avionics system is designed around the industrial grade Virtex-5FX130T, and thus much of the development work involving FPGA hardware modules and softcore processor design was accomplished with the commercial Virtex-5FX70T and Virtex-5FX130T.

4.3 MicroBlaze and Hardware Interfaces

A MicroBlaze softcore processor serves as the command and data handler (CDH) for REXIS, running on an industrial grade Virtex-5FX130T for the EM and on a Virtex-5QV for the FM. To support the MicroBlaze and meet requirements, the avionics

design uses several Xilinx IP cores along with several custom hardware modules to implement interfaces to devices external to the Virtex-5. Each of the IP cores and custom hardware modules communicates to the MicroBlaze processor through the Processor Local Bus (PLB), allowing FSW to read status information and write commands. Figure 4-3 shows the Xilinx IP cores and the custom hardware modules used in the Virtex-5 design, along with their connections to components on the REXIS Main Electronics Board (MEB) and to external components located elsewhere on the REXIS instrument. In Figure 4-3, Xilinx IP cores appear in yellow, and custom hardware modules and configuration logic appear in green, along with interfaces to external components.

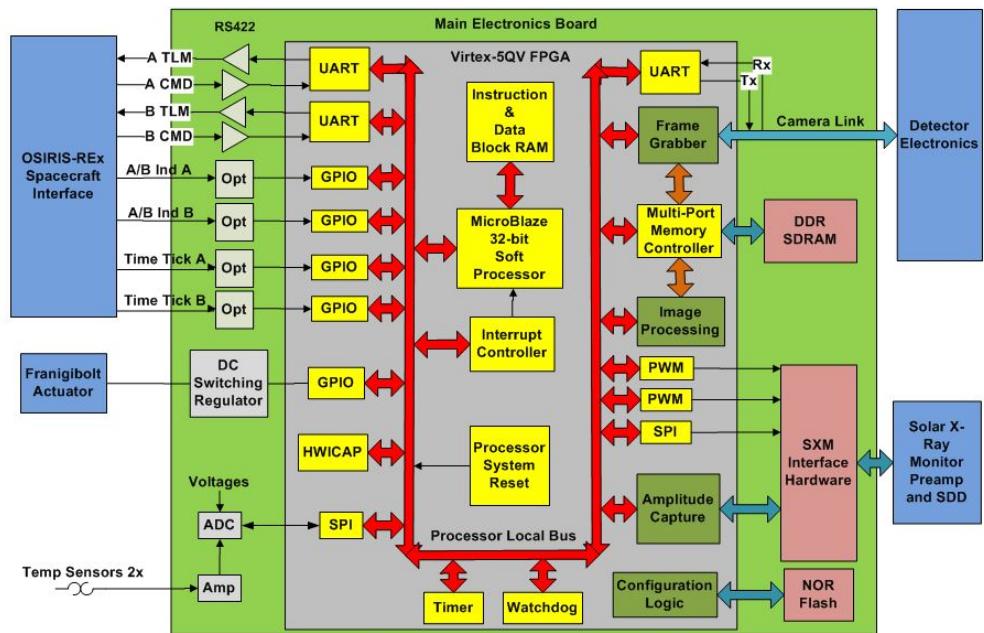


Figure 4-3: REXIS avionics system block diagram showing internal FPGA hardware modules

Table 4.1 lists each interface type to external components in the REXIS system. Each of these interfaces levies certain requirements on the system clock speed and instruction/data memory size, both of which are constrained by the MicroBlaze fault tolerance use case and implementation.

³General Purpose Input/Output

³Serial Peripheral Interface

³Pulse Width Modulation

Table 4.1: REXIS hardware interfaces

System	Device/Hardware	Interface
Avionics	Flash Memory SDRAM	BPI Up MPMC
Thermal	Temp Sensors	ADC Input
Structures	Frangibolt Actuator	GPIO ¹
Spacecraft Interface	RS422 Transceivers (x2)	UART
	Time Tick (x2)	GPIO
	Side Select (x2)	GPIO
Power	Voltage Sensors (x8) DC/DC Converter Inhibits (x2)	ADC Input GPIO
Housekeeping	ADC	SPI ²
Detector Electronics	Atmel MCU	UART
	Actel FPGA, Camera Link	Custom Hardware
Solar X-ray Monitor	Amplitude Capture Cockcroft-Walton Generator Thermoelectric Cooler DAC	Custom Hardware PWM ³ PWM SPI

4.3.1 Configuration Memory and Non-Volatile Storage

An Aeroflex 64-Mbit NOR flash memory unit stores the configuration bitstream for the Virtex-5. The Virtex-5 configuration hardware uses the Byte Peripheral Interface (BPI) Up configuration mode to read 16-bit words from the NOR Flash during configuration. Indirect BPI programming through the Virtex-5 facilitates writing of the bitstream onto the NOR Flash before it is used to configure the Virtex-5 [82].

Because the Virtex-5 configuration bitstream is approximately 50-Mbits (6.25 MBytes) in size, FSW uses the remaining 14-Mbits (1.75 MBytes) of space for non-volatile data and housekeeping information storage. A pull-up resistor sets the Write Protect signal high on the NOR Flash to avoid inadvertent writes to the non-volatile memory, thus requiring FSW to explicitly lower the FPGA output pin in order to write to non-volatile memory. Software restrictions will prohibit FSW from writing addresses in the first 50-Mbit of memory space in order to protect the FPGA configuration bitstream if it should be needed to reconfigure the Virtex-5 after a power-on reset commanded by the spacecraft.

4.3.2 Volatile Memory

An 3D-Plus 1-Gbit Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) provides volatile memory storage for the REXIS avionics system. Xilinx's MPMC provides the read/write interface to the MicroBlaze processor, accessing the SDRAM at 100 MHz and responding to read/write requests from the MicroBlaze at the processor system clock frequency.

The volatile memory stores the following structures for image processing: the bias map, the current frame, the possible x-ray events list (PXEL), and true x-ray events list (TXEL). Details of these structures appear in Section 4.4.

4.3.3 Power Management and Distribution System

The REXIS Power Management and Distribution System (PMAD) relies on one Rad-Hard EMI filter and seven RadHard DC-DC regulators to supply the required voltages to the REXIS system. Figure 4-4 shows the layout of the primary PMAD system. The 3.3V, 2.5V, and 1.0V regulators are designed to power up in a set sequence to ensure proper Virtex-5 power initialization: 1.0V voltage rail first, followed by 2.5V rail, and finally the 3.3V rail.

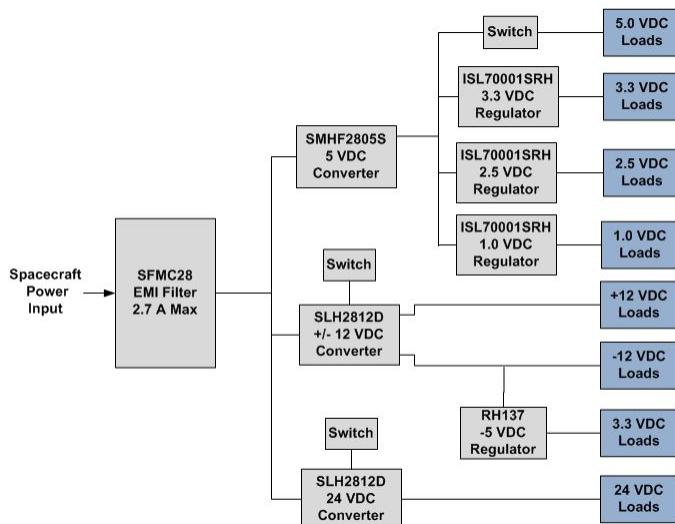


Figure 4-4: Block diagram of the REXIS primary power management and distribution system

4.3.4 Spacecraft Interface

The REXIS electrical interface to the OSIRIS-REx spacecraft consists of input power, asynchronous command and telemetry lines, and discrete time tick and side select digital signal lines. The OSIRIS-REx avionics system contains two separate CDH units (referred to as Side A and Side B, respectively) in order to provide a dual-string redundancy in the spacecraft avionics design. Although only one side of the spacecraft avionics is active at any one time, REXIS supports hardware interfaces to both Side A and Side B.

Asynchronous Command/Telemetry The command and telemetry interface to the OSIRIS-REx spacecraft is implemented according to the RS422 standard using the UART protocol. Two UART hardware modules implemented in the Virtex-5 facilitate communication with the spacecraft via RadHard Intersil RS422 transceivers. When data from the spacecraft appears on either of the command lines, the UART modules generate interrupt signals to the Interrupt Controller IP core, which prompts FSW to process the commands.

Discrete Time Tick and Side Select Each spacecraft CDH side provides a time tick signal as a method to synchronize the REXIS instrument clock to the spacecraft clock, as well as a side select signal indicating whether or not the spacecraft CDH side is active. Four Xilinx General Purpose Input/Output (GPIO) IP cores implemented in the Virtex-5 monitor the time tick and side select signals via a RadHard Avago optocoupler. When a rising or falling edge occurs on either of the time tick signal lines, the GPIO modules produce an interrupt to the Interrupt Controller IP core, which signals FSW to synchronize the instrument clock based on information received in a time update message over the command/telemetry interface. When a rising edge occurs on one of the side select lines, the GPIO triggers an interrupt to FSW through the Interrupt Controller, resulting in FSW changing the UART module to which it listens for commands and sends telemetry.

4.3.5 Detector Electronics Interface

The Detector Electronics (DE) provide the interface to, and control of, the four CCID-41 detectors in the REXIS detector array. The DE converts the analog signal from the detectors into a digital signal for storage and image processing and is capable of controlling up to four CCDs. FSW controls the DE via a UART interface at 115,200 bits/sec. On command from FSW, the DE measure and transmit the pixel values from the CCID-41 detector array to the Frame Grabber custom hardware module at 30 MHz in the Camera Link format. At the time of this writing, the DE provide 16-bits of energy resolution per CCD pixel measured. Appendix A provides details of the DE design and operation.

4.3.6 Frame Grabber and Hardware Image Processing

Custom VHDL and Verilog logic designs in the fabric of the Virtex-5 implement the Frame Grabber module, which receives CCD digital pixel energies from the Detector Electronics in the Camera Link format and writes them to external SDRAM via an interface with the MPMC IP core.

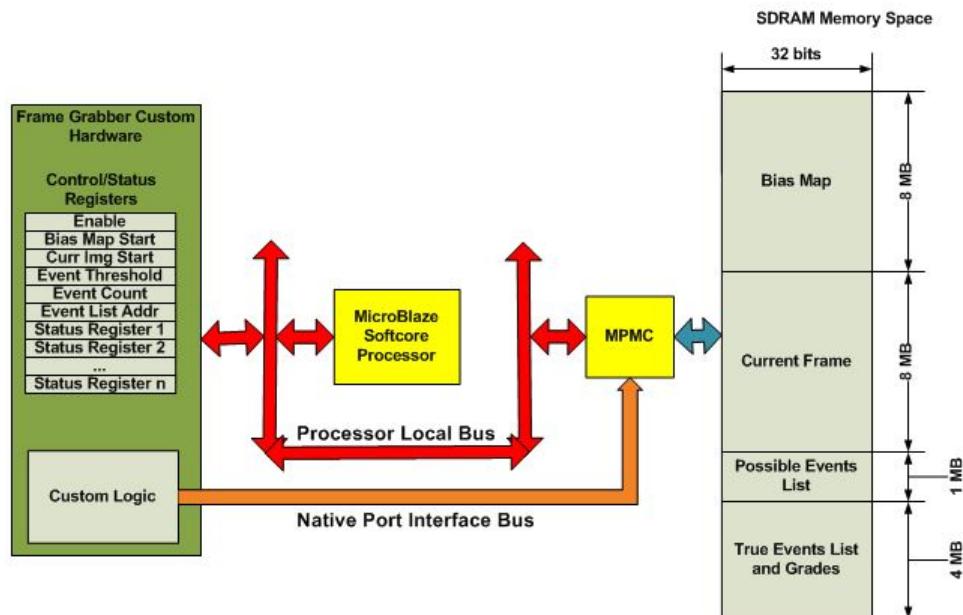


Figure 4-5: Frame grabber and image processing control and status registers shown with MPMC interface to SDRAM memory regions used for image processing

Figure 4-5 provides an illustration of the connections between the custom frame grabber logic, control registers, MicroBlaze, MPMC, and SDRAM. The Native Port Interface (NPI) of the MPMC allows the custom logic to read and write the SDRAM memory, where it stores the current frame in a specific format to re-create the image in memory as it receives it from the DE. This specific format facilitates simpler algorithmic access to each pixel in the frame for image processing.

The MicroBlaze processor controls the Frame Grabber and Image Processing custom hardware modules through 32-bit wide control and status registers accessible via the PLB. Through a PLB interface to the MPMC, the MicroBlaze may also read and write values in SDRAM, allowing it to perform event grading on x-ray events. The final x-ray event list for transmission to the spacecraft as science data is stored in MicroBlaze BRAM data memory.

4.3.7 Solar X-ray Monitor Interface

The Solar X-ray Monitor (SXM) provides solar x-ray activity calibration data for the REXIS instrument. A block diagram appears in Figure 4-6, and Appendix B provides details of the SXM design. Similar to the frame grabber and image processing modules, the MicroBlaze controls and reads data from the SXM custom interface hardware via a set of 32-bit wide control, status, and data registers accessible via the PLB.

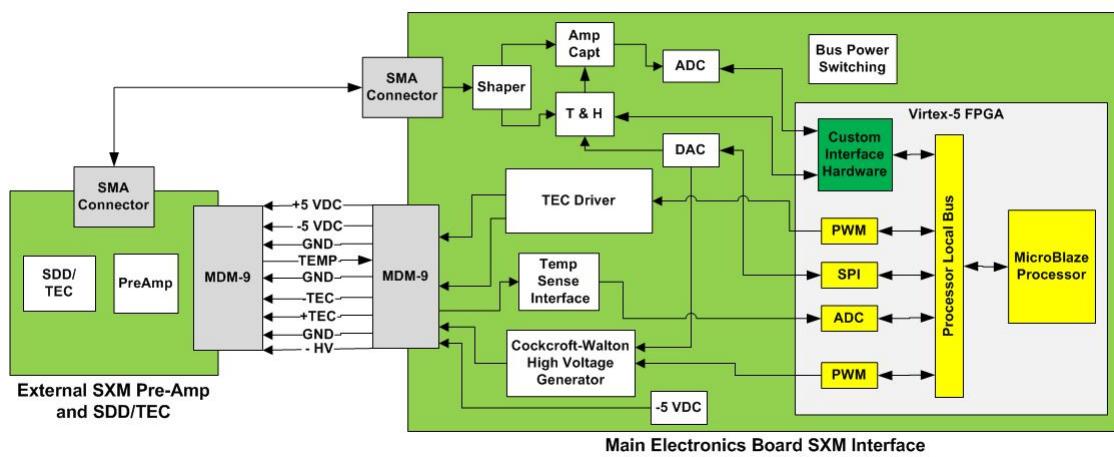


Figure 4-6: Solar X-ray Monitor Functional Diagram

The SXM custom hardware module provides 320 energy bins of 32 bits each to record the number of events detected in each energy bin during the histogram update period (i.e. integration time of the SXM). FSW reads values in the energy bins to create a histogram of event energies at a configurable rate (baseline of once every 100 seconds), and then generates an SXM histogram science packet for transmission to the spacecraft.

4.3.8 Frangibolt Actuation Circuit

The Frangibolt radiation release cover mechanism controlled by the Frangibolt actuation circuit provides the capability to open the radiation cover protecting the CCID-41 detectors during the cruise phase of the REXIS mission. A RadHard M.S. Kennedy MSK5055RH switching regulator controller along with two external Rad-Hard n-channel MOSFETs and supporting components switch the spacecraft bus voltage down to 9VDC to supply power to the Frangibolt actuator during actuation. REXIS FSW controls a dedicated GPIO IP core, the output of which is connected to the enable pin on the MSK5055RH controller.

4.3.9 Housekeeping

A RadHard Texas Instruments 12-bit ADC with a built-in 8:1 multiplexer provides voltage measurement capability for system monitoring and housekeeping data collection. Housekeeping values include temperature readings from platinum temperature resistors (PRTs) and the voltage of each voltage rail in the REXIS PMAD system. The MicroBlaze communicates with the ADC via a Xilinx SPI interface IP core.

4.4 Image Processing

This section details the onboard image processing of CCD data for x-ray events performed by the avionics system. Image processing requirements drive the required system clock frequency and MicroBlaze instruction/data memory space, both of which

are affected by the MicroBlaze fault tolerance use case and implementation. REXIS image processing consists of several steps performed on each frame readout from the CCDs: bias subtraction, event finding, and energy summing and event grading. Additionally, FSW performs bias map generation at the start of each science run (each time REXIS FSW enters image processing mode).

4.4.1 Algorithm Heritage

The REXIS image processing algorithms draw on experience from the Advanced Satellite for Cosmology and Astrophysics (ASCA) x-ray imaging mission, Advanced CCD Imaging Spectrometer (ACIS) x-ray imaging payload, and Suzaku (ASTRO E) x-ray imaging spectrometer mission. More background and detail of these designs appear in Appendix A.

4.4.2 Bias Map Generation

Based on experience from the ASCA, ACIS, and Suzaku missions, distinguishing X-ray events within a CCD pixel from background noise requires knowledge of the pixel energy value the analog charge readout electronics on the DE would measure in the absence of any event or background—this quantity is known as the pixel’s “bias level” [77]. To facilitate this determination, an array of bias levels known as the bias map is stored in memory, which the imaging system must subtract from the incoming data pixels prior to any further image processing [39]. Bias subtraction also removes inherent noise from each frame—this noise characteristic is unique to each of the four nodes of each CCID-41 detector and the associated DE readout electronics for each node.

At the beginning of each REXIS science run (each time REXIS FSW enters image processing mode), FSW generates a bias map from multiple frames collected from the CCID-41 detector array. First, FSW takes a series of bias conditioning frames in order to measure an estimated base bias level for each pixel in the detector array. Then FSW selectively averages pixel values from approximately 12 frames, pixel by

pixel, to generate the bias map array. FSW and the Frame Grabber hardware module store the eight megabyte bias map in external SDRAM.

4.4.3 Bias Subtraction and Event Finding

After bias map generation is complete, FSW performs bias subtraction and event finding for each frame readout from the CCID-41 detectors while in image processing mode. Once the Frame Grabber hardware module has completed frame capture, FSW starts the Image Processing hardware module via a control register write. The Image Processing module then subtracts each bias map pixel value stored in SDRAM from the corresponding current frame pixel value. After bias subtraction, if the current frame pixel value is above the event threshold (ET), the Image Processing module records its memory address in the possible x-ray events list (PXL). Once bias subtraction and event finding are complete, the image processing module generates an interrupt through the Interrupt Controller IP core to signal FSW.

Testing of the bias subtraction and event finding algorithm with software and hardware implementations demonstrated the advantages of employing FPGA hardware for these algorithms, as shown below in Table 4.2.

Table 4.2: Comparison of Bias Subtraction and Event Finding Times for Software and Hardware Implementations

Implementation	Execution Time (s)
Software	3.1
Hardware	1.2

The custom-designed Image Processing hardware module implemented in VHDL/Verilog clocked at 125 MHz performed 2.5 times faster than a C-based implementation on the MicroBlaze processor clocked at 125 MHz. In this comparison, both the hardware Image Processing module and MicroBlaze software implementation used the MPMC interface to external DDR2 SDRAM at 125 MHz on the Xilinx ML507 development platform. Each case was executed on the Virtex-5FX70T on the ML507 development

board using a four megapixel image stored in DDR2 SDRAM with 4000 simulated x-ray events placed in the image prior to bias subtraction and event finding.

4.4.4 Energy Summing and Event Grading

After the Image Processing module identifies possible x-ray events in the current frame, FSW performs energy summing and event grading to produce the true x-ray event list (TXEL) which eventually (after possible selective low energy filtering) constitutes REXIS primary science data. Event grading is used because x-ray photons may deposit charge in more than one pixel when striking the detector arrays, and this approach is based on image processing techniques used on the ASCA, ACIS, and Suzaku systems. FSW sums and grades each possible event in the PXL by means of examining a 3x3 pixel grid surrounding each pixel energy in the PXL. Figure 4-7 shows the 3x3 grid of eight pixels surrounding the center pixel (possible x-ray event with energy above the event threshold), which is colored green and labeled “(i,j)”. Once energy summing and event grading are complete, FSW writes the pixel’s (x,y) location on the detector array, total energy, and event grade to the True X-ray Events List (TXEL), with which FSW may perform selective low energy filtering based on the total number of true x-ray events detected.

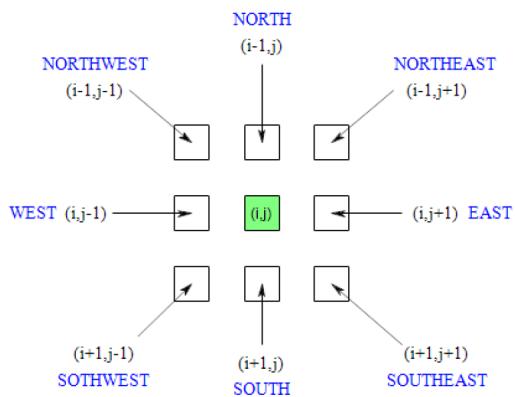


Figure 4-7: 3x3 pixel grid used for event grading

Energy Summing

If the pixel energy is a local maximum with respect to the energies of the eight surrounding pixels in the 3x3 grid, then FSW performs energy summing. If the energy of each pixel in the 3x3 grid exceeds the split-threshold (ST, sometimes known as the secondary threshold), FSW adds its energy to the energy of the center pixel (the center pixel being above the primary event threshold), thus creating a summation of total event energy. The ST is configurable in software by command.

ASCA Event Grading

To provide information on the distribution of x-ray event energy within the 3x3 pixel grid, FSW performs an event grading function based on the same technique used on the ASCA mission. As shown in Figure 4-8, each pixel in the 3x3 grid surrounding the center pixel (grade 0) is assigned a distinct power of two. If the energy in a pixel is above the split threshold, then FSW adds its corresponding event grade value to the grade for the event. For example, if all eight pixels surrounding the center pixel contain energies above the ST, then the event is a grade 255. If only the north pixel directly above the center pixel contains an energy above the ST, then the event is grade 64. Thus, the geometric arrangement of pixels exceeding the ST determines the grade code [39].

32	64	128
8	0	16
1	2	4

Figure 4-8: ASCA 3x3 grading model for an X-ray event [15]

The event grading algorithm also rejects cosmic rays at this time through a combination of high energy rejection and rejection of certain patterns of charge collection (the grade code) [39] from the TXEL. Cosmic rays have energies on the order of MeV, much higher than the 0.5 keV to 8 keV range of x-ray photon energies REXIS

is designed to measure.

Low Energy Filter

As mentioned previously, REXIS has a limited science data budget for instrument housekeeping and science data downlinked to earth. Based on the data budget and the amount of operational time allotted to REXIS during the mission, FSW may send a maximum of 200 x-ray events per frame. If the Image Processing Module detects more than 200 events, FSW implements a selective low energy filter to trim the TXEL down to a final event list to 200 events before sending the event list to the spacecraft.

4.4.5 Image Processing Testing

This section provides a brief overview of frame grabbing and image processing testing the REXIS team conducted with CCID-41 detectors under irradiation from an Iron-55 soft x-ray calibration source. The test setup consisted of the REXIS Virtex-5 design running on a Xilinx ML507 development board with a Camera Link interface to the prototype DE, which were connected to two CCID-41s in a thermal vacuum chamber (TVAC). Testing of the REXIS image processing system with live CCID-41 detectors has demonstrated the importance of bias subtraction in the image processing algorithms.

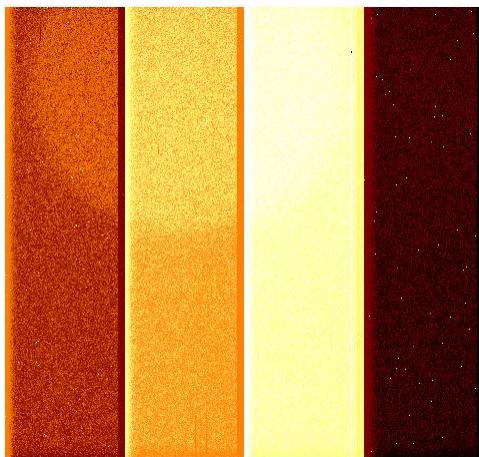


Figure 4-9: ds9 visualization of pixels on CCID-41 detector under Iron-55 irradiation

The detector temperature during this test was approximately -70° Celsius, which prevents dark current from adding noise to the measurements. As noted previously, each analog electronics chain that measures charge from each of the CCD output nodes has a characteristic noise level different from the other chains. Additionally, each node of the CCID-41 has slightly different readout characteristics, which are visibly apparent in Figure 4-9. The color scheme in Figure 4-9 uses histogram equalization, making x-ray events appear white against the darker background of non-event pixels in each node.

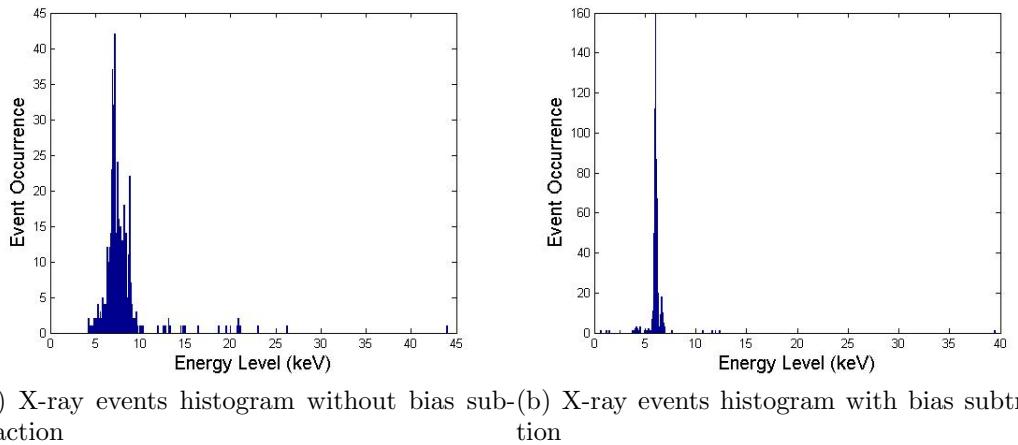


Figure 4-10: Comparison of X-ray histogram with and without bias map subtraction performed prior to event grading

Figure 4-10a shows a histogram generated by the REXIS event grading algorithm on the frame shown in Figure 4-9 without including bias subtraction prior to event grading. The primary energy line of Iron-55 at 5.9 keV is visible as the largest peak in the histogram, however, the secondary energy line at 6.3 keV is not definitively distinguishable amongst the many secondary energy lines to the right of the 5.9 keV line.

In contrast, Figure 4-10b shows a histogram generated by the REXIS event grading algorithm on the frame shown in Figure 4-9 with bias subtraction performed prior to event grading. The primary energy line at 5.9 keV is better defined and the secondary peak is more distinctly grouped around 6.3 keV than in the histogram generated without bias subtraction.

4.5 Flight Software

This section briefly outlines the design and operation of the REXIS Flight Software (FSW). REXIS FSW does not use an operating system, but instead relies on a single thread, non-preemptible structure based around the four second integration time of the CCD detectors, which FSW nomenclature refers to as the four second image processing loop.

4.5.1 Operating States

REXIS FSW operates in one of two states: safe mode or image processing mode. In safe mode, FSW sends aliveness messages to the spacecraft once every four seconds, and housekeeping packets once every minute, but does not perform any science data acquisition or processing. In image processing mode, FSW performs CCD data acquisition and processing, sending CCD event list packets to the spacecraft once every four seconds as dictated by the image processing loop. Additionally, FSW reads and transmits SXM histogram packets once every 100 seconds and housekeeping packets once every minute. Figure 4-11 provides a simplified state transition diagram for FSW operating states.

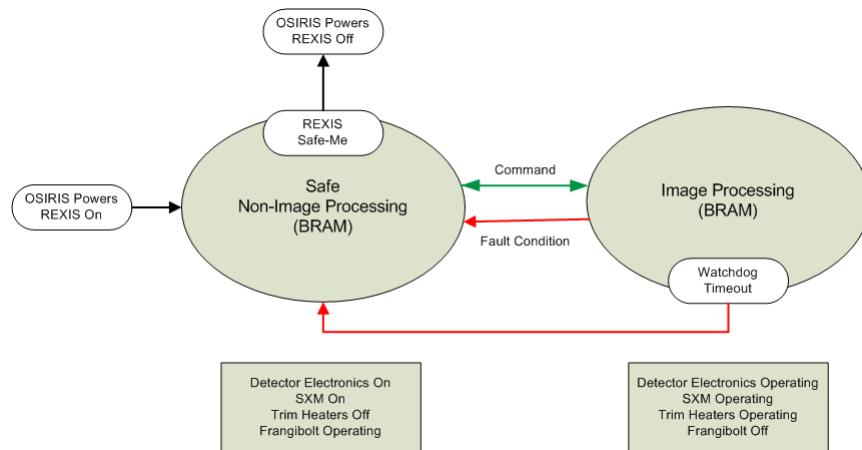


Figure 4-11: Simplified REXIS FSW state transition diagram

REXIS Image Processing Loop

While in image processing mode, FSW steps through the image processing loop once every four seconds based on the required maximum allowable integration time of the CCD detectors, which is four seconds. During the loop, FSW executes each of the steps described in Section 4.4: bias subtraction, event finding, energy summing and event grading, and selective low energy filtering (if necessary), followed by transmission of the final x-ray event list to the spacecraft. A hardware Timer IP core provides interrupts to FSW once every four seconds to initiate entry into the loop. Successful and timely execution of the image processing loop is essential to ensuring REXIS provides sufficient science data production to map the surface of the asteroid Bennu.

4.6 Fault Tolerant Design Application

4.6.1 Configuration Monitoring

As discussed in Chapter 3, configuration monitoring is a desirable feature for a SRAM-based FPGA operating in a space environment, even a RHBD model. In considering what monitoring scheme to apply in the REXIS avionics system, the REXIS team did not opt for an external configuration monitor due to the associated increases in design complexity, interface complexity, required PCB area, power, and cost. Additionally, the REXIS instrument can rely on the OSIRIS-REx spacecraft as a psuedo watchdog for instrument aliveness and correct functionality. If the REXIS MicroBlaze suffers a major functional error due to an SEU, then the spacecraft FSW can reset REXIS by removing power and then reapplying power, which will cause a reconfiguration of the Virtex-5 and clear the error.

An internal configuration monitoring and scrubbing scheme proved more attractive to the REXIS design. Although not yet implemented in the REXIS Virtex-5 system at the time of this writing, The REXIS avionics team plans to add a version of the Virtex-5 SEU controller discussed in 3 into the REXIS design. One possibility would be to include the SEU controller outside the EDK platform studio project (which

contains the MicroBlaze and supporting peripherals). In this scheme, the MicroBlaze would communicate to the SEU controller via a UART IP core connected to the SEU controller’s UART control/status lines. This approach could prove simple because the SEU controller can be treated as a black box with defined commands and output data as presented in Chapman’s application note [33]. Another option is to modify the SEU controller to incorporate it as a semi-custom hardware module that connects to the MicroBlaze PLB.

4.6.2 MicroBlaze Fault Tolerance

The REXIS avionics design stores instruction/data memory for FSW in Virtex-5 BRAM, which is the most vulnerable non-RHBD special function hardware module in the Virtex-5QV. The REXIS team plans to implement the typical fault tolerance use case in the MicroBlaze system to facilitate generation of an interrupt if the instruction or data LMB controllers detect errors in BRAM. The Flight Model of the MicroBlaze system will not employ the full fault tolerance use case to avoid the possibility of inadvertently writing incorrect data into memory using the fault injection registers. However, the team may employ the full use case for fault response handling and characterization during development with the Engineering Model.

As anticipated by the analysis and results presented in Chapter 3, applying additional fault tolerant design techniques to the REXIS MicroBlaze system constrains the design. Restrictions on the MicroBlaze instruction/data memory size and MicroBlaze processor system clock speed are the primary effects of applying fault tolerance to the REXIS design, the implications of which are restricted code size and slower execution times for software tasks, respectively. This section details these effects and their impact on the REXIS architecture.

Based on the REXIS FSW architecture design, FSW must perform all required functions within the four second image processing loop time. To mitigate SEU upsets in the instruction/data stored in BRAM, REXIS will employ a fault tolerance use case in the MicroBlaze system, which will require a slower clock frequency resulting in slower execution times for REXIS FSW. To characterize the effects of slowing the

processor clock frequency to accommodate a MicroBlaze fault tolerance use case, the execution times of energy summing and event grading and required FSW tasks were measured using the Virtex-5FX70T on the Xilinx ML507 development board. Table 4.3 provides a characterization of the increase in execution time for energy summing and event grading algorithms (as described in Section 4.4) running with a 62.5 MHz processor frequency as compared to a 125 MHz processor frequency.

Table 4.3: Energy summing and Event grading execution time on simulated x-ray events with varying system clock speeds and fixed SDRAM interface speed of 125 MHz

Events Graded in Frame	62.5 MHz (ms)	125 MHz (ms)
32	0.383	0.225
64	0.764	0.447
128	1.525	0.890
200	2.465	1.345
255	3.048	1.779
512	6.074	3.54
1024	12.121	7.055
2048	28.40	14.07

Processor system clock frequencies of 62.5 MHz and 125 MHz were the selected frequencies for comparison due to limitations on the DDR2 SDRAM interface clock frequency on the ML507 development board. The Xilinx EDK enforces a 1:1 or 1:2 ratio between the processor system clock frequency and the MPMC-external memory interface clock frequency, and the lowest MPMC-external memory interface clock frequency for the DDR2 SDRAM on the ML507 is 125 MHz. To provide an appropriate basis for execution time comparison between different processor clock frequencies, the MPMC-external memory clock frequency should remain constant. Given the DDR2 SRAM and MPMC restrictions, processor system clock frequencies of 62.5 MHz and 125 MHz are the available options for comparison. Since the REXIS system will use DDR SDRAM capable of operating at slower frequencies, slower processor system clock frequencies will be available for consideration in the final REXIS design.

Table 4.4 shows the measured execution times for required FSW tasks that must execute within the four second imaging loop. Due to the status of FSW builds at the time of this writing, fault/error handling and checksum generation/validation execution times are not included in Table 4.4. The execution time for transmission of housekeeping, SXM histogram, and CCD event list packets does not include the UART transmit interrupt handling time. However, the execution times for these tasks is not expected to increase significantly the total execution time for all required tasks.

Table 4.4: Execution time in ms for FSW tasks at different processor system clock frequencies with 125 MHz SDRAM interface clock speed

FSW Task	62.5 MHz (ms)	125 MHz (ms)
Process Command	0.295	0.174
Housekeeping	0.579	0.287
Housekeeping TX	0.18	0.37
SXM Histogram	0.329	0.160
SXM Histogram TX	0.048	0.020
CCD Event Energy Sum & Grade	28.4	14.07
CCD Event List TX	0.134	0.066
Total	29.97	15.147

The results in Table 4.4 demonstrate the REXIS system can execute required FSW tasks within the four second image processing loop time with substantial margin, even with a reduced processor clock frequency resulting from implementation with a MicroBlaze fault tolerance use case. The total FSW task execution time is small relative to the four second imaging loop time primarily because the Image Processing custom hardware module implementation frees FSW from performing the time-intensive tasks of the event finding and bias subtraction algorithms (see Table 4.2). If other design and system constraints dictated the event finding and bias subtraction functions execute in software, the system might fail to meet the four second imaging loop requirement as a result of a slower processor clock frequency.

4.7 Conclusion

The REXIS avionics system provides a case study of the effects of applying additional fault tolerance to a system designed for implementation on a RHBD SRAM-based FPGA and initially for implementation on a commerical SRAM-based FPGA. These effects can be critical to ensuring the FPGA system design functions correctly and meets time-based processing requirements, especially in a design centered around a softcore processor. Beginning a system design and trade space exploration with these effects and constraints in mind can save designers significant time as well as improve the overall reliability of the design.

Chapter 5

Conclusion and Future Work

This thesis began with a literature review of radiation effects on FPGAs, FPGA radiation testing and effects prediction, and an overview of the RHBD SRAM-based Virtex-5QV to provide a foundation for the primary contributions of this work. It then identified the additional design techniques designers should use when implementing a system based around a RHBD SRAM-based FPGA. The additional design techniques focus on configuration management and scrubbing, adding fault tolerance to non-RHBD special function modules, and adding fault tolerance to MicroBlaze softcore processor system designs. This work also quantified the cost of implementing the techniques and provided a list of recommendations toward their implementation in system design.

For configuration management, this work detailed the advantages and disadvantages of external scrubbing schemes and internal scrubbing schemes, as well as analyzing several published external schemes and internal schemes. For special function hardware modules, this thesis quantified the area and power cost of adding additional hardware modules to incorporate fault tolerance through redundancy. For softcore processor use, this work quantified the frequency and internal BRAM constraints imposed by adding fault tolerance use cases to the MicroBlaze softcore processor.

This thesis also demonstrated the implementation of several of the additional design techniques on the REXIS instrument avionics system as a case study. The nexus of real world requirements and constraints such as spacecraft-to-payload interfaces,

component radiation hardening requirements, and the effect of thermal cycling and mechanical vibration on avionics design choices (to name a few), with desired fault tolerance and error mitigation schemes demonstrates how a flight system can prove more complicated than a lab test bench proof of concept. However, these challenges make REXIS, and specifically the REXIS avionics system, a worthy research effort—one from which current and future designers and engineers can learn.

5.1 Future Work

This thesis identified the baseline additional design techniques for use of a RHBD SRAM-based FPGA, while leaving room for follow-on research and more thorough exploration of fault tolerant designs with the special function hardware modules of the Virtex-5QV. One principal area for further work is the creation of a DCM/PLL error monitoring design along with measurement of its resource consumption and error detection accuracy and resolution.

In the REXIS design, ECC has been implemented on the BRAM storing the instruction and data memory of the MicroBlaze. ECC implementation and handling on the FIFO that transfers pixel values between the Detector Electronics Camera Link interface and the MPMC interface to SDRAM has yet to be implemented. Also, ECC on the BRAM in the MPMC interface to the DDR SDRAM has yet to be implemented. Appropriate handling procedures and functions for errors in each of these vulnerable BRAMs will require planning and development time, as well as a proper analysis of their impacts on performance of the frame grabber and image processing functions.

Apropos configuration management and scrubbing, much work remains to facilitate the integration of some form of the Virtex-5 SEU controller as an internal configuration manager and scrubber in the REXIS Virtex-5 design. Additionally, a detailed plan to monitor configuration status via an ICAP module should be developed along with a set of FSW responses to error signals detected in the status. Such a plan and implementation on REXIS would provide a higher level of fault tolerance

to the design while also providing the opportunity to produce interesting on-orbit statistics of configuration status and internal configuration monitoring performance.

Given the opportunities to implement multiple softcore processors on a single FPGA design in conjunction with the logic resource and power utilization estimated in Chapter 3, the possibility of designing the REXIS system with multiple MicroBlaze processors could open several avenues of research. The trade space available from a combination of redundant MicroBlaze processors and fault tolerant software techniques [65] could offer substantially more protection from SEU-induced faults as compared to using only a single MicroBlaze with an ECC fault tolerance use case enabled. Triplication of the MicroBlaze instruction/data BRAM system followed by testing with fault injection also holds the promise of adding additional fault mitigation to the fault tolerance options already existing in the BRAM controllers, as well as providing an area ripe for research.

An early driver of the selection of the Virtex-5QV for the REXIS instrument was the opportunity to employ reconfiguration on-orbit. This possibility was attractive to the system design team in the early phases of the project, before the team completely understood the details of system implementation with an SRAM-based FPGA. On-orbit reconfiguration likely requires either an external configuration monitor or partial reconfiguration, and each of these options comes with a cost. The team did not opt for an external configuration monitor due to the associated increases in design complexity, interface complexity, required PCB area, power, and cost. Thus, partial reconfiguration is an option for the REXIS design. Implementing partial reconfiguration in the REXIS system and studying how to apply fault tolerance to increase its reliability are prime candidates for further research and effort.

Appendix A

CCDs and Detector Electronics

This appendix reviews the basic functionality of CCDs as scientific instruments, the basic structure and capabilities of the CCID-41 detector, and the functionality of the TESS prototype Detector Electronics.

A.1 Charge Coupled Devices

A.1.1 CCD Operation

CCDs function similarly to proportional counters, in that individual photons striking a CCD photoelectrically liberate a number of electrons roughly proportional to the x-ray photon energy [58]. The generated electrons (charge) are stored in the depletion region of a metal-oxide-semiconductor (MOS) capacitor, which are placed very close together in the CCD array [52]. Controlling readout electronics move the charges in the CCD circuit by manipulating the voltages on the gates of the capacitors so as to allow the charge to spill from one capacitor to the next. Thus the name “charge-coupled” device [52].

In the three-phase CCD, such as the CCID-41, the gates are arranged in parallel, and every third gate is connected to the same clock driver signal. The basic cell in the CCD, which corresponds to one pixel, consists of a triplet of these gates, each separately connected to phase-1, phase-2 and phase-3 clocks making up a pixel register

[52]. Figure A-1 is a diagram of a three-phase CCD, showing the orientation of both the vertical (parallel) and horizontal (serial) registers.

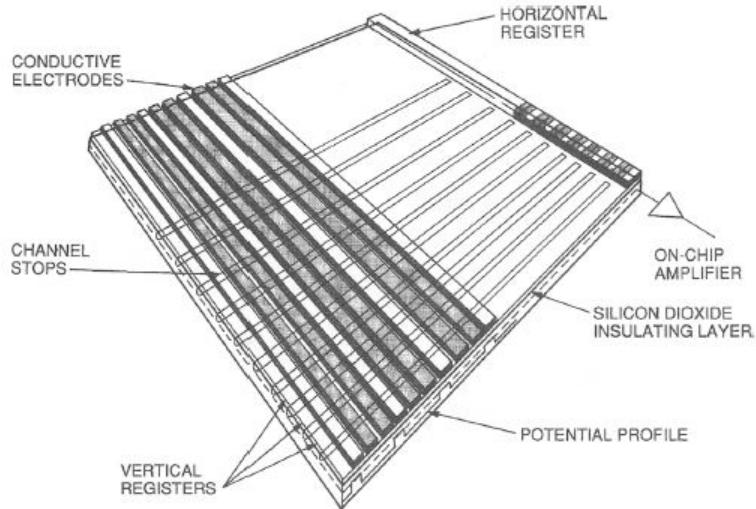


Figure A-1: Primary components of a three-phase CCD [52]

A CCD image is read out by a succession of vertical shifts through the vertical registers, or parallel registers. For each vertical shift, a line of pixels is transferred into a horizontal, or serial, register which is oriented perpendicular to the parallels. Before the next line is shifted, the charge in the serial register is transferred to the output amplifier (video chain the case of the Detector Electronics), which converts the charge contained in each pixel to a voltage. Readout electronics serially read out the device line-by-line, pixel-by-pixel, creating a representation of the scene of photons incident on the device. [52]

Ideally, the charge from a single x-ray photon would be confined to a single pixel (referred to as the target pixel), and the surrounding pixels would contain no charge. In practice, the photon is sometimes absorbed below the CCD's depletion layer, in a field-free region. Charge generated there diffuses into neighboring pixels, an indicator of degraded charge collection efficiency(CCE) performance. Also, imperfect charge transfer causes some of the charge from the target pixel to "lag" during successive transfers so that an x-ray event exhibits a "tail" of deferred charge. The size and shape of this tail is an indicator of charge transfer efficiency (CTE) performance. [52]

A.1.2 Iron-55 Calibration

Iron-55 is a standard soft x-ray source for CCD calibration. An Iron-55 atom is inherently unstable and decays into a Manganese atom when its nucleus quantum mechanically absorbs a K-Shell electron (half-life is 2.7 years). An electron generates an x-ray when it drops from either the L-shell or the M-shell to fill the newly vacant K-shell. This action produces either a K_{α} (5.9 keV) or a K_{β} (6.3 keV) x-ray, respectively. The production of an alpha x-ray is 7 times more likely than a beta x-ray [52]. Additionally, a 5.9 keV photon generates 1620 electrons in the CCD, resulting in a conversion factor of 3.65 eV per electron.

A.2 Mission Heritage

A.2.1 ASCA

The Advanced Satellite for Cosmology and Astrophysics (ASCA, formerly Astro-D) was Japan’s fourth cosmic x-ray astronomy mission, and the second for which the United States provided part of the scientific payload [12].



Figure A-2: Artist’s rendering of the ASCA spacecraft [12]

ASCA carried two Solid-state Imaging Spectrometers (SIS), the hardware for which was supplied as a joint effort by MIT, the Institute of Space and Astronautical Science (ISAS), and Osaka University [6]. The SIS units on ASCA represent the first successful space flight use of X-ray CCDs as photon counting and spectroscopic imagers.

The SIS observed x-rays in the energy range of 0.4 keV to 10 keV, with a resolution of two percent at 5.9 keV (Iron-55 K_{α} line), using Lincoln Lab CCID7s [58].

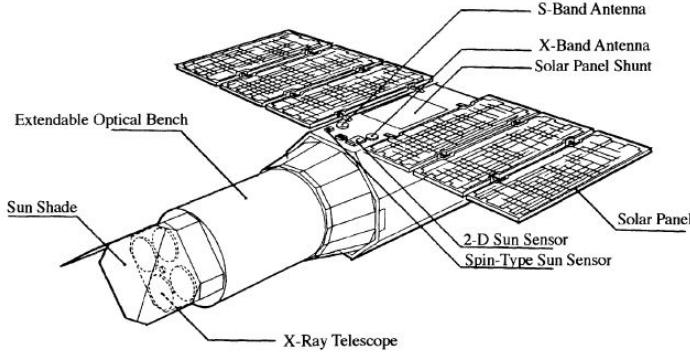


Figure A-3: Drawing of ASCA spacecraft with major components labeled [58]

ASCA operated successfully for seven years until attitude control was lost on 14 July 2000. After completing its mission, ASCA reentered the atmosphere on 2 March 2001.

ASCA used 54HC series logic chips to control the readout of the CCDs, CS5012 ADCs to measure the charge accumulated in each pixel, and a Fujitsu digital signal processor for video processing. Energy consumption for the readout electronics was approximately $65 \mu\text{J}/\text{pixel}$.

A.2.2 ACIS

The Advanced CCID Imaging Spectrometer (ACIS) launched aboard the Chandra X-ray observatory (CXO) on July 23, 1999. The CXO is designed for high resolution ($1/2$ arcsec) X-ray imaging and spectroscopy. The ACIS imaging system consists of ten CCDs, four front illuminated (FI) arranged in a square configuration and six in a linear array [39]. At the time of this writing, ACIS continues to operate on-orbit aboard Chandra, providing scientific data. Figure A-4 is an artist's rendering of the CXO spacecraft.

The ACIS parallel clocks shift charge from row to row in $40 \mu\text{s}$, which is four times the pixel rate of $10 \mu\text{s}$. Approximately 3.2 seconds are required to readout all of the pixels from the frame store and measure the charge stored in each. Energy



Figure A-4: Artist's rendering of the Chandra spacecraft [1]

consumption from sensors to downlinked telemetry was about $25 \mu\text{J}/\text{pixel}$ for ACIS.

ACIS uses Actel antifuse FPGAs to control the readout of the CCDs, CS5012 ADCs, and a Mongoose processor. The Mongoose is a radiation hardened MIPS R3000 32-bit microprocessor fabricated on CMOS Silicon-on-Insulator (SOI) [7]. ACIS electronics shift pixels from the imaging area to the framestore in 41 ms and typically expose the imaging area for 3.24 seconds [39].

Additionally, analysis of CCD data from the ASCA mission demonstrated the CCD bias levels changed significantly in a spatially random manner (presumably resulting from radiation damage). Following this realization, the ACIS team added bias map generation and bias subtraction capabilities to the ACIS image processing system [77], both of which are included in the REXIS image processing design.

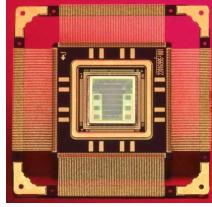


Figure A-5: Mongoose-V RadHard MIPS processor [7]

A.2.3 Suzaku

Suzaku (formerly Astro-E2) is Japan's fifth x-ray astronomy mission. The X-ray Imaging Spectrometer (XIS) consists of both front-illuminated and back-illuminated CCDs (X-ray Imaging Spectrometer on Suzaku).

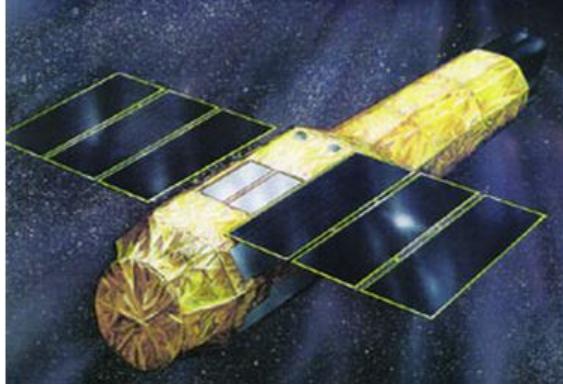


Figure A-6: Artist's rendering of the Suzaku spacecraft [5]

A.2.4 TESS

The mission of the Transiting Exoplanet Survey Satellite (TESS) is to locate exoplanets using four Lincoln Laboratory CCID-68 detectors for visible light sensing. At the time of this writing, NASA selected the TESS program for funding under the Small Explorer's program, scheduled for launch in 2017.

The TESS charge sensing circuits will have noisier, lower responsivity, allowing them to handle relatively large signals, on the order of hundreds of thousands of electrons per pixel. The maximum signal for TESS will be larger than 200,000 electrons, with a goal of detecting up to 500,000 electrons, while the noise is designed to be less than 20 electrons per pixel. This yields a dynamic range of $200,000 / 20 = 10,000$. TESS requires a higher resolution ADC (at least 16 bits) to provide accurate measurements and sufficient resolution for science data processing.

The TESS CCD detector array will be 16 megapixels in size, making it four times the size of the 4 megapixel REXIS CCD detector array. TESS science requirements dictate frames must be transferred from the detector array once every two seconds, which is a driving requirement for the TESS DE.



Figure A-7: Artist's rendering of the TESS spacecraft [10]

A.3 CCID-41

The section provides an overview of the Lincoln Laboratory CCID-41 detectors used on the REXIS instrument. The CCID-41 is a back illuminated (BI) CCD, meaning incident photons enter the back of the device to achieve the highest quantum efficiency possible [52]. The total size of the CCID-41 is 1024 columns of pixels x 1026 rows of pixels, but the bottom two rows (#1205 and #1026) exist to accommodate misalignment of the light shield used in the CCD mounting assembly . Thus the active imaging area of the CCID-41 is 1024 x 1024 pixels. The imaging array is divided into four “nodes” of 1026 pixels in height x 256 pixels in width each, for a total of 262,656 pixels per node (262,144 active pixels excluding the two bottom rows). Each serial register (Serial Register AB and Serial Register CD) has 520 pixels total, eight of which are the four additional pixels (sometimes called underclock pixels) at each serial register output, thus $256 * 2 = 512$, $512 + 8 = 520$.

A.3.1 Frame Store

The frame store provides a storage area for the camera electronics to readout the charge of each pixel in the framestore while the next image is ”integrating” on the imaging array. The framestore scheme allows the system to operate without a shutter [39]. Integration time is the amount of time the imaging array is exposed to external

radiation for charge collection. The CCID-41 frame store is divided into two sections, each 512 pixels in width by 1026 pixels in height.

A.3.2 Serial Register

Underclocks

As in earlier devices, Each CCID-41 output node includes four extra stages (extended register pixels) between the first column and the output gate. Image processing algorithms may use these "pre-scan" or "underclock" pixels values as a base reference for noise levels.

Bidirectional Readout

The serial register allows the controlling electronics to direct charge from two nodes to two output ports at either end of the register. Due to the bidirectional readout design, the readout electronics (frame grabber) must reverse the pixel order on two of the four nodes to reconstruct the image (usually Nodes B and D).

A.3.3 Output Stage

The CCID-41 output stage consists of a single-stage source follower with an off-chip load resistor that feeds the gate of a U309 which also is to be used in the follower mode. Both the first-stage load resistor and U309 are placed inside the package next to the CCD, but user must supply the U309 load resistor outside the package.

A.3.4 Charge Injection

The fundamental enhancement of the CCID-41 from its predecessor CCDs is the addition of a charge injection register at the top of the imager. This allows the controlling electronics to inject precise and uniform amounts of charge into each column to mitigate the effects of charge-transfer inefficiency, particularly for displacement damage

from radiation. The TESS DE did not include charge injection circuitry at the time the REXIS avionics team used the TESS DE for development.

A.4 TESS DE

This section presents the design, functionality, and operation of the TESS prototype Detector Electronics (DE), which the REXIS avionics team used for development efforts and testing with CCID-47 and CCID-41 detectors. The TESS DE provide readout control of up to four CCDs, frame transfer via the Camera Link format, and command/control via a UART interface. The readout electronics use the clamp/dual slope sampling method (correlated double sampling) to measure charge in each pixel of the CCD array, with heritage from ACIS on Chandra, the Soft X-ray Camera (SXC) on the High Energy Transient Explorer (HETE)-2 mission, and XIS on Suzaku. The TESS DE prototype unit consists of two PCBs: the driver board and the video board.

A.4.1 TESS Requirements

TESS science requirements dictate the readout electronics must readout an entire 16 megapixel frame once every 2 seconds. If the pixel charge measurement and readout were completed serially, then the pixel readout time would need to be less than or equal to 119 ns/pixel as shown in Equation A.1.

$$\frac{2 \text{ seconds}}{16 \text{ megapixels}} = 119 \text{ ns/pixel} \quad (\text{A.1})$$

However, the DE has the capability to readout 16 pixels simultaneously because it contains 16 separate video chains. This parallelization significantly reduces the pixel charge measurement time to 1.9 $\mu\text{s}/\text{pixel}$, as shown in Equation A.2.

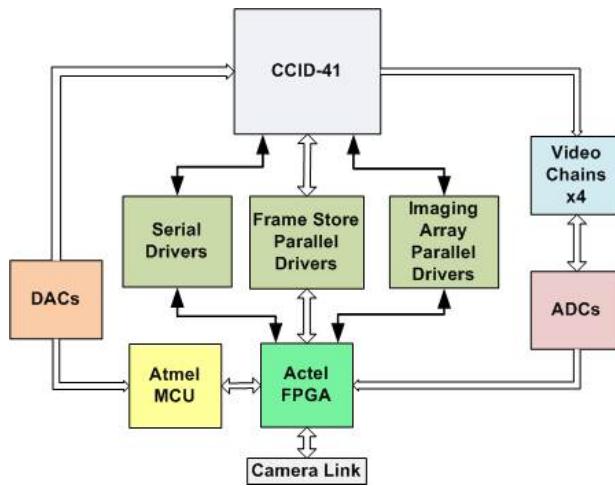
$$\frac{2 \text{ seconds}}{1 \text{ megapixel}} = 1.9 \mu\text{s}/\text{pixel} \quad (\text{A.2})$$

A pixel charge measurement period of 1.9 μs is significantly more feasible for the readout and processing electronics than 119 ns. Based on the decision to use

the Camera Link standard to output pixels to a frame grabber, 30 MHz is the base frequency from which the DE operates

Figure A-8 shows a diagram of the major functional blocks on the DE prototype unit.

Figure A-8: Detector Electronics functional block diagram



A.4.2 Driver Board

The DE driver board houses the Atmel microcontroller (MCU), Actel FPGA, serial and parallel clock regulators, and capacitor banks for parallel clocking (imaging area to framestore). Figure A-9 shows the driver PCB.

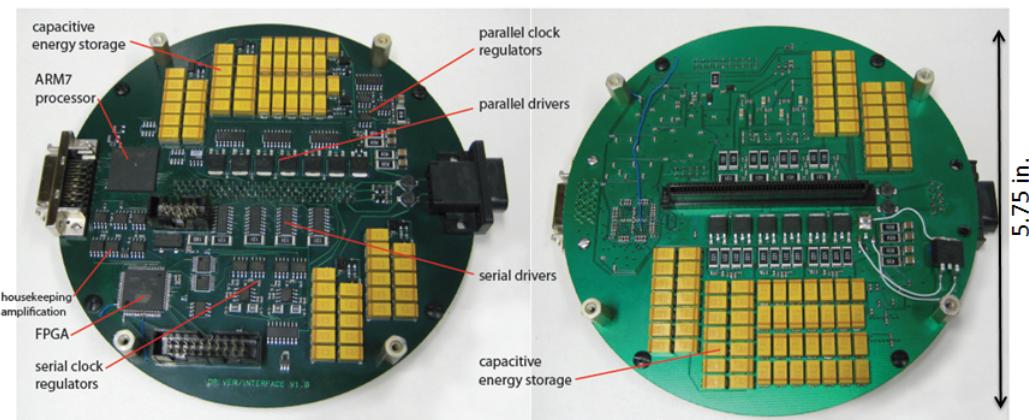


Figure A-9: Top (left) and bottom (right) sides of TESS prototype Detector Electronics driver board with major circuit components labeled

Atmel MCU

The Atmel MCU is the "brain" of the DE, as it receives commands and passes telemetry over the UART interface, controls the clock sequencer implemented on the Actel FPGA, sets the clock driver signal voltages, and manages housekeeping acquisition. LSE is used to program and interface with the Atmel MCU.

LSE LSE is a variant of the Forth programming language, first developed in 1802 machine language by Bob Goeke at MIT. Scientists and engineers in the MIT CCD lab were its main users. The version implemented on the Atmel MCU was coded in C by John Doty of Noqsi Aerospace.

Actel FPGA

Logic designs on an Actel ProASIC3 A3P600-FGG256 Flash-based FPGA mounted on the driver board provides the functionality below:

- Clock Sequencer (control lines to Driver)
- ADC Control (timing from Sequencer)
- Pixel word formatter (Camera Link Subsystem)
- 3.3V CMOS to 2.5V Low Voltage Differential Signaling (LVDS) conversion (Camera Link & Spare Control)
- LVDS Serializer

The clock sequencer on the Actel FPGA is the Trakimas-Larosa-Doty (TLD) sequencer, developed by Engineers at the then MIT Center for Space Research (now the Kavli Institute for Astrophysics and Space Research) in 2003 as a means to control CCD detectors in development [55].

A.4.3 Video Board

The video board houses the video measurement chains, along with op amps and multiplexers for temperature measurement and housekeeping voltage acquisition. Figure A-10 is a picture of the top side of the video board.

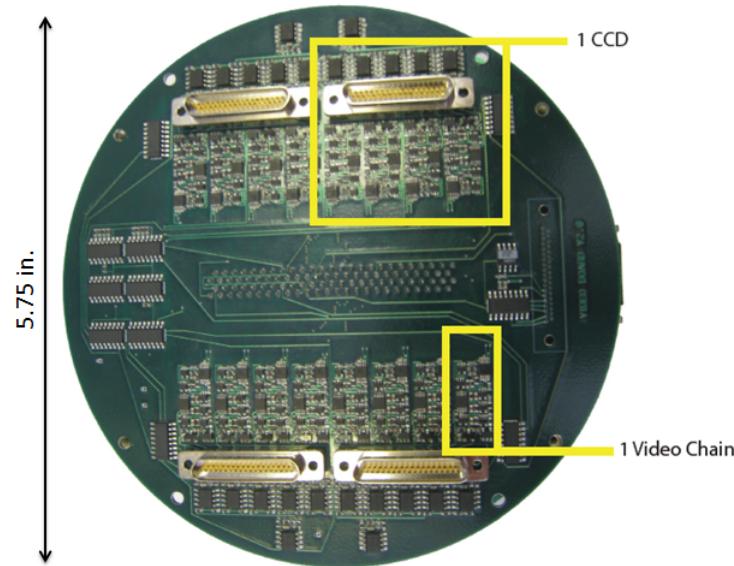


Figure A-10: Bottom side of TESS prototype Detector Electronics video board with video chain labeled

Video Chain

The video chains measure the analog signal output for each pixel from the CCD output nodes and convert them into digital signals for storage and image processing. There are 16 video chains on the video board, one for each node of four CCDs. The video chains use the clamp/dual slope method of measuring the charge stored in each pixel of a CCD.

Clamp/Dual Slope Sampling The clamp/dual slope sampling method combines the advantages of the clamp sampling and dual slope sampling methods, as shown in Figure A-11. Its advantages include good bandwidth/phase control, optimum rejection of white noise, near optimum rejection of flicker noise, excellent isolation between pixels as they are read out, immunity to DC drift, rejection of flicker

noise, absence of a critical integrate/deintegrate balance requirement, and sufficient processing speed. The clamp/dual slope sampling method has flight heritage on ACIS on Chandra, SXC on HETE-2, the star trackers on HETE-2, and XIS on Suzaku.

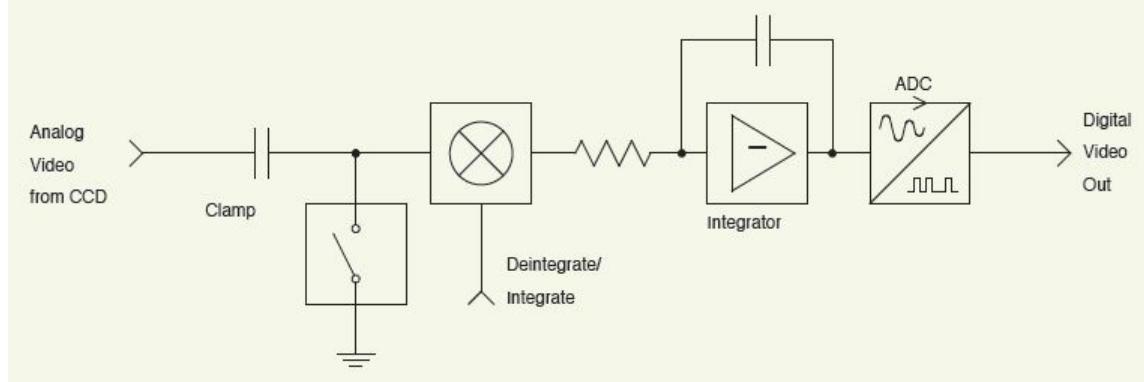


Figure A-11: Clamp/dual slope sampling method

Figure A-12 is a simplified schematic of each video chain (highlighted with yellow box and labeled in Figure A-10) that measures the charge of each pixel as it is output from the output gate via the serial register. The Int, Hold, and Clamp signal shown in Figure A-12 are the same measurement chain control signals appearing in the timing diagram shown in Figure A-13.

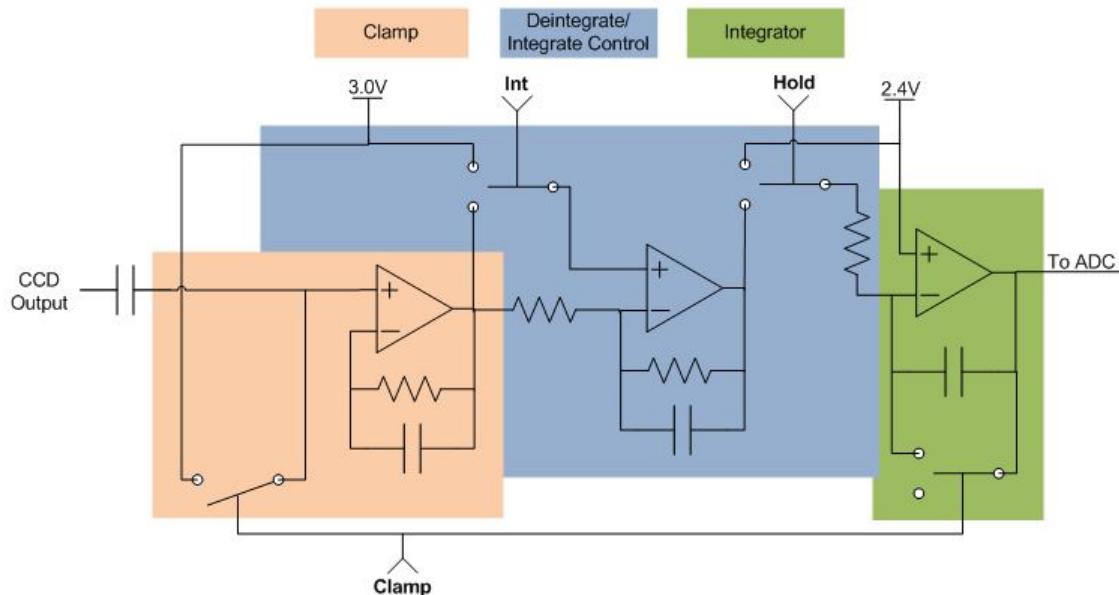


Figure A-12: Simplified video chain schematic with clamp and dual slope measurement components highlighted

The "pix" block in the LSE file example (shown in Section A.5) generates the signals shown in Figure A-13 to clock out and measure the charge in one CCD pixel. Additionally, the "pix", "pixA", and "pixB" blocks are contiguous in memory, meaning each time "pix" is executed, "pixA" and "pixB" are also executed. Since each pix block reads out and measures two pixels, the video chains readout a total of six pixels per node when the Atmel MCU directs the Actel FPGA to execute the "pix" block. The 6-pixel readout timing block is necessary because the step execution is constant within the Actel FPGA, and pixel readouts are 6 times faster than parallel transfer rates. Charge is inefficiently transferred if the parallel transfer rate is too high.

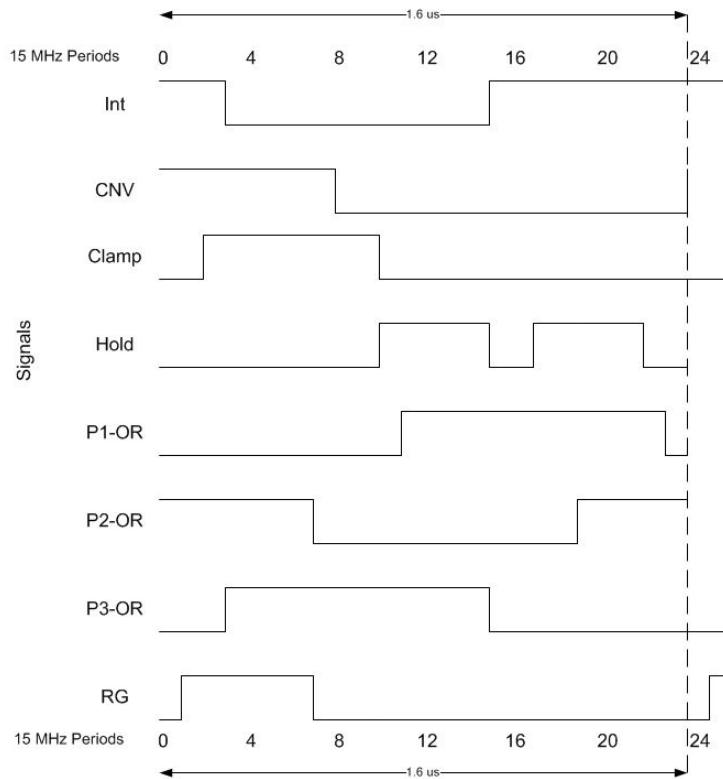


Figure A-13: CCD readout and measurement chain control signal timing shown relative to 15 MHz periods specified in LSE code

A.4.4 Frame Readout Via Camera Link

The DE outputs pixels using Camera Link protocol. For REXIS testing, the Frame Grabber custom hardware module implemented on the Virtex-5 FPGA receives the

pixels according to the Camera Link standard and then rearranges the pixel order to create a coherent image in SDRAM for later image processing.

Overclocks and Underclocks

During the course of a science run lasting some mission specific amount of time (from 1000 to 100,000 seconds on ACIS [39], for example), each pixel's bias values vary with slow changes in the DC level of the analog readout electronics. These variations are compensated by "overclocking" the CCD, i.e., reading pixels from the frame store that never received charge from imaging pixels [77]. These "overclock" or "overscan" pixels have no residual parallel clock artifacts. The average value of the overclock pixels will directly measure the change in DC level, and can therefore be used to correct it [77].

In the output of the DE to the frame grabber, the overclocks appear "after" the image pixels in each row of pixels read out, and the underclocks appear "before" the image pixels in each row. Figure A-14 shows this ordering. The number of overclocks is configurable in the LSE code used to program the Atmel MCU—four overclock pixels appear in Figure A-14.

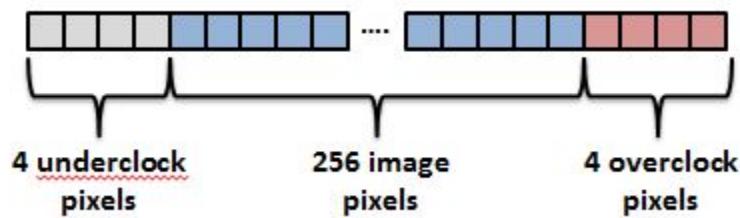


Figure A-14: Relative position of underclock pixels, image pixels, and overclock pixels in each row of DE frame readout

Frame Readout Timing

The following discussion of pixel readout format assumes a four CCID-41 array with CCID-41 dimensions of 1024 horizontal pixels x 1024 vertical pixels, 256 horizontal pixels per row, 4 underclock pixels per row, and 4 overclock pixels per row. Pixel

readout over the Camera Link Interface is based on pixel clusters of 16 pixels each, with each pixel being from one of the 16 nodes in the four CCD detector array. As shown in Figure A-15, the FPGA hardware reads in the measured value on a single pixel from each node in the four CCD detector array and places all 16 measured pixel values into a single pixel cluster for transmission via the Camera Link protocol.

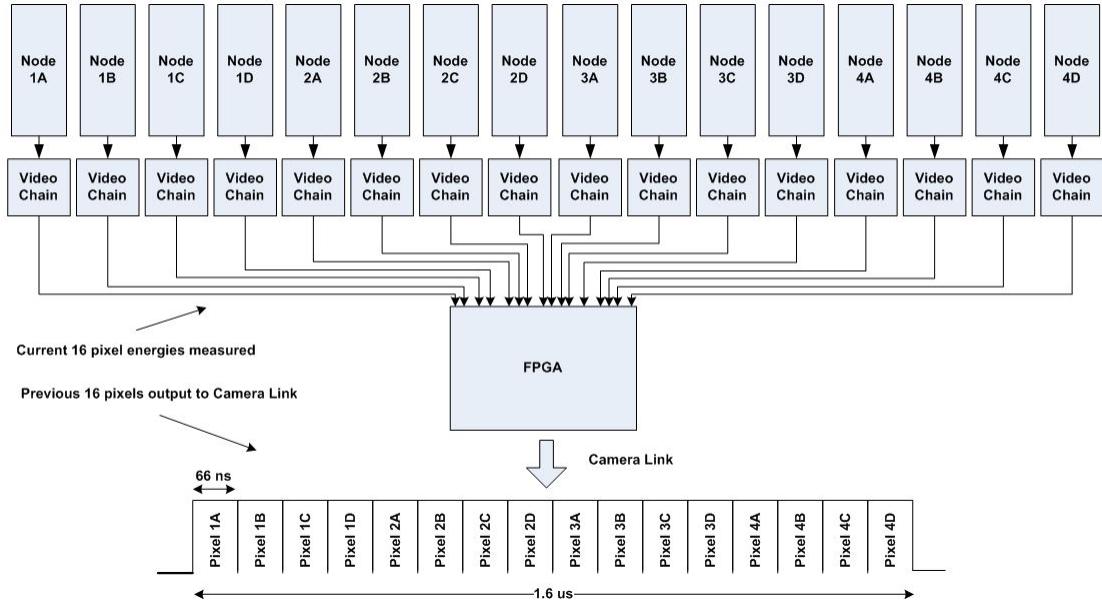


Figure A-15: Visualization of construction of a single pixel cluster of 16 pixel values

The transmit time duration of a single pixel cluster is $1.6 \mu s$. Since each row in each CCD node is effectively 264 horizontal pixels wide (4 underclock "pixels" + 256 image pixels + 4 overclock "pixels"), and each pixel cluster contains one pixel from each node, 264 pixel clusters are required to transfer an entire row from each node (16 total rows). The time required to transfer an entire row is given in Equation A.3

$$256 \text{ pixel clusters} * \frac{1.6 \mu s}{\text{pixel cluster}} = 422.4 \mu s \quad (\text{A.3})$$

After all of the pixels in each of the serial registers are measured and read out, the electronics transfer the next row of pixels from the frame store into the serial register, which requires $9.6 \mu s$ (the LSE commands for the frame store to serial transfer appear in the "fr2serial" block in the LSE example in Section A.5). Thus the total time to readout and transmit one row from each of the CCD nodes is $422.4 \mu s + 9.6 \mu s =$

432 μ s, and the total time to transfer an entire frame of 1024 is given in Equation A.4:

$$\frac{432 \mu\text{s}}{\text{row}} * \frac{1024 \text{ rows}}{\text{frame}} = \frac{442.368 \text{ ms}}{\text{frame}} \quad (\text{A.4})$$

The LSE command "row1 : serials1 pix ld_go 1 fr2serial ld_go" performs a measurement and readout of pixel values in the serial register for one row of each CCD node followed by a vertical transfer of pixels from the frame store to the serial register. The LSE command "serial_read1 : parallels1 row1 iterate" iterates the "row1" command "parallels1" times.

Table A.1: Execution timed for LSE blocks responsible for pixel readout and measurement

LSE Block	66.6 ns steps	Block execution time
interline	24	1.6 μ s
fr2serial	144	9.6 μ s
image2fr	121	8.066 μ s
pix	48	3.2 μ s

Readout Format

In Figure A-16, each node is labeled according to which CCD it belongs to in the four CCD detector array. For example, nodes 1A, 1B, 1C, and 1D are the four nodes of CCID #1 in the detector array. The horizontal arrows in Figure A-16 indicate the serial register output order for each node, while the vertical arrows represent the direction of row readouts as each row is transferred from the frame store to the serial register. In Figure A-16 and Table A.2, the "L" (i.e. "L1") stands for "Last" to indicate the last pixels in each node output during a frame readout.

Table A.2: Camera Link pixel output order, based on pixel numbers in Figure A-16

Pixel Cluster	Pixel Readout Order															
1st	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
2nd	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Last	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16

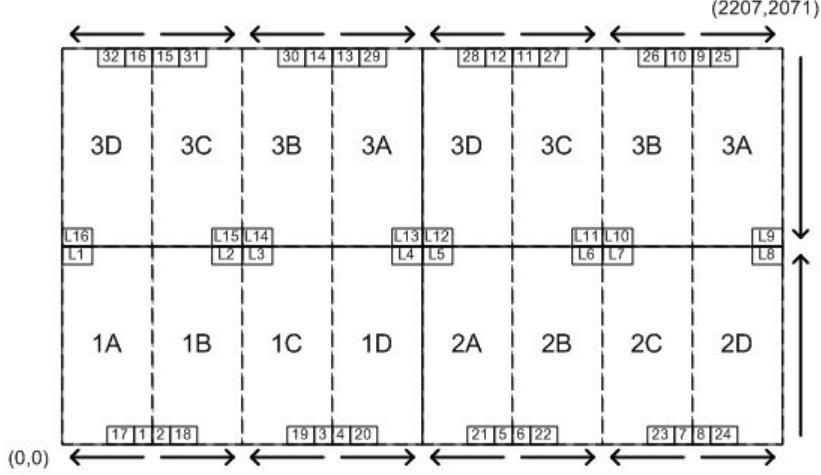


Figure A-16: Pixel cluster readout order, demonstrating bi-directional readout of each pair of serial registers

Figure A-17 shows the sequence of pixel clusters transfers that make up each row followed by the sequence of row transfers that make up a complete frame transfer via the Camera Link interface. In the Camera Link format, FVAL high indicates a pixel is valid within an image frame, LVAL high means a pixel is valid within a line (referred to as rows in CCD parlance), and DVAL is clock to signal the receiving device to accept a pixel value. The DVAL signal period is 66.6 ns, during which time the Camera Link data bits representing the pixel value are kept constant while DVAL change from high to low. [54]

A.4.5 Parallel Clocking

ASCA and ACIS employed parallel transfer rates of 20 - 100 kHz. Faster parallel transfer rates improve the duty cycle and reduce the number of misplaced photons. If no capacitor bank is present to store charge for parallel transfer, then the limiting factor of parallel clocking speed is the capacity of the power supply to provide the required current surge. The required current is calculated using Equation A.5 below:

$$I = C \times V \times A \times f \quad (\text{A.5})$$

where C is a process dependent constant, V is the voltage swing of the parallel

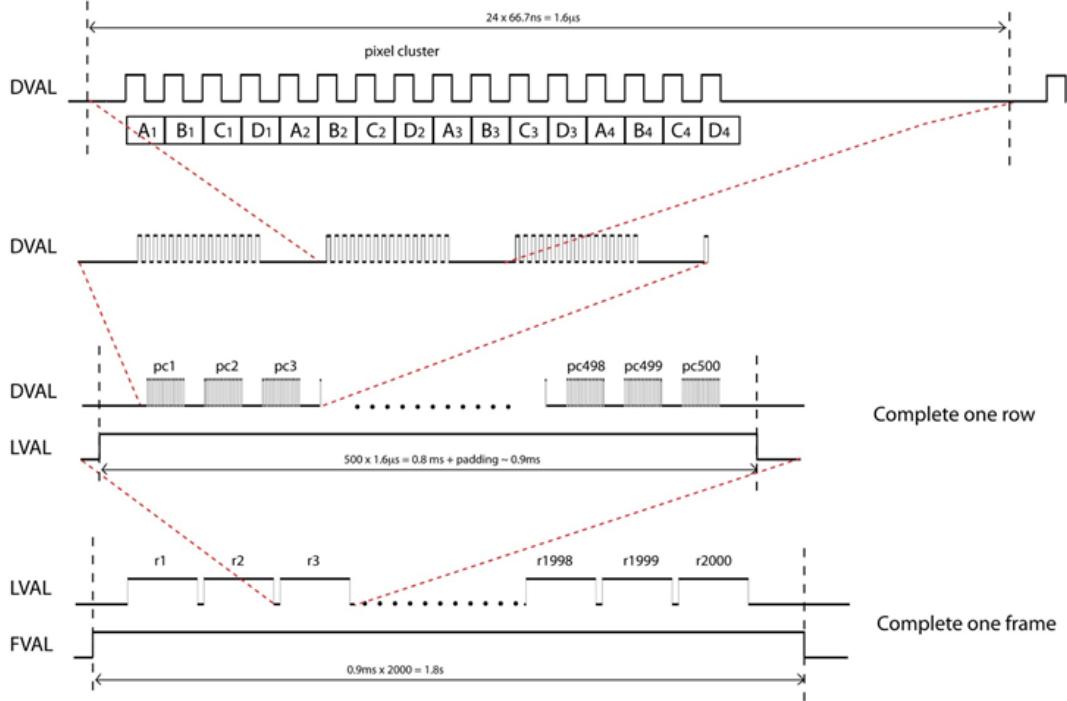


Figure A-17: Camera Link frame output order [54]

clock voltages, A is the total area of image and frame store regions of the CCD, and f is the parallel clock frequency.

A.5 LSE File Example

```

File{

step2 : 2 steps
step3 : 3 steps
step4 : 4 steps
step5 : 5 steps
step7 : 7 steps

pix :block{
    LVAL high FVAL high Int high CNV high step  \# A0 start new conversion
    RG high step                                \# 1
    Clamp high step                             \# 2
    P3-OR high Int low step                     \# 3
    step                                         \# 4
    step                                         \# 5
    step                                         \# 6
}
}

```

```

P2-OR low RG low step          \# 7
CNV low step                  \# 8
step                           \# 9 MSB shows up at ADC output
Clamp low Hold high step      \# 10
P1-OR high step               \# 11
step                           \# 12
step                           \# 13
step                           \# 14 Start integration
P3-OR low Hold low Int high step \# 15
step                           \# 16
Hold high step                \# 17
step                           \# 18
P2-OR high step               \# 19 Hold
step                           \# 20
step                           \# 21
Hold low step                 \# 22
P1-OR low step               \# 23
CNV high step                 \# 24 start new conversion
RG high step                  \# 25
Clamp high step               \# 26
P3-OR high Int low step       \# 27
step                           \# 28
step                           \# 29
step                           \# 30
P2-OR low RG low step          \# 31
CNV low step                  \# 32
step                           \# 33 MSB shows up at ADC output
Clamp low Hold high step      \# 34
P1-OR high step               \# 35
step                           \# 36
step                           \# 37
step                           \# 38 Start integration
P3-OR low Hold low Int high step \# 39
step                           \# 40
Hold high step                \# 41
step                           \# 42
P2-OR high step               \# 43 Hold
step                           \# 44
step                           \# 45
Hold low step                 \# 46
P1-OR low step               \# 47
}block

```

```

pixA :block{
    LVAL high FVAL high Int high CNV high step  \# A0 start new conversion

```

RG high step	\# 1
Clamp high step	\# 2
P3-OR high Int low step	\# 3
step	\# 4
step	\# 5
step	\# 6
P2-OR low RG low step	\# 7
CNV low step	\# 8
step	\# 9 MSB shows up at ADC output
Clamp low Hold high step	\# 10
P1-OR high step	\# 11
step	\# 12
step	\# 13
step	\# 14 Start integration
P3-OR low Hold low Int high step	\# 15
step	\# 16
Hold high step	\# 17
step	\# 18
P2-OR high step	\# 19 Hold
step	\# 20
step	\# 21
Hold low step	\# 22
P1-OR low step	\# 23
CNV high step	\# 24 start new conversion
RG high step	\# 25
Clamp high step	\# 26
P3-OR high Int low step	\# 27
step	\# 28
step	\# 29
step	\# 30
P2-OR low RG low step	\# 31
CNV low step	\# 32
step	\# 33 MSB shows up at ADC output
Clamp low Hold high step	\# 34
P1-OR high step	\# 35
step	\# 36
step	\# 37
step	\# 38 Start integration
P3-OR low Hold low Int high step	\# 39
step	\# 40
Hold high step	\# 41
step	\# 42
P2-OR high step	\# 43 Hold
step	\# 44
step	\# 45

```

Hold low step          \# 46
P1-OR low step        \# 47
}block

pixB :block{
    LVAL high FVAL high Int high CNV high step  \# A0 start new conversion
    RG high step          \# 1
    Clamp high step       \# 2
    P3-OR high Int low step \# 3
    step                  \# 4
    step                  \# 5
    step                  \# 6
    P2-OR low RG low step \# 7
    CNV low step          \# 8
    step                  \# 9 MSB shows up at ADC output
    Clamp low Hold high step \# 10
    P1-OR high step        \# 11
    step                  \# 12
    step                  \# 13
    step                  \# 14 Start integration
    P3-OR low Hold low Int high step \# 15
    step                  \# 16
    Hold high step         \# 17
    step                  \# 18
    P2-OR high step        \# 19 Hold
    step                  \# 20
    step                  \# 21
    Hold low step          \# 22
    P1-OR low step          \# 23
    CNV high step          \# 24 start new conversion
    RG high step          \# 25
    Clamp high step        \# 26
    P3-OR high Int low step \# 27
    step                  \# 28
    step                  \# 29
    step                  \# 30
    P2-OR low RG low step \# 31
    CNV low step          \# 32
    step                  \# 33 MSB shows up at ADC output
    Clamp low Hold high step \# 34
    P1-OR high step        \# 35
    step                  \# 36
    step                  \# 37
    step                  \# 38 Start integration
    P3-OR low Hold low Int high step \# 39

```

```

step                                \# 40
Hold high step                      \# 41
step                                \# 42
P2-OR high step                     \# 43 Hold
step                                \# 44
step                                \# 45
Hold low step                       \# 46
P1-OR low step                      \# 47
}block

```

transfer one row into the serial register

```

fr2serial :block{
LVAL low FVAL high P1-IA low P1-FS low step2 \# 0
Clamp high step                      \# 2
Int low step7                         \# 3
Clamp low Hold high step5            \# 10
Int high Hold low step2              \# 15
Hold high step                        \# 17
P1-OR high step4                     \# 18
Hold low step2                        \# 22
P3-IA high P3-FS high step2          \# 24
Clamp high step                      \# 26
Int low step7                         \# 27
Clamp low Hold high step5            \# 34
Int high Hold low step2              \# 39
Hold high step5                       \# 41
Hold low step2                        \# 46
P2-IA low P2-FS low step2             \# 48
Clamp high step                      \# 50
Int low step7                         \# 51
Clamp low Hold high step5            \# 58
Int high Hold low step2              \# 63
Hold high step5                       \# 65
Hold low step2                        \# 70
P1-IA high P1-FS high step2          \# 72
Clamp high step                      \# 74
Int low step7                         \# 75
Clamp low Hold high step5            \# 82
Int high Hold low step2              \# 87
Hold high step5                       \# 89
Hold low step2                        \# 94
P3-IA low P3-FS low step2             \# 96
Clamp high step                      \# 98
Int low step3                         \# 99

```

```

P1-OR low step4          \# 102
Clamp low Hold high step5      \# 106
Int high Hold low step2      \# 111
Hold high step5          \# 113
Hold low step2           \# 118

P2-IA high P2-FS high step2
Clamp high step          \# 122
Int low step7            \# 123
Clamp low Hold high step5 \# 130
Int high Hold low step2   \# 135
Hold high step5          \# 140
Hold low step2           \# 142

}block

# fast transfer from image section to frame store

interline :block{
    LVAL low FVAL high step \# 0
    step                  \# 1
    step                  \# 2
    step                  \# 3
    step                  \# 4
    step                  \# 5
    step                  \# 6
    step                  \# 7
    CNV low Clamp high step \# 8
    step                  \# 9
    step                  \# 10
    Clamp low Hold high step \# 11
    step                  \# 12
    step                  \# 13
    step                  \# 14
    Int low step          \# 15
    step                  \# 16
    step                  \# 17
    step                  \# 18
    Hold low Int high step \# 19
    step                  \# 20
    step                  \# 21
    step                  \# 22
    step                  \# 23

}block

image2fr :block{
    FVAL low LVAL low CNV high P1-IA low P1-FS low P1-OR low RG high pstep \# 0

```

```

P3-IA high P3-FS high P3-OR high pstep      \# 24
CNV low P2-IA low P2-FS low P2-OR low pstep  \# 48
P1-IA high P1-FS high P1-OR high pstep      \# 72
P3-IA low P3-FS low P3-OR low pstep         \# 96
P2-IA high P2-FS high P2-OR high pstep      \# 120
}block

# readout pixels from all four nodes "ffff"
2 \ ffff writeSeq
44 serials1 :constant
1024 parallels1 :constant
frame_delay1 : 100000 usec iterate

row1 : serials1 pix ld_go 1 fr2serial ld_go
serial_read1 : parallels1 row1 iterate
raster1 : frame_delay1 parallels1 image2fr ld_go serial_read1 frame_delay
run1 : raster1 iterate
g1 : 1 run1
go1 : g1 repeat

}File

```


Appendix B

Solar X-ray Monitor Design

This appendix details the REXIS Solar X-ray Monitor (SXM) design. It begins with a brief background on the science motivation for the SXM in the REXIS system and estimates of the solar x-ray flux the SXM will be required to measure during the mission. Next, the design of each of the major electronics circuits constituting the SXM is presented. The schematics presented in this appendix correspond to the REXIS SXM Engineering Test Unit (ETU) design, which is separate from the REXIS SXM electronics design on the MEB appearing in Appendix C, although the SXM electronics on the MEB are closely based on the SXM ETU design. This appendix closes with test results for the REXIS SXM ETU PCB.

B.1 Overview

The REXIS SXM ETU design consists of an Amptek Silicon Drift Diode (SDD) with built-in thermoelectric cooler (TEC), a preamplifier, supporting measurement and control electronics, and an FPGA interface. Figure B-1 shows a diagram with each of these primary component groups labeled in the REXIS Engineering and Flight Model configuration. In the SXM ETU, measurement and control electronics sit on the SXM ETU PCB with a connector to the Virtex-5 ML507 development board for the FPGA interface, and the SDD/TEC and preamplifier sit on a separate PCB with two separate connectors to the SXM ETU PCB. In the REXIS Engineering and Flight

Models, the measurement and control electronics sit on the REXIS MEB along with the Virtex-5 FPGA, while the SDD/TEC package and preamplifier, shown in Figure B-2, sits on a different face of the OSIRIS-REx spacecraft than the main REXIS instrument. In Figure B-2, the MDM9 connector (labeled “AXON”) provides power and interface control signals, while the SMA connector carries the analog output of the preamplifier to the measurement electronics on the MEB.

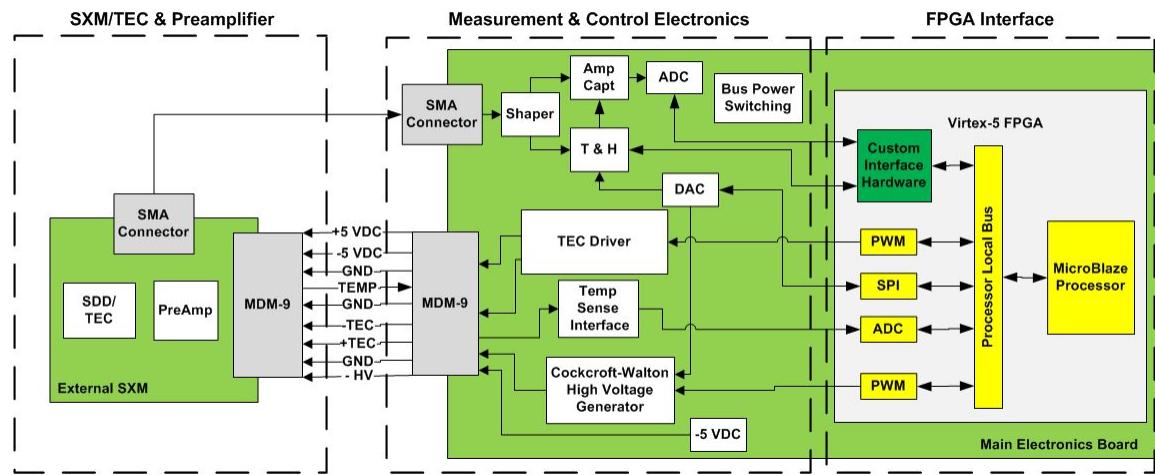


Figure B-1: Solar X-ray Monitor functional block diagram



Figure B-2: CAD rendering of REXIS SDD/TEC and preamplifier inside aluminum housing

B.1.1 Science Motivation

REXIS maps the asteroid Bennu (formerly 1999 RQ36) by using the Sun as an X-ray source to illuminate Bennu, which absorbs these X-rays and fluoresces its own X-rays based on the chemical composition of the asteroid surface. However, solely pointing the REXIS CCD detectors at the asteroid and identifying, for example, a

very bright or very dim section on the surface map could lead project scientists to incorrectly interpret the data; these sections result from a compositional change in the asteroid regolith or from solar variability providing more or less-than-expected illumination of the asteroid. To provide context for the data collected with the CCD detectors, REXIS will support the SXM to measure the x-ray spectrum of the Sun during REXIS operation. [46]

The SXM measurements allow for decoupling of solar activity from the collected CCD data and facilitate production of maps of RQ36 that are independent of the number of X-rays incident on the asteroid. Some of the solar x-rays also will reflect off the asteroid into REXIS CCDs and imprint the solar spectrum onto the CCD data. This imprinting will appear as systematic noise scientists can subtract out with knowledge of the Sun's activity at the time REXIS measured the CCD data. The SXM also provides solar variability data of general scientific interest and of interest to other teams on the OSIRIS-REx project. While data from the Geostationary Operational Environmental Satellites (GOES) or ground measurements of the Sun's activity taken on Earth could be used for any of the project's needs, including a spectrometer on the OSIRIS-REx satellite itself allows for accurate measurements of solar spectra at the asteroid location. As an added bonus, scientists could use REXIS SXM data to verify models of the Sun's radiation at distances between the orbits of Earth and Mars. [46]

Given the desired energy measurement range of the SXM is approximately 10 keV, which corresponds closely to the sensitive range of the REXIS CCD detectors, and the required SXM resolution is 0.03125 keV, 320 energy bins are required to produce a histogram of solar x-rays incident on the SXM. Figure B-3 is a plot of estimated photon count vs. energy the Sun will produce during REXIS operation. The curves represent the current best estimate of quantum efficiency for 26 days of accumulation. The vertical orange dashed lines indicate spectral lines for Iron, Magnesium, Aluminum, Silicon, and Sulfur, and the Oxygen spectral line is not shown.

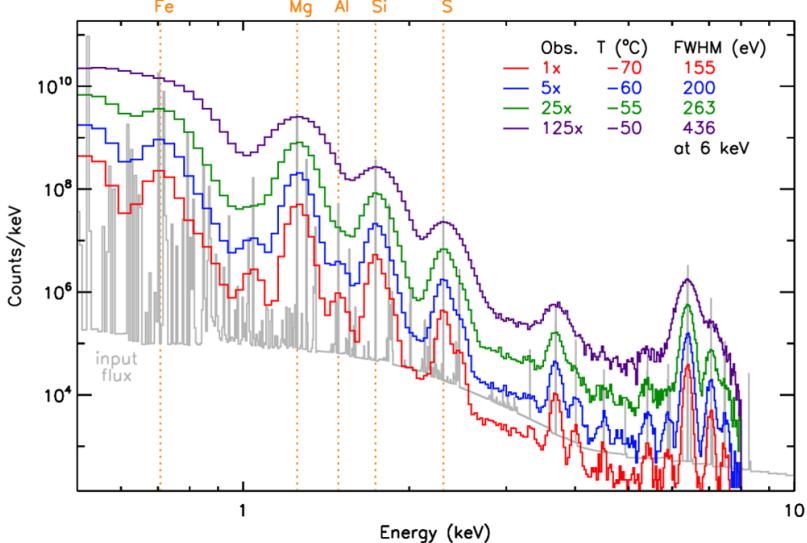


Figure B-3: Solar spectral model simulated histogram using chondrite spectrum and experimental data

B.1.2 NICER Heritage

The REXIS SXM design draws on heritage from the detector system design of the Neutron Star Interior Composition Explorer (NICER) program. NICER is a NASA Explorer Mission of Opportunity designed to study the gravitational, electromagnetic, and nuclear-physics of neutron stars [41]. The NICER design consists of 56 Amptek SDDs along with signal shaping and processing circuitry [71]. By studying the timing and spectroscopic properties of X-ray millisecond pulsars, NICER will allow scientists to infer the masses and radii of neutron stars [71]. At the time of this writing, NASA had selected NICER for launch to the ISS in December of 2016 with a planned mission life of 18 months.

The primary difference between the NICER Measurement/Power unit (MPU)[56] electronics design (which forms the basis for the REXIS SXM electronics design) is NICER's requirement to measure both the energy and arrival time of each x-ray photon striking the Amptek SDD. REXIS science calibration requires only measurement of the energy of each x-ray photon incident on the SDD.

B.2 SSD and Preamplifier

The REXIS SSD is the Amptek XR100SDD, a 25 mm^2 detector with a thin aluminized entrance window for good low energy response. Each detector is mounted on a thermoelectric cooler, which maintains the detector at approximately negative 60° Celsius while the package is at room temperature. Figure B-4 shows the structure of the Amptek SSD and TEC package.

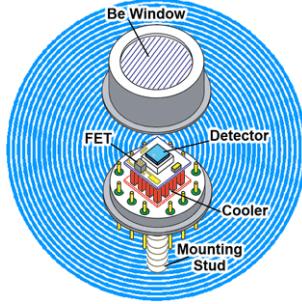


Figure B-4: Amptek AXR SSD, showing Beryllium window on metal housing, Thermoelectric Cooler, and pins for electrical interface on mounting [20]

The SSD silicon structure includes a classic series of p+ rings on a high resistivity n-type substrate. Applying higher voltages to the more remote rings creates a potential gradient in the radial direction, guiding signal electrons to a very small, low capacitance anode in the center. The detector anode is connected to the input of charge sensitive amplifier which converts signal electrons generated by an X-ray photon into a voltage step [71], as shown in Figure B-5. The voltage step is proportional to the energy deposited by a photon incident on the SDD. As opposed to conventional photodiodes, which use two planar contacts for cathode and anode, the SDD uses a single small anode. The anode's small area significantly decreases the input capacitance, which decreases the overall noise in the detector's measurements [8].

B.2.1 Preamplifier Circuit

The preamplifier amplifies the voltage output of the SDD/TEC packages's internal JFET. The JFET on the SDD/TEC package collects the signal current generated by

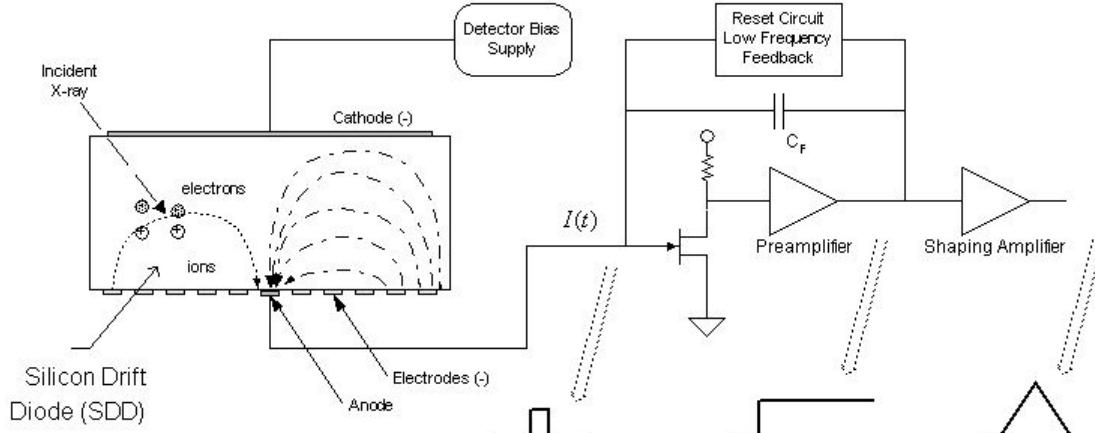


Figure B-5: Amptek SDD operation and signal processing flow [8]

an x-ray strike on the SDD.

B.3 Measurement Electronics

To measure the energy of each photon incident on the SDD, the SXM design combines a shaper circuit, trigger circuit, and amplitude capture circuit to form a measurement chain. The measurement chain feeds an ADC to convert the analog voltage representative of an x-ray event into a digital value for histogram binning.

B.3.1 Shaper Circuit

The shaper circuit (Figure B-6) shapes the analog signal output of the preamplifier to facilitate measurement of the peak energy of an x-ray incident on the SDD, as well as removing high frequency noise generated by the preamplifier. Passing the preamplifier output through a low pass filter smooths out the noise and produces a step—the step’s rate of rise is proportional to the charge pulse generated by a photon on the SDD. Differentiating the step produces a pulse with height proportional to the charge. Differentiating a second time produces a signal crossing zero at the time the charge pulse occurs on the SDD, delayed by the filter group delay, other amplifier delay, and cable delays. [56]

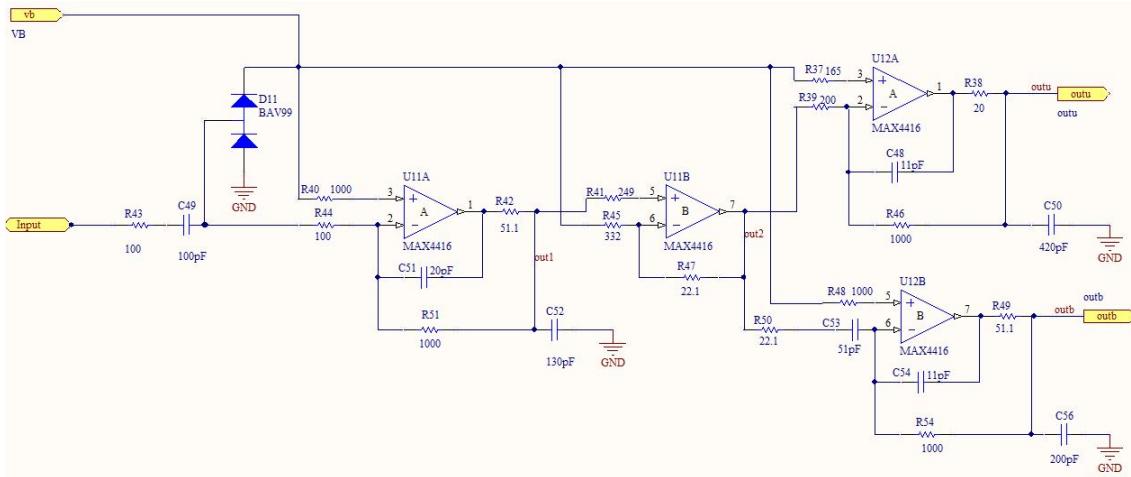


Figure B-6: Schematic of SXM ETU shaper circuit

B.3.2 Trigger Circuit

The trigger circuit detects when the preamplifier output is above the event threshold (configurable in software), which corresponds to an X-ray strike on the SDD. It also detects the moment of maximum energy when FSW should sample the shaper first derivative output (*outu*) read by the ADC, based on the second derivative output (*outb*) of the shaper circuit. FSW then stores the ADC digital output value in the appropriate histogram bin.

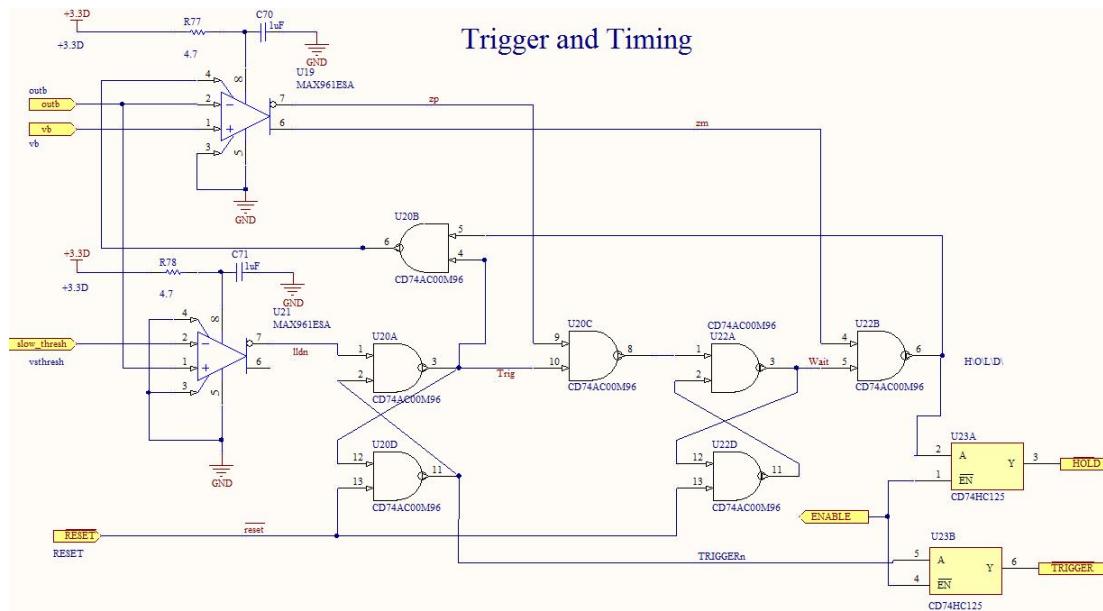


Figure B-7: Schematic of SXM ETU trigger circuit

As shown in Figure B-7 two S/R latches along with the internal latch in the U19 comparator form a state machine to detect threshold crossing and peak energy. In the normal inactive state, *Trig* and *Wait* are inactive (low), and \overline{TRIG} and \overline{HOLD} are also inactive (high). When the second derivative from the shaper (*outb*) exceeds the low level threshold (*slow_thresh*), *lldn* goes low and forces *Trig* high. When *Trig* goes high, the latch feature of U19 is disabled. Next, when U7 asserts *zp*, which normally occurs within a few nanoseconds since the *outb* signal should be above *vb*, *Wait* goes high and arms the zero crossing detection. When *outb* crosses *vb* (analogous to crossing zero), U7 asserts the *zm* signal, which asserts \overline{HOLD} (low) and reenables the latch function of U7. [56] When the trigger circuit asserts *HOLD*, FSW should read the voltage on the ADC inputs and store it in the appropriate energy bin.

When FSW asserts the \overline{RESET} signal (low), both \overline{TRIG} and \overline{HOLD} deassert (both high). If *lldn* is high (meaning no pulse is in progress), asserting \overline{RESET} fully resets the state machine to the inactive state. If *lldn* is high when FSW asserts \overline{RESET} (meaning a pulse is in progress), then the state machine will immediately assert \overline{TRIG} and arm the zero crossing detection. This design ensures the trigger logic can cleanly capture a photon pulse that begins before \overline{RESET} deasserts, so long as the pulse is above the low level threshold (*slow_thresh*) when FSW deasserts \overline{RESET} . [56]

Based on the possibility of erroneous states, FSW should assert \overline{RESET} if the trigger circuit asserts *HOLD* without first asserting $\overline{TRIGGER}$. FSW should also assert \overline{RESET} after changing the low level threshold (*slow_thresh*).

B.3.3 Amplitude Capture

The amplitude capture circuit stores the voltage corresponding to the maximum energy for an X-ray event across a capacitor. The voltage is stored when the trigger module asserts the Hold signal. As shown in the amplitude capture module circuit schematic in Figure B-8, R2 delays the charging of C2 slightly to compensate for delays in the HOLD signal. Zero amplitude corresponds to the *vb* voltage value (approximately 1.2V). Employing a balanced differential configuration with the *PH+*

and $PH-$ signals cancels charge injection from the switch and output drift due to op amp bias current. The outputs of the amplitude capture circuit $PH+$ and $PH-$ feed the differential inputs of the AD7984 ADC used to digitize the $outu$ signal from the shaper representing the photon energy. [56]

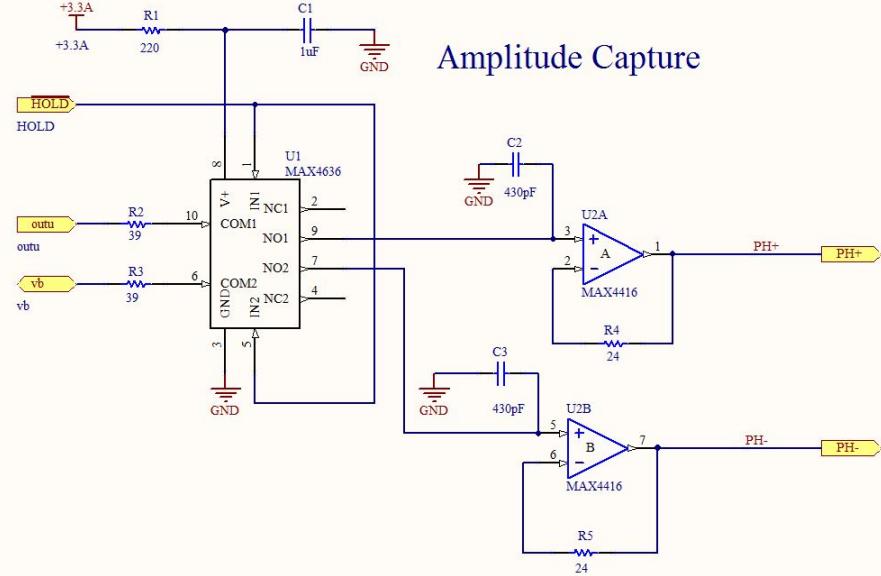


Figure B-8: Schematic of SXM ETU amplitude capture circuit

B.4 Control Electronics

B.4.1 Threshold Control

Dual diode D13 serves as a quiet, approximately 1.2V, bias voltage source (vb), while op amp U18A translates the $VLLD$ ground-referenced input from the DAC to input levels relative to the 1.2V bias, vb [56], as shown in Figure B-9.

B.4.2 TEC Driver

The REXIS FSW and controlling electronics must control the voltage across the inputs of the TEC on the Amptek SDD module in order to maintain a sufficiently cold SDD temperature for effective operation. The TEC driver is a buck switching

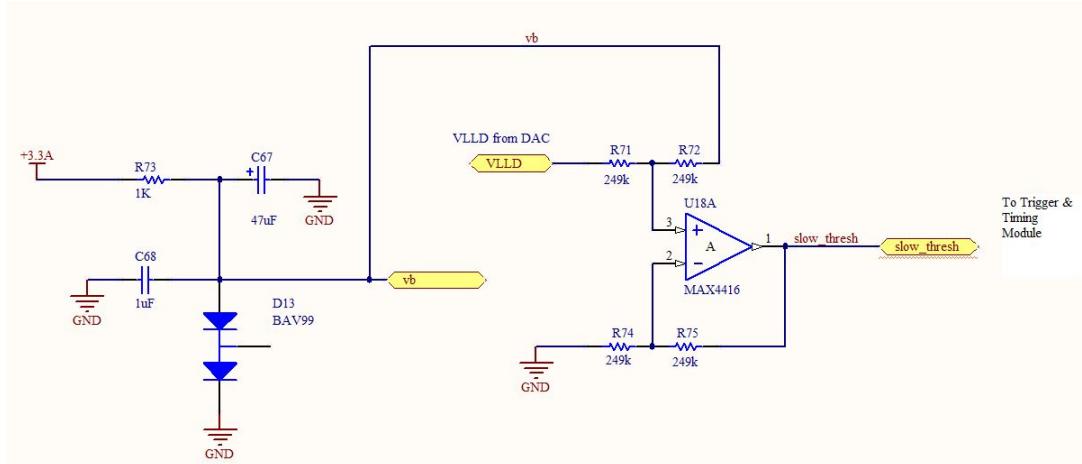


Figure B-9: Schematic of SXM ETU threshold control circuit

power converter implementing Pulse Width Modulation (PWM) of the input voltage from the spacecraft.

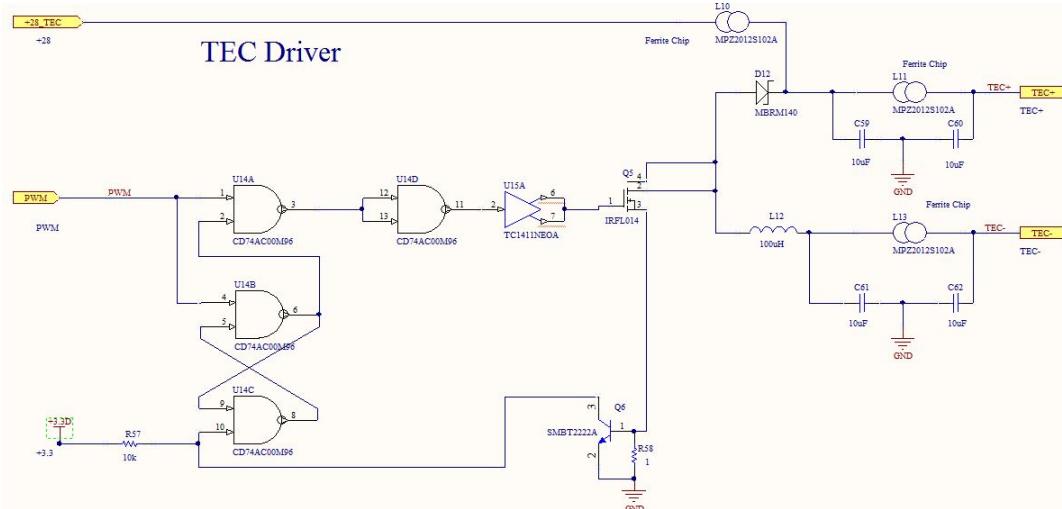


Figure B-10: Schematic of SXM ETU TEC driver circuit

If the switch current exceeds $\approx 0.25\text{A}$, Q6 turns on and causes the U14 NAND gate to turn off the PWM drive to the MOSFET. PWM pulse widths should be substantially shorter than $1\mu\text{s}$ and much longer than the 25ns switching time of the MOSFET driver U15. [56]

B.4.3 Cockcroft-Walton High Voltage Generator

The Cockcroft-Walton High Voltage Generator provides the negative high voltage (≈ -115 V) bias for the SDD. The input PWM from the FPGA (controlled by FSW) is nominally 32 kHz. As shown in Figure B-11 double pole single throw (DPST) switch U5 slices and dices the nominally 28V input to drive a six stage Cockcroft-Walton voltage multiplier. The resistors around U5 prevent destructive current surges on start-up and protect against SEL, while R25 and C25 reduce ripple of the raw input supply voltage. High voltage transistors Q3 and Q4 form an amplifier with a gain $\approx R24/R15$, which is ≈ 100 . Feedback from the U4A op amp's output through R21 regulates the output of the circuit, while U4B provides a significantly attenuated and inverted housekeeping voltage for flight software to monitor the Cockcroft-Walton's high voltage output. The Cockcroft-Walton circuit provides a regulated output voltage range from 0V to -127V. [56]

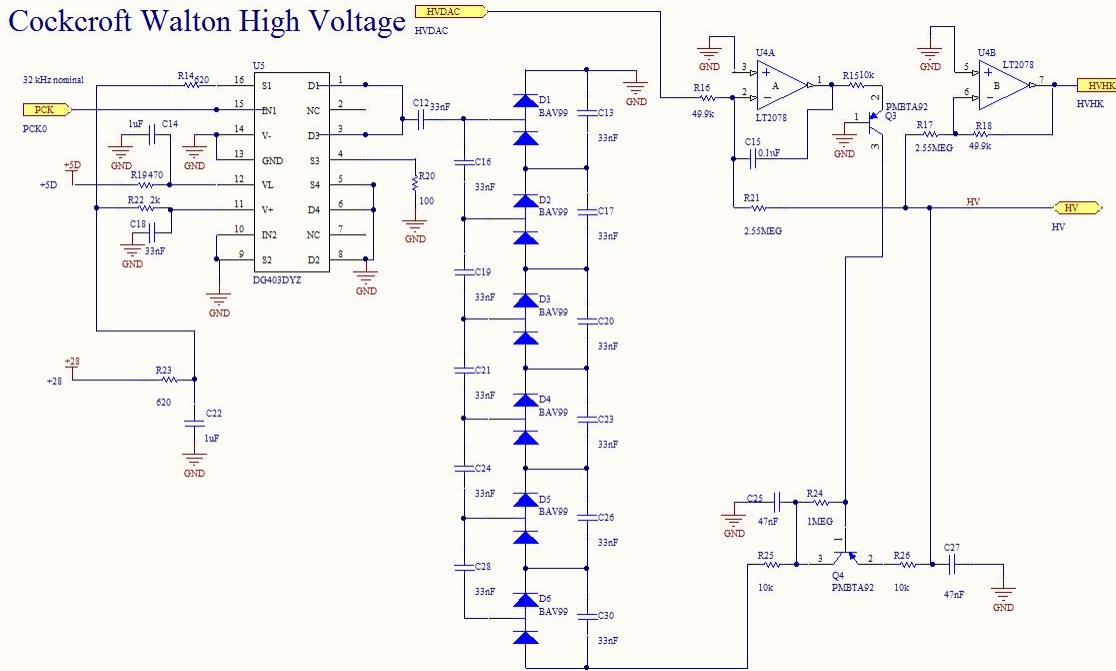


Figure B-11: Schematic of SXM ETU cockcroft walton high voltage generator circuit

Although the SXM ETU was designed to receive a regulated 28V input similar to the NICER MPU design, the SXM electronics design on the REXIS MEB was designed to receive the unregulated spacecraft input voltage from the OSIRIS-REx

interface. This input voltage can range between 26 and 34 VDC, which requires REXIS FSW to actively monitor the high voltage output via the *HVK* signal.

B.4.4 SSD Temperature Interface

The Amptek SSD contains a silicon diode to serve as a temperature sensor, thus providing feedback to FSW for controlling the TEC driver PWM. Forward voltage of the SSD diode is typically 600 mV at 25° Celsius and low current, changing $\approx -2\text{mV}/\text{K}$. The U16A and U16B op amps serve as a 100 mA current source to the diode. The U17A op amp buffers and amplifies the diode voltage. Over an input range of 0.45V to 0.9V, U34A will output 0V to 3V, which nominally corresponds to 375K to 150K. [56]

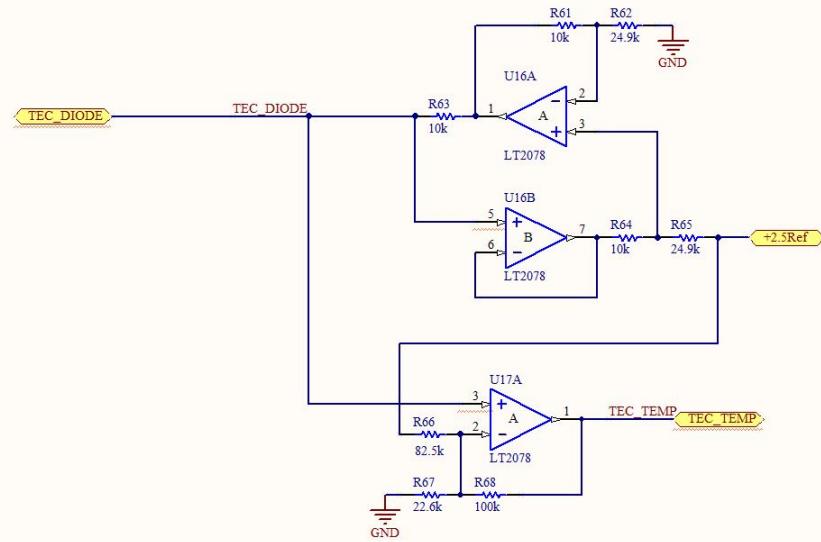


Figure B-12: Schematic of SXM ETU SSD temperature interface circuit

B.5 FPGA Interface

For the REXIS SXM system on the REXIS EM, the custom hardware module on the Virtex-5 FPGA will provide 320 energy bins of 32 bits each in order to record the number of events detected in each energy bin during the histogram update period

(integration time of the SXM). The histogram update period is configurable by FSW command, with the baseline value set to 100 seconds.

Each time the measurement chain detects an event above the low level threshold, the custom hardware module commands the ADC to read the voltage on its inputs, records the ADC's digital output, and increments the 32-bit count of the histogram bin into which the measured voltage (corresponding to photon energy) falls.

B.6 SXM Electronics Testing

This section documents lab bench testing of the REXIS SXM ETU PCB. At the time of this writing, test of the SXM ETU PCB with external SDD/TEC and preamplifier under Iron-55 irradiation had not yet taken place.

B.6.1 Shaper

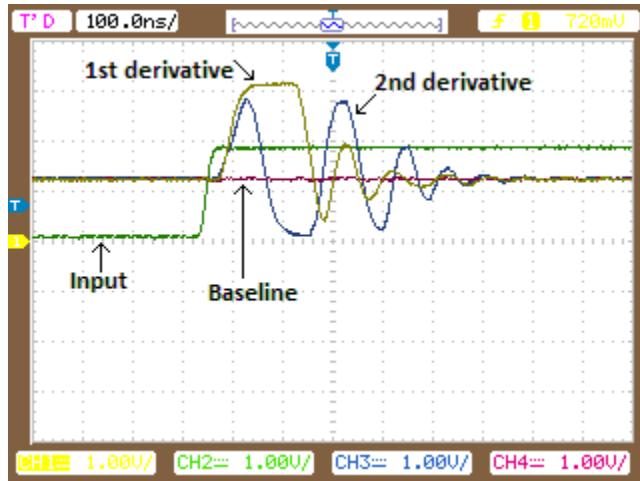


Figure B-13: SXM waveforms captured on oscilloscope during testing

Figure B-13 shows the first derivative (out_u) signal labeled as "1st derivative" and second derivative (out_b) signal labeled as "2nd derivative" from the shaper circuit following a step-like input signal labeled "Input." The first derivative signal peaks with the peak input voltage, and the second derivative crosses zero as the 1st derivative peaks, demonstrating the correct waveforms for capture of the peak value of the input

signal. The signal labeled "Baseline" is vb signal, approximately 1.2V. Due to the magnitude of the signal labeled "Input," some clipping is evident on the 1st derivative signal. The input voltage used in testing (approximately 2V) was significantly higher than the voltages which x-ray photons of 10 keV in energy or less are expected to produce.

Figure B-14 shows the \overline{HOLD} signal asserting (low) correctly just after the zero crossing of the second derivatives signal ($outb$) from the shaper circuit, with the delay resulting from the switching time of comparators. At the moment \overline{HOLD} asserts (low), FSW should command a read of the ADC and bin the measured voltage output of the ADC.

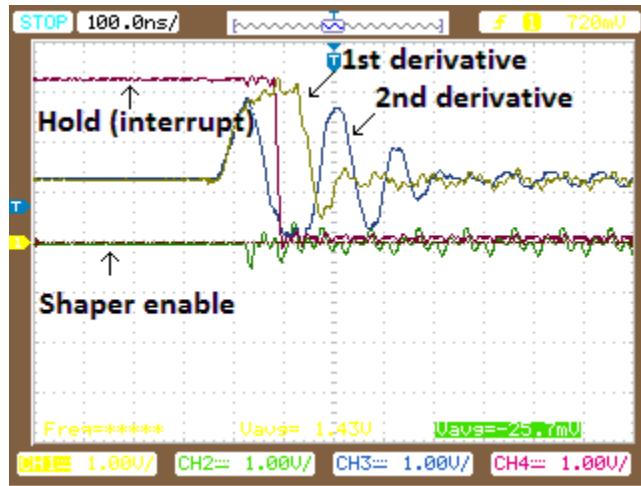


Figure B-14: SXM waveforms captured on oscilloscope during testing, showing assertion of hold signal

B.7 SXM ETU PCB

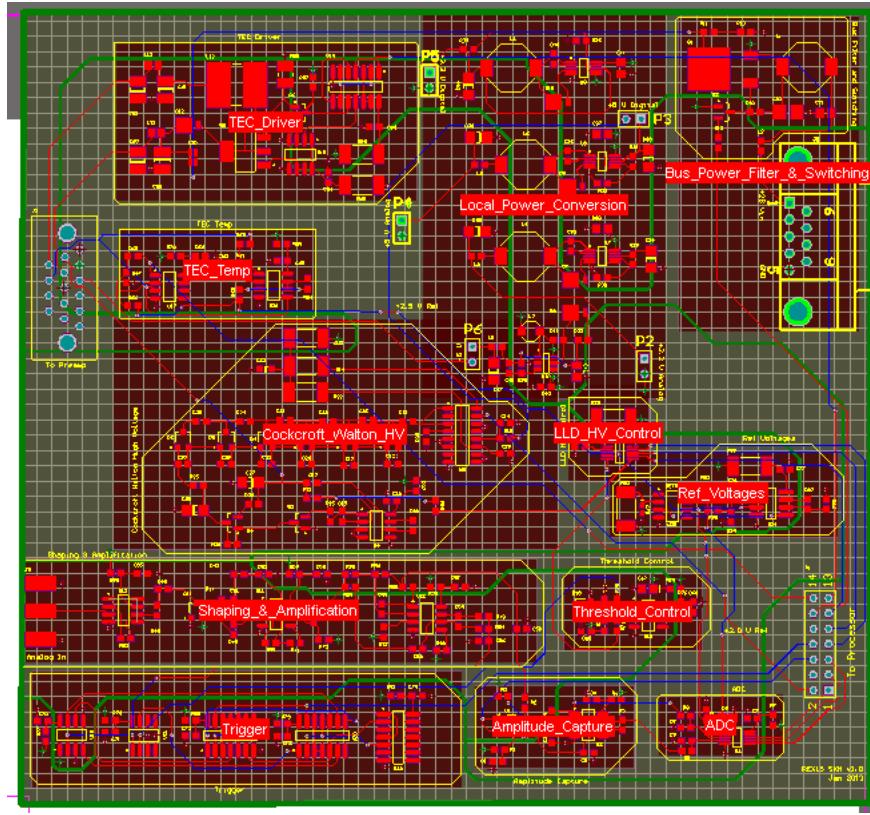


Figure B-15: SXM ETU PCB version 1.0

Appendix C

REXIS MEB Schematics

The following figures are the detailed schematic designs for the REXIS Engineering Model Main Electronics Board, the design of which appears in Chapter 4.

C.1 Engineering Model MEB Schematics

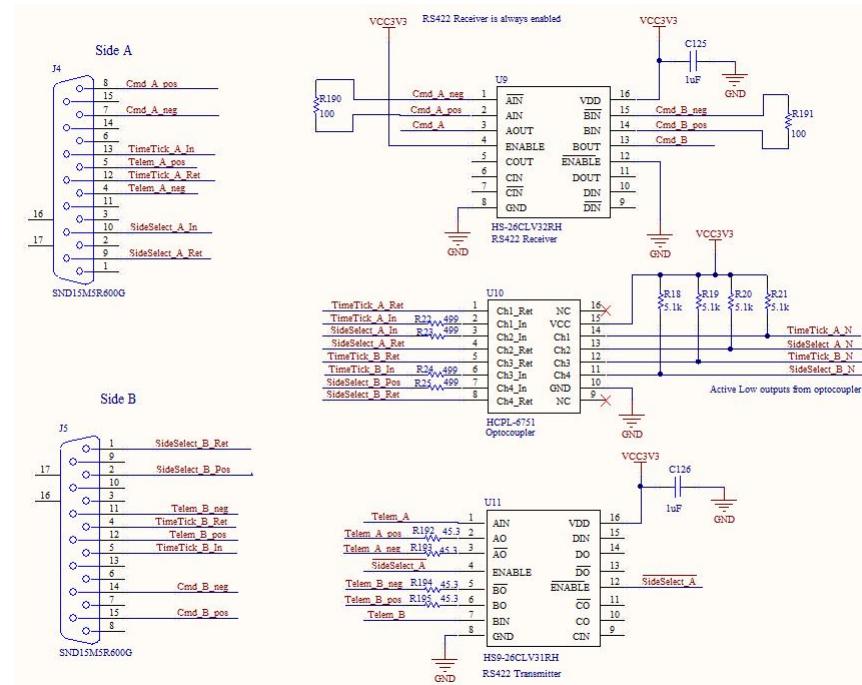


Figure C-1: Spacecraft communications interfaces: optocoupler, RS422 transceivers

TI 8:1 Analog to Digital Converter

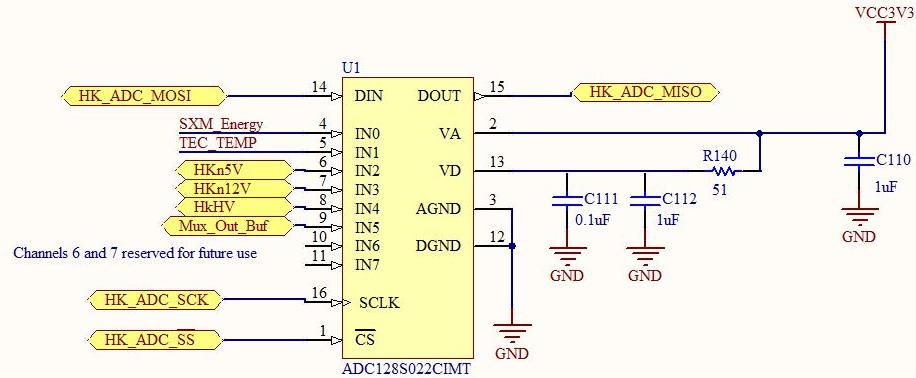


Figure C-2: Analog-Digital Converter with internal 8:1 multiplexer

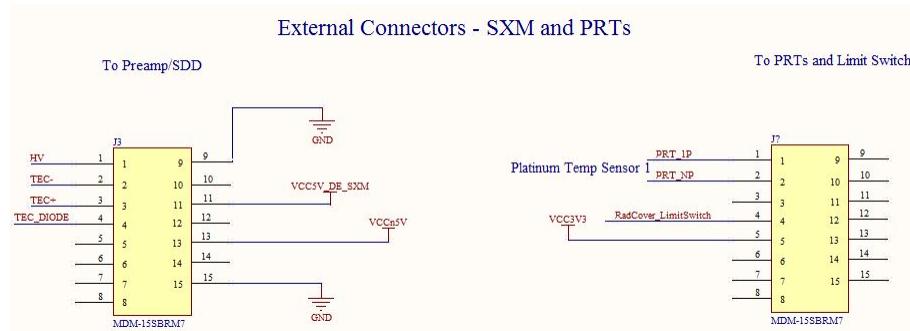


Figure C-3: External connectors to SDD/TEC and preamplifier, PRTs, and Frangibolt limit switch

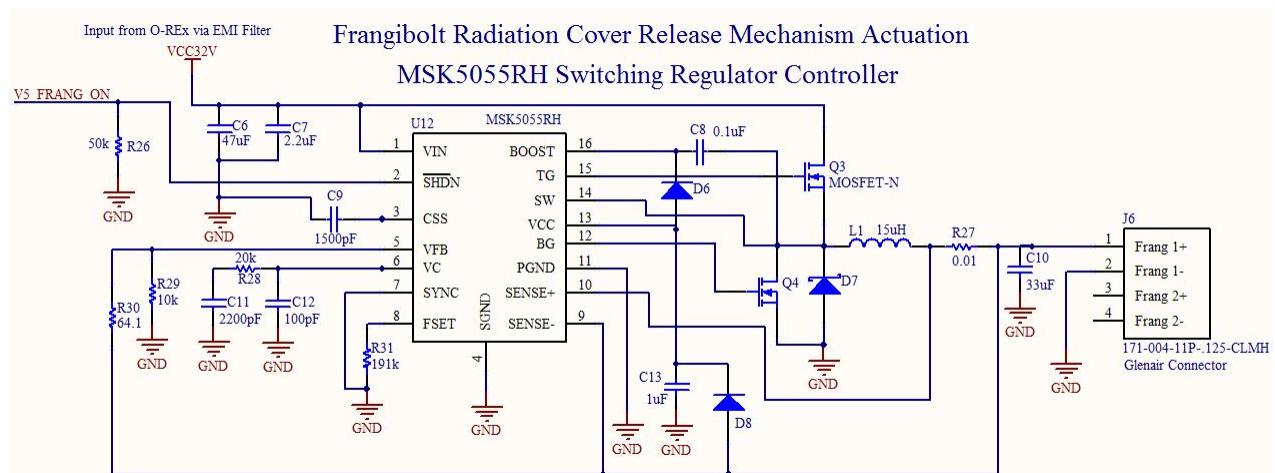


Figure C-4: Frangibolt radiation cover release mechanism actuation circuit, featuring the MSK5055RH switching regulator controller

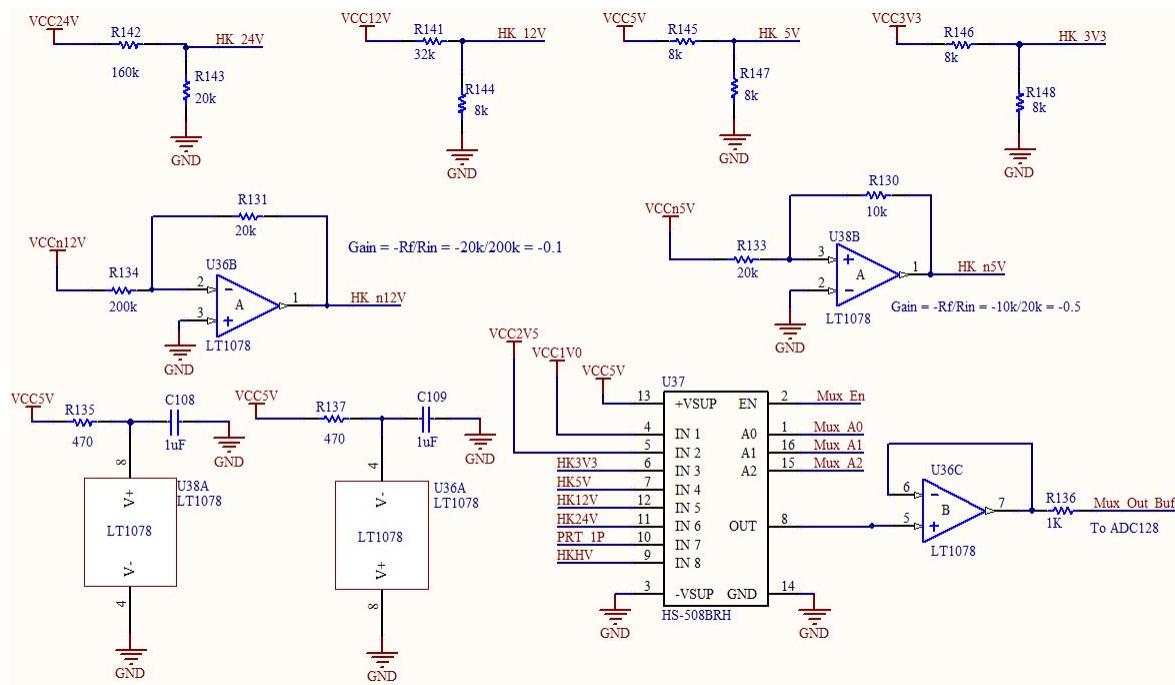


Figure C-5: Housekeeping voltage generation and multiplexing

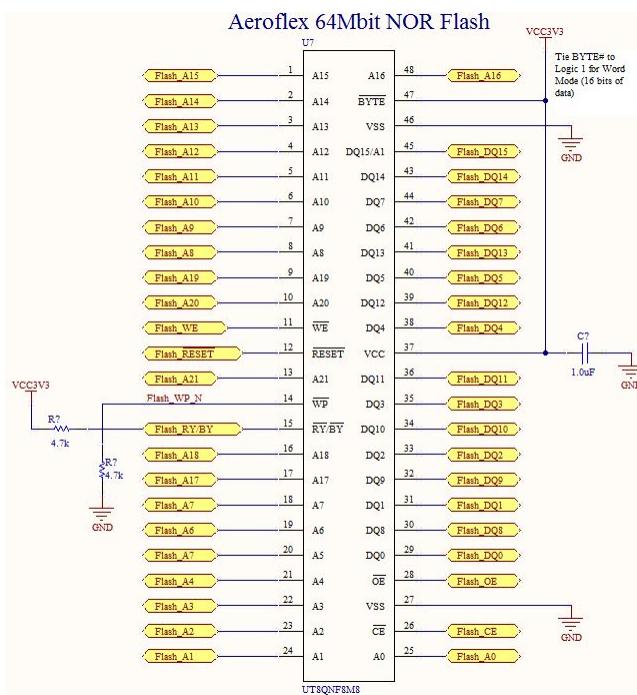


Figure C-6: Aeroflex 64Mbit NOR Flash for configuration bistream storage

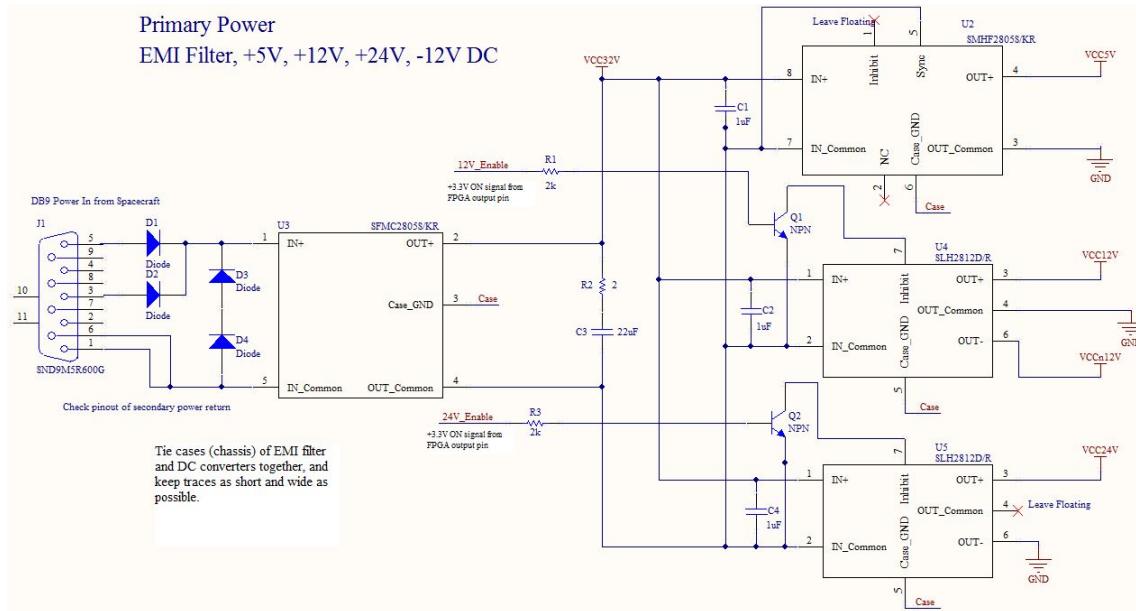


Figure C-7: EMI filter and primary DC/DC regulators

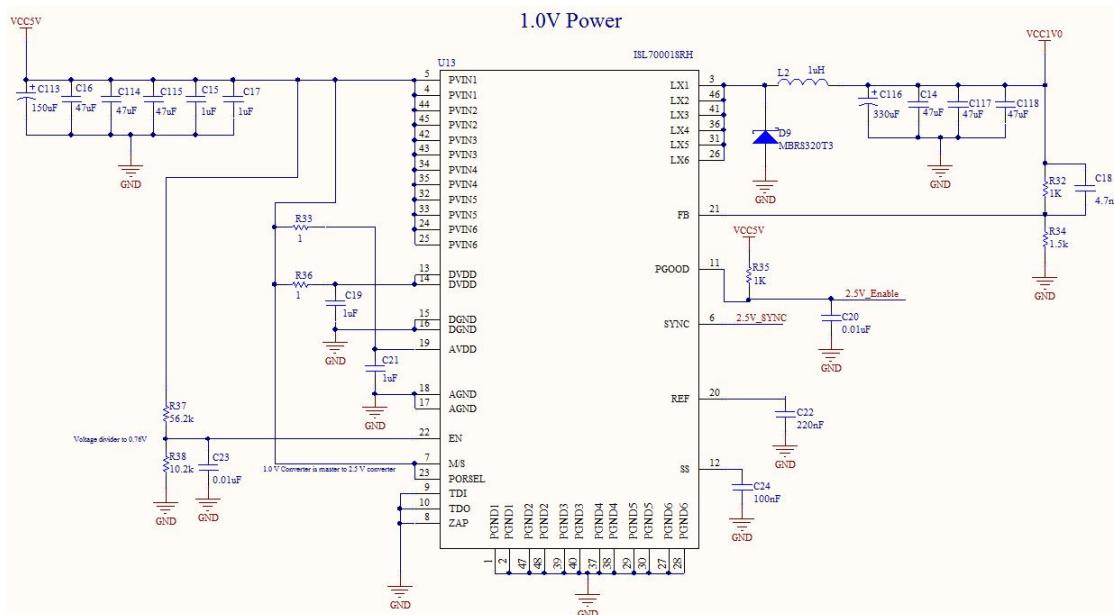


Figure C-8: 1.0V DC/DC Converter

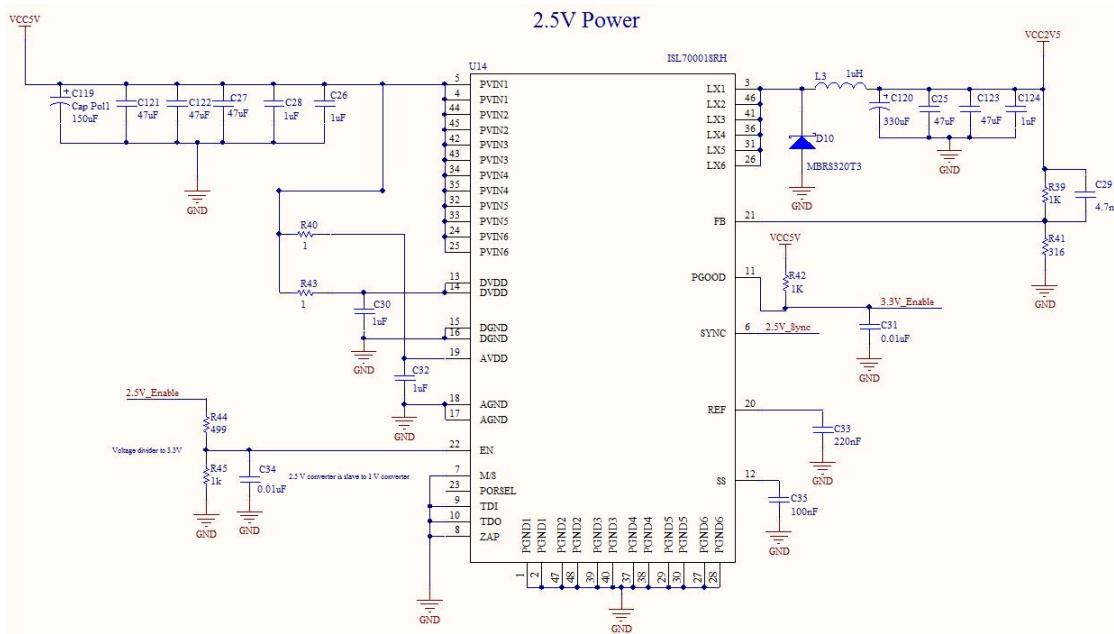


Figure C-9: 2.5V DC/DC Converter

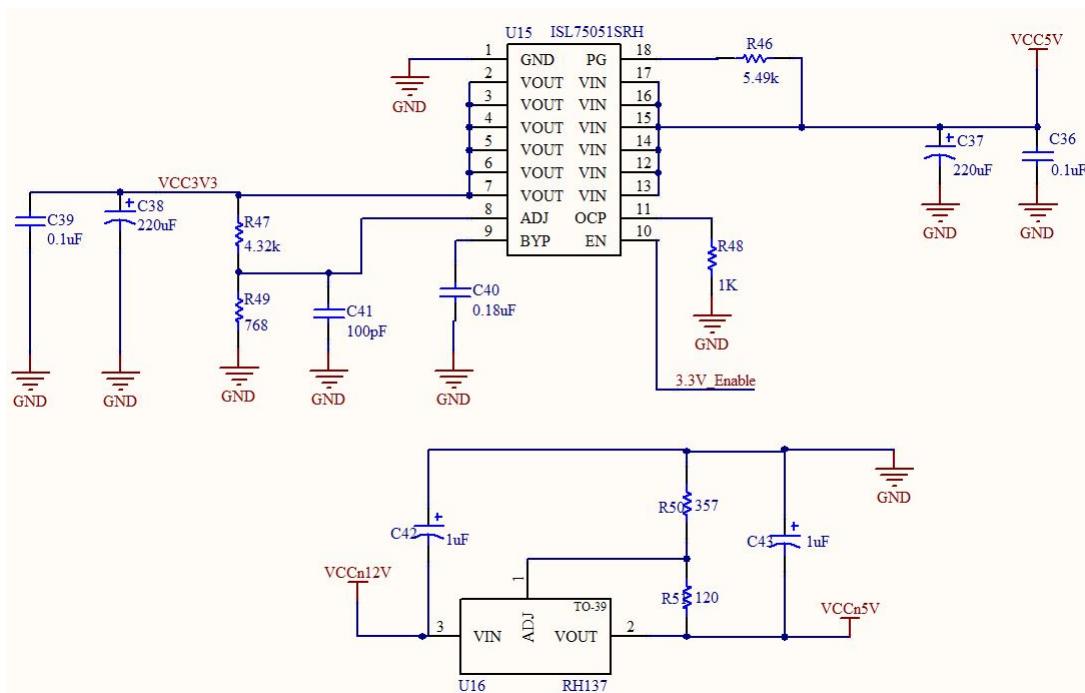


Figure C-10: 3.3V DC/DC Converter and -5V DC Regulator

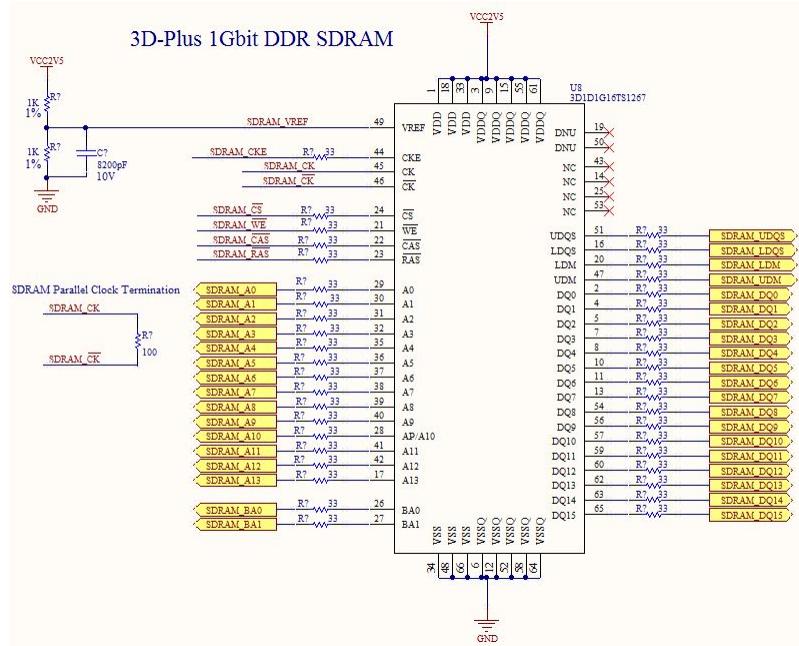


Figure C-11: 3D-Plus SDRAM Module

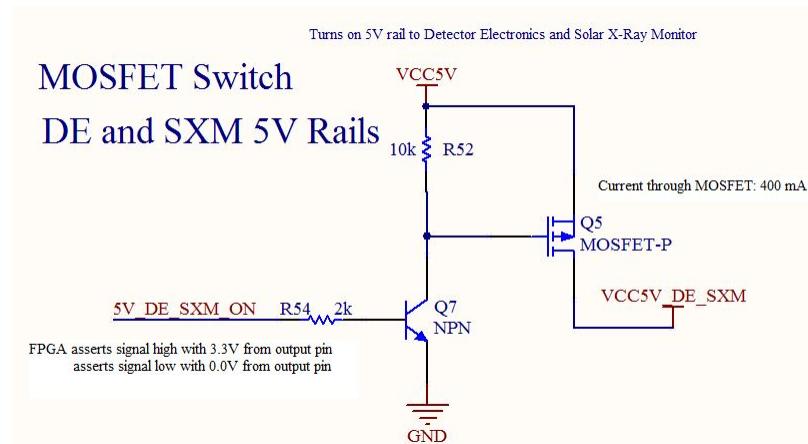


Figure C-12: MOSFET switch used to control power to DE and SXM

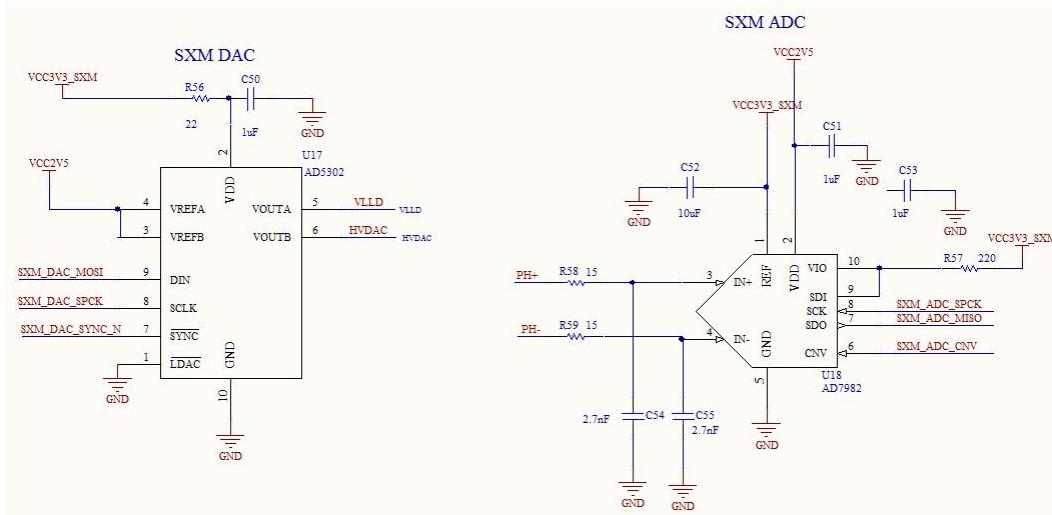


Figure C-13: SXM DAC and ADC

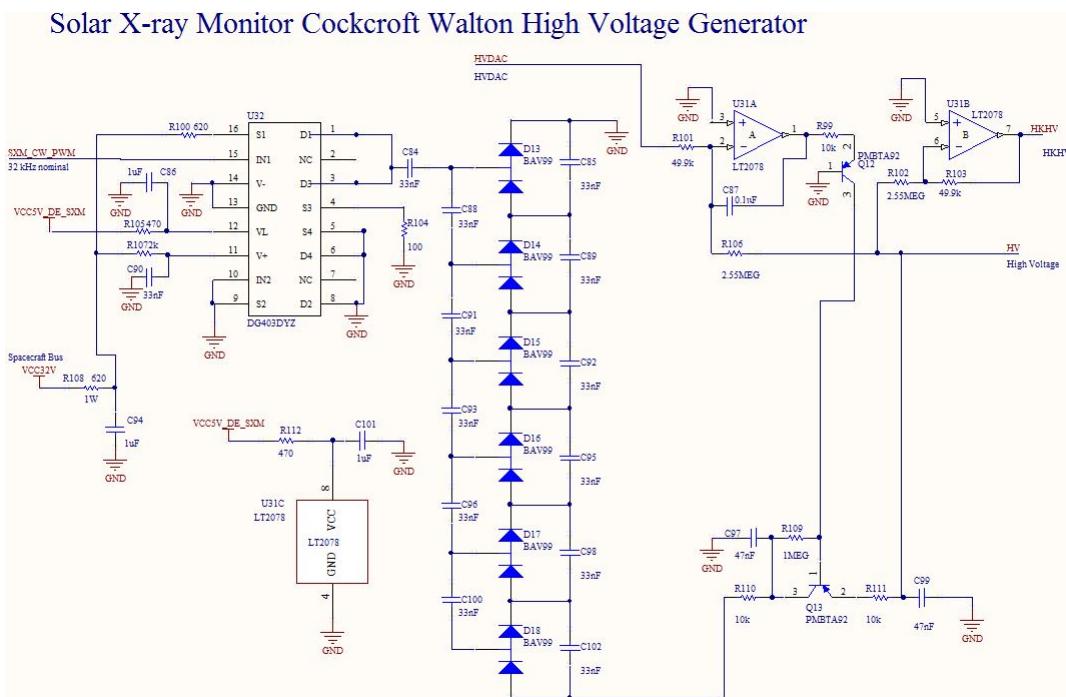


Figure C-14: SXM cockcroft walton high voltage generator

Solar X-ray Monitor Cockcroft Walton High Voltage Generator

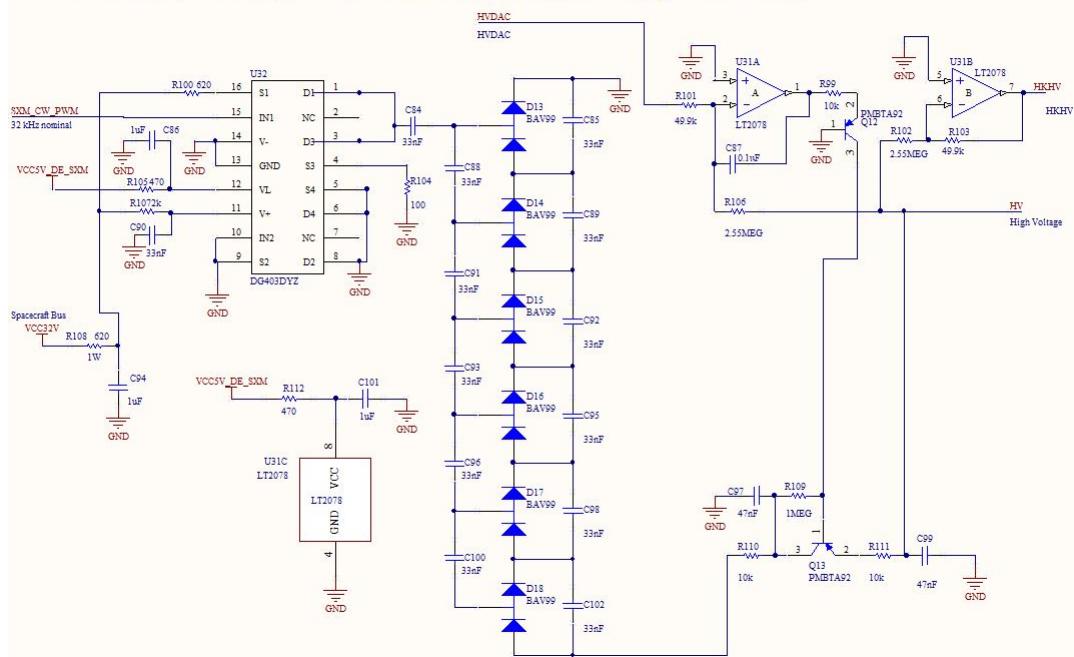


Figure C-15: SXM cockcroft walton high voltage generator

Solar X-ray Monitor Shaping and Amplification

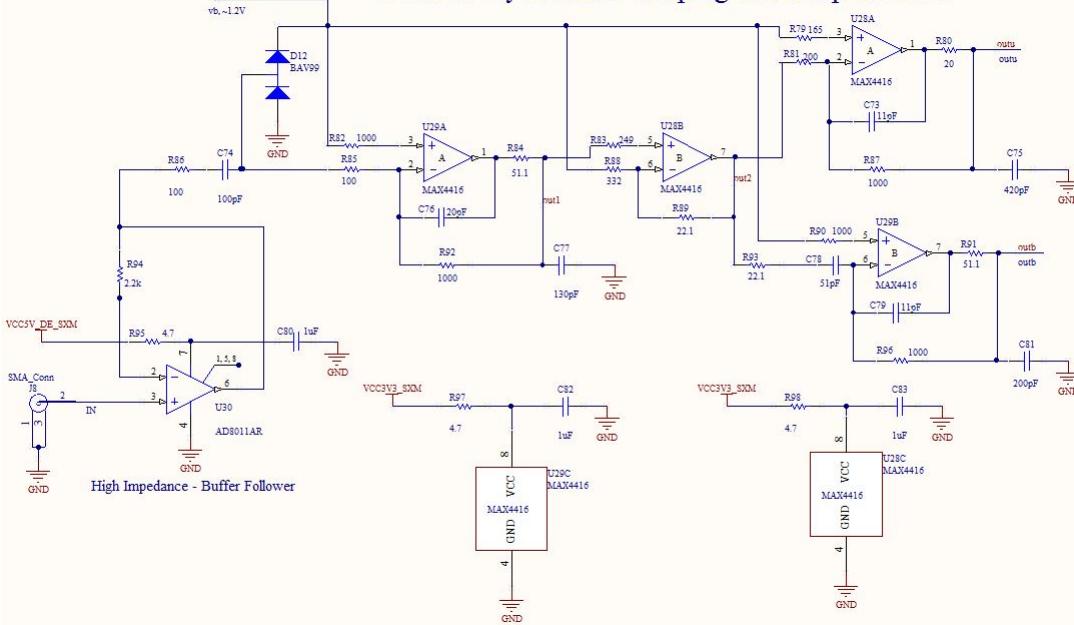


Figure C-16: SXM shaper

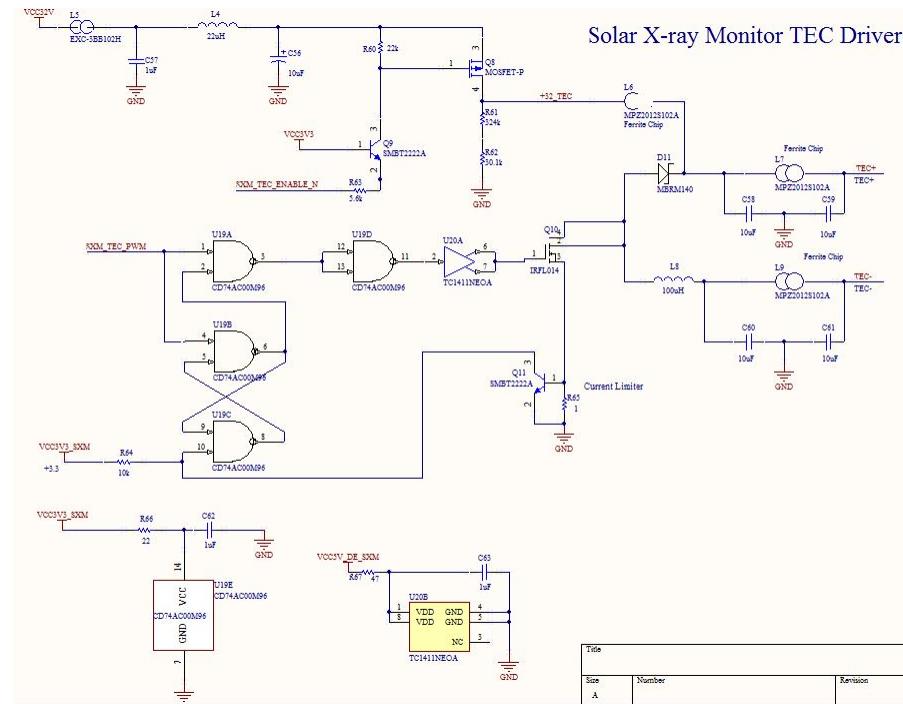


Figure C-17: SXM TEC

Solar X-ray Monitor TEC Temperature Interface

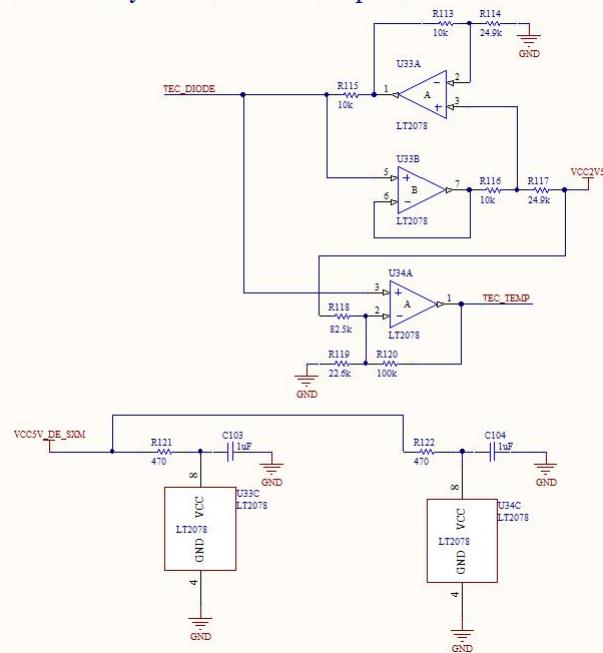


Figure C-18: SXM SDD temp interface

Solar X-ray Monitor Threshold Control

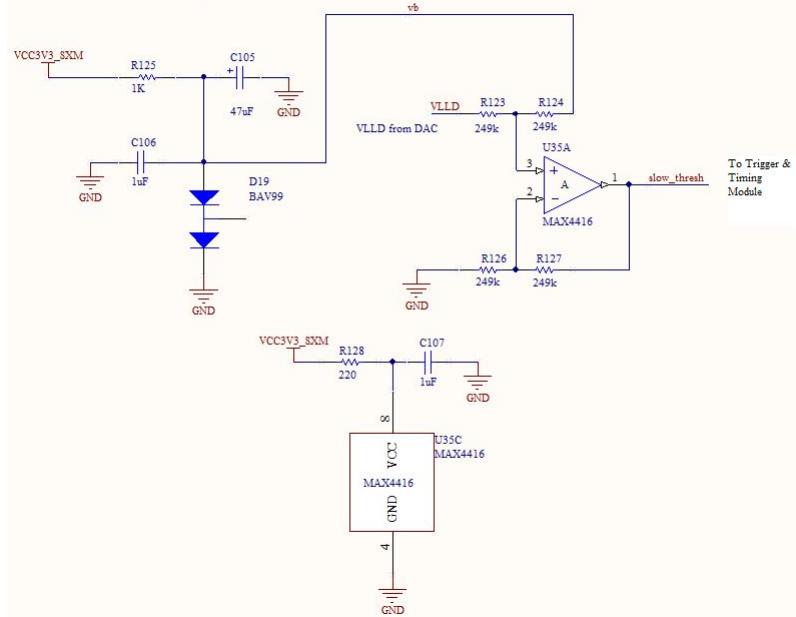


Figure C-19: SXM threshold control

Solar X-ray Monitor Trigger and Timing

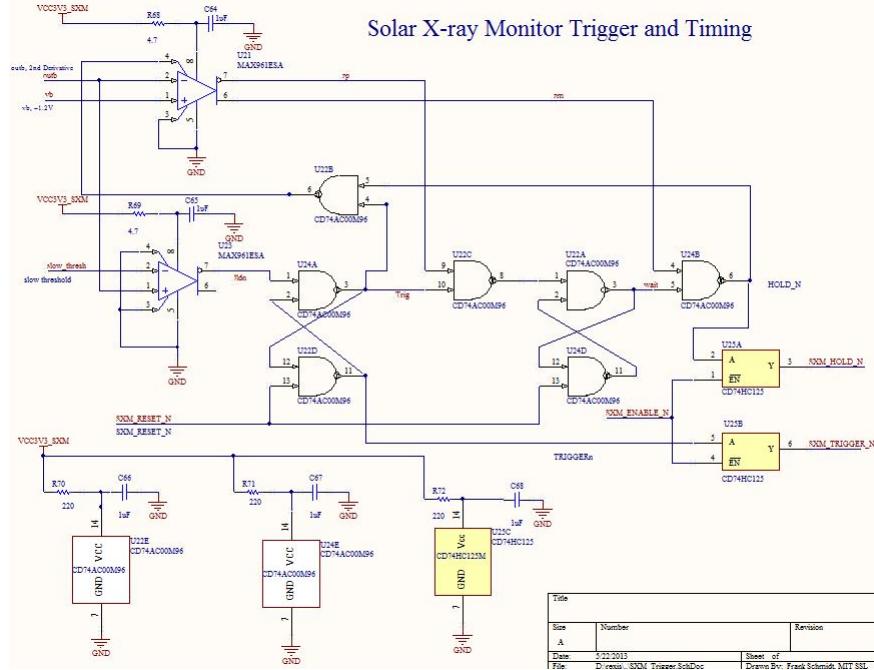


Figure C-20: SXM trigger

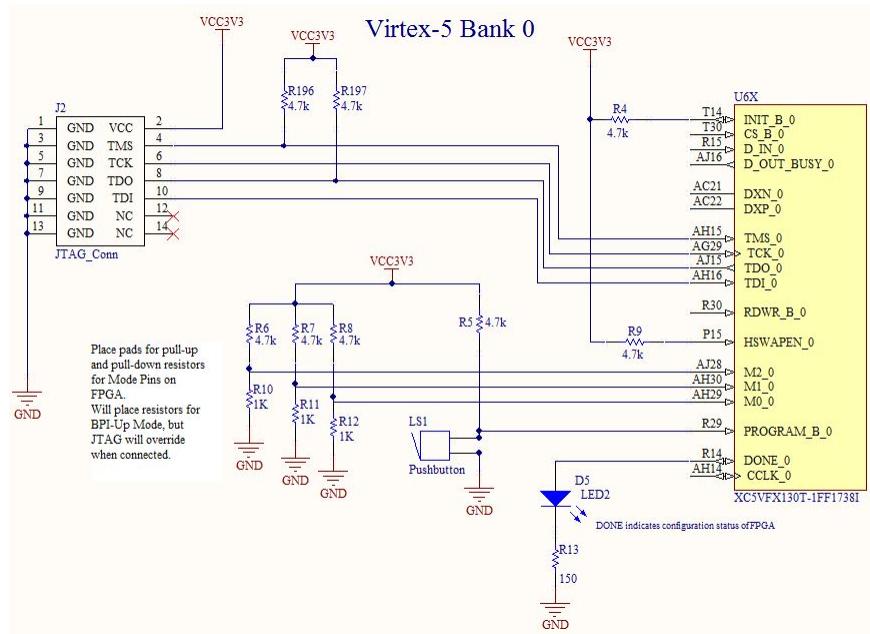


Figure C-21: Bank 0 of the Virtex-5FX130T

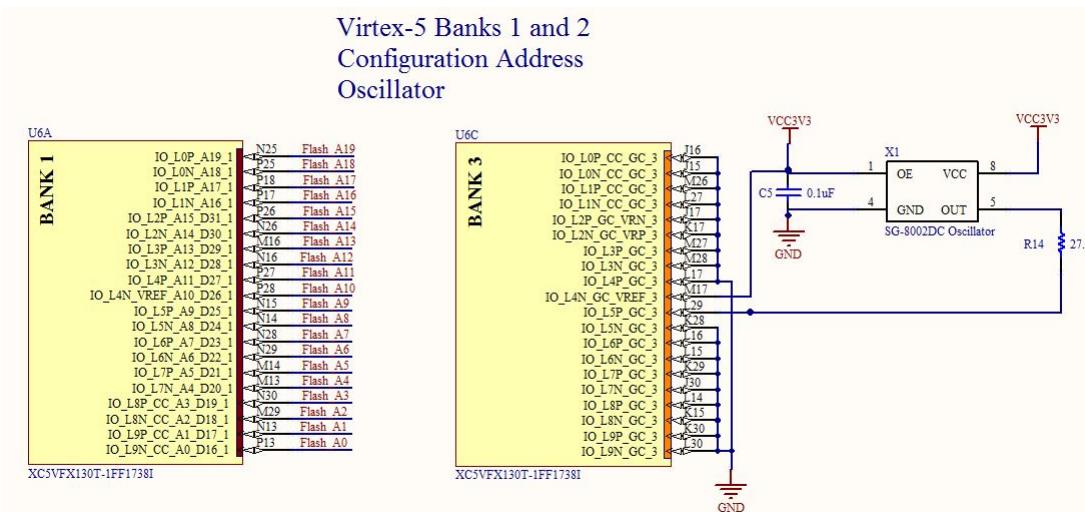


Figure C-22: Banks 1 and 2 of the Virtex-5FX130T

Virtex-5 Banks 1 and 2
Configuration Address, Data, & BPI Control

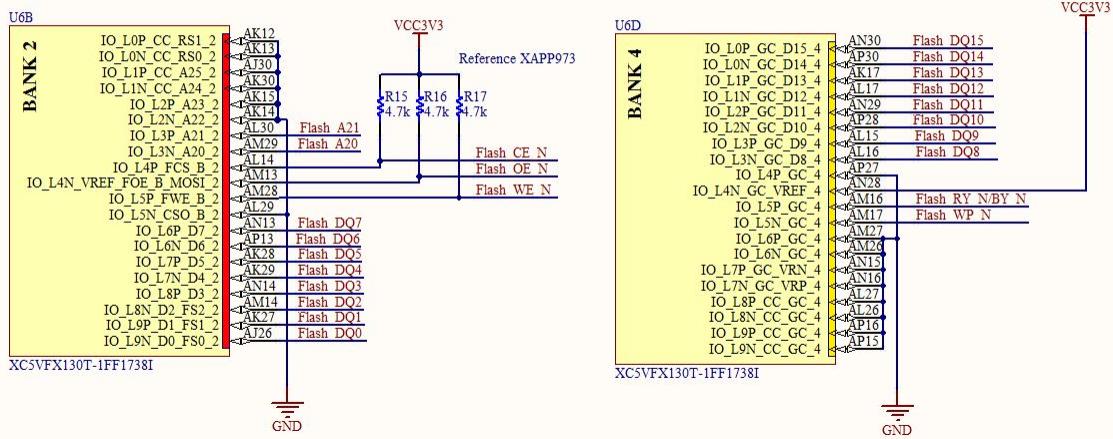


Figure C-23: Banks 3 and 4 of the Virtex-5FX130T

Virtex-5 Banks 5, 6

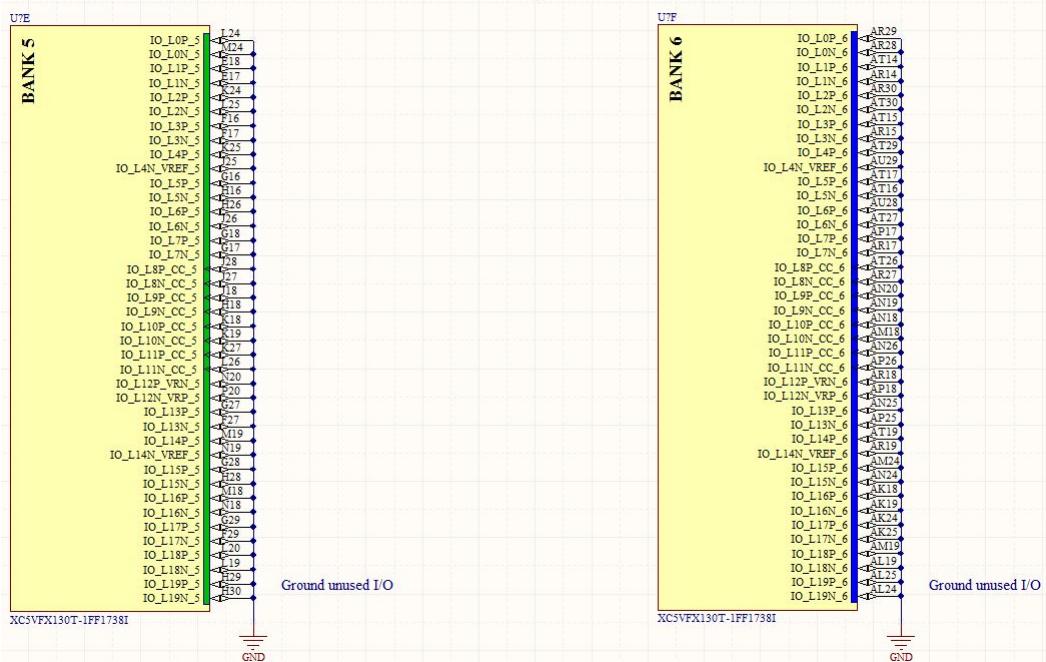


Figure C-24: Banks 5 and 6 of the Virtex-5FX130T

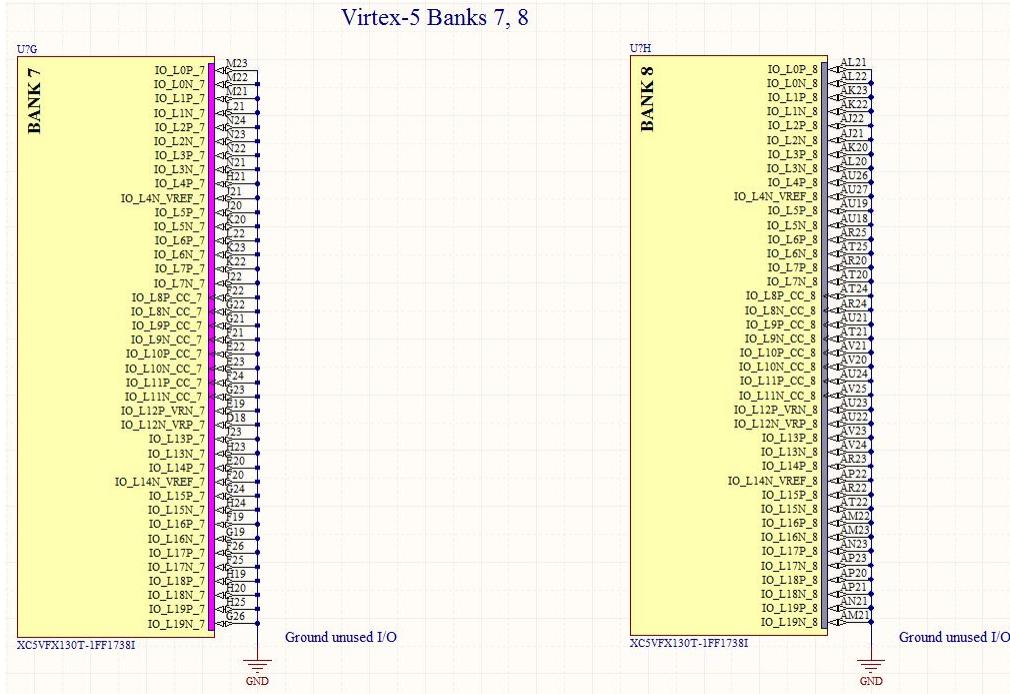


Figure C-25: Banks 7 and 8 of the Virtex-5FX130T

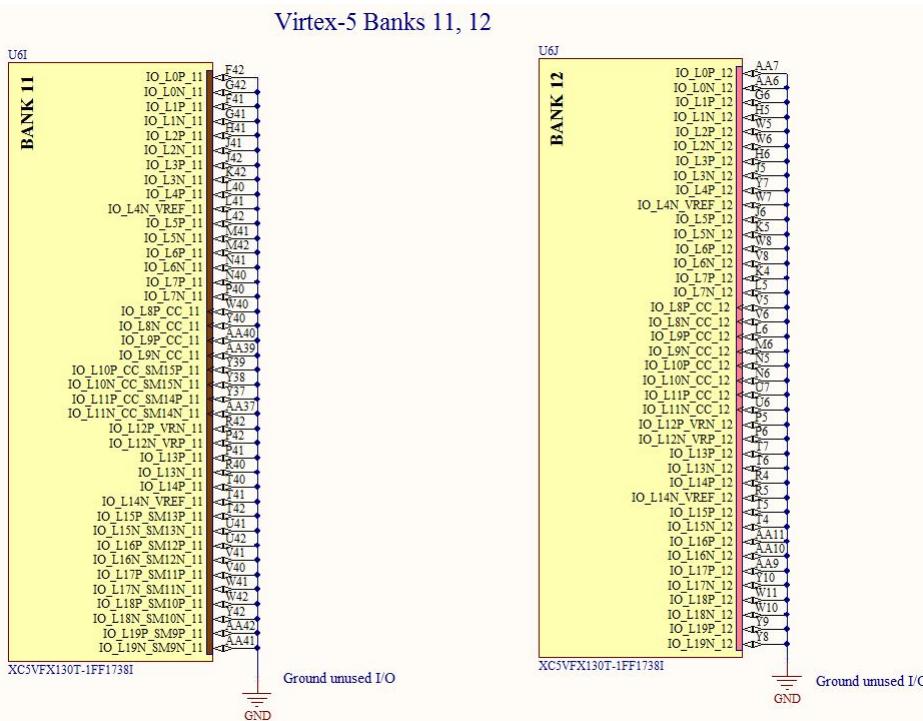


Figure C-26: Banks 11 and 12 of the Virtex-5FX130T

Virtex-5 Banks 13, 15

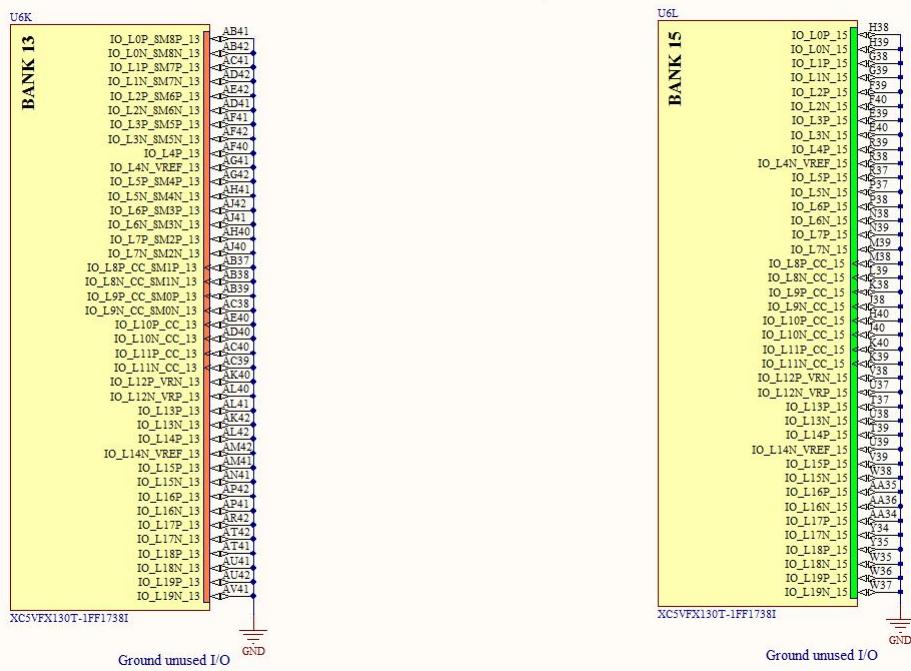


Figure C-27: Banks 13 and 15 of the Virtex-5FX130T

Virtex-5 Banks 19, 20

DDR SDRAM Data

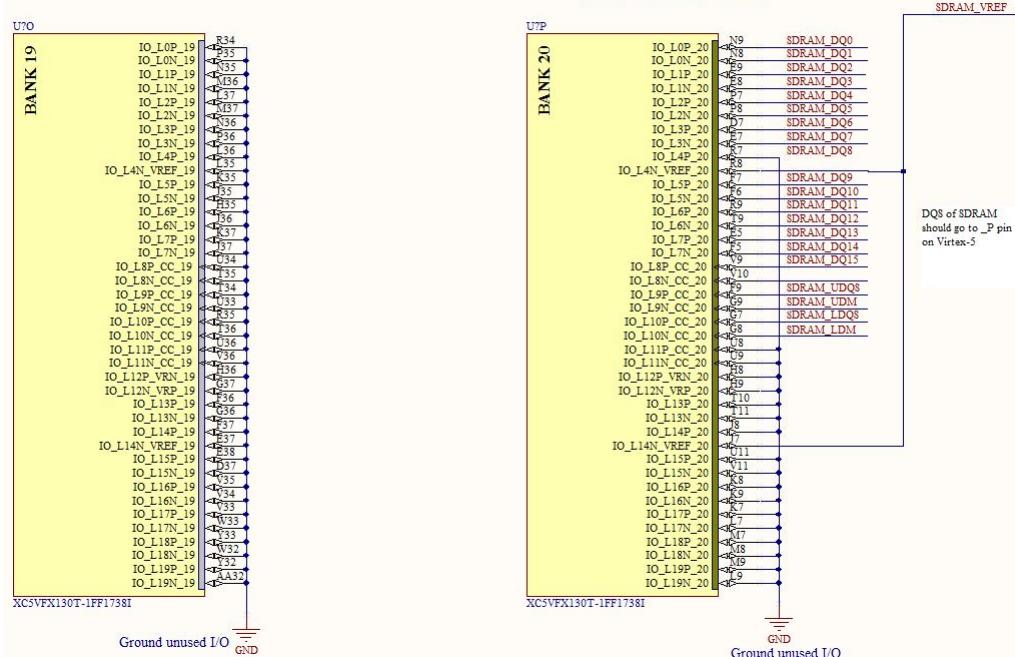


Figure C-28: Banks 19 and 20 of the Virtex-5FX130T

Virtex-5 Banks 20, 21, 24

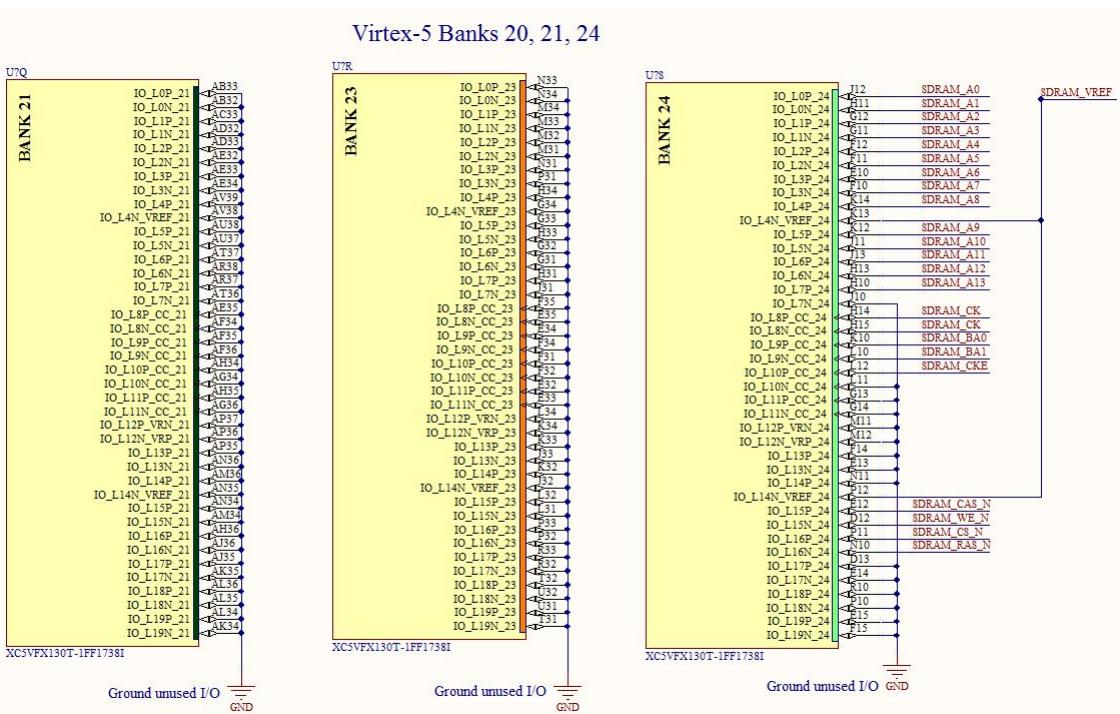


Figure C-29: Banks 21, 23, and 24 of the Virtex-5FX130T

Virtex-5 Banks 25, 26

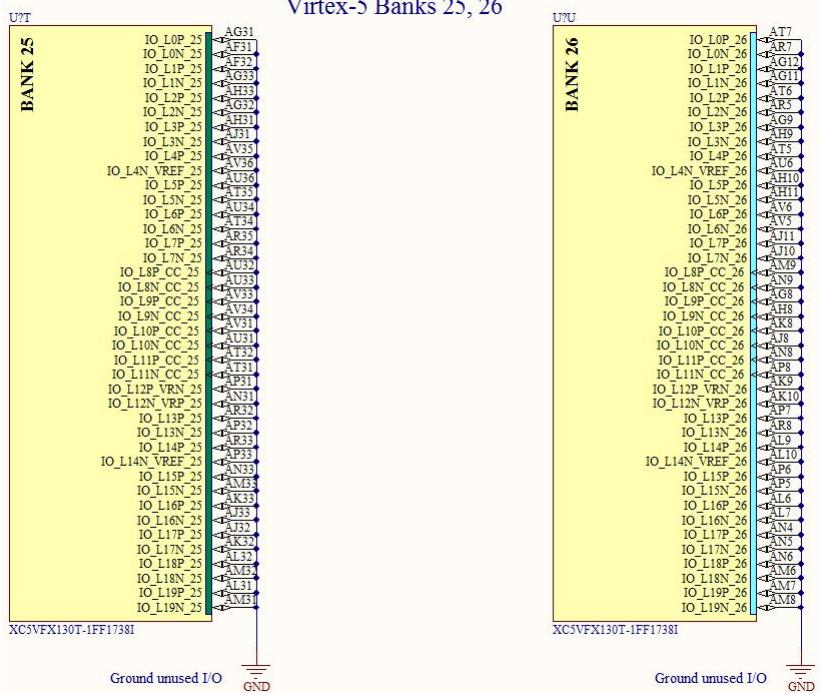


Figure C-30: Banks 25 and 26 of the Virtex-5FX130T

Virtex-5 Bank 27, 29
3.3V I/O

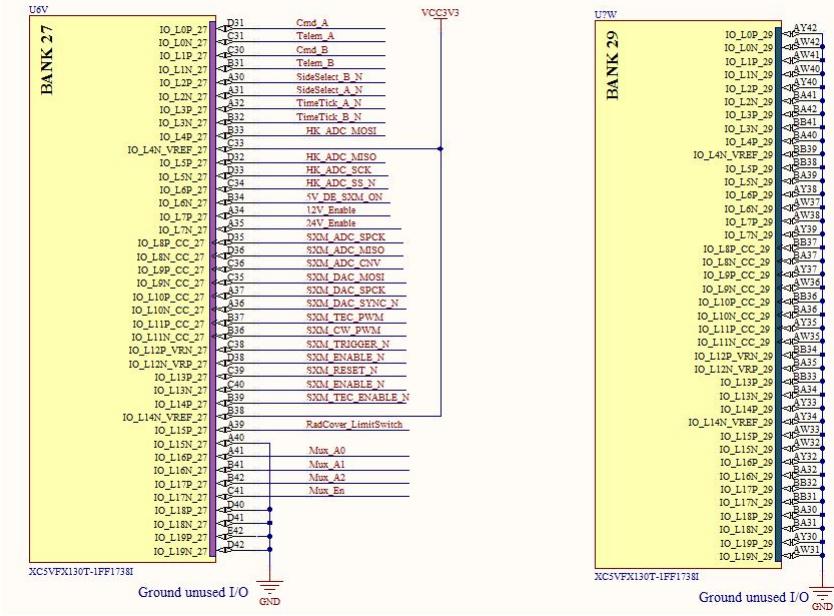
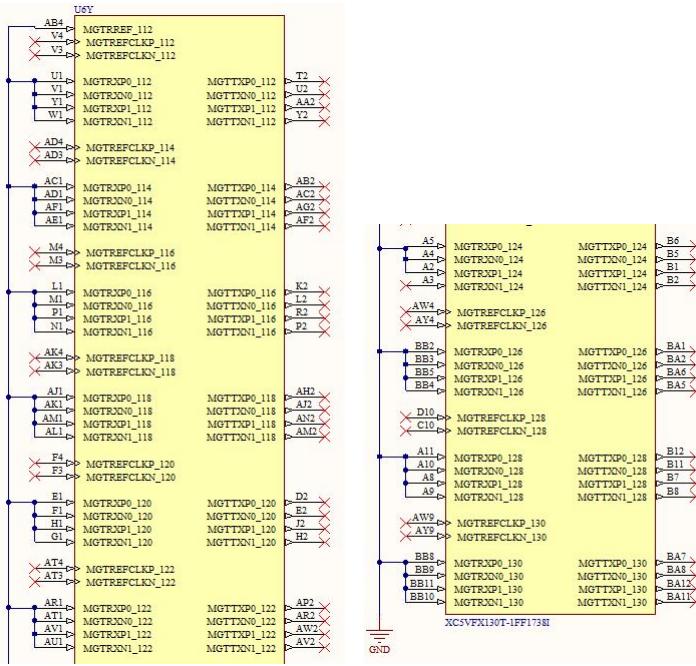
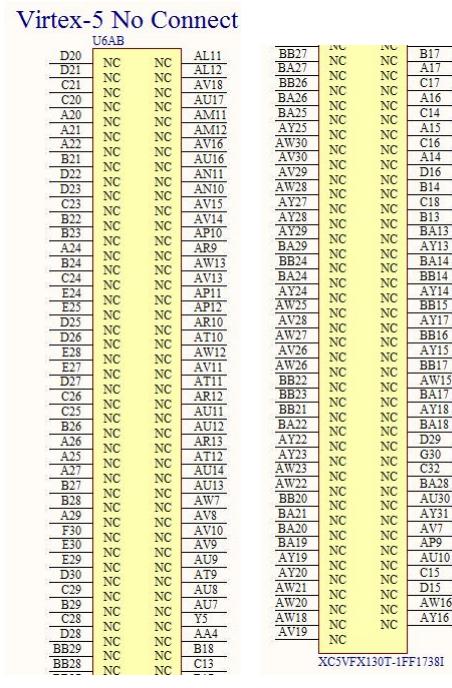


Figure C-31: Banks 27 and 29 of the Virtex-5FX130T





(a) (b)

Figure C-33: No connect pins of Virtex-5FX130T

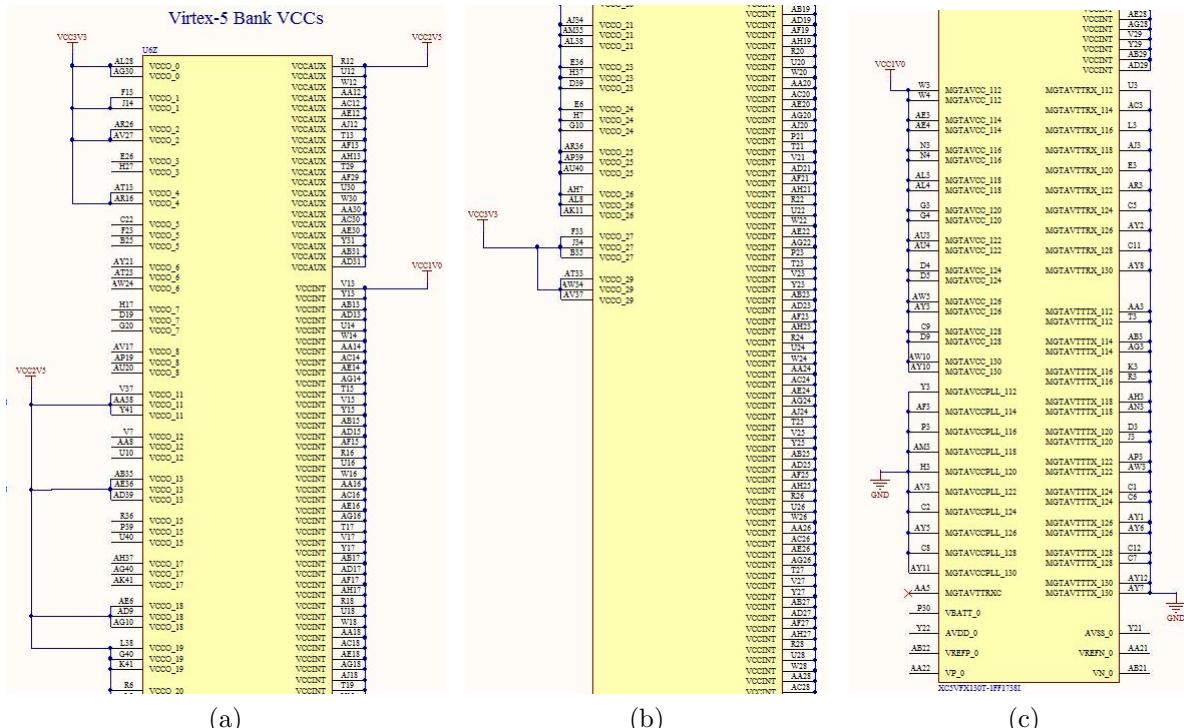


Figure C-34: VCC pins of Virtex-5FX130T

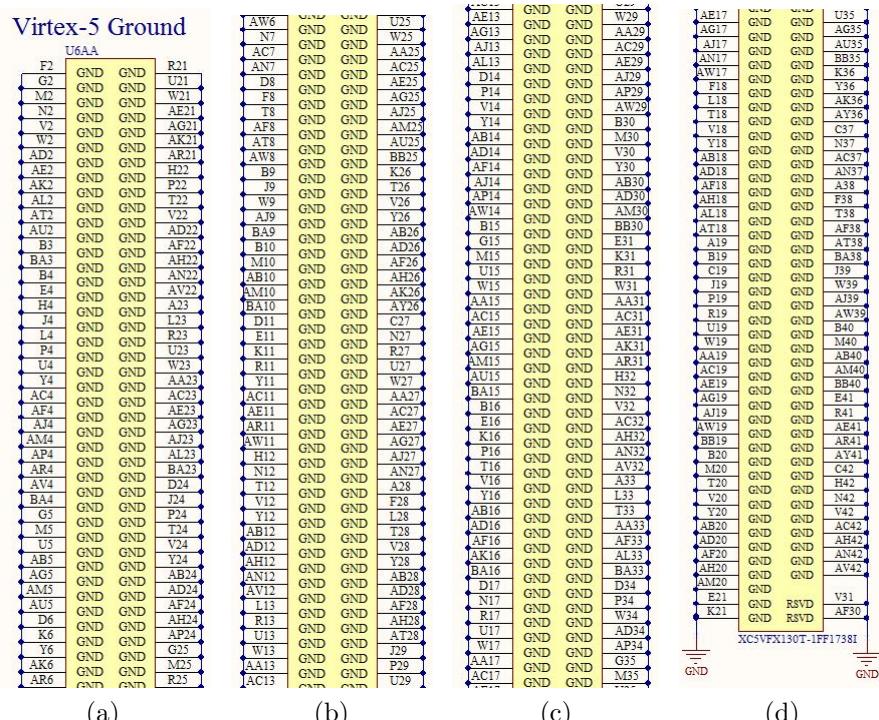


Figure C-35: Ground pins of Virtex-5FX130T

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