UNIVERSITI MALAYSIA SABAH

PEPERIKSAAN AKHIR
SEMESTER 2 SESI 2021/2022

FINAL EXAMINATION
SEMESTER 2 SESSION 2021/2022

JULAI/*JULY* 2022	**MASA/*TIME*: 3 JAM/*HOURS***

FAKULTI : **FAKULTI KEJURUTERAAN**
FACULTY : ***FACULTY OF ENGINEERING***

KOD KURSUS
/*COURSE CODE* : **KS32403**

TAJUK KURSUS : **KEAKITEKTURAN KOMPUTER**
COURSE NAME : ***COMPUTER ARCHITECTURE***

ARAHAN : **SILA JAWAB SEMUA SOALAN.**
SEMUA JAWAPAN MESTILAH DALAM BENTUK TULISAN TANGAN MENGGUNAKAN PEN.
JAWAB SETIAP SOALAN DI MUKA SURAT YANG BAHARU.
TULISKAN NOMBOR MATRIKS ANDA PADA BAHAGIAN ATAS SETIAP KERTAS JAWAPAN.
IMBAS KERTAS JAWAPAN ANDA KE BENTUK PDF DAN MUAT NAIK KE SMARTV3.

INSTRUCTIONS : ***ANSWER ALL QUESTIONS.***
ALL ANSWERS MUST BE HANDWRITTEN IN PEN.
ANSWER EACH QUESTION ON A NEW PAGE.
WRITE YOUR MATRICS NO. ON TOP OF EACH PAGE OF YOUR ANSWER PAPER.
SCAN YOUR ANSWER SCRIPT INTO A PDF AND UPLOAD IT TO SMARTV3.

Question 1 (25 Marks)

a) The shared bus architecture was used to transfer data in the conventional computer system, while the point-to-point interconnect is used in the modern computer system. Explain how the data movement was initiated and performed between the Memory, Processor, and I/O in the shared bus architecture.

(5 marks)

b) Based on your answer in (a), explain the limitation of the shared bus architecture.

(2 marks)

c) The point-to-point interconnect was designed to overcome the limitation of the shared bus. Discuss how point-to-point interconnect architecture can solve the limitation of the shared bus defined in (b).

(6 marks)

d) The computer system employs a memory hierarchy that includes the main memory and cache. To map the memory blocks to the cache lines, three techniques are used: direct, associative, and set-associative. Determine the main memory address format for the following techniques using the organization in Figure 1.

i) Direct mapping

ii) Associative mapping

iii) Two-way set-associative mapping

(9 marks)

The cache can hold 64 kB.

Data are transferred between main memory and the cache in blocks of 4 bytes each.

The main memory consists of m MB, with each byte directly addressable by a 24-bit address (m is the last two digits of your student number).

Figure 1

e) Show how the address ***m*** is divided into the three formats obtained in (d). Assume that ***m*** is the last six digits of your student number in hexadecimal.

(3 marks)

Question 2 (25 Marks)

a) In a multiprogramming system, the "user" part of memory is subdivided to accommodate multiple processes. The subdivision task is carried out dynamically by the Operating System and is known as memory management. Several techniques are implemented, namely Swapping, Partitioning, and Paging. Using appropriate diagrams, compare the Swapping, Partitioning, and Paging techniques.

(9 marks)

b) Figure 2 shows the timing diagram for nine instructions with a six-stage pipelining strategy. Assume that there are no memory conflicts and that each stage has an equal duration.

i) Redraw the diagram to show how many time units are needed for eight instructions if using a two-stage pipeline (fetch, execute).

(2 marks)

ii) Assume a pipeline with four stages: Fetch Instruction (FI), Decode Instruction and Calculate Addresses (DA), Fetch Operand (FO), and Execute (EX). Redraw the diagram for a sequence of eight instructions, in which the ***m***-th instruction is a branch that is taken and in which there are no data dependencies (***m*** is the last digit of your student number).

(4 marks)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Instruction 1	FI	DI	CO	FO	EI	WO								
Instruction 2		FI	DI	CO	FO	EI	WO							
Instruction 3			FI	DI	CO	FO	EI	WO						
Instruction 4				FI	DI	CO	FO	EI	WO					
Instruction 5					FI	DI	CO	FO	EI	WO				
Instruction 6						FI	DI	CO	FO	EI	WO			
Instruction 7							FI	DI	CO	FO	EI	WO		
Instruction 8								FI	DI	CO	FO	EI	WO	
Instruction 9									FI	DI	CO	FO	EI	WO

Figure 2

c) Assume the RISC machine has the instruction stages as in Figure 3. Show the pipelining timing for the program segment in Figure 4 for one memory access per stage.

(8 marks)

For **register to register** operations, a RISC instruction cycle has the following two stages:

- I: Instruction fetch.
- E: Execute. Performs an ALU operation with register input and output.

For **load and store** operations, a RISC instruction cycle has the following three stages:

- I: Instruction fetch.
- E: Execute. Calculates memory address.
- D: Memory. Register-to-memory or memory-to-register operation.

Figure 3

```
LOOP    LOAD R1,A        ; load A into register R1
        LOAD R2,B        ; load B into register R2
        ADD  R3,R1,R2    ; add R2 to R1 and store in R3
        JUMP LOOP        ; jump to LOOP
        LOAD R4,C        ; load C into register R4
        NOOP             ;
        ADD  R5,R4,R3    ; add R3 to R4 and store in R5
```

Figure 4

Question 3 (25 Marks)

a) An I/O module is a mediator between the processor and I/O devices. Explain why the I/O devices are not directly connected to the processor.

(4 marks)

b) There are three techniques possible for I/O operations: Programmed I/O, Interrupt Driven I/O, and Direct Memory Access. Contrast these three techniques using appropriate diagrams/flowcharts.

(12 marks)

c) Using the timing diagrams, compare and choose the best technique among the ordinary pipeline, super-pipelined, and super-scalar. Assume that the instruction has a four-stage cycle: fetch (F), decode (D), execute (EX) and write (WR).

(9 marks)

Question 4 (25 Marks)

a) Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. What is the maximum directly addressable memory capacity (in bytes)?

(2 marks)

b) For the microprocessor in (a), analyze the impact on the system speed if the microprocessor bus has:

i) 32-bit local address bus and an ***m***-bit local data bus, or

ii) 16-bit local address bus and an ***m***-bit local data bus.

(***m*** is the last digit of your student number or the second last digit if the last digit is 0)

(6 marks)

c) Consider a 32-bit microprocessor with a 16-bit external data bus, driven by an ***m***-MHz input clock (***m*** is the last digit of your student number or the second last digit if the last digit is 0). Assume that this microprocessor has a bus cycle with a minimum duration of four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain in bytes/sec?

(3 marks)

d) To increase the performance of the microprocessor in (c), would it be better to make its external data bus 32 bits or double the external clock frequency supplied to the microprocessor? State any other assumptions you make and explain.

(4 marks)

e) Consider the instruction mix in Table 1 (***m*** is the last digit of your student number or the second last digit if the last digit is 0).

i) Determine the overall effective CPI.

(4 marks)

ii) How much faster would the machine be if a better data cache had reduced the average load time to 2 cycles?

(3 marks)

iii) How does the answer in (ii) compare with reducing the branch instruction to 1 cycle?

(3 marks)

Table 1

Instruction type	Frequency (%)	Cycles
ALU	40	1
Load	20	***2m***
Store	20	3
Branch	20	2