Optimizing Power Consumption in Differential Amplifiers

SuperVisor Teacher :-

Dr. RishiBrind Upadhyay

TEAM NAME :-

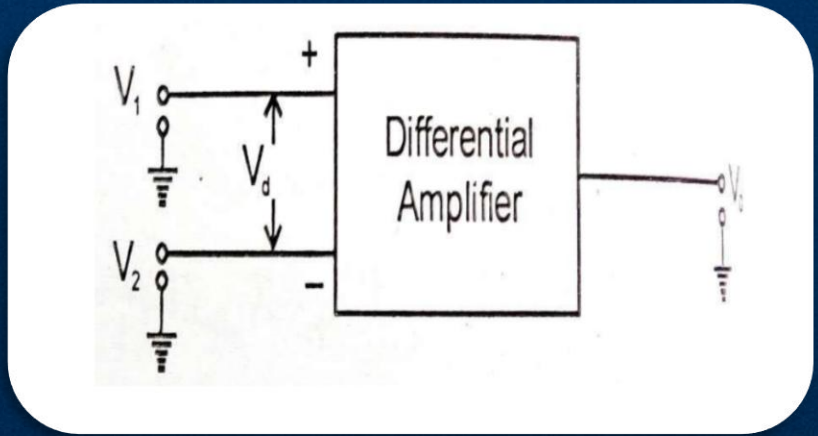
Priyanshu Aggarwal A8 22102236

Harsheeta Agarwal A8 22102187

What is Differential Amplifier

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages while rejecting any signals common to both inputs.

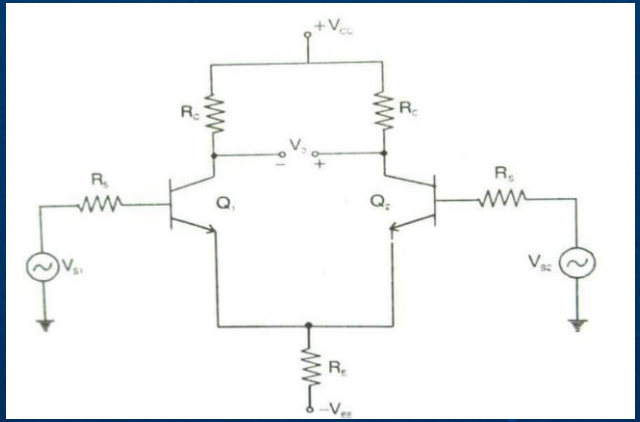
Widely used in analog circuits, operational amplifiers, and sensor applications. It is also the basic input stage of an integrated amplifier.



The output signal in a differential amplifier is directly proportional to the difference between the two input signals. Mathematically, it can be expressed as:

$$V_o \propto (V_1 - V_2)$$

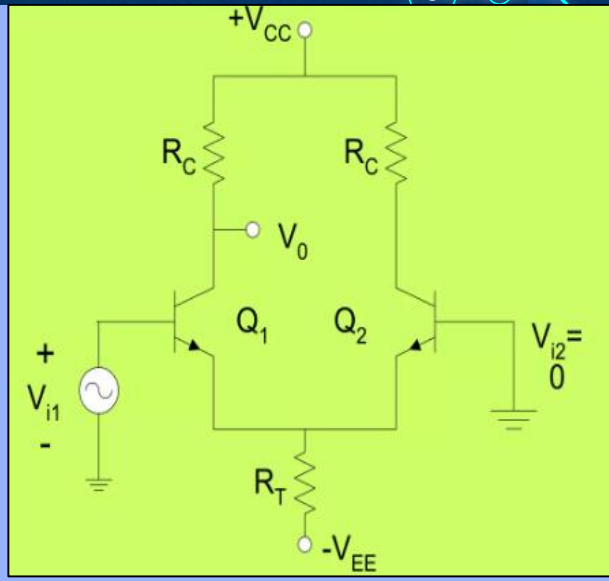
Where:
V_1 and V_2 are the two input signals.
V_o is the single-ended output voltage.



Basic configuration of a differential amplifier

Single-Ended Mode

In **single-ended mode**, only one input receives the signal, while the other is grounded or held at a fixed reference voltage.



Operation

- If the signal is applied to the **non-inverting input** (+), the output is **in phase** with the input:

$$V_o = A \cdot V_{in}$$

- If the signal is applied to the **inverting input** (-), the output is **180° out of phase** with the input:

$$V_o = -A \cdot V_{in}$$

Key Points

✔ Simple circuit configuration.

✔ Susceptible to noise and interference.

Differential Mode

In **differential mode**, the amplifier amplifies the difference between the two input signals.

Operation

- Two inputs:

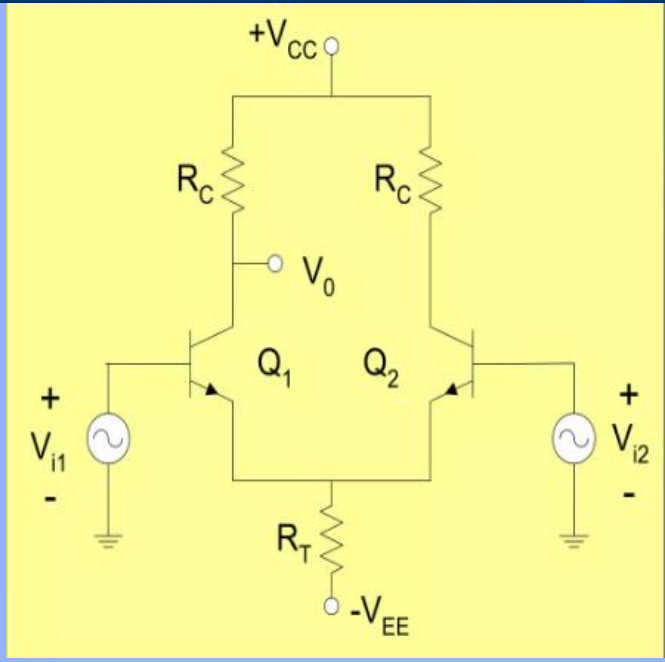
$$V_1 = +\frac{V_d}{2}, \quad V_2 = -\frac{V_d}{2}$$

  where $V_d = V_1 - V_2$ is the **differential input voltage**.

- The output is given by:

$$V_o = A_d(V_1 - V_2)$$

  where A_d is the **differential gain**.



Key Points

✔ High noise immunity (rejects common-mode noise).

✔ Used for **high-precision signal amplification**.

Common Mode

In **common-mode operation**, both input terminals receive the same signal.

Operation

- Inputs:

$$V_1 = V_{cm}, \quad V_2 = V_{cm}$$

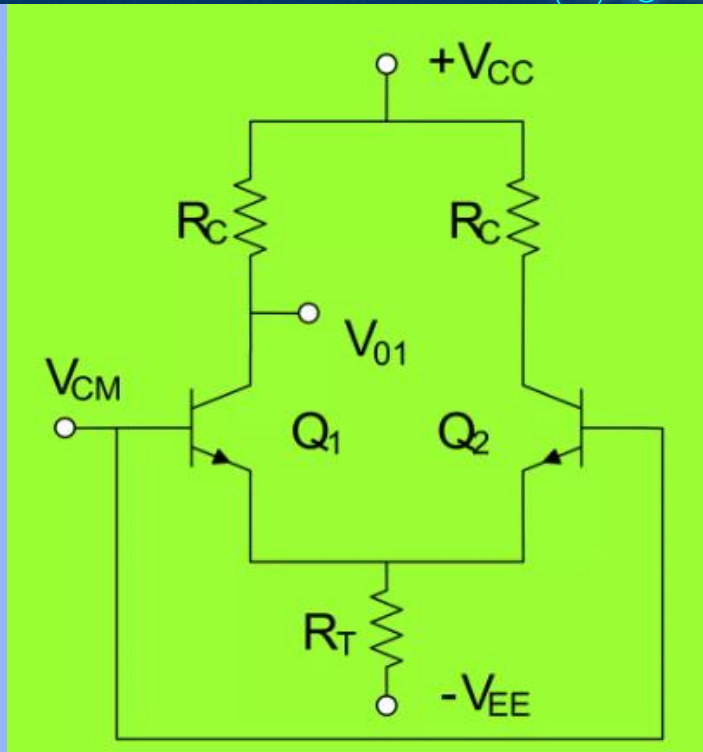
- Ideally, the output should be:

$$V_o = A_d(V_1 - V_2) = 0$$

- However, due to imperfections, a small unwanted output appears:

$$V_o = A_{cm} V_{cm}$$

where A_{cm} is the **common-mode gain**.



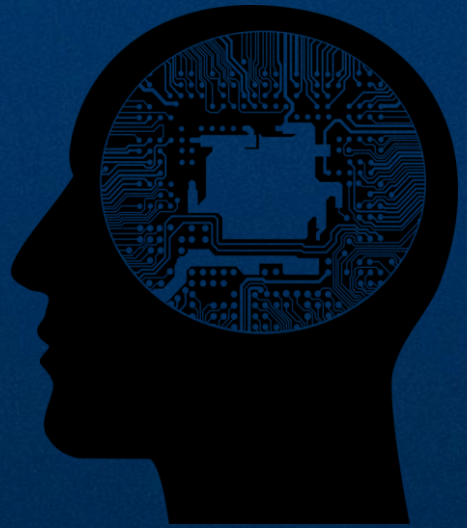
Common Mode Rejection Ratio

•The ability of a **differential amplifier** to reject **common-mode signals** (unwanted noise or interference).
•Defined as the ratio of **differential gain** to **common-mode gain**.

Mathematical Expression:

$$CMRR = \frac{A_d}{A_{cm}}$$

A_d = Differential gain
A_{cm} = Common-mode gain



Key Points:

✓ **Higher CMRR** → Better noise rejection.
✓ Used in **instrumentation amplifiers, biomedical applications (ECG, EEG), and communication systems**.
✓ Ideally, **CMRR should be infinite**, but practical values range from **60 dB to 120 dB**.

Differential Gain

- **Differential Gain (Ad) is the gain with which the differential amplifier amplifies the difference between two input voltages (V_1 - V_2).**
- **It represents how well the amplifier responds to the difference in signals applied at the two inputs.**

Mathematical Expression:

$$V_o=A_d(V_1-V_2)$$

V_o is the output voltage.
$V_1-V_2=V_d$ is the difference of the two input voltages (Differential Input).
A_d is the differential gain.

A more detailed formula for differential gain is:

$$A_d=V_o/V_d=-g_mR_C$$

where:

- G_m is the **transconductance** of the transistor.
- R_C is the **collector resistor**.

Common Mode Gain

- **Common Mode Gain (Ac)** represents how much of the **common part** of the input signals is amplified by the differential amplifier.
- If both input signals are equal, their average is called the **common mode signal**

Mathematical Expression:

$$V_c = \frac{V_1 + V_2}{2}$$

Effect on Output Voltage:

Since the differential amplifier is not perfect, it also produces some output proportional to the common mode signal. The output due to common mode is given by:

$$V_o = A_c V_c$$

Total Output Voltage of the Differential Amplifier:

Since the amplifier responds to both **differential signals** and **common mode signals**, the total output is given by:

$$V_o = A_d V_d + A_c V_c$$

Circuits of Differential Amplifier

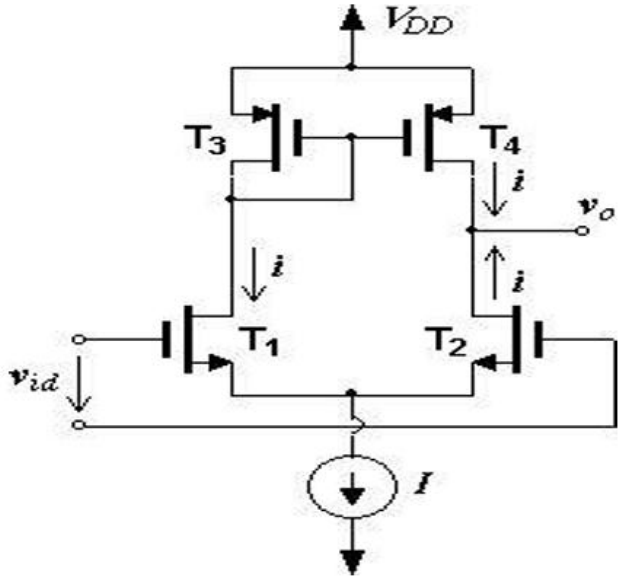
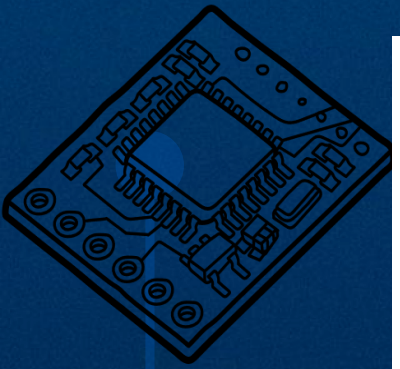


Fig 4: Differential Amplifier with Active Current Mirror Configuration.

Circuits of Differential Amplifier



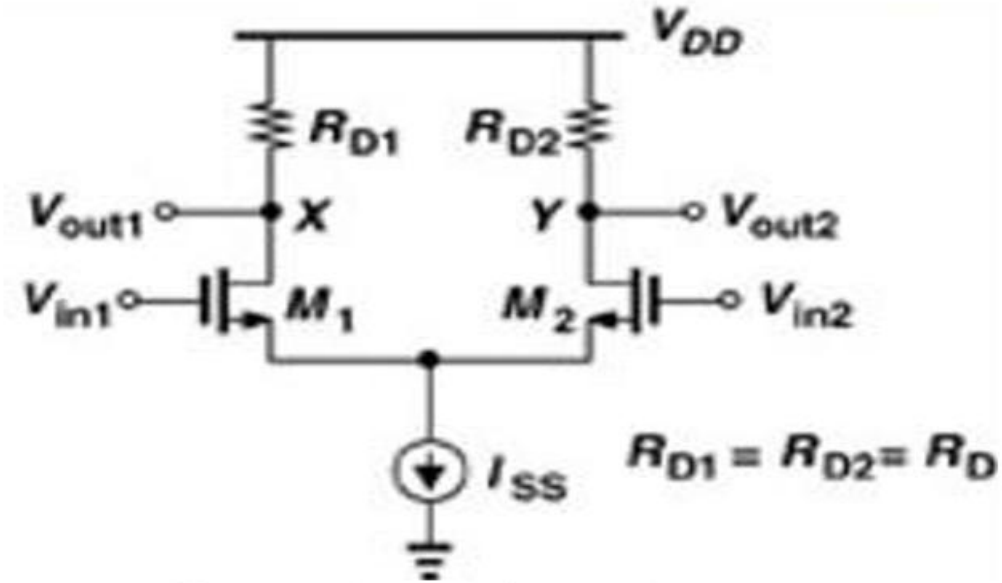
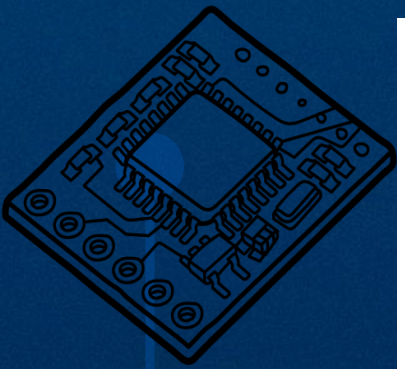


Fig2: Differential Amplifier with Current Source.

Circuits of Differential Amplifier



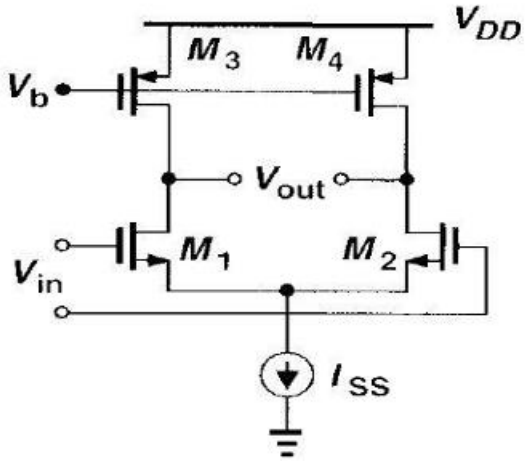


Fig3: Differential amplifier with active load

Comparison of Different Differential Amplifier Topologies

Topology	Voltage Gain (dB)	Bandwidth (GHz)	Power Dissipation (mW)
Current Mirror Load	14.22	7.99	5.72
Active Load	21.19	7.5	2.13
Diode-Connected Load	35.43	7.98	1.83

Impact of Different Load Configurations

1.Passive Load:

1. Uses resistors, leading to **lower gain** and **higher power dissipation**.
2. Simple to design but inefficient for **low-power applications**.

2.Current Mirror Load:

1. Improves **current sourcing**, leading to better **gain stability**.
2. Reduces power consumption but still **limited in gain**.

3.Active Load:

1. Uses MOSFET-based loads instead of resistors, **significantly boosting gain**.
2. **Lower power dissipation**, making it ideal for **low-power VLSI applications**.

4.Diode-Connected Load:

1. Provides **highest gain** but at the cost of reduced bandwidth.
2. Suitable for **high-gain, low-frequency applications**.

Enhancing Gain in Differential Amplifiers

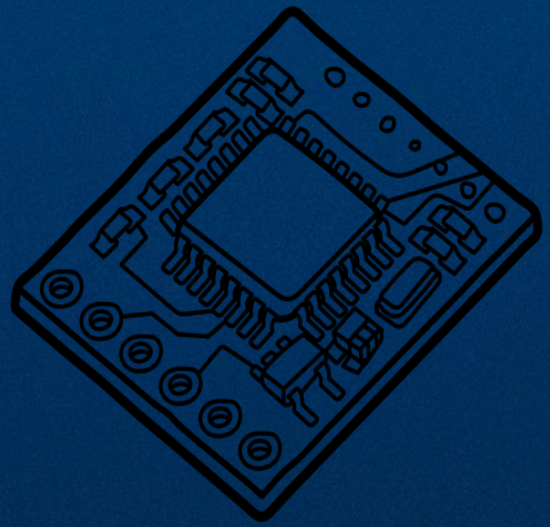
1. **Using Active Load Instead of Passive Load**
   - Replaces resistors with **MOSFET-based current sources** to increase gain.
   - **Formula for gain:**

$$A_d = -g_m R_C$$

   - Where g_m is the **transistor's transconductance**, and R_C is the **load resistance**.
2. **Cascode Configuration**
   - Stacks **two transistors** to **reduce Miller effect**, thereby improving **gain and bandwidth**.
   - **Gain formula in cascode:**

$$A_d = g_m (r_{ds1} \parallel r_{ds2})$$

   - **Advantages:**
     - **Increases gain** without increasing power consumption.
     - **Improves bandwidth** by reducing parasitic capacitance.
3. **Current Mirror Load for Gain Enhancement**
   - Replaces resistor-based loads with **MOSFET current mirrors**, offering:
     - **Higher output resistance**, which improves gain.
     - **Better biasing stability**.



Simulation and Technology Used

Technology Details

•Simulation Software: Cadence Virtuoso

•Technology Node: 180nm CMOS Process

•Supply Voltage: 1.8V

•Simulation Types:

- **DC Analysis:** To analyze operating point & biasing.
- **AC Analysis:** To measure gain, bandwidth, and phase margin.
- **Transient Analysis:** To observe time-domain signal behavior.

Comparison of Simulation Results -

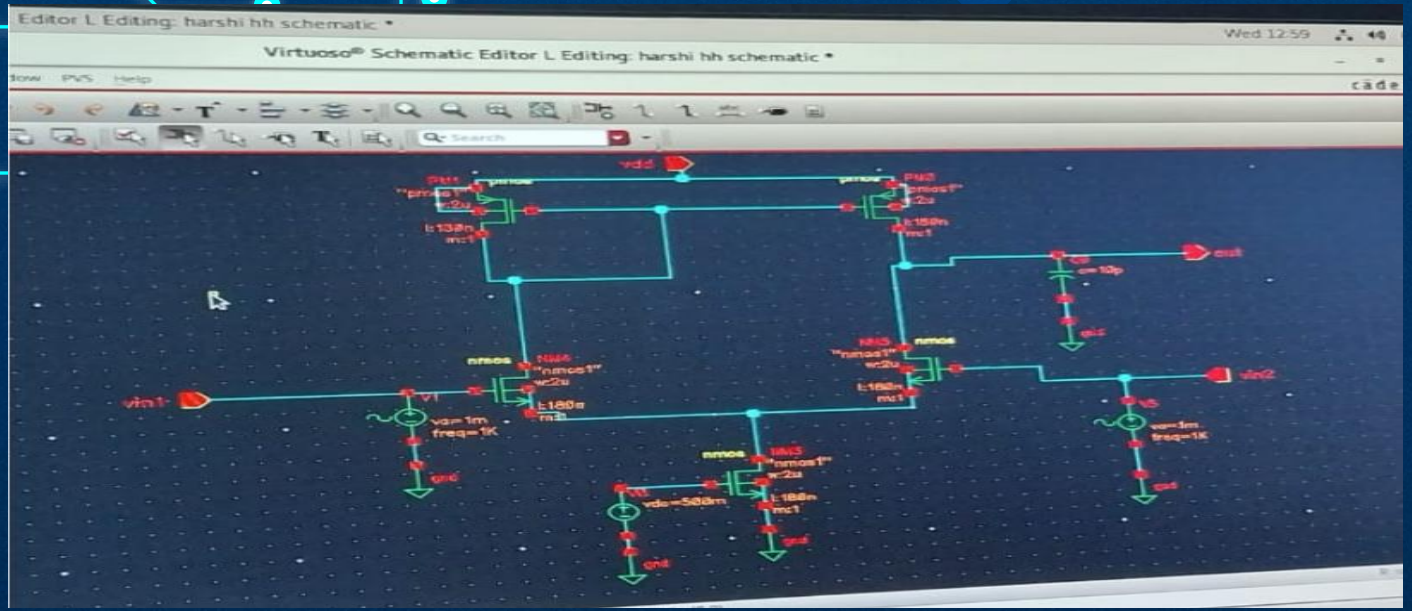
Parameter	IRJET Paper	Your Project (Expected)
Gain (dB)	35.43	30-40
Bandwidth (GHz)	7.98	8-10
Power Dissipation (mW)	1.83	≤ 2.0
CMRR (dB)	80+	85+

Scope of the Project

GLOBAL SCOPE

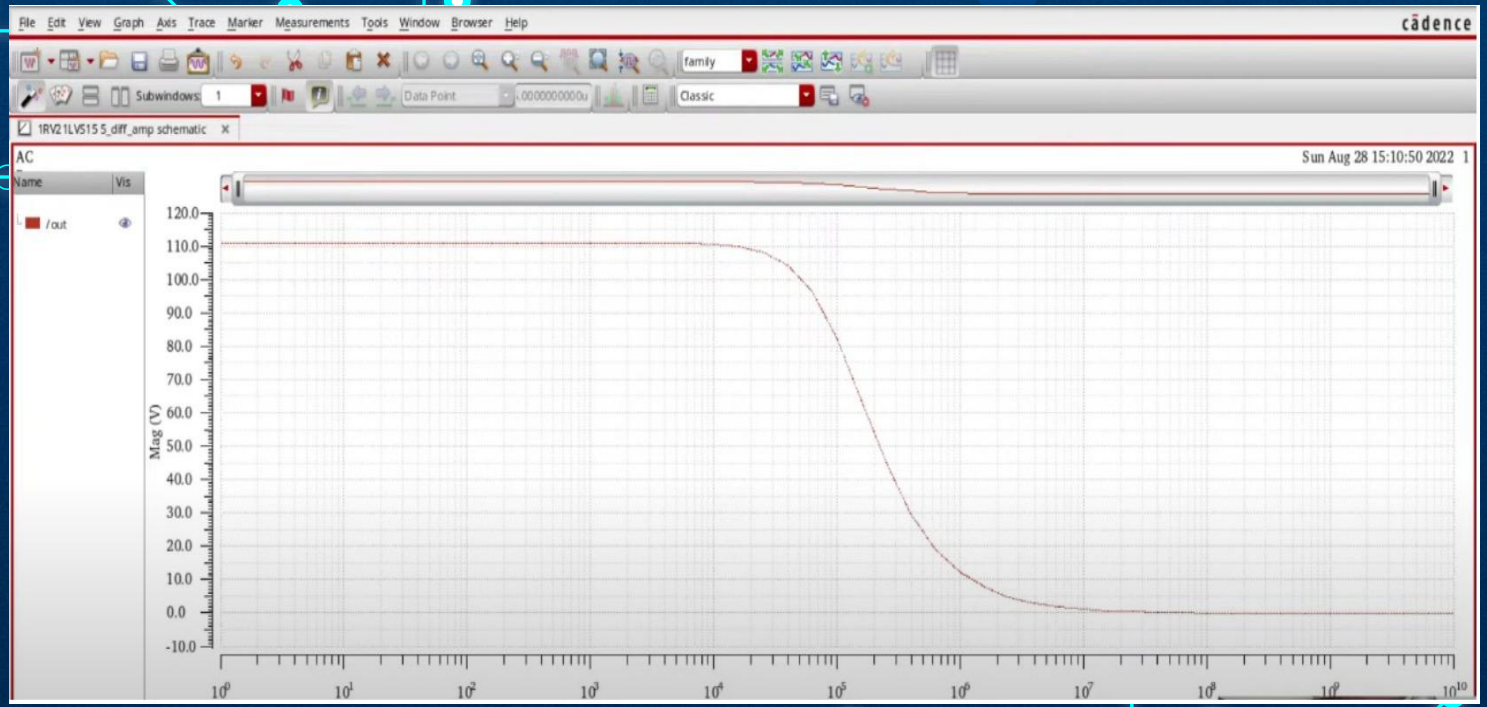
- **Medical Electronics:** Differential amplifiers are widely used in **ECG, EEG, and biosignal amplifiers**.
- **Consumer Electronics:** Low-power designs are essential for **smartphones, audio systems, and IoT devices**.
- **Communication Systems:** Differential amplifiers improve **signal integrity in 5G and high-speed networks**.

Active Load Circuit



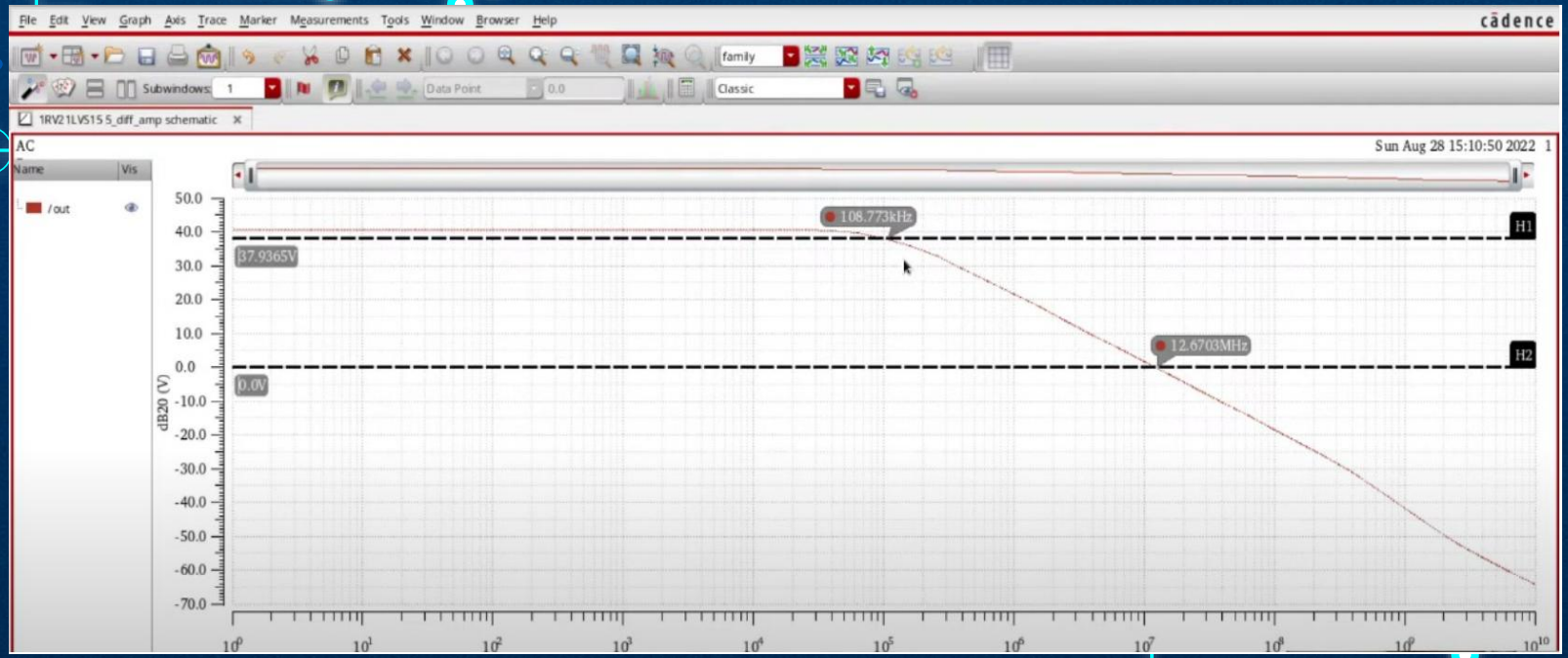
CIRCUIT DIAGRAM OF ACTIVE LOAD DIFFERENTIAL AMPLIFIER

Active Load Circuit



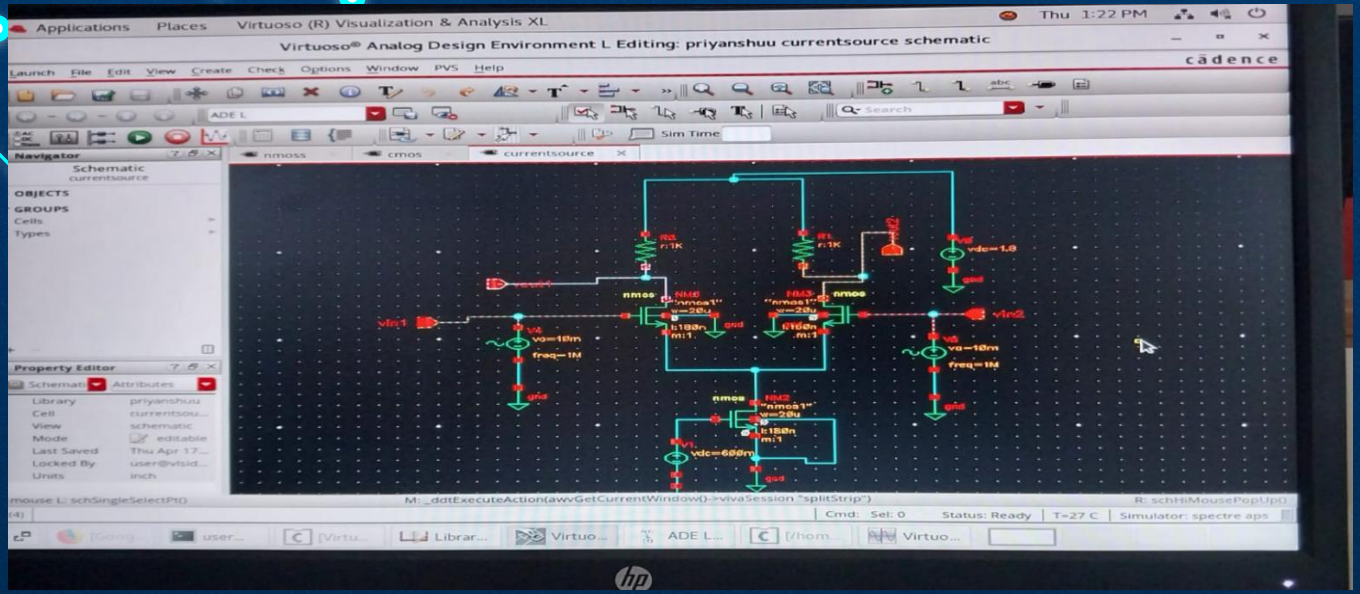
V-F GRAPH OF ACTIVE LOAD DIFFERENTIAL AMPLIFIER

Active Load Circuit



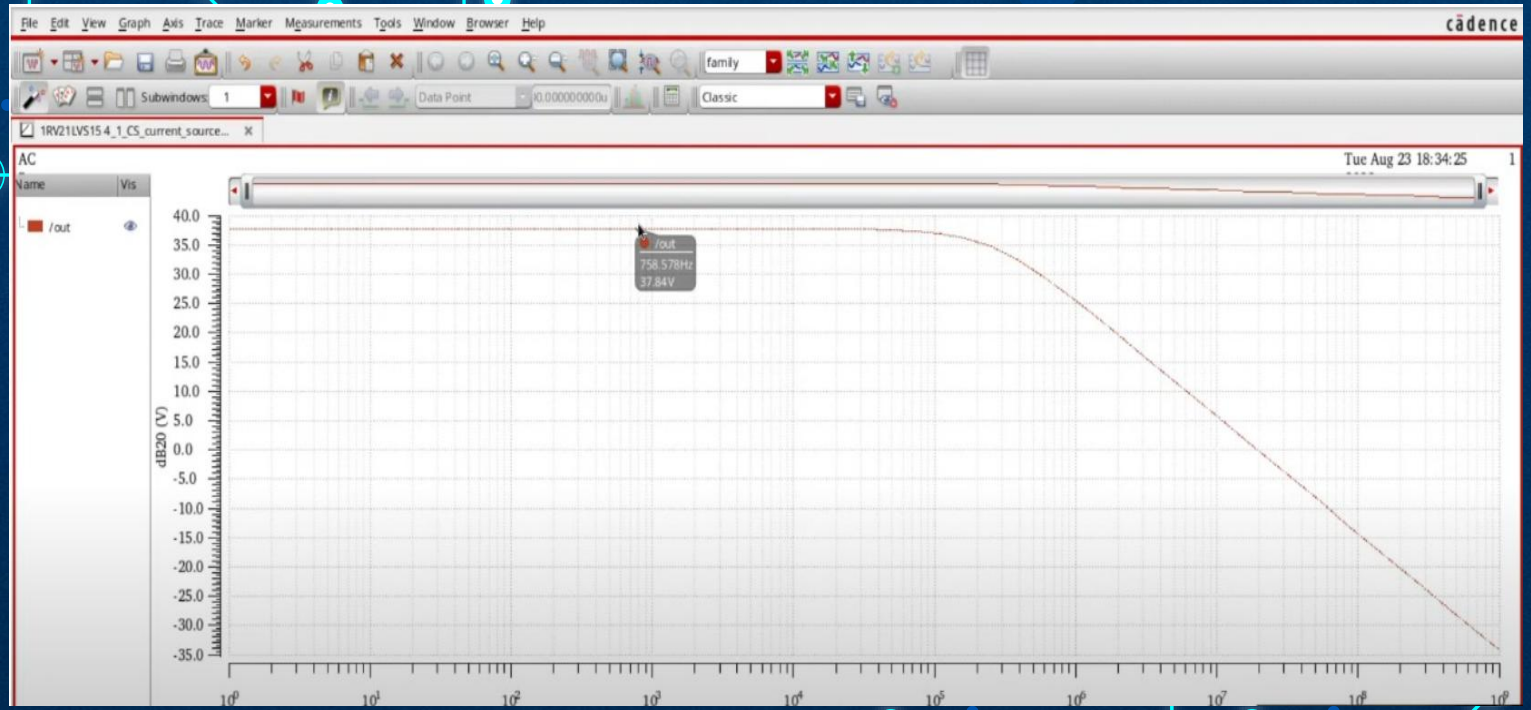
V-F GRAPH OF ACTIVE LOAD DIFFERENTIAL AMPLIFIER

Current source Load Circuit



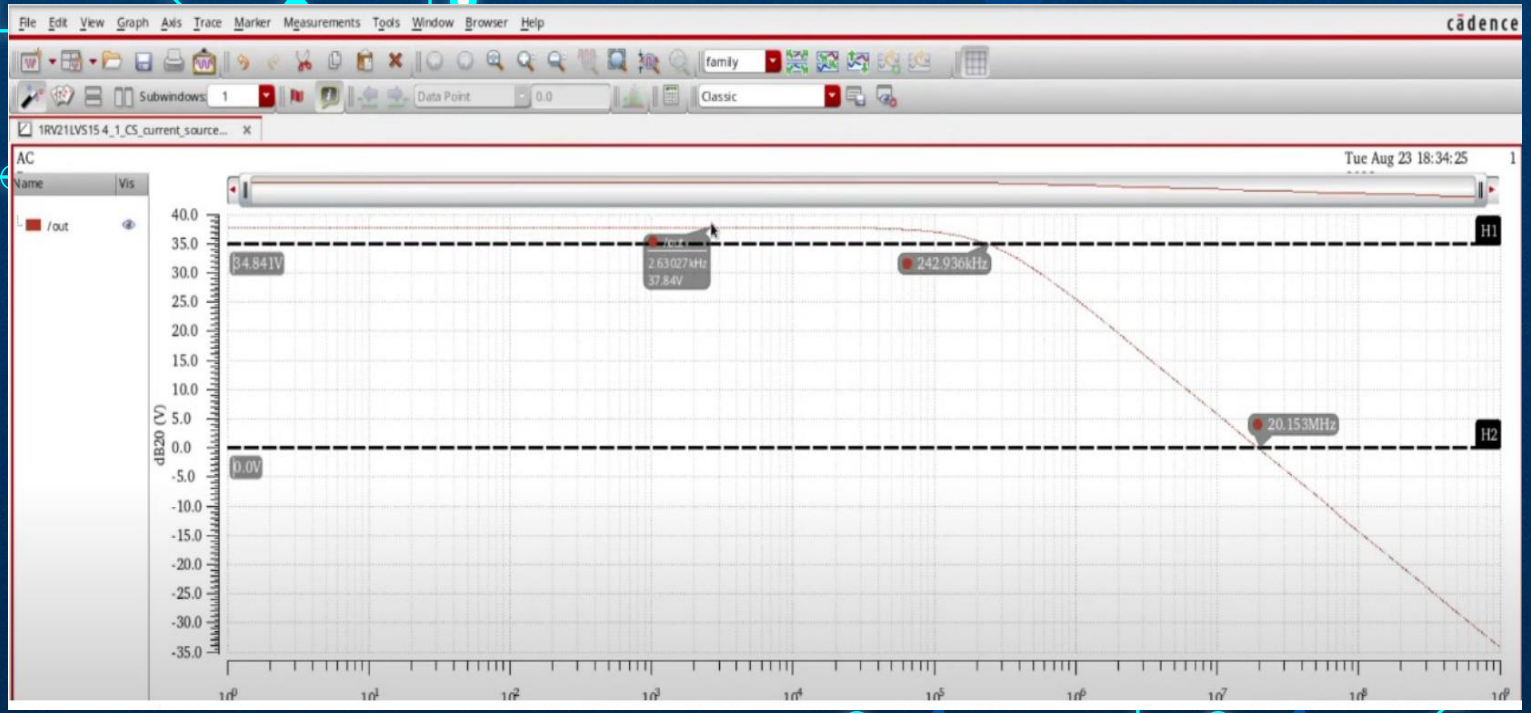
CIRCUIT DIAGRAM OF CURRENT SOURCE LOAD DIFFERENTIAL AMPLIFIER

Current source Load Circuit



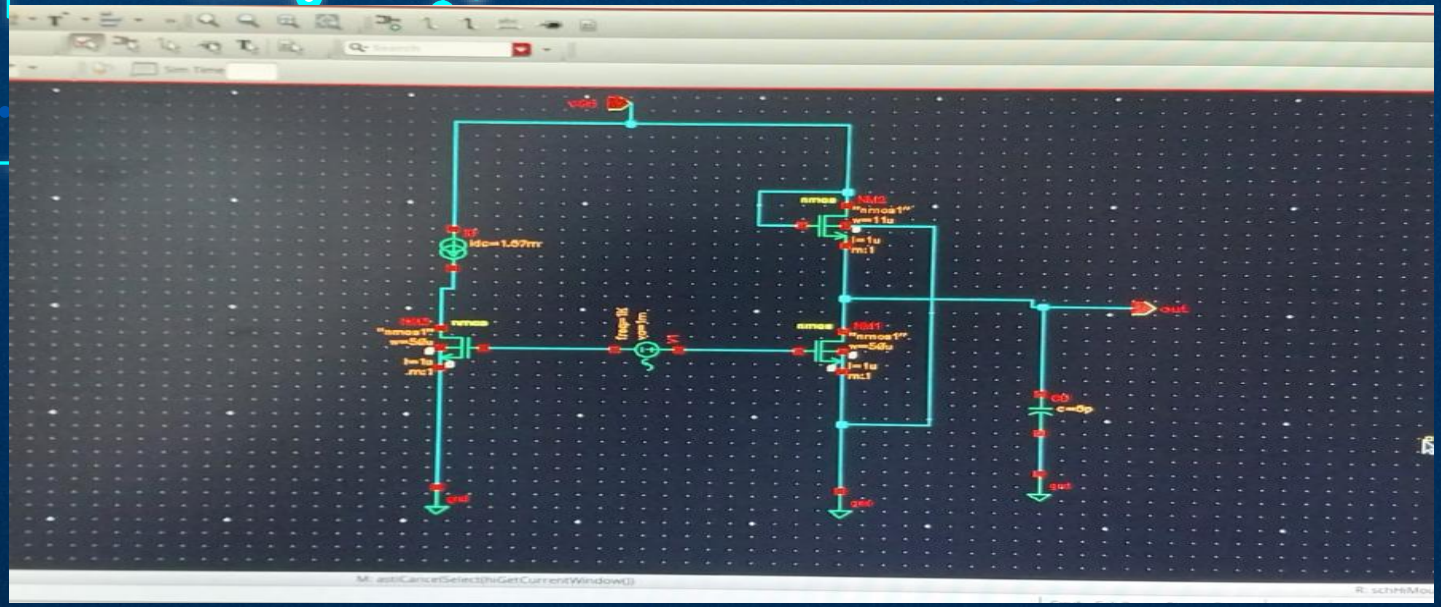
V-F GRAPH OF Current Source Load DIFFERENTIAL AMPLIFIER

Current source Load Circuit



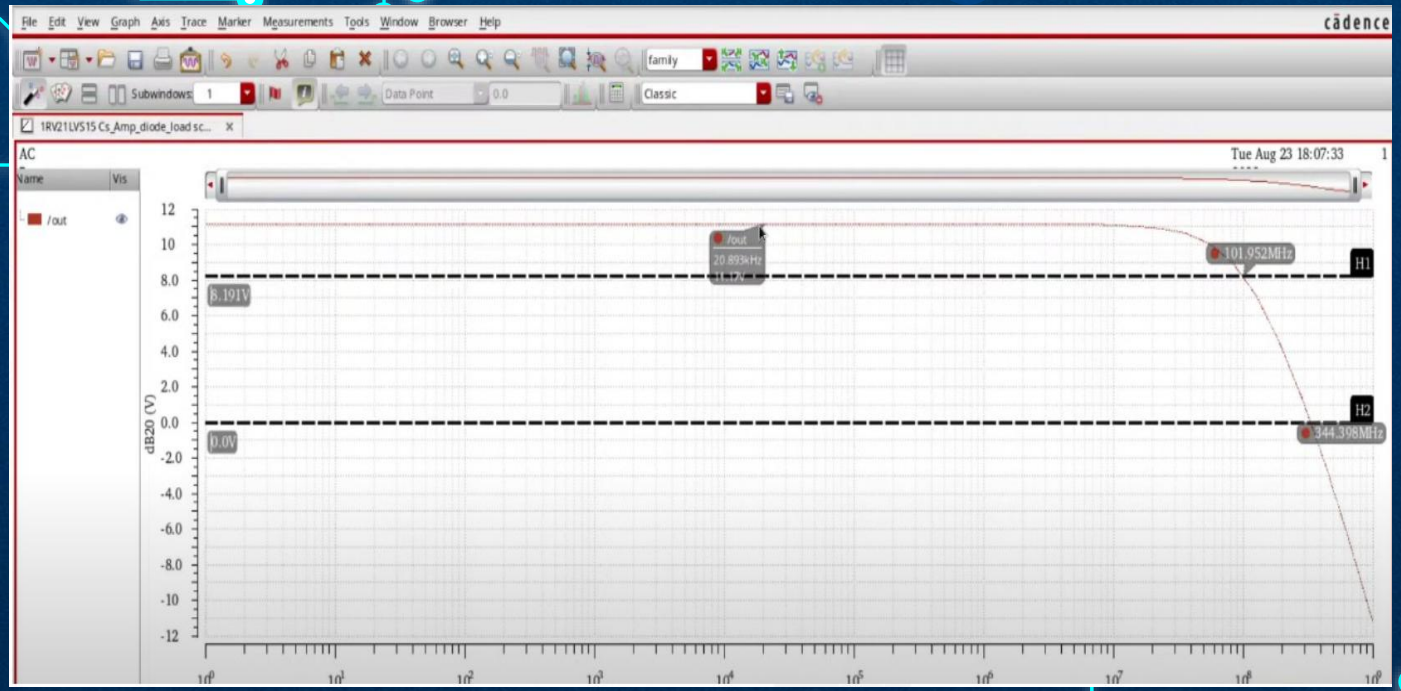
V-F GRAPH OF Current Source LOAD DIFFERENTIAL AMPLIFIER

Diode Connected Load Circuit



CIRCUIT DIAGRAM OF Diode Connected Load DIFFERENTIAL AMPLIFIER

Diode Connected Load Circuit

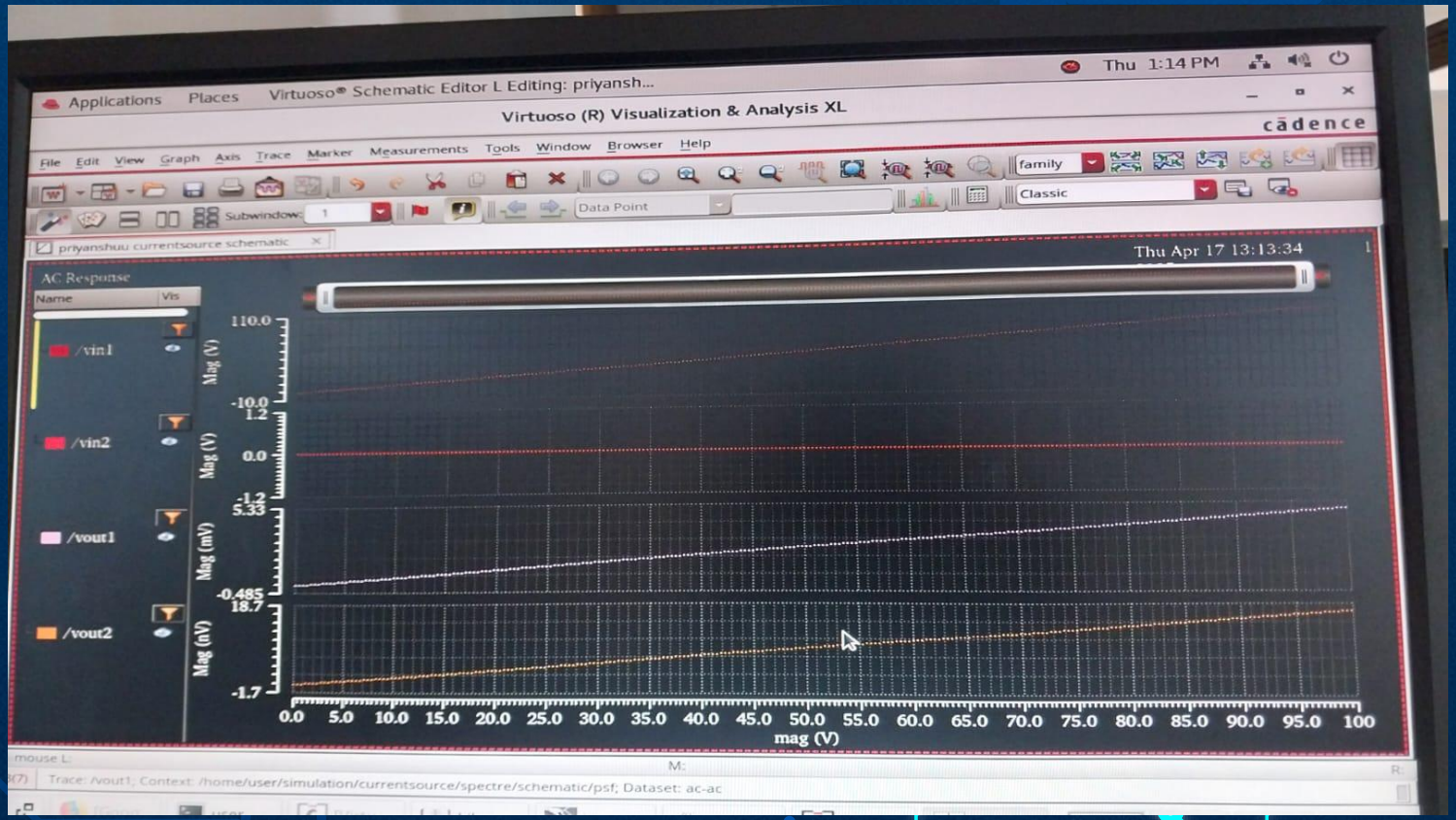


V-F GRAPH OF Diode Connected Load DIFFERENTIAL AMPLIFIER

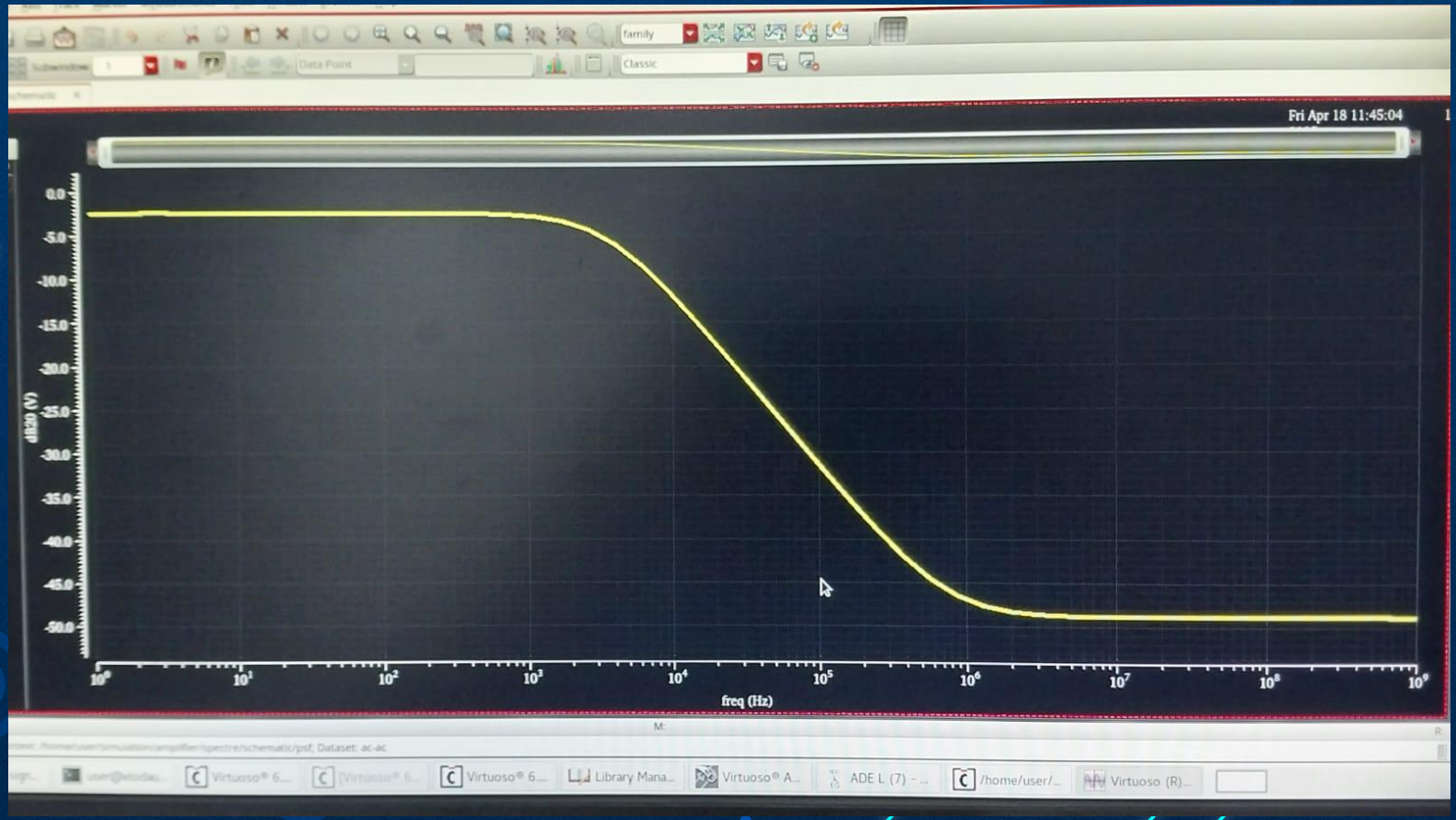
FINAL PARAMETERS COMPARISON TABLE

Feature	Active Load	Current Source Load	Diode Connected Load
Supply Voltage (Vdd)	5V	5V	5V
Output Voltage (Vo)	~1.6V	~1.45V	~0.7V
Tail Current (Itail)	0.32 mA	0.24 mA	0.42 mA
Transconductance (gm)	1.6 mS	1.2 mS	2.1 mS
Output Resistance (ro)	312.5 kΩ	416.67 kΩ	476.19 Ω (very low)
Differential Gain (Ad)	~500	~500	~1
Output Voltage Swing	High	Moderate	Very Low
Power Dissipation (P)	0.256 mW	0.174 mW	0.147 mW
Complexity	Medium	High	Very Low
Best Application	High Gain Amplifiers	Precision Circuits	Fast, Low-power circuits

SOME FAILED RESULTS



SOME FAILED RESULTS

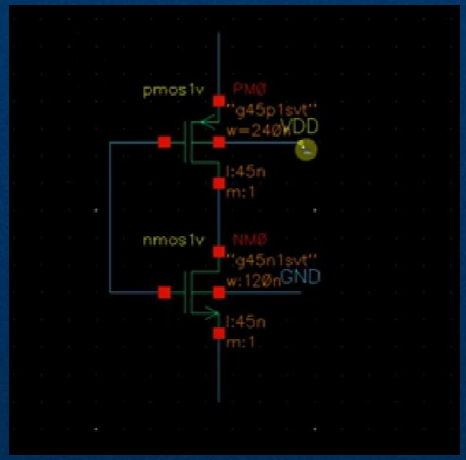


INTRODUCTION TO SOFTWARE

📌 **Cadence Virtuoso** is a leading **EDA tool** for **analog, digital, and mixed-signal circuit design** used in **VLSI and CMOS technology**.

📌 Enables **high-precision simulations** for **low-power, high-gain** circuits like **differential amplifiers**.

📌 Supports **deep-submicron technologies (180nm, 65nm, etc.)** and is widely used in **sensor circuits, amplifiers, and communication systems**.



◆ **Key Features Used in Our Project:**

✓ **Schematic Editor** – Designed the **differential amplifier circuit**.

✓ **Spectre Simulator** – Performed **DC, AC, and transient analysis**.

✓ **Virtuoso Layout Suite** – Ensured **DRC (Design Rule Check) & LVS (Layout vs. Schematic) verification**.

Application in Our Project & Advantages

📌 Used Virtuoso to design, simulate, and optimize differential amplifier topologies.
📌 Compared power efficiency, gain, and noise rejection across different designs.
📌 Implemented power-saving techniques while maintaining high gain and performance.

◆ **Why Virtuoso?**

✓ **Industry-standard for IC design & low-power VLSI applications.**
✓ **High-accuracy simulations for real-world performance analysis.**
✓ **Optimized circuit design for better gain and power efficiency.**

References

"Design of CMOS Two Stage Op-Amp and Differential Amplifier Using Cadence Virtuoso" – A. Vikas, K. Harini, M. Sripriya, T. Shashank (IJCRT)

"Design and Analysis of High Gain Differential Amplifier Using Various Topologies" – Samarla Shilpa, J. Srilatha (IRJET)

"Two Stage CMOS Operational Amplifier Using Cadence 180nm Technology" – Rakshitha M, Rakshitha Urs S, Shreyas R (IJIRSET)

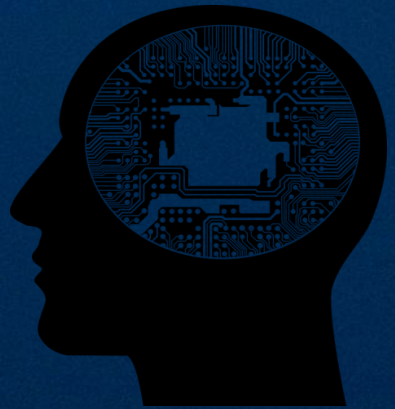
"Design of High Gain OP-AMP using CMOS with 180nm Technology and its Application using Cadence Virtuoso" – Podila Keerthi, R. Chennakeshavulu (IJEECS)

Conclusion & Future Work

CONCLUSION

•The project successfully **optimizes power consumption** while maintaining high **gain and noise rejection**.

•**CMOS technology & advanced topologies (active load, cascode) improve amplifier performance**



FUTURE WORK

1.Exploring Subthreshold Region: Reducing power further using **subthreshold operation**.

2.Integration into IoT Systems: Designing **ultra-low-power sensors**.

3.Fabrication on 65nm Technology: Reducing area and improving efficiency.