VLSI DESIGN AND AUTOMATION SUMMER INTERNSHIP

WEEK 4 SUBMISSION

RESOURCE: WEEK 6 (ENC,NETLIST and DATA files are here)

VERILOG CODE AND WAVE FORM

VERILOG CODE :

```
`timescale 1ns / 1ps
module digital_safe (
    input clk,
    input rst,
    input [31:0] entered_code,
    input [31:0] master_code,
    input [31:0] duress_code,
    input reset_code_button,
    input [31:0] new_code,
    input confirm_reset,
    output reg unlocked,
    output reg alert
);

    reg [1:0] attempts;
    reg [31:0] current_code;
    reg locked;
    reg [19:0] lock_timer;
```

```
    localparam MAX_ATTEMPTS = 2'd3;
    localparam LOCK_TIME = 20'd15_000_000; // Adjust as per clock frequency (e.g., ~5 min for 50MHz)

    always @(posedge clk or posedge rst) begin
        if (rst) begin
            current_code <= 32'h12345678;
            attempts <= 0;
            locked <= 0;
            lock_timer <= 0;
            unlocked <= 0;
            alert <= 0;
        end else begin
            if (locked) begin
                if (lock_timer > 0)
                    lock_timer <= lock_timer - 1;
                else begin
                    locked <= 0;
                    attempts <= 0;
                end
            end else if (reset_code_button && confirm_reset) begin
                current_code <= new_code;
            end else begin
                if (entered_code == current_code || entered_code == master_code) begin
                    unlocked <= 1;
                    alert <= 0;
```

```
            attempts <= 0;
        end else if (entered_code == duress_code) begin
            unlocked <= 1;
            alert <= 1;
            attempts <= 0;
        end else begin
            attempts <= attempts + 1;
            if (attempts == MAX_ATTEMPTS - 1) begin
                locked <= 1;
                lock_timer <= LOCK_TIME;
                unlocked <= 0;
                alert <= 0;
            end
        end
    end
  end

endmodule
```

TEST BENCH CODE :

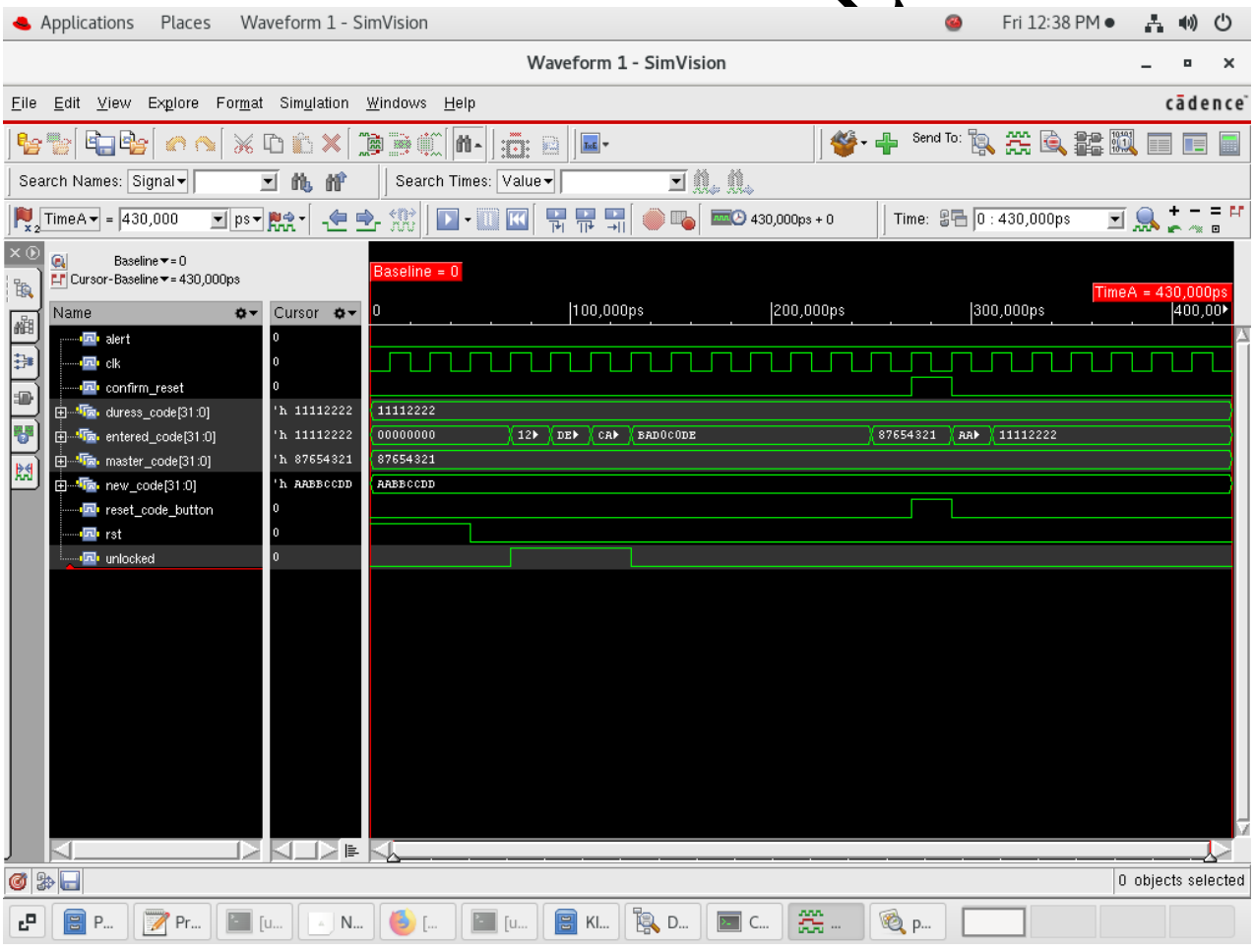
```
`timescale 1ns / 1ps

module tb_digital_safe;

    reg clk;
    reg rst;
    reg [31:0] entered_code;
    reg [31:0] master_code;
    reg [31:0] duress_code;
    reg reset_code_button;
    reg [31:0] new_code;
    reg confirm_reset;
    wire unlocked;
    wire alert;

    digital_safe uut (
        .clk(clk),
        .rst(rst),
        .entered_code(entered_code),
        .master_code(master_code),
        .duress_code(duress_code),
        .reset_code_button(reset_code_button),
        .new_code(new_code),
        .confirm_reset(confirm_reset),
```

```
    .unlocked(unlocked),
    .alert(alert)
);

// Clock Generation
initial begin
    clk = 0;
    forever #10 clk = ~clk; // 50 MHz clock
end

initial begin
    // Initialize Inputs
    rst = 1;
    entered_code = 32'h0;
    master_code = 32'h87654321;
    duress_code = 32'h11112222;
    reset_code_button = 0;
    new_code = 32'hAABBCCDD;
    confirm_reset = 0;

    #50;
    rst = 0;

    // Test correct code
    #20;
```

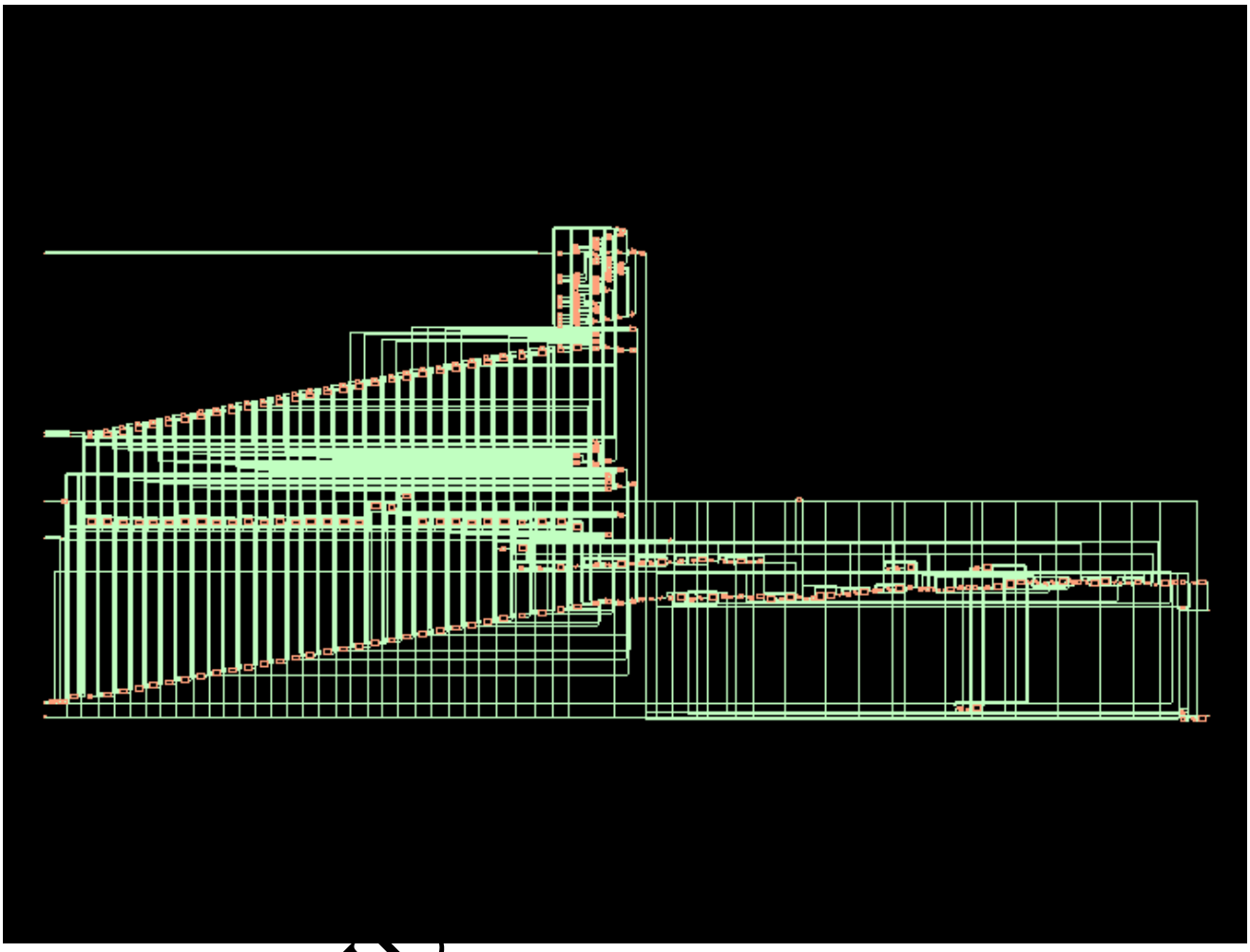
```
entered_code = 32'h12345678;
#20;

// Test incorrect attempts
entered_code = 32'hDEADBEEF; #20;
entered_code = 32'hCAFEBABE; #20;
entered_code = 32'hBAD0C0DE; #20;

// Wait for lock
#100;

// Test master code unlock
entered_code = 32'h87654321; #20;

// Reset password
reset_code_button = 1;
confirm_reset = 1;
#20;
reset_code_button = 0;
confirm_reset = 0;

// Test with new code
entered_code = 32'hAABBCCDD; #20;

// Test duress code
```

```
        entered_code = 32'h11112222; #20;

        #100;
        $stop;
    end

endmodule
```


WAVE FORM :



WEEK 2 :



REPORT (WEEK 2) :

legacy_genus:/> report power

Info : Joules engine is used. [RPT-16]

: Joules engine is being used for the command report_power.

Info : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist

: digital_safe

Info : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%

Info : ACTP-0001 Activity propagation ended for stim#0

Info : PWRA-0001 [PwrInfo] compute_power effective options

: -mode : vectorless

: -skip_propagation : 1

: -frequency_scaling_factor : 1.0

: -use_clock_freq : stim

: -stim :/stim#0

: -fromGenus : 1

Info : ACTP-0001 Timing initialization started

Info : ACTP-0001 Timing initialization ended

Info : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap

: option..

Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless

: flow. Ignoring frequency scaling.

Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode

: of power analysis, ignored this option.

Info : PWRA-0002 Started 'vectorless' power computation.

Info : PWRA-0009 [PwrInfo] Power Computation Progress Report : 100%

Info : PWRA-0002 Finished power computation.

Info : PWRA-0007 [PwrInfo] Completed successfully.

: Info=6, Warn=2, Error=0, Fatal=0

Instance: /digital_safe

Power Unit: W

PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	1.01576e-07	2.60008e-05	2.46144e-06	2.85635e-05	33.88%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	1.57909e-07	3.48826e-05	2.07134e-05	5.57539e-05	66.12%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	2.59485e-07	6.08834e-05	2.31746e-05	8.43174e-05	100.00%
Percentage	0.31%	72.21%	27.48%	100.00%	100.00%

```
legacy_genus:/> report area
====================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jul 25 2025  12:44:06 pm
  Module:                 digital_safe
  Technology library:     fast
  Operating conditions:   fast (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================

  Instance   Module  Cell Count  Cell Area  Net Area  Total Area   Wireload
-----------------------------------------------------------------------------
digital_safe              329      0.000     0.000       0.000 <none> (D)
  (D) = wireload is default in technology library

legacy_genus:/> report timing
====================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
```

Generated on: Jul 25 2025 12:44:09 pm

Module: digital_safe

Technology library: fast

Operating conditions: fast (balanced_tree)

Wireload mode: enclosed

Area mode: timing library

==========

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
current_code_reg[1]/CK				0	+0	0	R
current_code_reg[1]/QN	SDFFRX4	1	2.5	13	+111	111	F
csa_tree_ADD_TC_OP16_groupi_g2187/B					+0	111	
csa_tree_ADD_TC_OP16_groupi_g2187/CO	ADDFXL	1	2.0	37	+66	176	F
csa_tree_ADD_TC_OP16_groupi_g2186/CI					+0	176	
csa_tree_ADD_TC_OP16_groupi_g2186/CO	ADDFXL	1	2.0	38	+67	243	F
csa_tree_ADD_TC_OP16_groupi_g2185/CI					+0	243	
csa_tree_ADD_TC_OP16_groupi_g2185/CO	ADDFXL	1	2.0	38	+67	310	F
csa_tree_ADD_TC_OP16_groupi_g2184/CI					+0	310	
csa_tree_ADD_TC_OP16_groupi_g2184/CO	ADDFXL	1	2.0	38	+67	377	F
csa_tree_ADD_TC_OP16_groupi_g2183/CI					+0	377	
csa_tree_ADD_TC_OP16_groupi_g2183/CO	ADDFXL	1	2.0	38	+67	444	F

```
csa_tree_ADD_TC_OP16_groupi_g2182/CI                    +0    444
csa_tree_ADD_TC_OP16_groupi_g2182/CO  ADDFXL      1  2.0  38  +67    511 F
csa_tree_ADD_TC_OP16_groupi_g2181/CI                    +0    511
csa_tree_ADD_TC_OP16_groupi_g2181/CO  ADDFXL      1  2.0  38  +67    578 F
csa_tree_ADD_TC_OP16_groupi_g2180/CI                    +0    578
csa_tree_ADD_TC_OP16_groupi_g2180/CO  ADDFXL      1  2.0  38  +67    644 F
csa_tree_ADD_TC_OP16_groupi_g2179/CI                    +0    644
csa_tree_ADD_TC_OP16_groupi_g2179/CO  ADDFXL      1  2.0  38  +67    711 F
csa_tree_ADD_TC_OP16_groupi_g2178/CI                    +0    711
csa_tree_ADD_TC_OP16_groupi_g2178/CO  ADDFXL      1  2.0  38  +67    778 F
csa_tree_ADD_TC_OP16_groupi_g2177/CI                    +0    778
csa_tree_ADD_TC_OP16_groupi_g2177/CO  ADDFXL      1  2.0  38  +67    845 F
csa_tree_ADD_TC_OP16_groupi_g2176/CI                    +0    845
csa_tree_ADD_TC_OP16_groupi_g2176/CO  ADDFXL      1  2.0  38  +67    912 F
csa_tree_ADD_TC_OP16_groupi_g2175/CI                    +0    912
csa_tree_ADD_TC_OP16_groupi_g2175/CO  ADDFXL      1  2.0  38  +67    979 F
csa_tree_ADD_TC_OP16_groupi_g2174/CI                    +0    979
csa_tree_ADD_TC_OP16_groupi_g2174/CO  ADDFXL      1  2.0  38  +67   1046 F
csa_tree_ADD_TC_OP16_groupi_g2173/CI                    +0   1046
csa_tree_ADD_TC_OP16_groupi_g2173/CO  ADDFXL      1  2.0  38  +67   1113 F
csa_tree_ADD_TC_OP16_groupi_g2172/CI                    +0   1113
csa_tree_ADD_TC_OP16_groupi_g2172/CO  ADDFXL      1  2.0  38  +67   1180 F
csa_tree_ADD_TC_OP16_groupi_g2171/CI                    +0   1180
```

csa_tree_ADD_TC_OP16_groupi_g2171/CO ADDFXL 1 2.0 38 +67 1246 F

csa_tree_ADD_TC_OP16_groupi_g2170/CI +0 1246

csa_tree_ADD_TC_OP16_groupi_g2170/CO ADDFXL 1 2.0 38 +67 1313 F

csa_tree_ADD_TC_OP16_groupi_g2169/CI +0 1313

csa_tree_ADD_TC_OP16_groupi_g2169/CO ADDFXL 1 2.0 38 +67 1380 F

csa_tree_ADD_TC_OP16_groupi_g2168/CI +0 1380

csa_tree_ADD_TC_OP16_groupi_g2168/CO ADDFXL 1 2.0 38 +67 1447 F

csa_tree_ADD_TC_OP16_groupi_g2167/CI +0 1447

csa_tree_ADD_TC_OP16_groupi_g2167/CO ADDFXL 1 2.0 38 +67 1514 F

csa_tree_ADD_TC_OP16_groupi_g2166/CI +0 1514

csa_tree_ADD_TC_OP16_groupi_g2166/CO ADDFXL 1 2.0 38 +67 1581 F

csa_tree_ADD_TC_OP16_groupi_g2165/CI +0 1581

csa_tree_ADD_TC_OP16_groupi_g2165/CO ADDFXL 1 2.0 38 +67 1648 F

csa_tree_ADD_TC_OP16_groupi_g2164/CI +0 1648

csa_tree_ADD_TC_OP16_groupi_g2164/CO ADDFXL 1 2.0 38 +67 1715 F

csa_tree_ADD_TC_OP16_groupi_g2163/CI +0 1715

csa_tree_ADD_TC_OP16_groupi_g2163/CO ADDFXL 1 2.0 38 +67 1782 F

csa_tree_ADD_TC_OP16_groupi_g2162/CI +0 1782

csa_tree_ADD_TC_OP16_groupi_g2162/CO ADDFXL 1 2.0 38 +67 1849 F

csa_tree_ADD_TC_OP16_groupi_g2161/CI +0 1849

csa_tree_ADD_TC_OP16_groupi_g2161/CO ADDFXL 1 2.0 38 +67 1916 F

csa_tree_ADD_TC_OP16_groupi_g2160/CI +0 1916

csa_tree_ADD_TC_OP16_groupi_g2160/CO ADDFXL 1 2.0 38 +67 1982 F

csa_tree_ADD_TC_OP16_groupi_g2159/CI +0 1982

csa_tree_ADD_TC_OP16_groupi_g2159/CO ADDFXL 1 2.0 38 +67 2049 F

csa_tree_ADD_TC_OP16_groupi_g2158/CI +0 2049

csa_tree_ADD_TC_OP16_groupi_g2158/CO ADDFXL 1 1.5 33 +64 2114 F

csa_tree_ADD_TC_OP16_groupi_g2/C +0 2114

csa_tree_ADD_TC_OP16_groupi_g2/Y XNOR3XL 1 0.9 28 +47 2161 R

g5348/D +0 2161

g5348/Y NAND4X1 1 0.9 54 +32 2192 F

g5497/AN +0 2192

g5497/Y NAND4BBX4 1 3.3 58 +70 2262 F

g5356/D +0 2262

g5356/Y NOR4BBX4 1 0.7 50 +26 2288 R

g5178/B1 +0 2288

g5178/Y AO22X1 2 1.2 20 +45 2332 R

g5174/B +0 2332

g5174/Y OR2X1 3 1.9 18 +26 2358 R

g5173/B +0 2358

g5173/Y OR2X1 3 2.2 20 +26 2384 R

g5168/B +0 2384

g5168/Y OR2X1 4 3.8 31 +32 2416 R

g5166/A +0 2416

g5166/Y CLKINVX2 5 3.9 19 +17 2433 F

g5143/B +0 2433

g5143/Y OR2X1 2 2.4 24 +39 2472 F

g5139/A +0 2472

g5139/Y CLKINVX2 11 7.0 28 +20 2491 R

g5132/B0 +0 2491

g5132/Y AO21X2 2 1.2 17 +31 2522 R

g5113/A1 +0 2522

g5113/Y AO21X2 1 0.8 16 +44 2566 R

lock_timer_reg[16]/D DFFRHQX8 +0 2566

lock_timer_reg[16]/CK setup 0 +35 2602 R

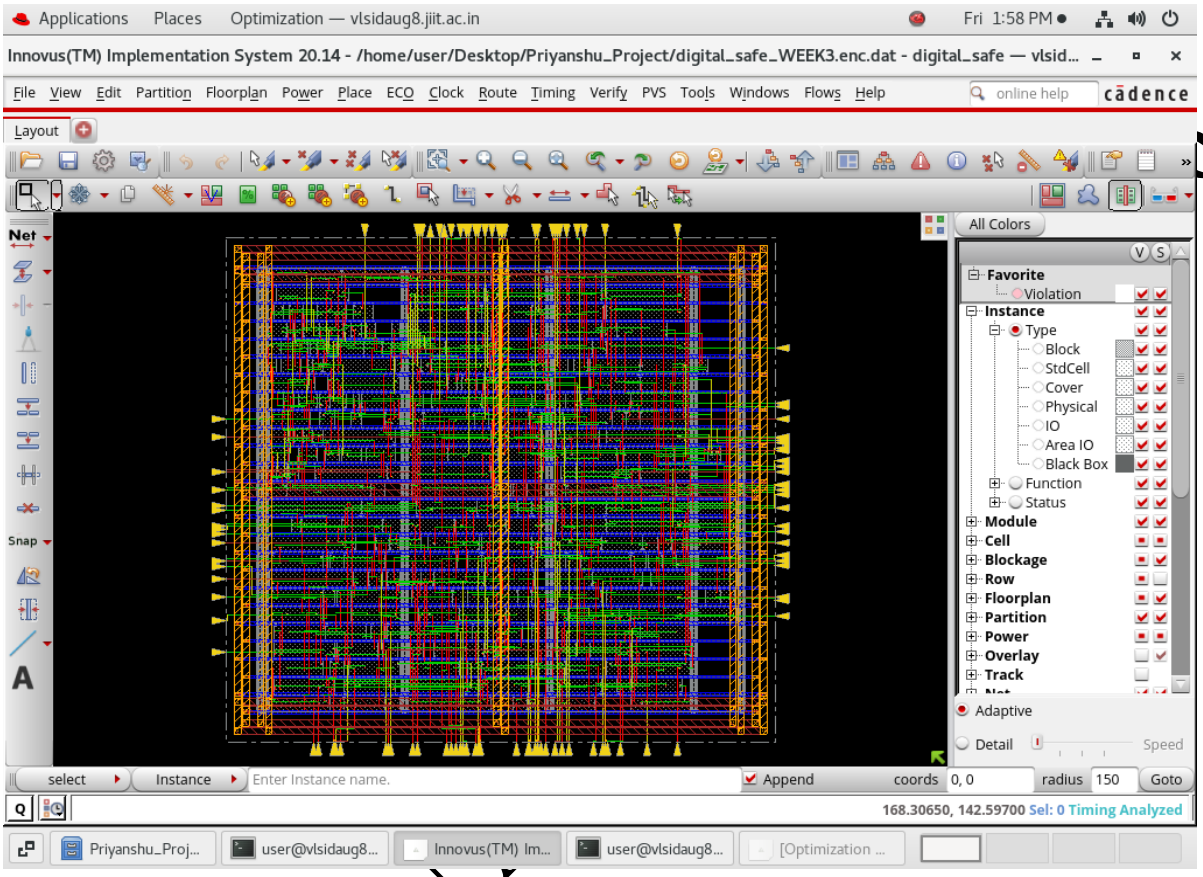
Timing slack : UNCONSTRAINED

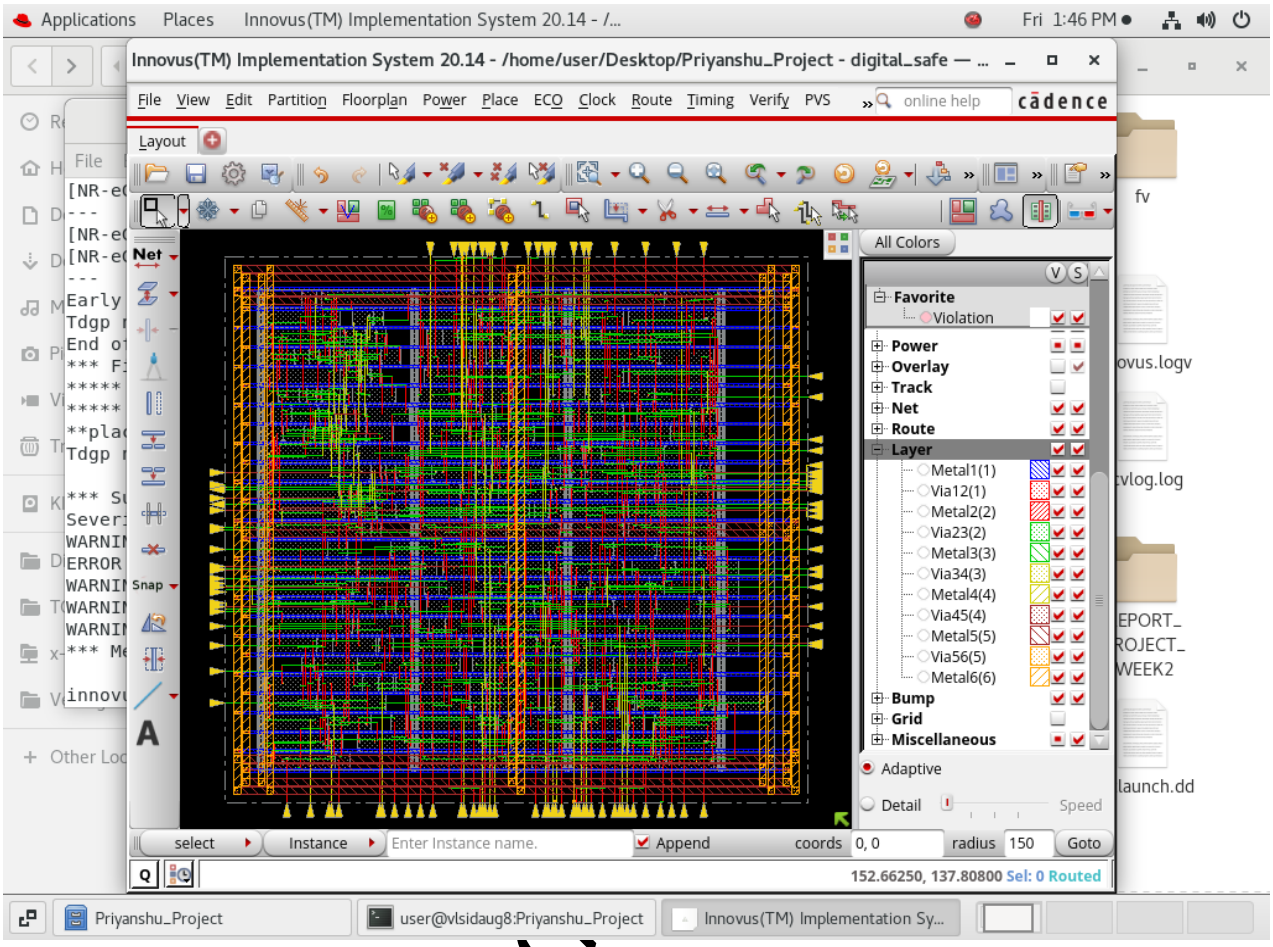
Start-point : current_code_reg[1]/CK

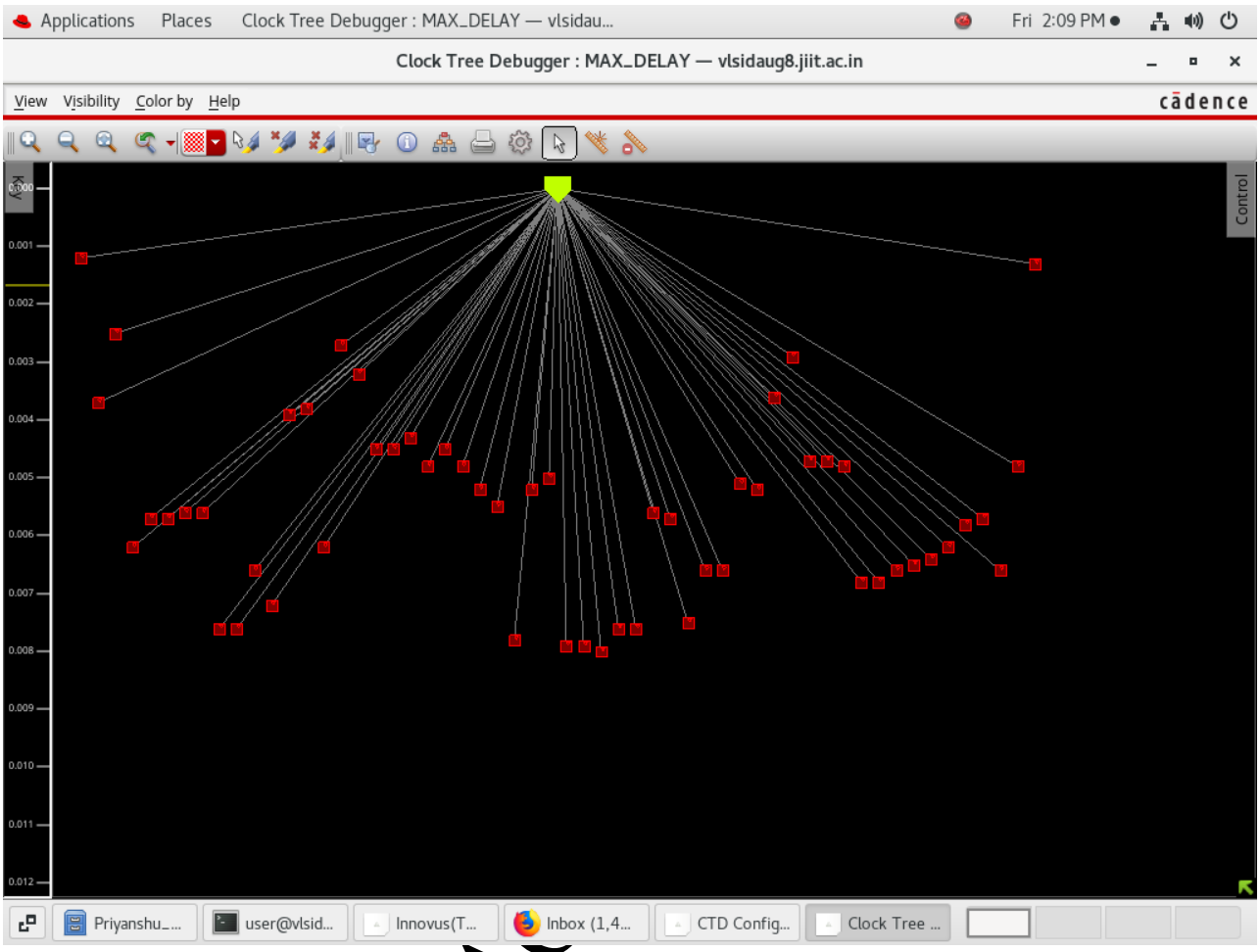
End-point : lock_timer_reg[16]/D

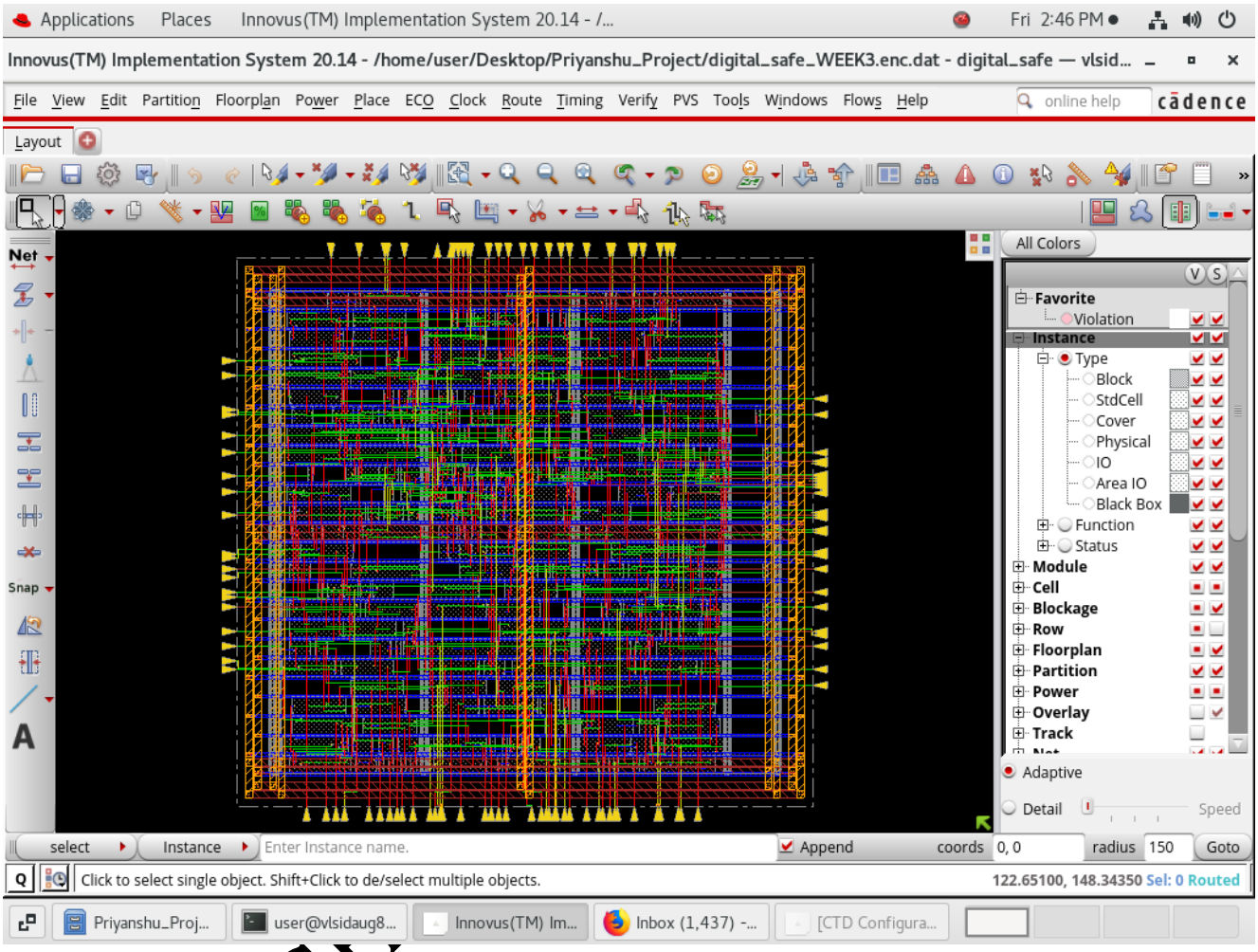
WEEK 3 & WEEK 4 :

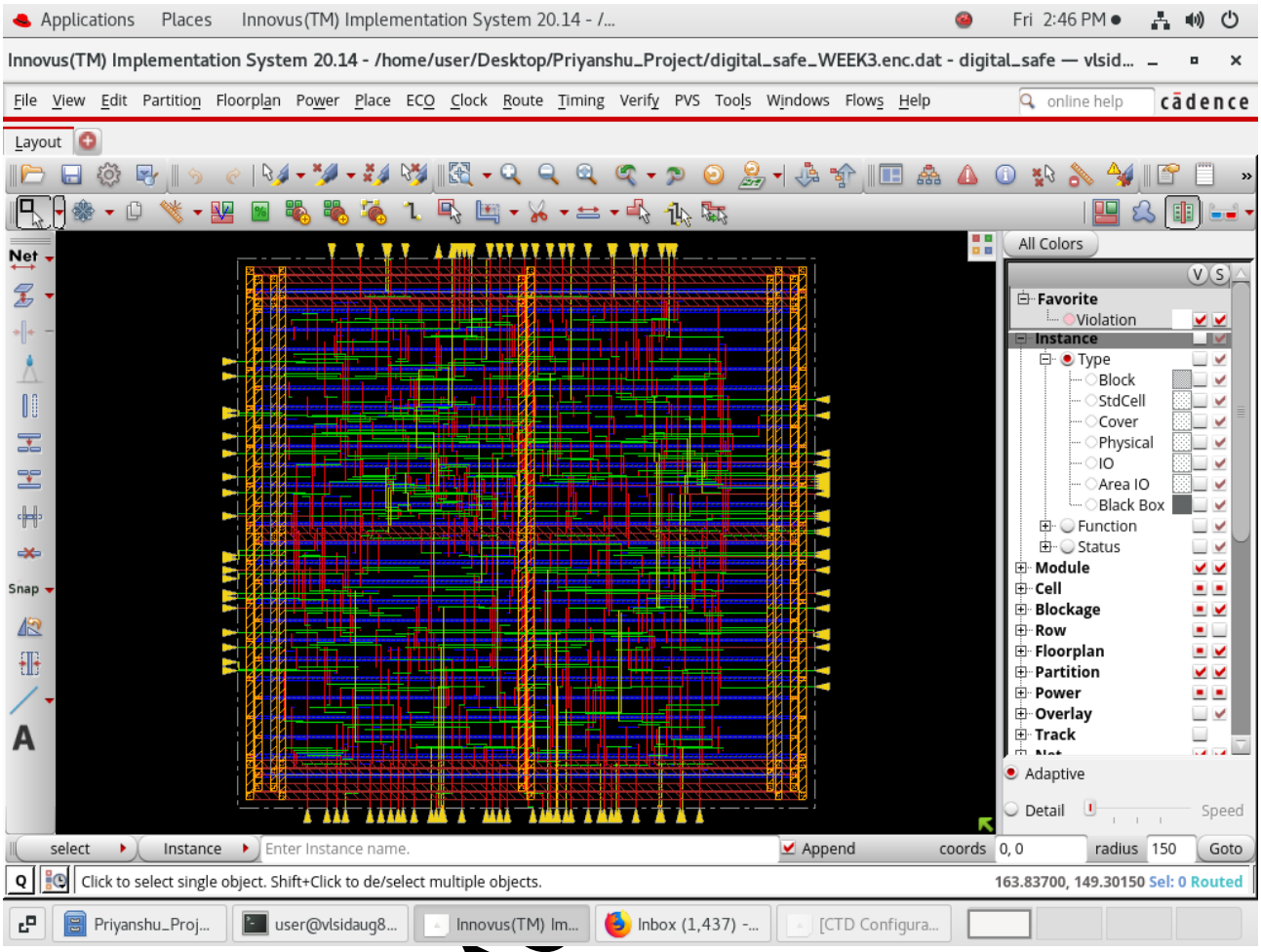
FLOOR PLACEMENT , POWER PLANNING , ROUTING , CTS








Applications
Places
Innovus(TM) Implementation System 20.14 - /...
Fri 2:46 PM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/Priyanshu_Project/digital_safe_WEEK3.enc.dat - digital_safe — vlsid...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Net
Snap
A
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords
0, 0
radius
150
Goto
Click to select single object. Shift+Click to de/select multiple objects.
122.65100, 148.34350 Sel: 0 Routed
Priyanshu_Proj...
user@vlsidaug8...
Innovus(TM) Im...
Inbox (1,437) -...
[CTD Configura...


Applications
Places
Innovus(TM) Implementation System 20.14 - /...
Fri 2:46 PM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/Priyanshu_Project/digital_safe_WEEK3.enc.dat - digital_safe — vlsid...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Net
Snap
A
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords
0, 0
radius
150
Goto
Click to select single object. Shift+Click to de/select multiple objects.
163.83700, 149.30150 Sel: 0 Routed
Priyanshu_Proj...
user@vlsidaug8...
Innovus(TM) Im...
Inbox (1,437) -...
[CTD Configura...

REPORT (WEEK 4) :

```
------------------------------------------------------------

        timeDesign Summary

------------------------------------------------------------
```

Setup views included:

WORST

```
+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|          WNS (ns):|  0.000  |   N/A   |  0.000  |
|          TNS (ns):|  0.000  |   N/A   |  0.000  |
|   Violating Paths:|    0    |   N/A   |    0    |
|        All Paths:|    0    |   N/A   |    0    |
+--------------------+---------+---------+---------+
```

```
+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
```

| max_cap | 1 (1) | -0.149 | 1 (1) |

| max_tran | 0 (0) | 0.000 | 0 (0) |

| max_fanout | 0 (0) | 0 | 0 (0) |

| max_length | 0 (0) | 0 | 0 (0) |

+----------+----------+----------+----------+

Density: 84.653%

Routing Overflow: 0.00% H and 0.34% V

Reported timing to dir timingReports

Total CPU time: 0.16 sec

Total Real time: 0.0 sec

Total Memory Usage: 1469.136719 Mbytes

*** timeDesign #1 [finish] : cpu/real = 0:00:00.1/0:00:00.6 (0.3), totSession cpu/real = 0:00:17.8/0:01:20.6 (0.2), mem = 1469.1M

innovus 1>

innovus 1> report_power

Power Net Detected:

Voltage	Name
0V	VSS
0.9V	VDD

Using Power View: WORST.

Set Default Frequency 100MHz.

Begin Power Analysis

0V	VSS
0.9V	VDD

Begin Processing Timing Library for Power Calculation

Begin Processing Timing Library for Power Calculation

Begin Processing Power Net/Grid for Power Calculation

Ended Processing Power Net/Grid for Power Calculation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1083.79MB/2621.09MB/1083.82MB)

Begin Processing Timing Window Data for Power Calculation

Ended Processing Timing Window Data for Power Calculation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1083.91MB/2621.09MB/1083.91MB)

Begin Processing User Attributes

Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1083.97MB/2621.09MB/1083.97MB)

Begin Processing Signal Activity

Starting Levelizing

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT)

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 10%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 20%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 30%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 40%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 50%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 60%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 70%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 80%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 90%

Finished Levelizing

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT)

Starting Activity Propagation

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT)

** INFO: (VOLTUS_POWR-1356): No default input activity has been set. Defaulting to 0.2.

Use 'set_default_switching_activity -input_activity' command to change the default activity value.

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 10%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 20%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 30%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 40%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 50%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 60%

Finished Activity Propagation

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT)

Ended Processing Signal Activity: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1084.23MB/2621.09MB/1084.23MB)

Begin Power Computation

# of cell(s) missing both power/leakage table: 0

# of cell(s) missing power table: 0

# of cell(s) missing leakage table: 0

# of MSMV cell(s) missing power_level: 0

Starting Calculating power

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT)

... Calculating switching power

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 10%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 20%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 30%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 40%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 50%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 60%

... Calculating internal and leakage power

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 70%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 80%

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT): 90%

Finished Calculating power

2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT)

Ended Power Computation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1084.67MB/2621.09MB/1084.68MB)

Begin Processing User Attributes

Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1084.68MB/2621.09MB/1084.75MB)

Ended Power Analysis: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1084.75MB/2621.09MB/1084.75MB)

Begin Boundary Leakage Calculation

Ended Boundary Leakage Calculation: (cpu=0:00:00, real=0:00:00,

mem(process/total/peak)=1084.75MB/2621.09MB/1084.76MB)

Begin Static Power Report Generation

*----------

* Innovus 20.14-s095_1 (64bit) 04/19/2021 14:41 (Linux 2.6.32-431.11.2.el6.x86_64)

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*

* Date & Time: 2025-Jul-25 13:56:14 (2025-Jul-25 08:26:14 GMT)

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*

* Design: digital_safe

*

* Liberty Libraries used:

* WORST: /home/user/Desktop/Priyanshu_Project/digital_safe_WEEK3.enc.dat/libs/lib/typ/slow.lib

*

* Parasitic Files used:

*

* Power View : WORST

*

* User-Defined Activity : N.A.

*

* Activity File: N.A.

*

* Hierarchical Global Activity: N.A.

*

* Global Activity: N.A.

*

* Sequential Element Activity: N.A.

*

* Primary Input Activity: 0.200000

*

* Default icg ratio: N.A.

*

* Global Comb ClockGate Ratio: N.A.

*

* Power Units = 1mW

*

* Time Units = 1e-09 secs

*

* report_power

*

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*

Total Power

Total Internal Power: 0.03519662 70.5921%

Total Switching Power: 0.01457984 29.2421%

Total Leakage Power: 0.00008270 0.1659%

Total Power: 0.04985916

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.01414	0.001209	3.199e-05	0.01538	30.86
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.02105	0.01337	5.071e-05	0.03447	69.14
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.0352	0.01458	8.27e-05	0.04986	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Default	0.9	0.004369	0	1.462e-05	0.004384	8.792
VDD	0.9	0.03083	0.01421	6.808e-05	0.0451	90.46

* Power Distribution Summary:

* Highest Average Power: g1426 (INVXL): 0.001766

* Highest Leakage Power: current_code_reg[31] (SDFFRHQX8): 7.563e-07

* Total Cap: 1.92485e-12 F

* Total instances in design: 329

* Total instances in design with no power: 0

* Total instances in design with no activty: 0

* Total Fillers and Decap: 0

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1084.98MB/2621.09MB/1685.09MB)

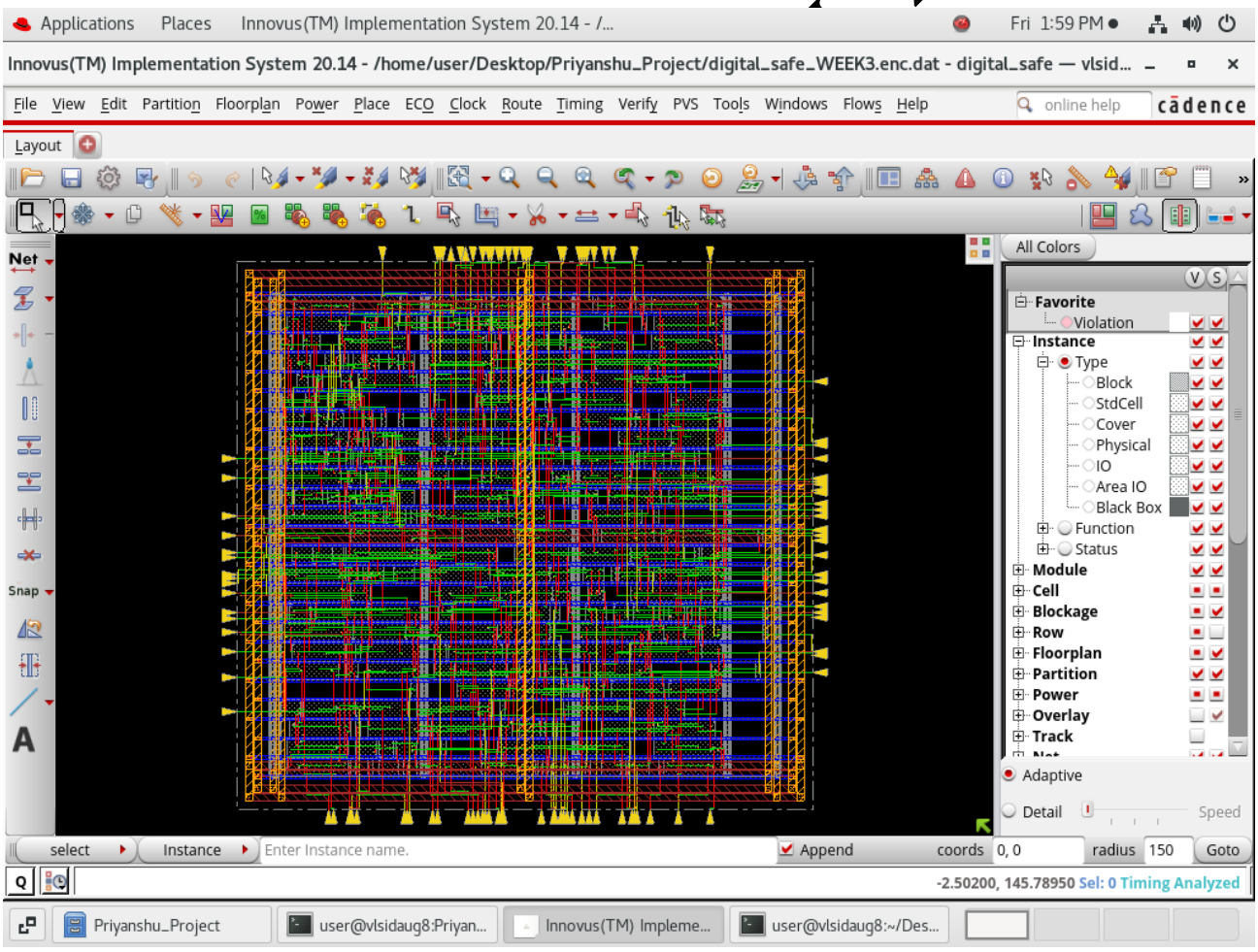
1

innovus 2> report_area

Hinst Name	Module Name	Inst Count	Total Area
digital_safe		329	13649.516

innovus 3>

OPTIMIZED CIRCUIT DESIGN :



PRIYANSHU AGGARWAL 2210236