JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY, NOIDA

Summer Internship Report

Submitted To:	Submitted By:	
Dr. RishiBrind Upadhyay	Enrolment No.	Name
Dr. Shivani	22102236	Priyanshu Aggarwal

VLSI design flow explained RTL to GDS II

1. **RTL (Register-Transfer Level) Design**

    - Write HDL (Hardware Description Language) code in Verilog or VHDL to describe the digital circuit.
    - RTL code describes the circuit's behavior in terms of registers, combinational logic, and clocked operations.

2. **Synthesis**

    - Convert RTL code into a netlist using a synthesis tool (e.g., Design Compiler).
    - The netlist contains gates and connections.
    - Optimize the netlist for area, power, and timing.

3. **DFT (Design for Testability)**

    - Insert scan chains and test logic to improve testability.
    - Ensure the design is testable and can be debugged.

4. **Place and Route**

    - **Floorplanning**: Plan the placement of blocks and IOs on the chip.
    - **Placement**: Place the standard cells (logic gates) on the chip.
    - **Clock Tree Synthesis**: Design the clock distribution network.
    - **Routing**: Connect the placed cells with wires.

5. Timing Analysis and Optimization

- Verify the design meets timing constraints (setup and hold times).
- Optimize the design for timing, area, and power.

6. Physical Verification

- **DRC (Design Rule Checking)**: Verify the design meets foundry-specific design rules.
- **LVS (Layout Versus Schematic)**: Verify the layout matches the netlist.
- **Antenna Effect**: Check for antenna effects and fix them.

7. GDSII Generation

- Create the final GDSII file for tape-out.
- The GDSII file contains the physical layout of the design.

WEEK 1
Cadence Entry and Simulations Verilog Codes and Waveforms

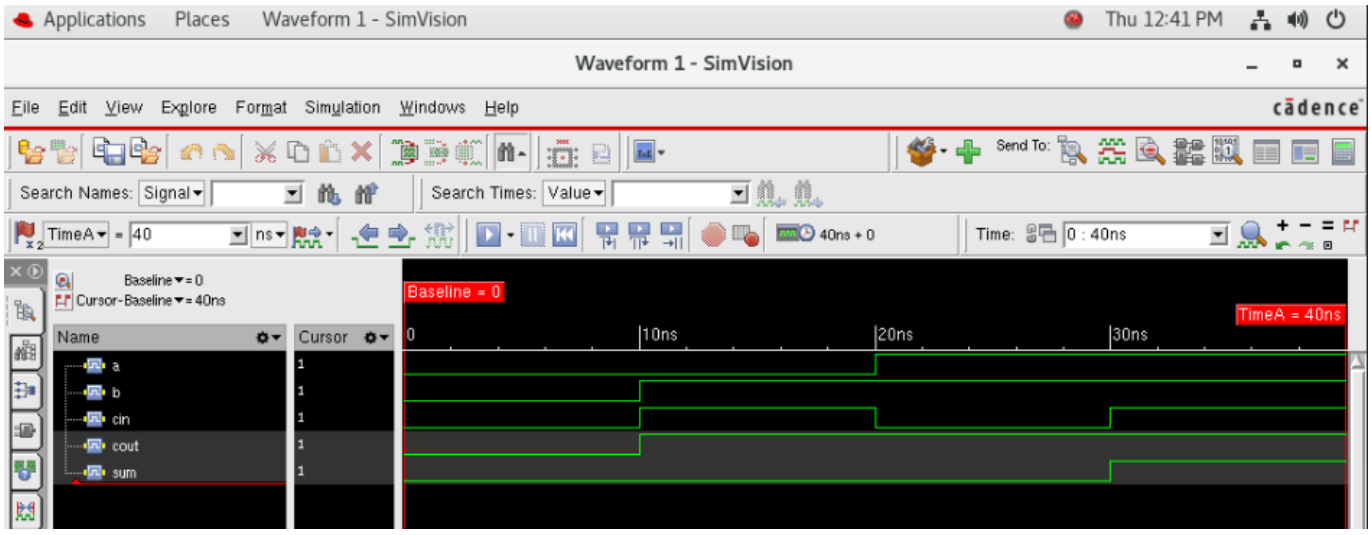
FULL ADDER:

```
module full_adder(input a, input b, input cin, output sum, output cout);
    assign {cout, sum} = a + b + cin;
endmodule
```

Test bench:

```
module full_adder_tb;
    reg a, b, cin;
    wire sum, cout;
    full_adder uut(.a(a), .b(b), .cin(cin), .sum(sum), .cout(cout));

    initial begin
        $monitor("a=%b b=%b cin=%b => sum=%b cout=%b", a, b, cin, sum, cout);
        a=0; b=0; cin=0; #10;
        a=0; b=1; cin=1; #10;
        a=1; b=1; cin=0; #10;
        a=1; b=1; cin=1; #10;
        $finish;
    end
endmodule
```

Waveform:



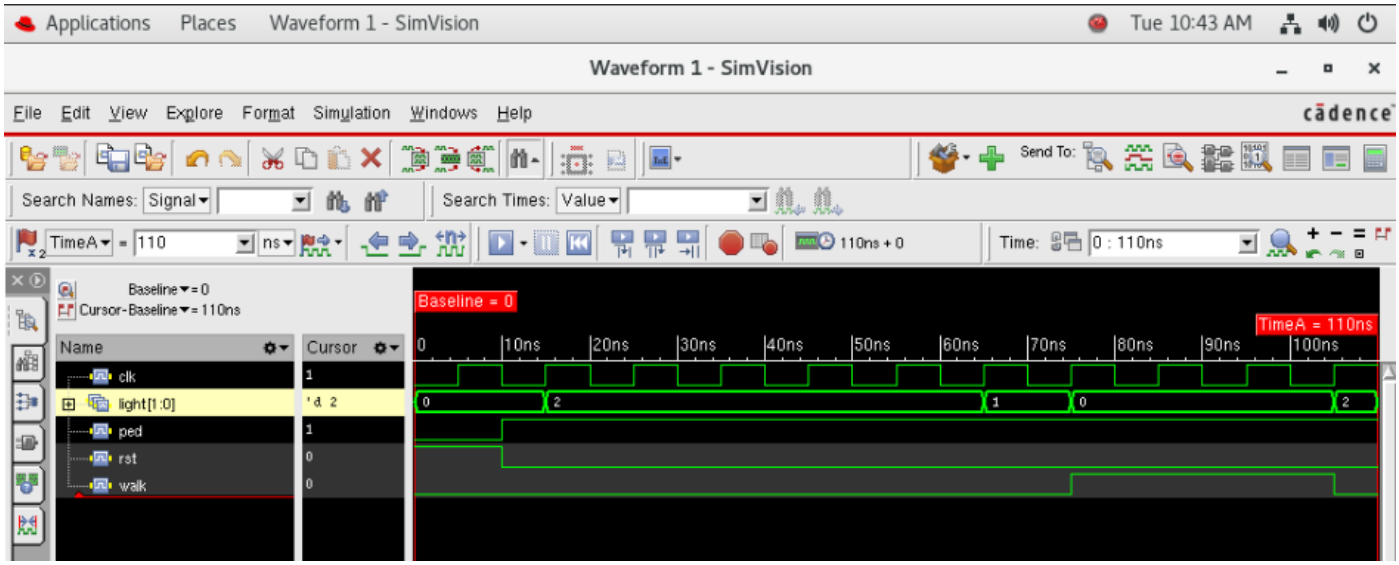
Traffic Light Controller:

```
module traffic_light_ctrl(
    input clk, input rst, input ped,
    output reg [1:0] light, // 00=Red, 01=Yellow, 10=Green
    output reg walk
);
reg [3:0] timer = 0;

always @(posedge clk or posedge rst) begin
    if (rst) begin
        light <= 2'b00;
        walk <= 0;
        timer <= 0;
    end else begin
        timer <= timer + 1;
        case (timer)
            0: begin light <= 2'b10; walk <= 0; end
            5: begin if (ped) begin light <= 2'b01; walk <= 0; end end
            6: begin if (ped) begin light <= 2'b00; walk <= 1; end end
            9: begin light <= 2'b10; walk <= 0; timer <= 0; end
        endcase
    end
end
endmodule
```

Test Bench:

```
module traffic_light_ctrl_tb;
reg clk = 0, rst, ped;
wire [1:0] light;
wire walk;

traffic_light_ctrl uut(.clk(clk), .rst(rst), .ped(ped), .light(light), .walk(walk));
always #5 clk = ~clk;

initial begin
    rst = 1; ped = 0; #10;
    rst = 0; ped = 1; #100;
    $finish;
end

initial $monitor("Time=%t Light=%b Walk=%b", $time, light, walk);
endmodule
```

Waveform:


Applications
Places
Waveform 1 - SimVision
Tue 10:43 AM
Waveform 1 - SimVision
File
Edit
View
Explore
Format
Simulation
Windows
Help
cadence
Send To:
Search Names:
Signal
Search Times:
Value
TimeA
110
ns
110ns + 0
Time:
0 : 110ns
Baseline = 0
Cursor-Baseline = 110ns
Name
Cursor
clk
light[1:0]
ped
rst
walk
Baseline = 0
TimeA = 110ns
0
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

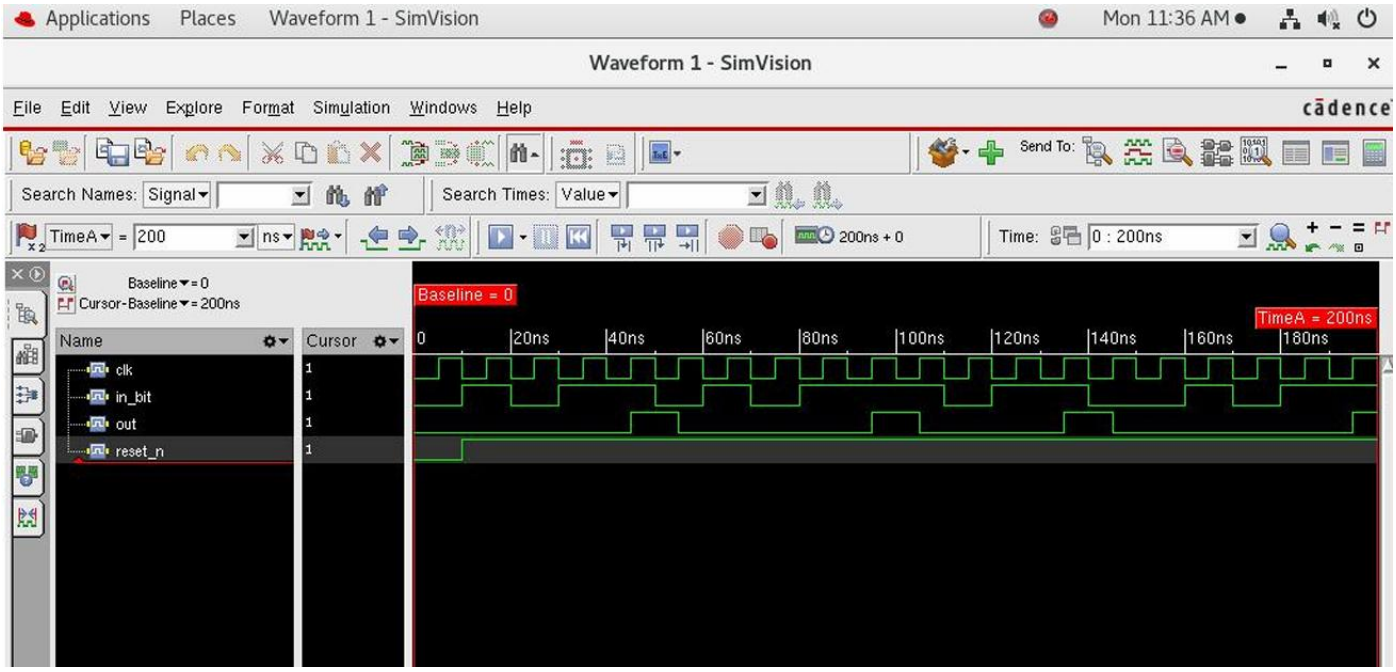
MEALY SEQUENCE DETECTOR:

```
module moore_seq_1011 (
input clk,
input reset_n,
input in_bit,
output reg out
);
parameter S0 = 3'b000;
parameter S1 = 3'b001;
parameter S2 = 3'b010;
parameter S3 = 3'b011;
parameter S4 = 3'b100;
reg [2:0] state, next_state;
always @(posedge clk or negedge reset_n) begin
if (!reset_n)
state <= S0;
else
state <= next_state;
end
always @(*) begin
case (state)
S0: next_state = in_bit ? S1 : S0;
S1: next_state = in_bit ? S1 : S2;
S2: next_state = in_bit ? S3 : S0;
S3: next_state = in_bit ? S4 : S2;
          S4: next_state = in_bit ? S1 : S2;
          default: next_state = S0;
     endcase
 end
 always @(*) begin
     case (state)
         S4: out = 1;
         default: out = 0;
     endcase
 end
endmodule
```

Test Bench:

```
module tb_moore_seq_1011;
 reg clk;
 reg reset_n;
 reg in_bit;
 wire out;
 moore_seq_1011 uut (
     .clk(clk),
     .reset_n(reset_n),
     .in_bit(in_bit),
     .out(out)
 );

 initial clk = 0;
 always #5 clk = ~clk;

 initial begin
     reset_n = 0; in_bit = 0; #10;
     reset_n = 1;

     in_bit = 1; #10;
     in_bit = 0; #10;
     in_bit = 1; #10;
     in_bit = 1; #10;

     in_bit = 0; #10;
     in_bit = 1; #10;
     in_bit = 0; #10;
     in_bit = 1; #10;
in_bit = 1; #10;
in_bit = 1; #10;
in_bit = 0; #10;
in_bit = 1; #10;
in_bit = 1; #10;
in_bit = 0; #10;
in_bit = 0; #10;
in_bit = 1; #10;
in_bit = 0; #10;
in_bit = 1; #10;
in_bit = 1; #10;
$finish;
end
initial begin
$monitor("Time=%0t in=%b out=%b", $time, in_bit, out);
end
endmodule
```

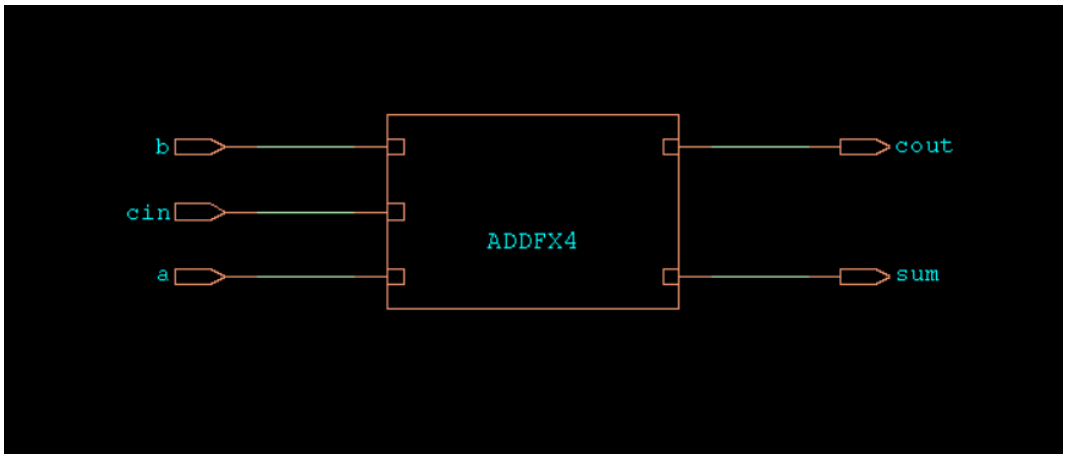
Waveform :


Applications
Places
Waveform 1 - SimVision
Mon 11:36 AM
Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Value
TimeA = 200 ns
200ns + 0
Time: 0 : 200ns
Baseline = 0
Cursor-Baseline = 200ns
Name
Cursor
clk
in_bit
out
reset_n
Baseline = 0
TimeA = 200ns
0
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns

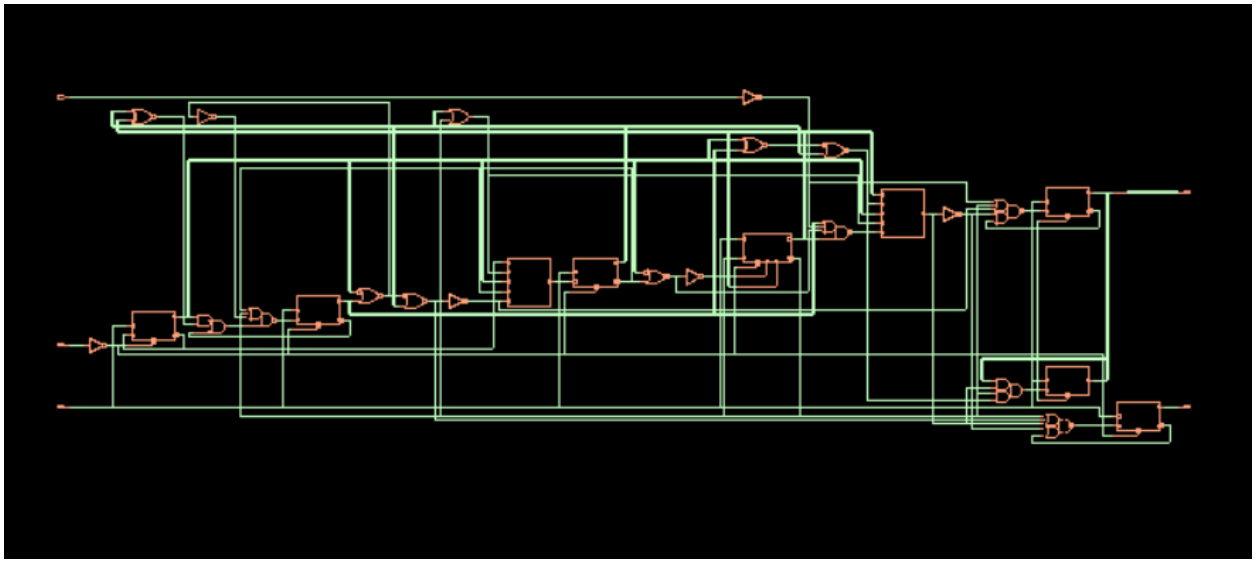
WEEK 2

Synthesis

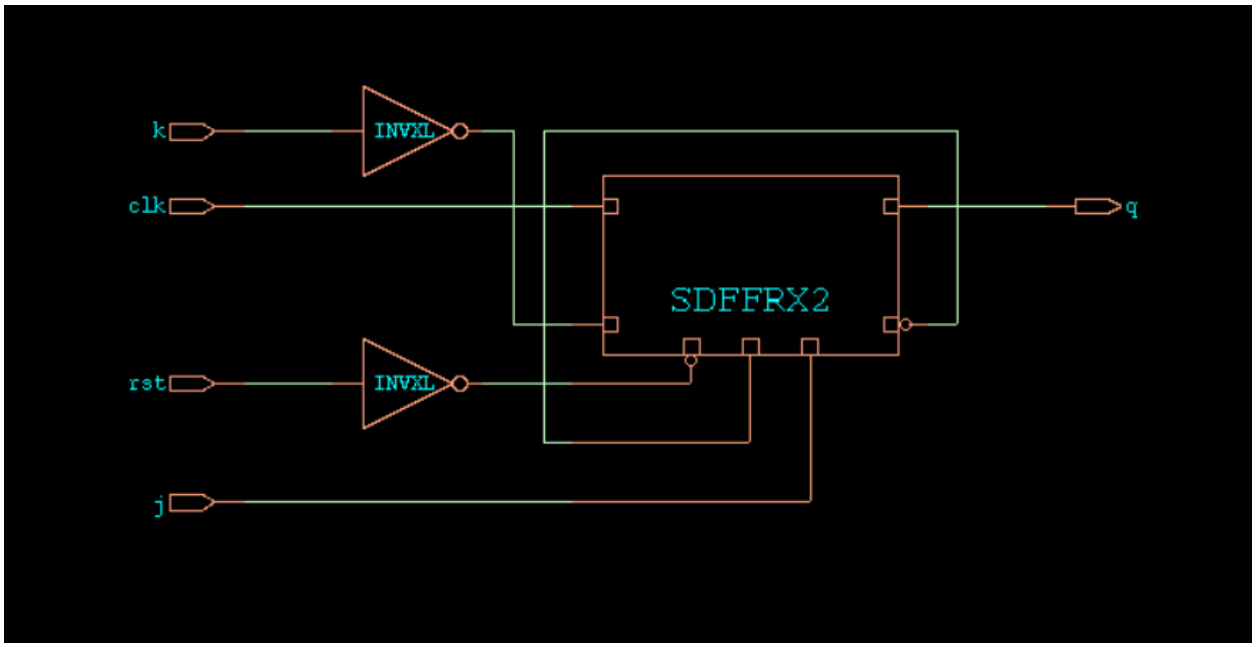
FULL ADDER



TRAFFIC LIGHT CONTROLLER



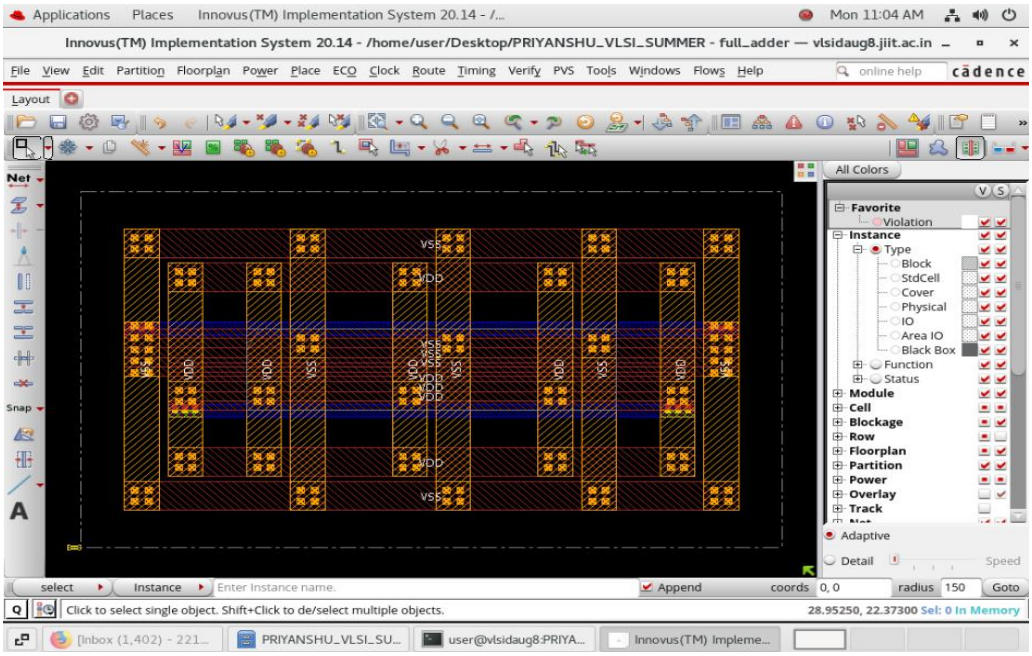
JK Flip Flop



Similarly, Simulated the Synthesis of 10 Digital circuits, including Combinational as well as Sequential Circuits

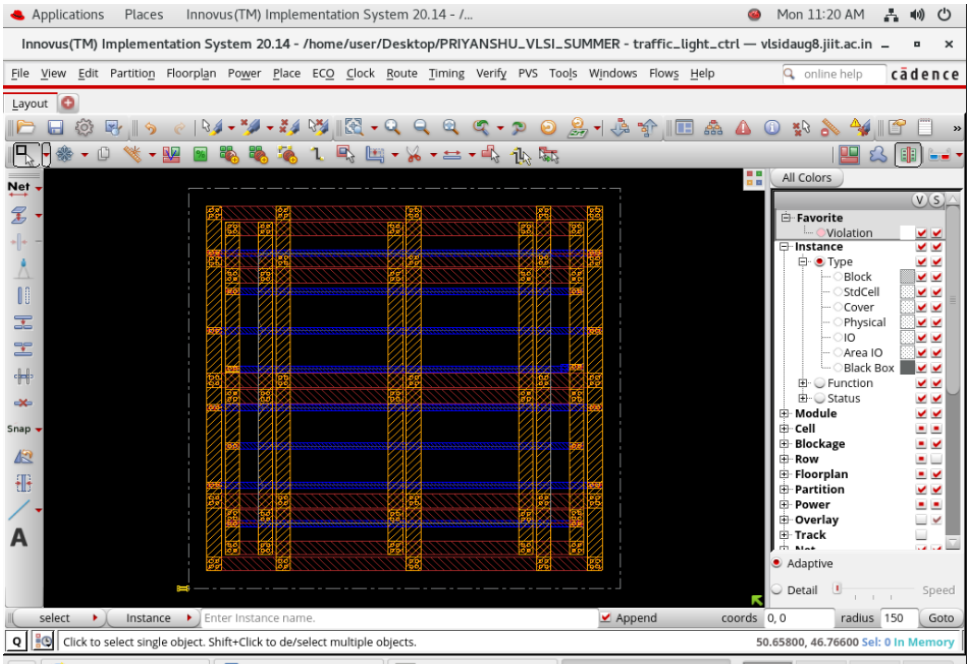
WEEK 3
Floor Planning and Power Planning

FULL ADDER




```
##############################################################################
#  Generated by:      Cadence Innovus 20.14-s095_1
#  OS:                Linux x86_64(Host ID vlsidaug8.jiit.ac.in)
#  Generated on:      Mon Jun 30 11:05:59 2025
#  Design:            full_adder
#  Command:           saveNetlist full_adder_WEEK_3_NETLIST.v
##############################################################################
*/
// Generated by Cadence Genus(TM) Synthesis Solution 20.11-s111_1
// Generated on: Jun 20 2025 10:36:49 IST (Jun 20 2025 05:06:49 UTC)
// Verification Directory fv/full_adder
module full_adder (
        a,
        b,
        cin,
        sum,
        cout);
   input a;
   input b;
   input cin;
   output sum;
   output cout;

   ADDFX4 g101 (.A(b),
        .B(cin),
        .CI(a),
        .CO(cout),
        .S(sum));
endmodule
```

TRAFFIC LIGHT CONTROLLER

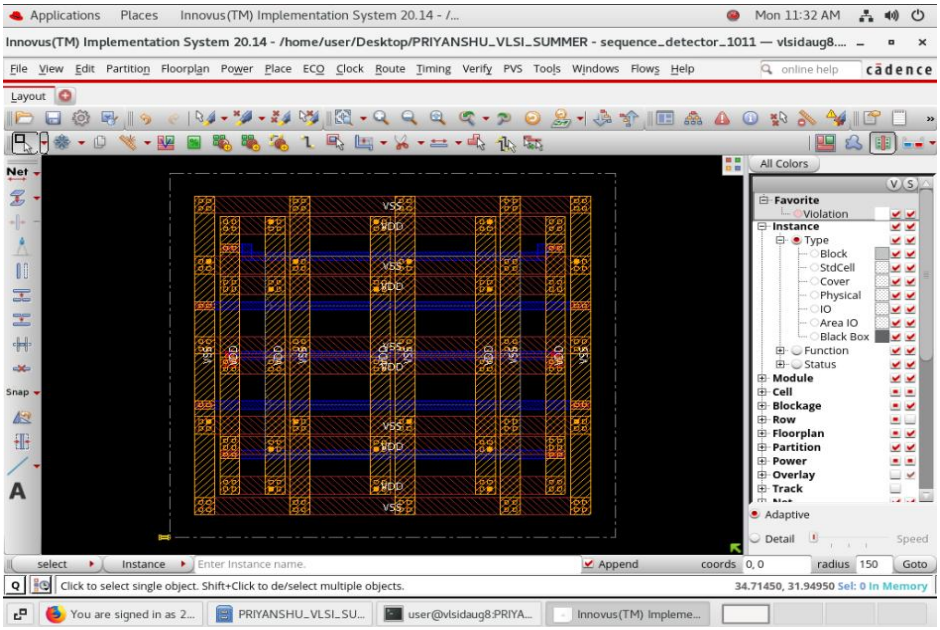



```
/*
##############################################################
#  Generated by:      Cadence Innovus 20.14-s095_1
#  OS:                Linux x86_64(Host ID vlsidaug8.jiit.ac.in)
#  Generated on:      Mon Jun 30 11:21:27 2025
#  Design:            traffic_light_ctrl
#  Command:           saveNetlist traffic_light_ctrl_WEEK_3_NETLIST.v
##############################################################
*/
// Generated by Cadence Genus(TM) Synthesis Solution 20.11-s111_1
// Generated on: Jun 20 2025 10:50:47 IST (Jun 20 2025 05:20:47 UTC)
// Verification Directory fv/traffic_light_ctrl
module traffic_light_ctrl (
        clk,
        rst,
        ped,
        light,
        walk);
   input clk;
   input rst;
   input ped;
   output [1:0] light;
   output walk;

   // Internal wires
   wire [3:0] timer;
   wire n_0;
   wire n_1;
   wire n_2;
   wire n_3;
   wire n_4;
   wire n_5;
   wire n_6;
   wire n_7;
   wire n_8;
   wire n_9;
   wire n_10;
   wire n_11;
   wire n_12;
   wire n_13;
```

```
  wire n_14;
  wire n_15;
  wire n_16;
  wire n_17;
  wire n_18;
  wire n_19;
  wire n_20;
  wire n_21;
  wire n_22;
  wire n_23;
  wire n_24;
  wire n_25;
  wire n_26;

  DFFRHQX4 \light_reg[1]  (.CK(clk),
       .D(n_21),
       .Q(light[1]),
       .RN(n_26));
  OAI32XL g688 (.A0(n_16),
       .A1(n_23),
       .A2(n_12),
       .B0(n_22),
       .B1(n_1),
       .Y(n_25));
  OAI32XL g686 (.A0(n_23),
       .A1(n_10),
       .A2(n_20),
       .B0(n_22),
       .B1(n_2),
       .Y(n_24));
  AO22X1 g689 (.A0(light[1]),
       .A1(n_20),
       .B0(n_23),
       .B1(n_19),
       .Y(n_21));
  INVXL g691 (.A(n_20),
       .Y(n_22));
  OAI221XL g693 (.A0(timer[2]),
       .A1(n_19),
       .B0(timer[0]),
       .B1(n_14),
       .C0(n_17),
       .Y(n_20));
  OAI31XL g695 (.A0(n_13),
       .A1(n_23),
       .A2(n_7),
       .B0(n_11),
       .Y(n_18));
  OAI31XL g700 (.A0(timer[3]),
       .A1(n_16),
       .A2(n_8),
       .B0(timer[2]),
       .Y(n_17));
  OAI221XL g694 (.A0(n_3),
       .A1(n_14),
       .B0(timer[0]),
       .B1(n_13),
       .C0(n_12),
       .Y(n_15));
  AO21X2 g696 (.A0(timer[0]),
       .A1(n_5),
       .B0(n_0),
       .Y(n_11));
  INVXL g697 (.A(n_10),
       .Y(n_12));
  NOR2BXL g698 (.AN(n_4),
       .B(timer[1]),
       .Y(n_19));
  NOR2BXL g699 (.AN(n_6),
       .B(timer[1]),
       .Y(n_10));
  INVXL g705 (.A(n_8),
       .Y(n_9));
  INVXL g702 (.A(n_6),
       .Y(n_7));
  XNOR2X1 g703 (.A(timer[1]),
       .B(timer[2]),
       .Y(n_5));
```

```
    XNOR2X1 g704 (.A(timer[0]),
         .B(timer[3]),
         .Y(n_4));
    NOR2BXL g706 (.AN(timer[0]),
         .B(n_13),
         .Y(n_8));
    OR2X1 g709 (.A(timer[1]),
         .B(n_23),
         .Y(n_14));
    NOR2BXL g708 (.AN(timer[0]),
         .B(timer[3]),
         .Y(n_6));
    INVXL g715 (.A(ped),
         .Y(n_16));
    INVXL g711 (.A(rst),
         .Y(n_26));
    DFFRX4 walk_reg (.CK(clk),
         .D(n_24),
         .Q(walk),
         .QN(n_2),
         .RN(n_26));
    DFFRX4 \light_reg[0]  (.CK(clk),
         .D(n_25),
         .Q(light[0]),
         .QN(n_1),
         .RN(n_26));
    DFFRX4 \timer_reg[3]  (.CK(clk),
         .D(n_18),
         .Q(timer[3]),
         .QN(n_0),
         .RN(n_26));
    DFFRX4 \timer_reg[0]  (.CK(clk),
         .D(n_3),
         .Q(timer[0]),
         .QN(n_3),
         .RN(n_26));
    DFFRX4 \timer_reg[1]  (.CK(clk),
         .D(n_15),
         .Q(timer[1]),
         .QN(n_13),
         .RN(n_26));
    SDFFRX4 \timer_reg[2]  (.CK(clk),
         .D(n_23),
         .Q(timer[2]),
         .QN(n_23),
         .RN(n_26),
         .SE(n_9),
         .SI(timer[2]));
endmodule
```

Mealy Sequence Detector

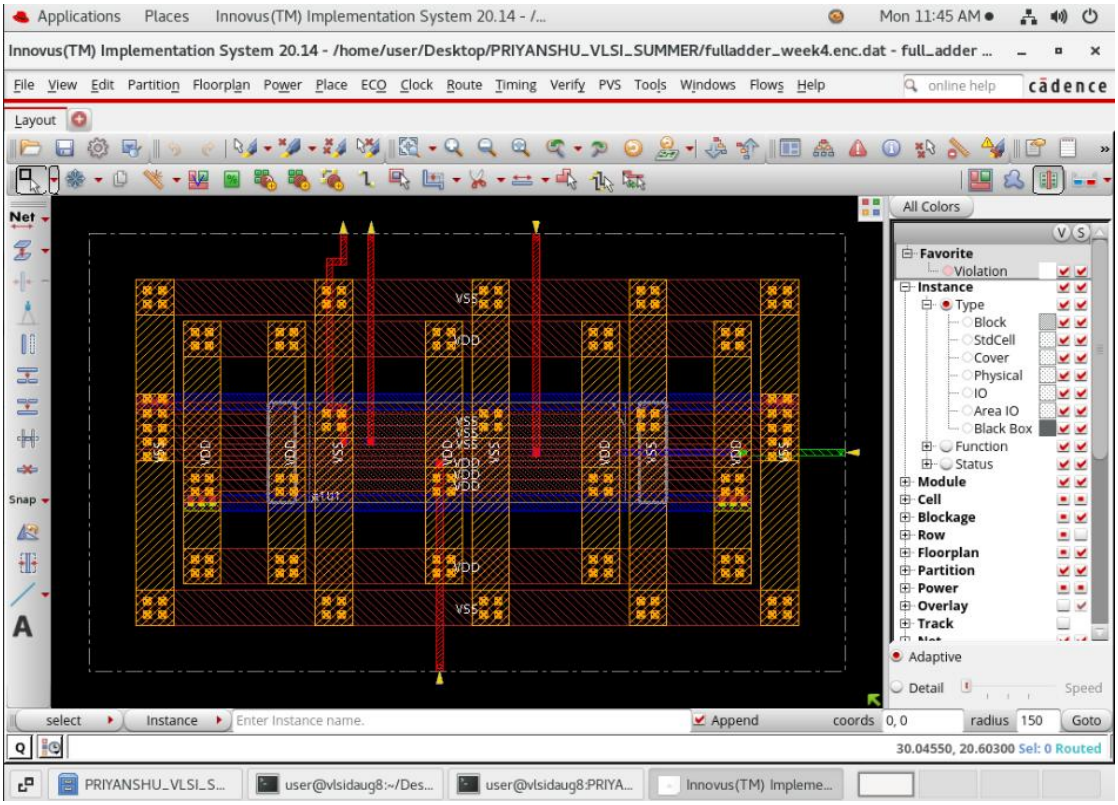



```
/*
##############################################################
#  Generated by:      Cadence Innovus 20.14-s095_1
#  OS:                Linux x86_64(Host ID vlsidaug8.jiit.ac.in)
#  Generated on:      Mon Jun 30 11:33:27 2025
#  Design:            sequence_detector_1011
#  Command:           saveNetlist sequence_detector_1011_WEEK_3_NETLIST.v
##############################################################
*/
// Generated by Cadence Genus(TM) Synthesis Solution 20.11-s111_1
// Generated on: Jun 30 2025 10:33:46 IST (Jun 30 2025 05:03:46 UTC)
// Verification Directory fv/sequence_detector_1011
module sequence_detector_1011 (
        clk,
        rst,
        in,
        detected);
   input clk;
   input rst;
   input in;
   output detected;

   // Internal wires
   wire [2:0] current_state;
   wire n_0;
   wire n_1;
   wire n_2;
   wire n_3;
   wire n_4;
   wire n_5;
   wire n_6;
   wire n_7;
   wire n_9;
   wire n_10;
   wire n_11;

   AO22X1 g373 (.A0(n_6),
        .A1(n_9),
        .B0(n_3),
        .B1(n_4),
```

```
      .Y(n_11));
  AO21X2 g378 (.A0(current_state[0]),
      .A1(n_1),
      .B0(detected),
      .Y(n_9));
  NOR2BXL g375 (.AN(n_2),
      .B(n_6),
      .Y(n_7));
  NOR2BXL g376 (.AN(n_4),
      .B(n_3),
      .Y(n_5));
  AND3X1 g379 (.A(current_state[2]),
      .B(n_0),
      .C(n_3),
      .Y(detected));
  ACHCONX2 g377 (.A(current_state[2]),
      .B(current_state[1]),
      .CI(current_state[0]),
      .CON(n_2));
  AND3X1 g380 (.A(in),
      .B(current_state[1]),
      .C(n_1),
      .Y(n_4));
  INVXL g385 (.A(in),
      .Y(n_6));
  INVXL g384 (.A(rst),
      .Y(n_10));
  DFFRX4 \current_state_reg[2]  (.CK(clk),
      .D(n_5),
      .Q(current_state[2]),
      .QN(n_1),
      .RN(n_10));
  DFFRX4 \current_state_reg[1]  (.CK(clk),
      .D(n_11),
      .Q(current_state[1]),
      .QN(n_0),
      .RN(n_10));
   DFFRX4 \current_state_reg[0]  (.CK(clk),
      .D(n_7),
      .Q(current_state[0]),
      .QN(n_3),
      .RN(n_10));
endmodule
```

WEEK 4
Placement, CTS, Routing, RC Extraction

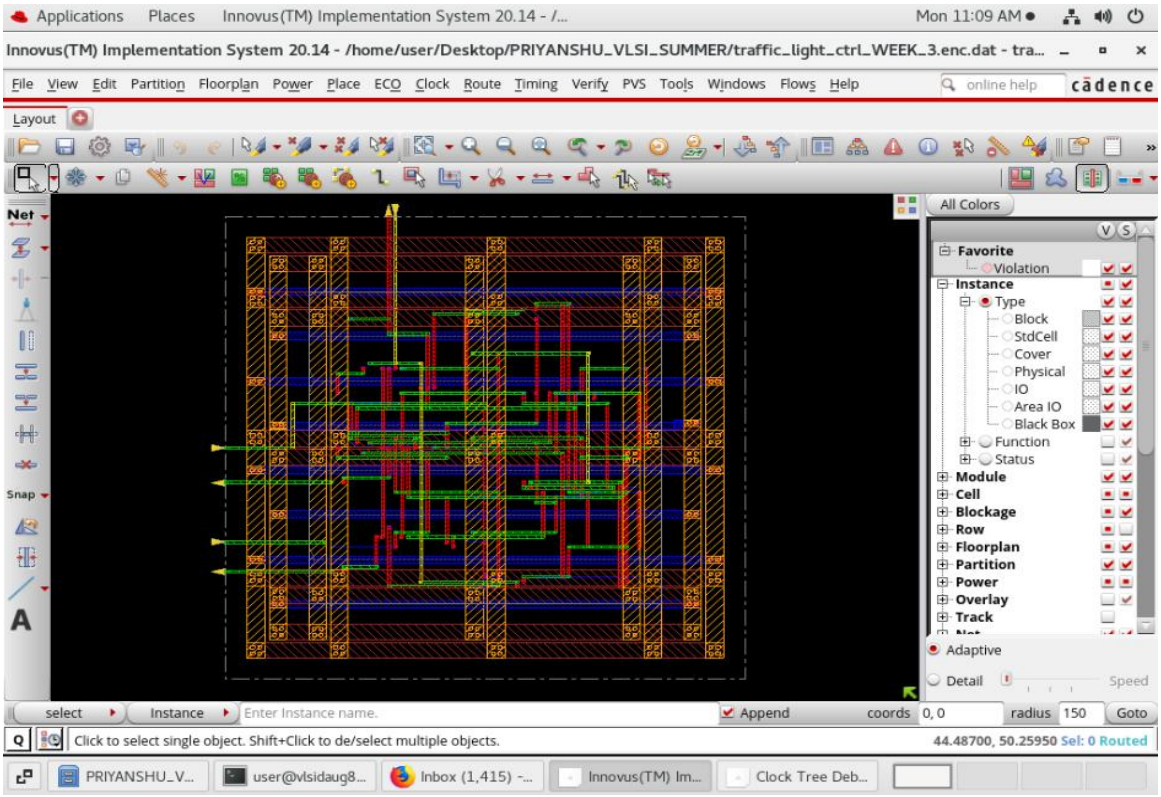
FULL ADDER

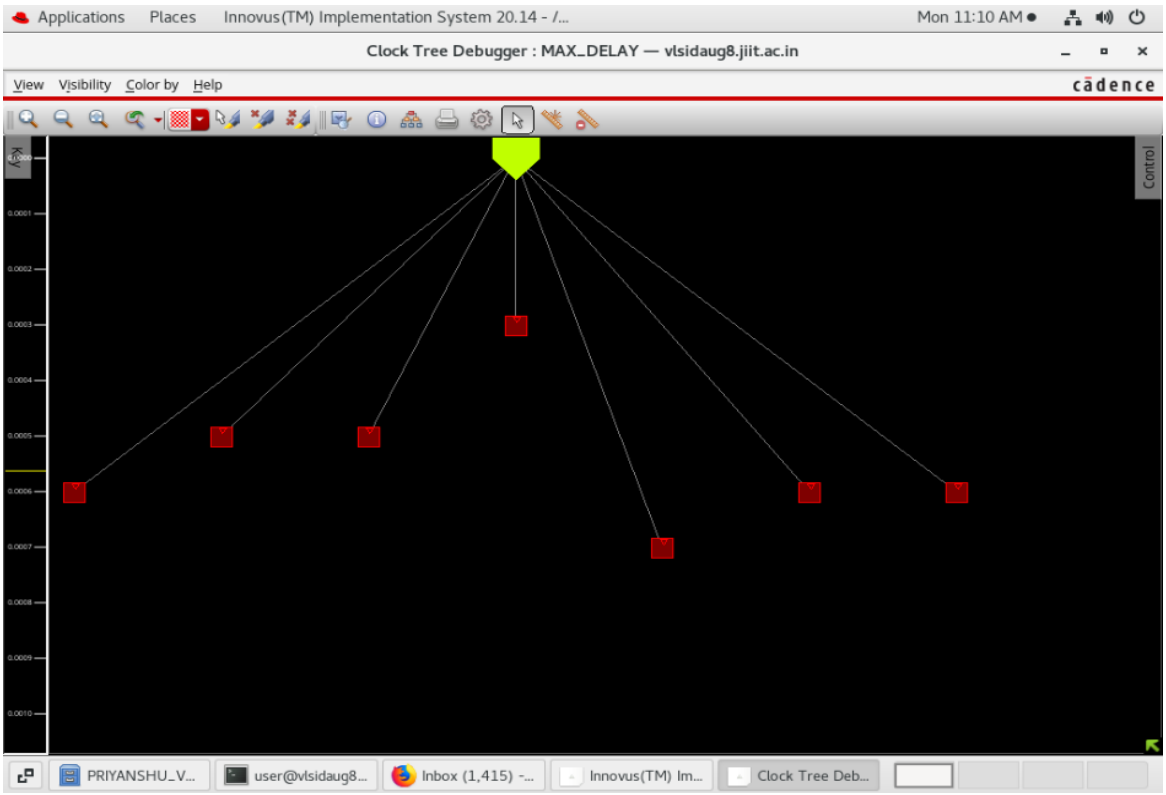



```
------------------------------------------------------------------
         time Design Summary
------------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+
|     Setup mode     |   all   | default |
+--------------------+---------+---------+
|           WNS (ns):|  0.000  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |
|          All Paths:|    0    |    0    |
+--------------------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 92.000%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.26 sec
Total Real time: 1.0 sec
Total Memory Usage: 1340.816406 Mbytes
*** timeDesign #1 [finish] : cpu/real = 0:00:00.3/0:00:00.8 (0.3), totSession cpu/real = 0:00:47.9/0:09:27.0 (0.1), mem = 1340.8M
```

```
Total Power
--------------------------------------------------------------------------------------
Total Internal Power:        0.00025389            90.5276%
Total Switching Power:       0.00002605             9.2891%
Total Leakage Power:         0.00000051             0.1833%
Total Power:                 0.00028045
--------------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------------
Sequential                             0          0           0           0           0
Macro                                  0          0           0           0           0
IO                                     0          0           0           0           0
Combinational                  0.0002539   2.605e-05   5.141e-07   0.0002805         100
Clock (Combinational)                  0          0           0           0           0
Clock (Sequential)                     0          0           0           0           0
--------------------------------------------------------------------------------------
Total                          0.0002539   2.605e-05   5.141e-07   0.0002805         100
--------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------------
VDD                       0.9  0.0002539   2.605e-05   5.141e-07   0.0002805         100


--------------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:                     g101 (ADDFX4):        0.0002805
*              Highest Leakage Power:                     g101 (ADDFX4):        5.141e-07
*                Total Cap:      2.57298e-15 F
*                Total instances in design:     1
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*                Total Fillers and Decap:     0
--------------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1043.44MB/2489.54MB/1051.72MB)

1
```

TRAFFIC LIGHT CONTROLLER

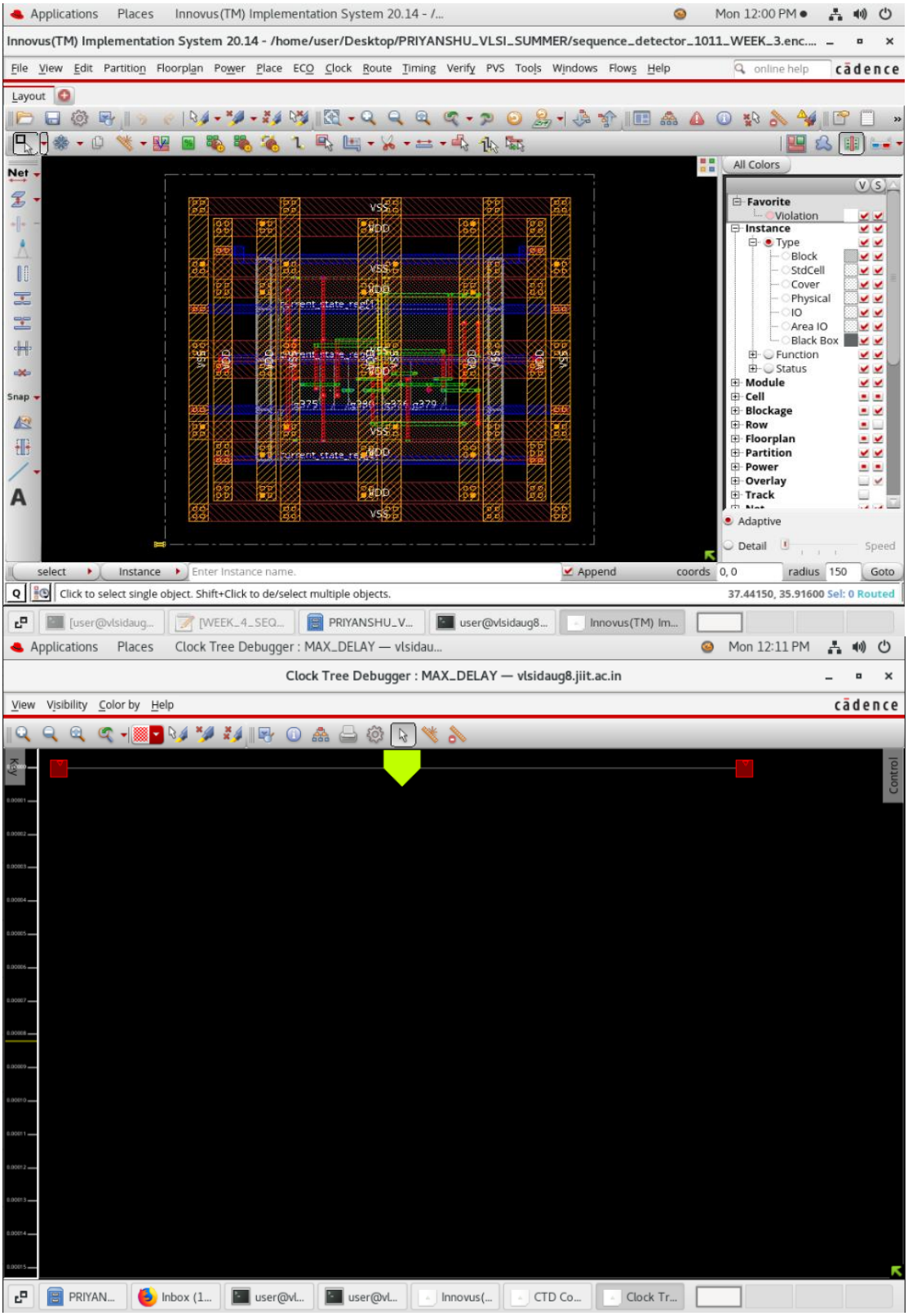




```
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.000  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|          All Paths:|    0    |   N/A   |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 85.434%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.16 sec
Total Real time: 0.0 sec
Total Memory Usage: 1539.128906 Mbytes
*** timeDesign #2 [finish] : cpu/real = 0:00:00.2/0:00:00.7 (0.2), totSession cpu/real = 0:00:43.0/0:08:36.3 (0.1), mem = 1539.1M
innovus 6>
```

```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:        0.00110828            72.5329%
Total Switching Power:       0.00041464            27.1364%
Total Leakage Power:         0.00000505             0.3307%
Total Power:                 0.00152797
-----------------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Sequential                   0.0009659   7.912e-05   3.865e-06    0.001049       68.65
Macro                               0           0           0           0           0
IO                                  0           0           0           0           0
Combinational                0.0001423   0.0003355   1.187e-06   0.0004791       31.35
Clock (Combinational)               0           0           0           0           0
Clock (Sequential)                  0           0           0           0           0
-----------------------------------------------------------------------------------------
Total                        0.001108   0.0004146   5.053e-06    0.001528         100
-----------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Default                   0.9   2.34e-05          0   1.893e-07   2.359e-05       1.544
VDD                       0.9   0.001085   0.000403   4.863e-06    0.001493       97.69


-----------------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:                    g711 (INVXL):        0.0002008
*              Highest Leakage Power:              timer_reg[2] (SDFFRX4):       6.106e-07
*                Total Cap:      1.70831e-13 F
*                Total instances in design:    28
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*                Total Fillers and Decap:     0
-----------------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1110.59MB/2690.07MB/1110.59MB)
```

MEALY SEQUENCE DETECTOR



```
------------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.000  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|          All Paths:|    0    |   N/A   |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 90.323%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.13 sec
Total Real time: 1.0 sec
Total Memory Usage: 1443.101562 Mbytes
*** timeDesign #1 [finish] : cpu/real = 0:00:00.1/0:00:00.5 (0.2), totSession cpu/real = 0:00:15.3/0:01:31.9 (0.2), mem = 1443.1M
innovus 1>
```

```
Total Power
--------------------------------------------------------------------------------------------------
Total Internal Power:        0.00096912            80.2065%
Total Switching Power:       0.00023640            19.5654%
Total Leakage Power:         0.00000276             0.2280%
Total Power:                 0.00120828
--------------------------------------------------------------------------------------------------


Group                           Internal    Switching     Leakage       Total  Percentage
                                Power       Power         Power         Power  (%)
--------------------------------------------------------------------------------------------------
Sequential                    0.0005899    8.03e-05   1.683e-06   0.0006719       55.61
Macro                                0           0           0           0           0
IO                                   0           0           0           0           0
Combinational                 0.0003792   0.0001561   1.072e-06   0.0005364       44.39
Clock (Combinational)                0           0           0           0           0
Clock (Sequential)                   0           0           0           0           0
--------------------------------------------------------------------------------------------------
Total                         0.0009691   0.0002364   2.755e-06    0.001208         100
--------------------------------------------------------------------------------------------------


Rail                  Voltage   Internal    Switching     Leakage       Total  Percentage
                                Power       Power         Power         Power  (%)
--------------------------------------------------------------------------------------------------
VDD                       0.9  0.0006682   0.0002032   1.964e-06   0.0008733       72.28
Default                   0.9  0.0003009           0   7.917e-07   0.0003017       24.97


--------------------------------------------------------------------------------------------------
*        Power Distribution Summary:
*               Highest Average Power:      current_state_reg[1] (DFFRX4):        0.0002675
*               Highest Leakage Power:                        g377 (ACHCONX2):        6.024e-07
*                 Total Cap:      4.92595e-14 F
*                 Total instances in design:    12
*                 Total instances in design with no power:     0
*                 Total instances in design with no activty:     0

*                 Total Fillers and Decap:     0
--------------------------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1090.36MB/2594.02MB/1090.41MB)
```

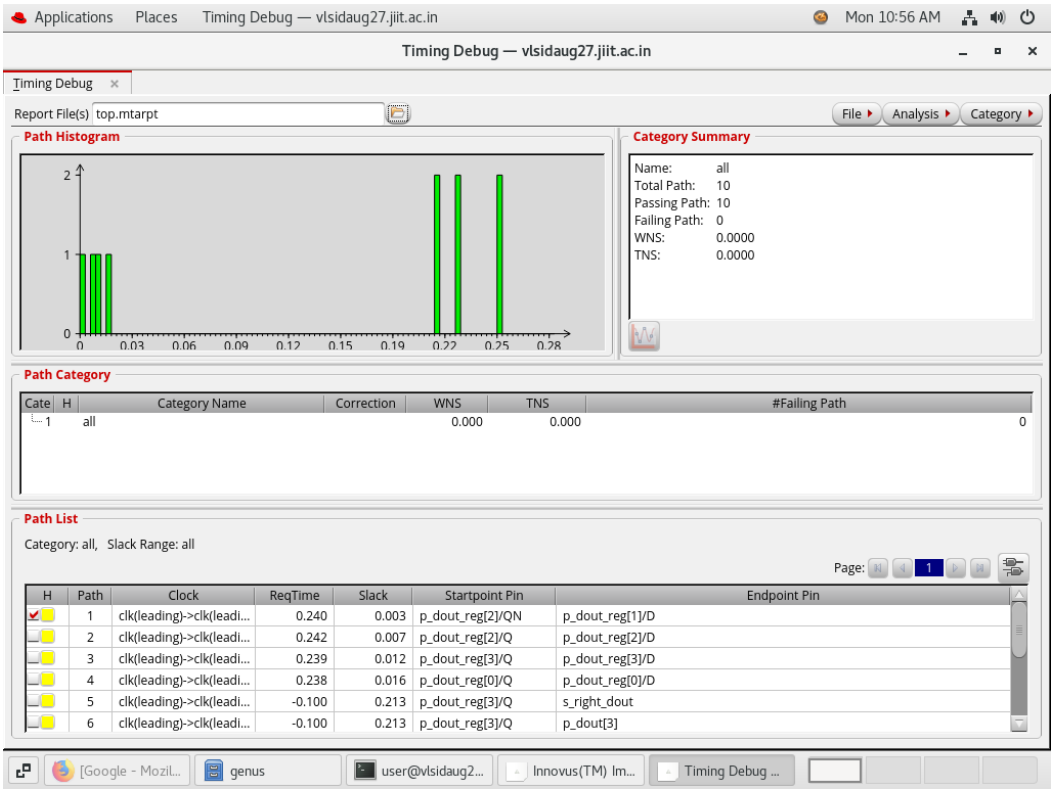
```
innovus 2> report_area
     Hinst Name          Module Name           Inst Count            Total Area
-------------------------------------------------------------------------------
sequence_detector_1011                                12               390.683
```

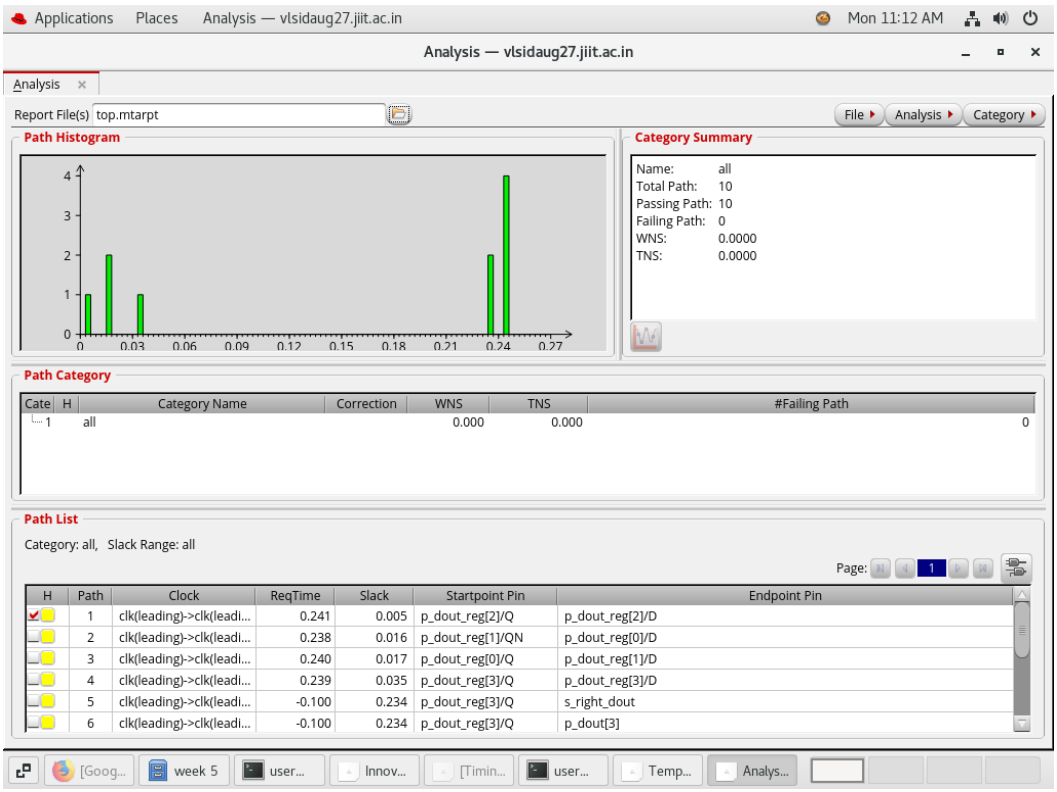
WEEK 5
STATIC TIMING ANALYSIS

FULL ADDER

```
------------------------------------------------------------------
          time Design Summary
------------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+
|     Setup mode     |   all   | default |
+--------------------+---------+---------+
|           WNS (ns):|  0.000  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |
|          All Paths:|    0    |    0    |
+--------------------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 92.000%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.26 sec
Total Real time: 1.0 sec
Total Memory Usage: 1340.816406 Mbytes
*** timeDesign #1 [finish] : cpu/real = 0:00:00.3/0:00:00.8 (0.3), totSession cpu/real = 0:00:47.9/0:09:27.0 (0.1), mem = 1340.8M
```

```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:        0.00025389            90.5276%
Total Switching Power:       0.00002605             9.2891%
Total Leakage Power:         0.00000051             0.1833%
Total Power:                 0.00028045
-----------------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Sequential                            0          0           0           0           0
Macro                                 0          0           0           0           0
IO                                    0          0           0           0           0
Combinational                 0.0002539   2.605e-05   5.141e-07   0.0002805         100
Clock (Combinational)                 0          0           0           0           0
Clock (Sequential)                    0          0           0           0           0
-----------------------------------------------------------------------------------------
Total                         0.0002539   2.605e-05   5.141e-07   0.0002805         100
-----------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
VDD                       0.9  0.0002539   2.605e-05   5.141e-07   0.0002805         100


-----------------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:                    g101 (ADDFX4):        0.0002805
*              Highest Leakage Power:                    g101 (ADDFX4):        5.141e-07
*                Total Cap:      2.57298e-15 F
*                Total instances in design:     1
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*                Total Fillers and Decap:     0
-----------------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1043.44MB/2489.54MB/1051.72MB)

1
```

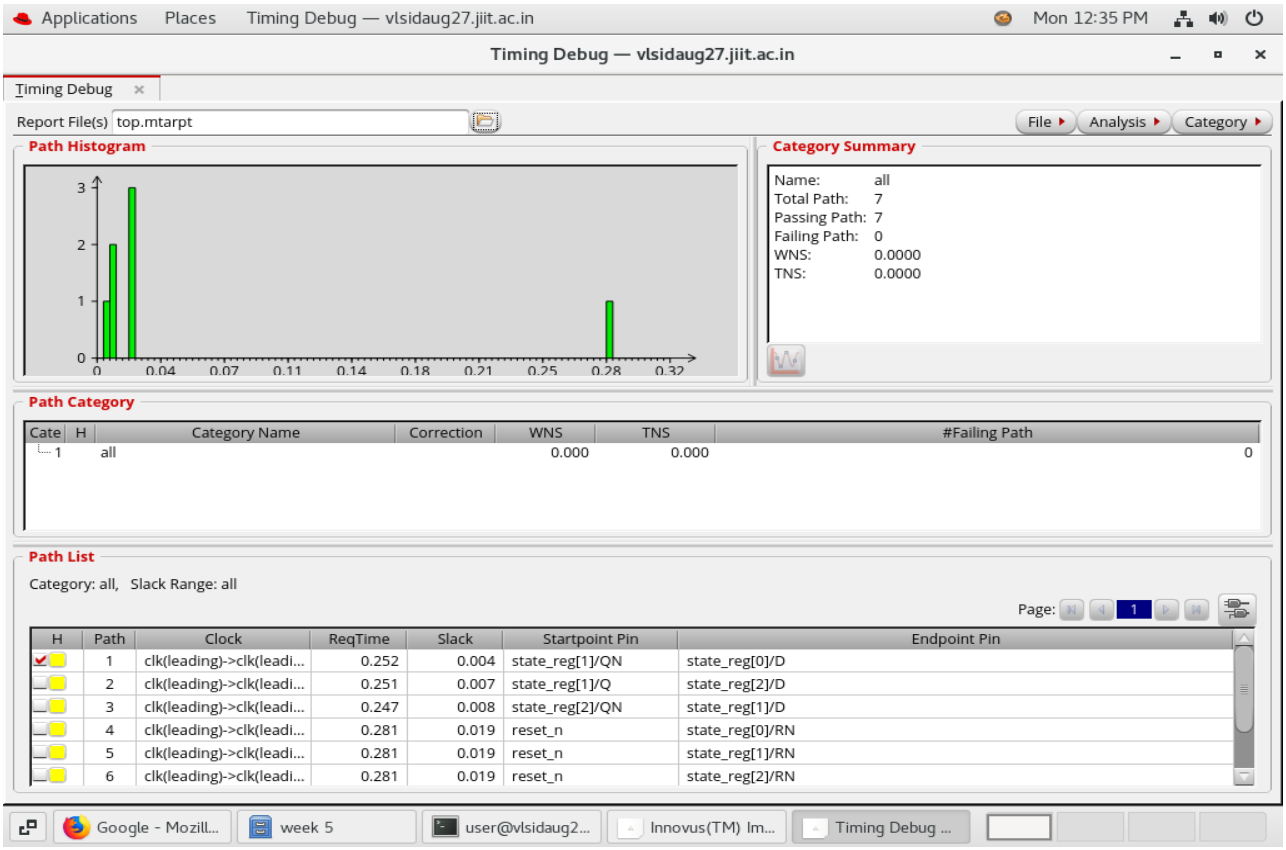

Applications Places Timing Debug — vlsidaug27.jiit.ac.in Mon 10:56 AM
Timing Debug — vlsidaug27.jiit.ac.in
Timing Debug
Report File(s) top.mtarpt
File Analysis Category
Path Histogram
Category Summary
Name: all
Total Path: 10
Passing Path: 10
Failing Path: 0
WNS: 0.0000
TNS: 0.0000
Path Category
Cate H Category Name Correction WNS TNS #Failing Path
1 all 0.000 0.000 0
Path List
Category: all, Slack Range: all
Page: 1
H Path Clock ReqTime Slack Startpoint Pin Endpoint Pin
1 clk(leading)->clk(leadi... 0.240 0.003 p_dout_reg[2]/QN p_dout_reg[1]/D
2 clk(leading)->clk(leadi... 0.242 0.007 p_dout_reg[2]/Q p_dout_reg[2]/D
3 clk(leading)->clk(leadi... 0.239 0.012 p_dout_reg[3]/Q p_dout_reg[3]/D
4 clk(leading)->clk(leadi... 0.238 0.016 p_dout_reg[0]/Q p_dout_reg[0]/D
5 clk(leading)->clk(leadi... -0.100 0.213 p_dout_reg[3]/Q s_right_dout
6 clk(leading)->clk(leadi... -0.100 0.213 p_dout_reg[3]/Q p_dout[3]
[Google - Mozil... genus user@vlsidaug2... Innovus(TM) Im... Timing Debug ...


Applications Places Analysis — vlsidaug27.jiit.ac.in Mon 11:12 AM
Analysis — vlsidaug27.jiit.ac.in
Analysis
Report File(s) top.mtarpt
File Analysis Category
Path Histogram
Category Summary
Name: all
Total Path: 10
Passing Path: 10
Failing Path: 0
WNS: 0.0000
TNS: 0.0000
Path Category
Cate H Category Name Correction WNS TNS #Failing Path
1 all 0.000 0.000 0
Path List
Category: all, Slack Range: all
Page: 1
H Path Clock ReqTime Slack Startpoint Pin Endpoint Pin
1 clk(leading)->clk(leadi... 0.241 0.005 p_dout_reg[2]/Q p_dout_reg[2]/D
2 clk(leading)->clk(leadi... 0.238 0.016 p_dout_reg[1]/QN p_dout_reg[0]/D
3 clk(leading)->clk(leadi... 0.240 0.017 p_dout_reg[0]/Q p_dout_reg[1]/D
4 clk(leading)->clk(leadi... 0.239 0.035 p_dout_reg[3]/Q p_dout_reg[3]/D
5 clk(leading)->clk(leadi... -0.100 0.234 p_dout_reg[3]/Q s_right_dout
6 clk(leading)->clk(leadi... -0.100 0.234 p_dout_reg[3]/Q p_dout[3]
[Goog... week 5 user... Innov... [Timin... user... Temp... Analys...

TRAFFIC LIGHT CONTROLLER

```
          timeDesign Summary
--------------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.000  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|         All Paths:|    0    |   N/A   |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 85.434%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.16 sec
Total Real time: 0.0 sec
Total Memory Usage: 1539.128906 Mbytes
*** timeDesign #2 [finish] : cpu/real = 0:00:00.2/0:00:00.7 (0.2), totSession cpu/real = 0:00:43.0/0:08:36.3 (0.1), mem = 1539.1M
innovus 6>
```

```
Total Power
----------------------------------------------------------------------------------------------
Total Internal Power:        0.00110828            72.5329%
Total Switching Power:       0.00041464            27.1364%
Total Leakage Power:         0.00000505             0.3307%
Total Power:                 0.00152797
----------------------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
----------------------------------------------------------------------------------------------
Sequential                   0.0009659   7.912e-05   3.865e-06    0.001049       68.65
Macro                               0           0           0           0           0
IO                                  0           0           0           0           0
Combinational                0.0001423   0.0003355   1.187e-06   0.0004791       31.35
Clock (Combinational)               0           0           0           0           0
Clock (Sequential)                  0           0           0           0           0
----------------------------------------------------------------------------------------------
Total                        0.001108   0.0004146   5.053e-06    0.001528         100
----------------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
----------------------------------------------------------------------------------------------
Default                   0.9   2.34e-05          0   1.893e-07   2.359e-05       1.544
VDD                       0.9   0.001085   0.000403   4.863e-06    0.001493       97.69


----------------------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:                    g711 (INVXL):        0.0002008
*              Highest Leakage Power:              timer_reg[2] (SDFFRX4):       6.106e-07
*                Total Cap:      1.70831e-13 F
*                Total instances in design:    28
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*                Total Fillers and Decap:     0
----------------------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1110.59MB/2690.07MB/1110.59MB)
```

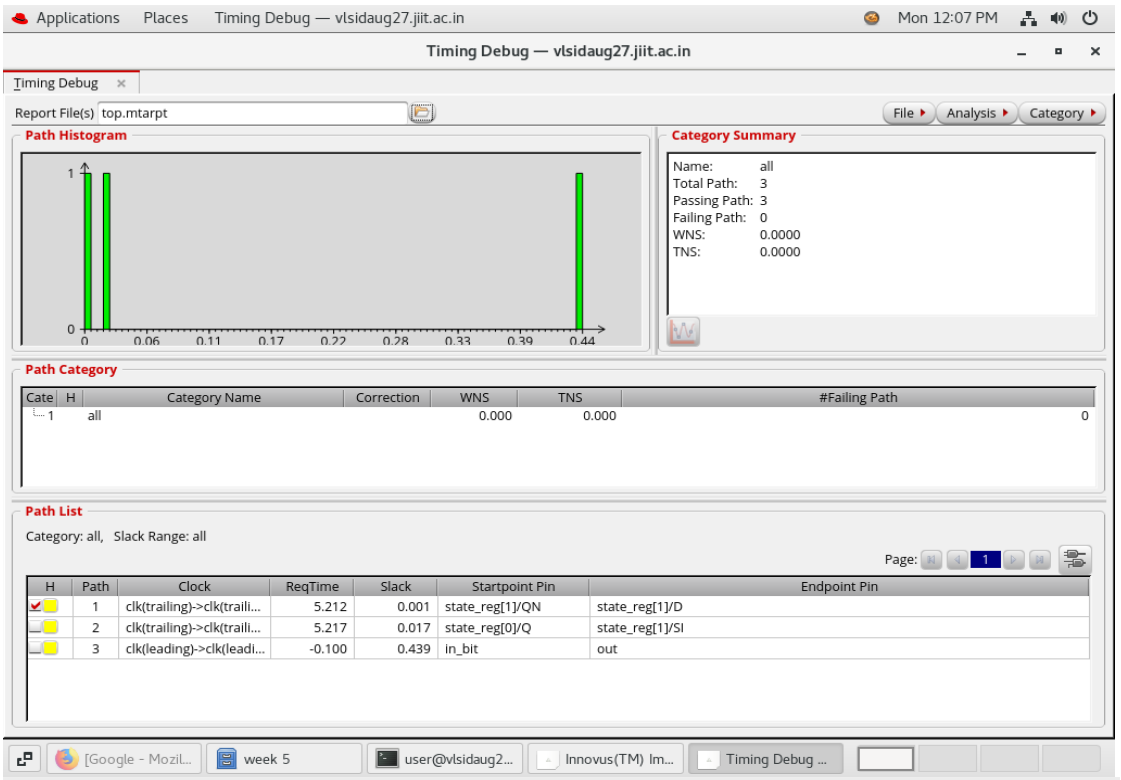


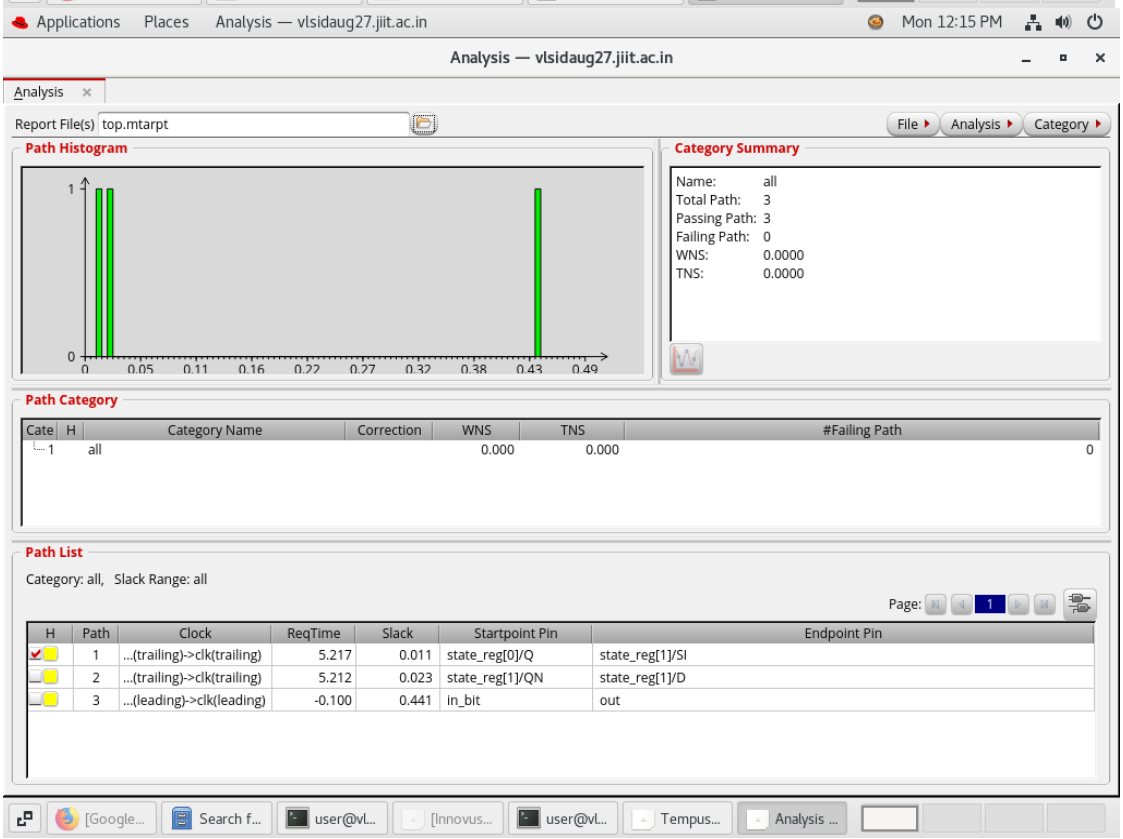
MEALY SEQUENCE DETECTOR

```
------------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.000  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|         All Paths:|    0    |   N/A   |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 90.323%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.13 sec
Total Real time: 1.0 sec
Total Memory Usage: 1443.101562 Mbytes
*** timeDesign #1 [finish] : cpu/real = 0:00:00.1/0:00:00.5 (0.2), totSession cpu/real = 0:00:15.3/0:01:31.9 (0.2), mem = 1443.1M
innovus 1>
```

```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:        0.00096912            80.2065%
Total Switching Power:       0.00023640            19.5654%
Total Leakage Power:         0.00000276             0.2280%
Total Power:                 0.00120828
-----------------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Sequential                   0.0005899    8.03e-05   1.683e-06   0.0006719       55.61
Macro                               0           0           0           0           0
IO                                  0           0           0           0           0
Combinational                0.0003792   0.0001561   1.072e-06   0.0005364       44.39
Clock (Combinational)               0           0           0           0           0
Clock (Sequential)                  0           0           0           0           0
-----------------------------------------------------------------------------------------
Total                        0.0009691   0.0002364   2.755e-06    0.001208         100
-----------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
VDD                       0.9  0.0006682   0.0002032   1.964e-06   0.0008733       72.28
Default                   0.9  0.0003009           0   7.917e-07   0.0003017       24.97


-----------------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:      current_state_reg[1] (DFFRX4):        0.0002675
*              Highest Leakage Power:                      g377 (ACHCONX2):        6.024e-07
*                Total Cap:      4.92595e-14 F
*                Total instances in design:    12
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*                Total Fillers and Decap:     0
-----------------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1090.36MB/2594.02MB/1090.41MB)
```

```
innovus 2> report_area
    Hinst Name          Module Name          Inst Count           Total Area
-------------------------------------------------------------------------------
sequence_detector_1011                             12               390.683
```


Applications Places Timing Debug — vlsidaug27.jiit.ac.in Mon 12:07 PM
Timing Debug — vlsidaug27.jiit.ac.in
Timing Debug
Report File(s) top.mtarpt
File Analysis Category
Path Histogram
Category Summary
Name: all
Total Path: 3
Passing Path: 3
Failing Path: 0
WNS: 0.0000
TNS: 0.0000
Path Category
Cate H Category Name Correction WNS TNS #Failing Path
1 all 0.000 0.000 0
Path List
Category: all, Slack Range: all
Page: 1
H Path Clock ReqTime Slack Startpoint Pin Endpoint Pin
1 clk(trailing)->clk(traili... 5.212 0.001 state_reg[1]/QN state_reg[1]/D
2 clk(trailing)->clk(traili... 5.217 0.017 state_reg[0]/Q state_reg[1]/SI
3 clk(leading)->clk(leadi... -0.100 0.439 in_bit out
[Google - Mozil... week 5 user@vlsidaug2... Innovus(TM) Im... Timing Debug ...


Applications Places Analysis — vlsidaug27.jiit.ac.in Mon 12:15 PM
Analysis — vlsidaug27.jiit.ac.in
Analysis
Report File(s) top.mtarpt
File Analysis Category
Path Histogram
Category Summary
Name: all
Total Path: 3
Passing Path: 3
Failing Path: 0
WNS: 0.0000
TNS: 0.0000
Path Category
Cate H Category Name Correction WNS TNS #Failing Path
1 all 0.000 0.000 0
Path List
Category: all, Slack Range: all
Page: 1
H Path Clock ReqTime Slack Startpoint Pin Endpoint Pin
1 ...(trailing)->clk(trailing) 5.217 0.011 state_reg[0]/Q state_reg[1]/SI
2 ...(trailing)->clk(trailing) 5.212 0.023 state_reg[1]/QN state_reg[1]/D
3 ...(leading)->clk(leading) -0.100 0.441 in_bit out
[Google... Search f... user@vl... [Innovus... user@vl... Tempus... Analysis ...

WEEK 6
PROJECT

Problem Statement : Digital Safe Lock System Design Problem
Design a digital controller for an electronic safe lock system used to secure valuables in homes, banks, or offices. The safe lock is operated via a digital keypad where the user enters a numeric passcode, typically 4 to 8 digits long. The safe's controller stores a master code in non-volatile memory and compares every entered code to this stored code.
When the user enters the correct passcode, the controller energises a solenoid to unlock the safe door for a fixed duration, such as 10 seconds, after which it automatically relocks. The controller must keep track of the door's status using a door sensor to ensure it closes properly before relocking.
If a user enters an incorrect passcode, the system increments a failed-attempt counter. After three consecutive wrong entries, the safe enters a lockout period lasting 5 minutes, during which the keypad is disabled and the user cannot make further attempts. During lockout, the system should display a "LOCKED OUT" message or light an LED indicator.
The safe must also support a duress mode. If the user enters a special duress code known only to authorised users, the safe unlocks normally, but the system quietly triggers a hidden alarm output to notify authorities of a possible coercion situation.
Furthermore, the safe should have a setup mode accessible only to the master user. This mode allows the master user to change the safe's passcode, enable or disable duress mode, and test the solenoid lock mechanism. The controller should store the new passcode securely and prevent unauthorised access to setup mode.
Inputs include keypad digit inputs, an enter key, door sensor signals, master setup mode activation, duress code entry, clock, and reset. Outputs include signals to control the solenoid lock, display or LED outputs for status messages (e.g., "ACCESS GRANTED," "WRONG CODE," "LOCKED OUT"), and a hidden alarm signal for duress conditions.
Design Constraints
The digital safe lock system must be implemented as a Mealy finite-state machine in a fully synthesisable RTL style suitable for ASIC synthesis and physical design. All logic must avoid combinational loops and should separate FSM control from the datapath handling code comparisons, counters, memory storage for codes, and timing management for lockout periods.

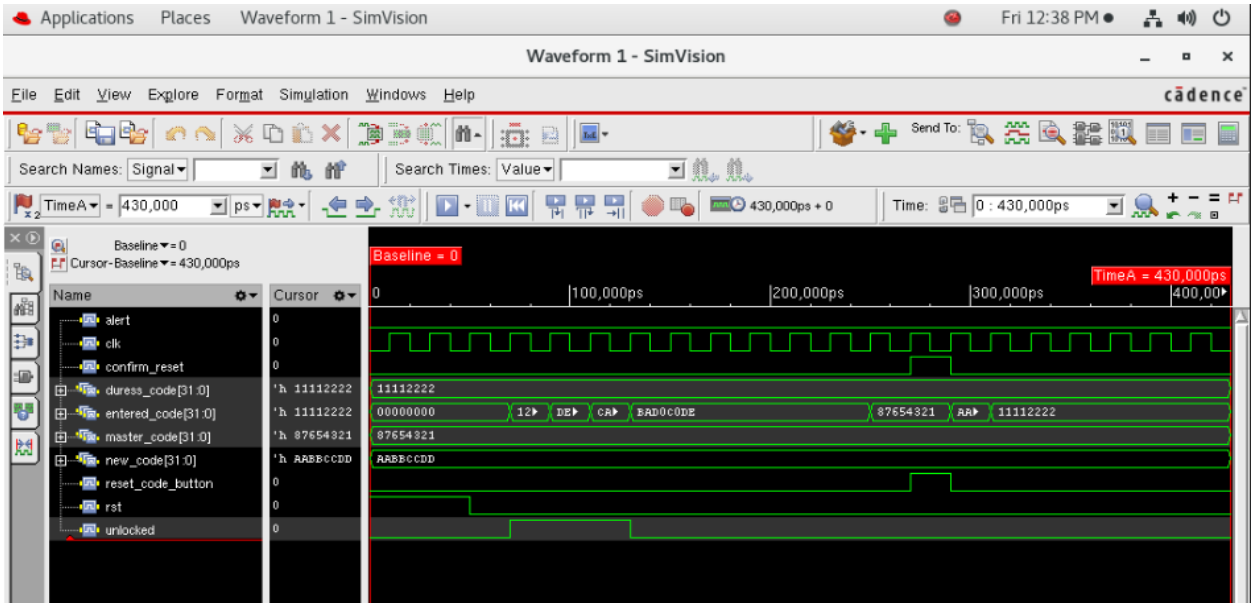
Project

```
`timescale 1ns / 1ps
module digital_safe (
    input clk,
    input rst,
    input [31:0] entered_code,
    input [31:0] master_code,
    input [31:0] duress_code,
    input reset_code_button,
    input [31:0] new_code,
    input confirm_reset,
    output reg unlocked,
    output reg alert
);

    reg [1:0] attempts;
    reg [31:0] current_code;
    reg locked;
    reg [19:0] lock_timer;

    localparam MAX_ATTEMPTS = 2'd3;
    localparam LOCK_TIME = 20'd15_000_000; // Adjust as per clock frequency (e.g., ~5 min for 50MHz)

    always @(posedge clk or posedge rst) begin
        if (rst) begin
            current_code <= 32'h12345678;
            attempts <= 0;
            locked <= 0;
            lock_timer <= 0;
            unlocked <= 0;
            alert <= 0;
        end else begin
            if (locked) begin
                if (lock_timer > 0)
                    lock_timer <= lock_timer - 1;
                else begin
                    locked <= 0;
                    attempts <= 0;
                end
            end else if (reset_code_button && confirm_reset) begin
                current_code <= new_code;
            end else begin
                if (entered_code == current_code || entered_code == master_code) begin
                    unlocked <= 1;
                    alert <= 0;
                    attempts <= 0;
                end else if (entered_code == duress_code) begin
                    unlocked <= 1;
                    alert <= 1;
                     attempts <= 0;
                 end else begin
                     attempts <= attempts + 1;
                     if (attempts == MAX_ATTEMPTS - 1) begin
                         locked <= 1;
                         lock_timer <= LOCK_TIME;
                         unlocked <= 0;
                         alert <= 0;
                     end
                 end
             end
         end
     end

endmodule
```

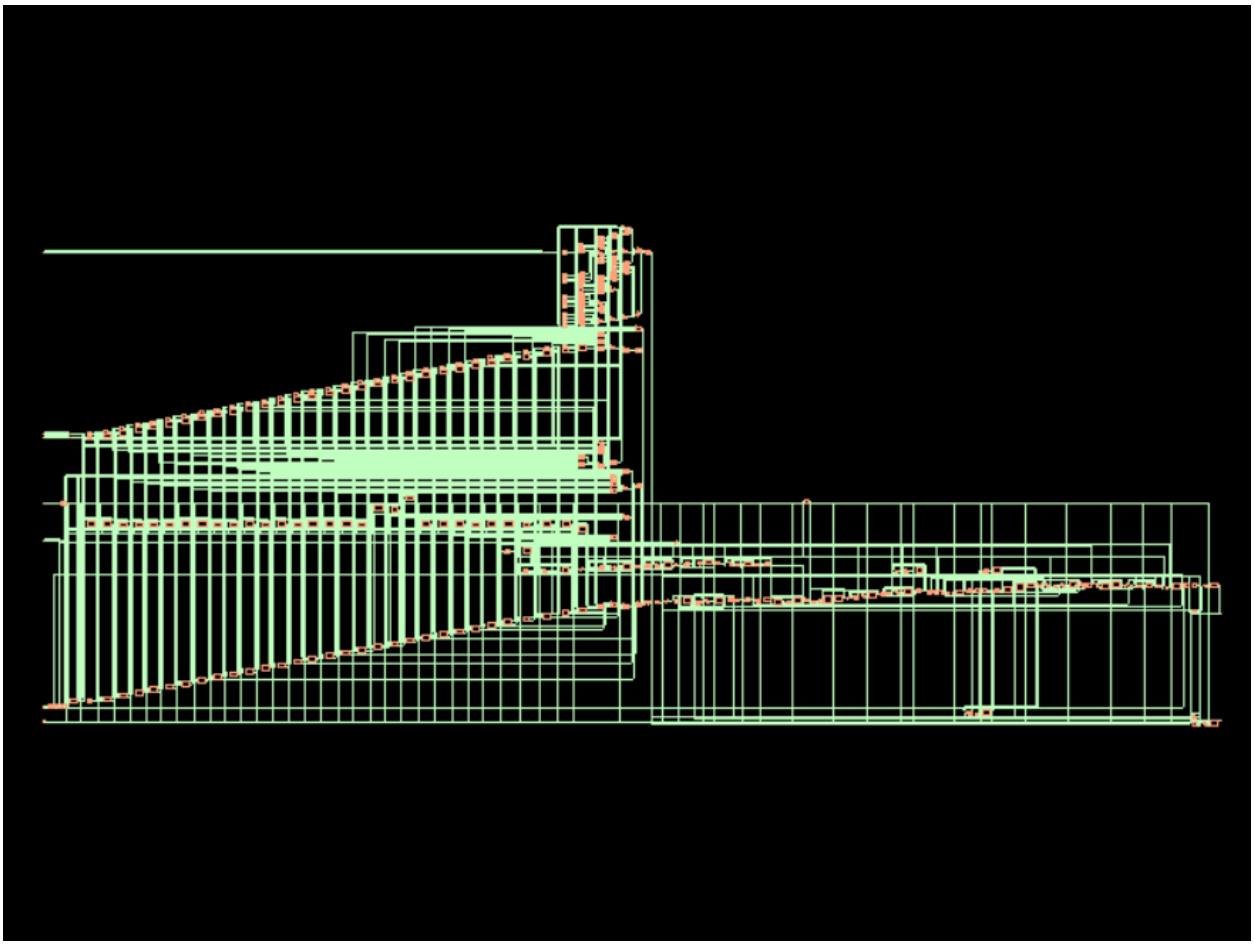
Test Bench

```
`timescale 1ns / 1ps

module tb_digital_safe;

    reg clk;
    reg rst;
    reg [31:0] entered_code;
    reg [31:0] master_code;
    reg [31:0] duress_code;
    reg reset_code_button;
    reg [31:0] new_code;
    reg confirm_reset;
    wire unlocked;
    wire alert;

    digital_safe uut (
        .clk(clk),
        .rst(rst),
        .entered_code(entered_code),
        .master_code(master_code),
        .duress_code(duress_code),
        .reset_code_button(reset_code_button),
        .new_code(new_code),
        .confirm_reset(confirm_reset),
        .unlocked(unlocked),
        .alert(alert)
    );

    // Clock Generation
    initial begin
        clk = 0;
        forever #10 clk = ~clk; // 50 MHz clock
    end

    initial begin
        // Initialize Inputs
        rst = 1;
        entered_code = 32'h0;
        master_code = 32'h87654321;
        duress_code = 32'h11112222;
        reset_code_button = 0;
        new_code = 32'hAABBCCDD;
        confirm_reset = 0;

        #50;
        rst = 0;

        // Test correct code
        #20;
        entered_code = 32'h12345678;
        #20;

        // Test incorrect attempts
        entered_code = 32'hDEADBEEF; #20;
        entered_code = 32'hCAFEBABE; #20;
        entered_code = 32'hBAD0C0DE; #20;

        // Wait for lock
        #100;

        // Test master code unlock
        entered_code = 32'h87654321; #20;

        // Reset password
        reset_code_button = 1;
        confirm_reset = 1;
        #20;
        reset_code_button = 0;
        confirm_reset = 0;

        // Test with new code
        entered_code = 32'hAABBCCDD; #20;

        // Test duress code
        entered_code = 32'h11112222; #20;

        #100;
        $stop;
    end

endmodule
```

Wave Form



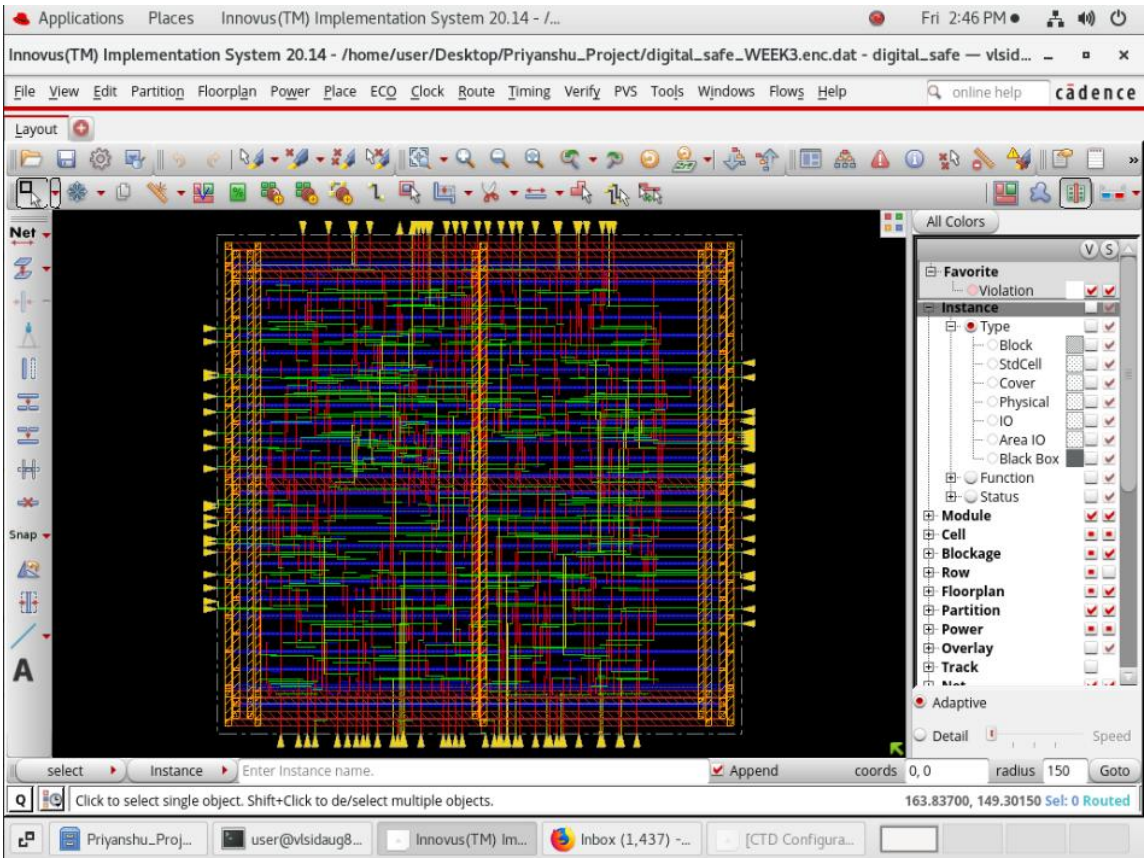
Synthesis

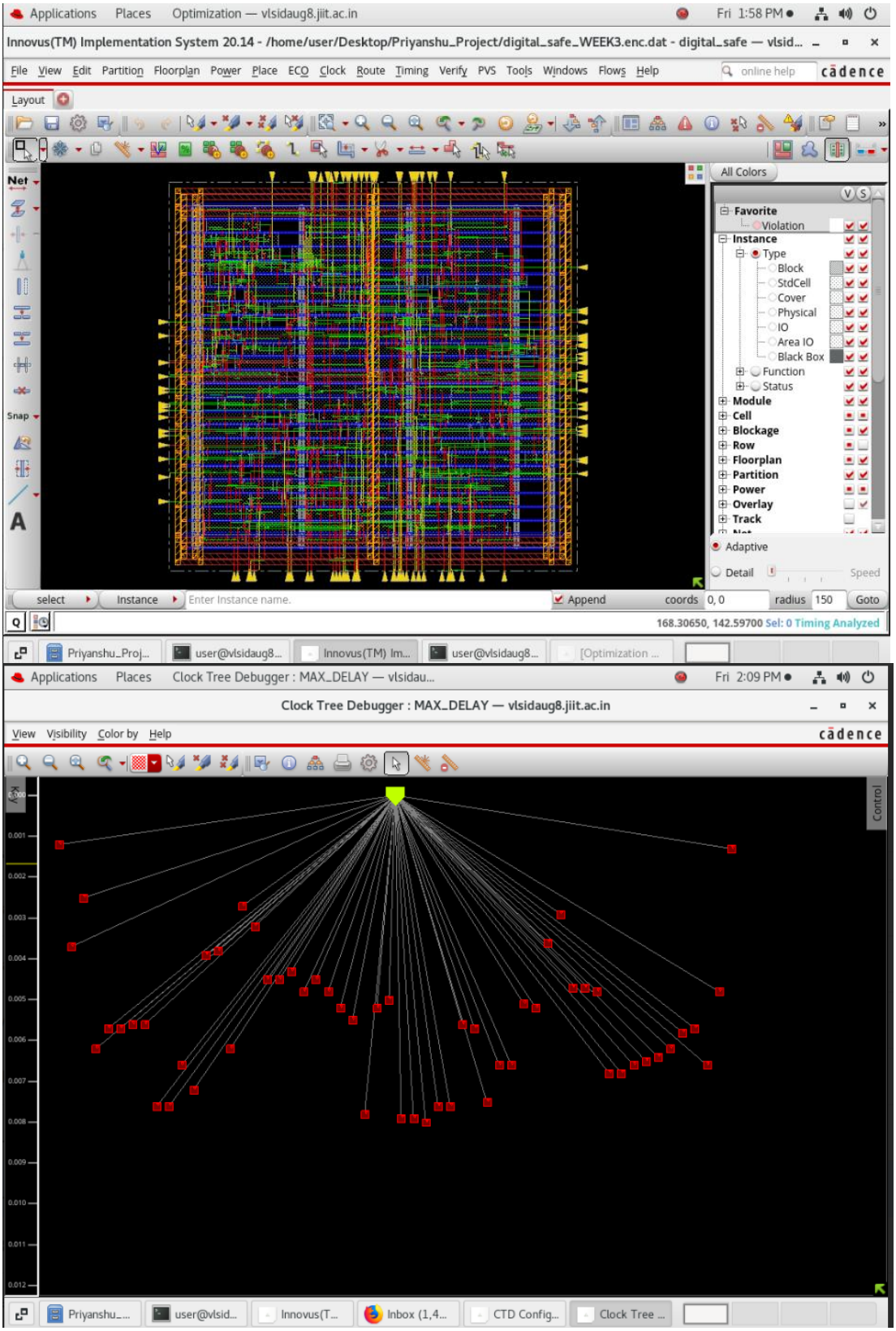


```
legacy_genus:/> report power
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Info    : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
        : digital_safe
Info    : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info    : ACTP-0001 Activity propagation ended for stim#0
Info    : PWRA-0001 [PwrInfo] compute_power effective options
        : -mode : vectorless
        : -skip_propagation : 1
        : -frequency_scaling_factor : 1.0
        : -use_clock_freq : stim
        : -stim :/stim#0
        : -fromGenus : 1
Info    : ACTP-0001 Timing initialization started
Info    : ACTP-0001 Timing initialization ended
Info    : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
        : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
        : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
        : of power analysis, ignored this option.
Info    : PWRA-0002 Started 'vectorless' power computation.
Info    : PWRA-0009 [PwrInfo] Power Computation Progress Report : 100%
Info    : PWRA-0002 Finished power computation.
Info    : PWRA-0007 [PwrInfo] Completed successfully.
        : Info=6, Warn=2, Error=0, Fatal=0
Instance: /digital_safe
Power Unit: W
PDB Frames: /stim#0/frame#0
  ---------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ---------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     1.01576e-07  2.60008e-05  2.46114e-06  2.85635e-05  33.88%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     1.57909e-07  3.48826e-05  2.07134e-05  5.57539e-05  66.12%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ---------------------------------------------------------------------------
    Subtotal     2.59485e-07  6.08834e-05  2.31746e-05  8.43174e-05 100.00%
  Percentage           0.31%       72.21%       27.48%      100.00% 100.00%
  ---------------------------------------------------------------------------



legacy_genus:/> report area
================================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jul 25 2025  12:44:06 pm
  Module:                 digital_safe
  Technology library:     fast
  Operating conditions:   fast (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================

  Instance   Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-------------------------------------------------------------------------------
digital_safe               329      0.000     0.000        0.000 <none> (D)
  (D) = wireload is default in technology library
```

```
legacy_genus:/> report timing
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jul 25 2025  12:44:09 pm
  Module:                 digital_safe
  Technology library:     fast
  Operating conditions:   fast (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

              Pin                      Type      Fanout Load Slew Delay Arrival
                                                      (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------------
current_code_reg[1]/CK                                          0    +0       0 R
current_code_reg[1]/QN               SDFFRX4         1  2.5   13  +111     111 F
csa_tree_ADD_TC_OP16_groupi_g2187/B                                 +0     111
csa_tree_ADD_TC_OP16_groupi_g2187/CO ADDFXL          1  2.0   37   +66     176 F
csa_tree_ADD_TC_OP16_groupi_g2186/CI                                +0     176
csa_tree_ADD_TC_OP16_groupi_g2186/CO ADDFXL          1  2.0   38   +67     243 F
csa_tree_ADD_TC_OP16_groupi_g2185/CI                                +0     243
csa_tree_ADD_TC_OP16_groupi_g2185/CO ADDFXL          1  2.0   38   +67     310 F
csa_tree_ADD_TC_OP16_groupi_g2184/CI                                +0     310
csa_tree_ADD_TC_OP16_groupi_g2184/CO ADDFXL          1  2.0   38   +67     377 F
csa_tree_ADD_TC_OP16_groupi_g2183/CI                                +0     377
csa_tree_ADD_TC_OP16_groupi_g2183/CO ADDFXL          1  2.0   38   +67     444 F
csa_tree_ADD_TC_OP16_groupi_g2182/CI                                +0     444
csa_tree_ADD_TC_OP16_groupi_g2182/CO ADDFXL          1  2.0   38   +67     511 F
csa_tree_ADD_TC_OP16_groupi_g2181/CI                                +0     511
csa_tree_ADD_TC_OP16_groupi_g2181/CO ADDFXL          1  2.0   38   +67     578 F
csa_tree_ADD_TC_OP16_groupi_g2180/CI                                +0     578
csa_tree_ADD_TC_OP16_groupi_g2180/CO ADDFXL          1  2.0   38   +67     644 F
csa_tree_ADD_TC_OP16_groupi_g2179/CI                                +0     644
csa_tree_ADD_TC_OP16_groupi_g2179/CO ADDFXL          1  2.0   38   +67     711 F
csa_tree_ADD_TC_OP16_groupi_g2178/CI                                +0     711
csa_tree_ADD_TC_OP16_groupi_g2178/CO ADDFXL          1  2.0   38   +67     778 F
csa_tree_ADD_TC_OP16_groupi_g2177/CI                                +0     778
csa_tree_ADD_TC_OP16_groupi_g2177/CO ADDFXL          1  2.0   38   +67     845 F
csa_tree_ADD_TC_OP16_groupi_g2176/CI                                +0     845
csa_tree_ADD_TC_OP16_groupi_g2176/CO ADDFXL          1  2.0   38   +67     912 F
csa_tree_ADD_TC_OP16_groupi_g2175/CI                                +0     912
csa_tree_ADD_TC_OP16_groupi_g2175/CO ADDFXL          1  2.0   38   +67     979 F
csa_tree_ADD_TC_OP16_groupi_g2174/CI                                +0     979
csa_tree_ADD_TC_OP16_groupi_g2174/CO ADDFXL          1  2.0   38   +67    1046 F
csa_tree_ADD_TC_OP16_groupi_g2173/CI                                +0    1046
csa_tree_ADD_TC_OP16_groupi_g2173/CO ADDFXL          1  2.0   38   +67    1113 F
csa_tree_ADD_TC_OP16_groupi_g2172/CI                                +0    1113
csa_tree_ADD_TC_OP16_groupi_g2172/CO ADDFXL          1  2.0   38   +67    1180 F
csa_tree_ADD_TC_OP16_groupi_g2171/CI                                +0    1180
csa_tree_ADD_TC_OP16_groupi_g2171/CO ADDFXL          1  2.0   38   +67    1246 F
csa_tree_ADD_TC_OP16_groupi_g2170/CI                                +0    1246
csa_tree_ADD_TC_OP16_groupi_g2170/CO ADDFXL          1  2.0   38   +67    1313 F
csa_tree_ADD_TC_OP16_groupi_g2169/CI                                +0    1313
csa_tree_ADD_TC_OP16_groupi_g2169/CO ADDFXL          1  2.0   38   +67    1380 F
csa_tree_ADD_TC_OP16_groupi_g2168/CI                                +0    1380
csa_tree_ADD_TC_OP16_groupi_g2168/CO ADDFXL          1  2.0   38   +67    1447 F
csa_tree_ADD_TC_OP16_groupi_g2167/CI                                +0    1447
csa_tree_ADD_TC_OP16_groupi_g2167/CO ADDFXL          1  2.0   38   +67    1514 F
csa_tree_ADD_TC_OP16_groupi_g2166/CI                                +0    1514
csa_tree_ADD_TC_OP16_groupi_g2166/CO ADDFXL          1  2.0   38   +67    1581 F
csa_tree_ADD_TC_OP16_groupi_g2165/CI                                +0    1581
csa_tree_ADD_TC_OP16_groupi_g2165/CO ADDFXL          1  2.0   38   +67    1648 F
csa_tree_ADD_TC_OP16_groupi_g2164/CI                                +0    1648
csa_tree_ADD_TC_OP16_groupi_g2164/CO ADDFXL          1  2.0   38   +67    1715 F
csa_tree_ADD_TC_OP16_groupi_g2163/CI                                +0    1715
csa_tree_ADD_TC_OP16_groupi_g2163/CO ADDFXL          1  2.0   38   +67    1782 F
csa_tree_ADD_TC_OP16_groupi_g2162/CI                                +0    1782
csa_tree_ADD_TC_OP16_groupi_g2162/CO ADDFXL          1  2.0   38   +67    1849 F
csa_tree_ADD_TC_OP16_groupi_g2161/CI                                +0    1849
csa_tree_ADD_TC_OP16_groupi_g2161/CO ADDFXL          1  2.0   38   +67    1916 F
csa_tree_ADD_TC_OP16_groupi_g2160/CI                                +0    1916
csa_tree_ADD_TC_OP16_groupi_g2160/CO ADDFXL          1  2.0   38   +67    1982 F
csa_tree_ADD_TC_OP16_groupi_g2159/CI                                +0    1982
csa_tree_ADD_TC_OP16_groupi_g2159/CO ADDFXL          1  2.0   38   +67    2049 F
csa_tree_ADD_TC_OP16_groupi_g2158/CI                                +0    2049
csa_tree_ADD_TC_OP16_groupi_g2158/CO ADDFXL          1  1.5   33   +64    2114 F
csa_tree_ADD_TC_OP16_groupi_g2/C                                    +0    2114
csa_tree_ADD_TC_OP16_groupi_g2/Y     XNOR3XL         1  0.9   28   +47    2161 R
g5348/D                                                             +0    2161
g5348/Y                              NAND4X1         1  0.9   54   +32    2192 F
g5497/AN                                                            +0    2192
g5497/Y                              NAND4BBX4       1  3.3   58   +70    2262 F
g5356/D                                                             +0    2262
g5356/Y                              NOR4BBX4        1  0.7   50   +26    2288 R
g5178/B1                                                            +0    2288
g5178/Y                              AO22X1          2  1.2   20   +45    2332 R
g5174/B                                                             +0    2332
g5174/Y                              OR2X1           3  1.9   18   +26    2358 R
g5173/B                                                             +0    2358
g5173/Y                              OR2X1           3  2.2   20   +26    2384 R
g5168/B                                                             +0    2384
g5168/Y                              OR2X1           4  3.8   31   +32    2416 R
g5166/A                                                             +0    2416
g5166/Y                              CLKINVX2        5  3.9   19   +17    2433 F
g5143/B                                                             +0    2433
g5143/Y                              OR2X1           2  2.4   24   +39    2472 F
g5139/A                                                             +0    2472
g5139/Y                              CLKINVX2       11  7.0   28   +20    2491 R
g5132/B0                                                            +0    2491
g5132/Y                              AO21X2          2  1.2   17   +31    2522 R
g5113/A1                                                            +0    2522
g5113/Y                              AO21X2          1  0.8   16   +44    2566 R
lock_timer_reg[16]/D                 DFFRHQX8                           +0    2566
lock_timer_reg[16]/CK                setup                      0   +35    2602 R
-------------------------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : current_code_reg[1]/CK
End-point    : lock_timer_reg[16]/D
```

Floor Planning, Power Planning , Placement , CTS , Routing and RC Extraction




Applications Places Optimization — vlsidaug8.jiit.ac.in
Fri 1:58 PM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/Priyanshu_Project/digital_safe_WEEK3.enc.dat - digital_safe — vlsid...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Net
Snap
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords 0, 0
radius 150
Goto
168.30650, 142.59700 Sel: 0 Timing Analyzed
Priyanshu_Proj...
user@vlsidaug8...
Innovus(TM) Im...
user@vlsidaug8...
[Optimization ...
Applications Places Clock Tree Debugger : MAX_DELAY — vlsidau...
Fri 2:09 PM
Clock Tree Debugger : MAX_DELAY — vlsidaug8.jiit.ac.in
View Visibility Color by Help
cadence
Control
Priyanshu_...
user@vlsid...
Innovus(T...
Inbox (1,4...
CTD Config...
Clock Tree ...

```
------------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.000  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|          All Paths:|    0    |   N/A   |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      1 (1)       |   -0.149   |      1 (1)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 84.653%
Routing Overflow: 0.00% H and 0.34% V
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.16 sec
Total Real time: 0.0 sec
Total Memory Usage: 1469.136719 Mbytes
*** timeDesign #1 [finish] : cpu/real = 0:00:00.1/0:00:00.6 (0.3), totSession cpu/real = 0:00:17.8/0:01:20.6 (0.2), mem = 1469.1M
innovus 1>
```

```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:        0.03519662           70.5921%
Total Switching Power:       0.01457984           29.2421%
Total Leakage Power:         0.00008270            0.1659%
Total Power:                 0.04985916
--------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
Sequential                      0.01414    0.001209   3.199e-05     0.01538       30.86
Macro                                 0           0           0           0           0
IO                                    0           0           0           0           0
Combinational                   0.02105    0.01337   5.071e-05     0.03447       69.14
Clock (Combinational)                 0           0           0           0           0
Clock (Sequential)                    0           0           0           0           0
--------------------------------------------------------------------------------
Total                            0.0352    0.01458    8.27e-05     0.04986         100
--------------------------------------------------------------------------------


Rail                 Voltage   Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
Default                  0.9   0.004369          0   1.462e-05    0.004384       8.792
VDD                      0.9    0.03083    0.01421   6.808e-05      0.0451       90.46


--------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:                    g1426 (INVXL):         0.001766
*              Highest Leakage Power:      current_code_reg[31] (SDFFRHQX8):        7.563e-07
*                Total Cap:      1.92485e-12 F
*                Total instances in design:   329
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*                Total Fillers and Decap:     0
--------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1084.98MB/2621.09MB/1085.09MB)



innovus 2> report_area
    Hinst Name       Module Name          Inst Count           Total Area
--------------------------------------------------------------------------
digital_safe                                    329            13649.516
innovus 3>
```