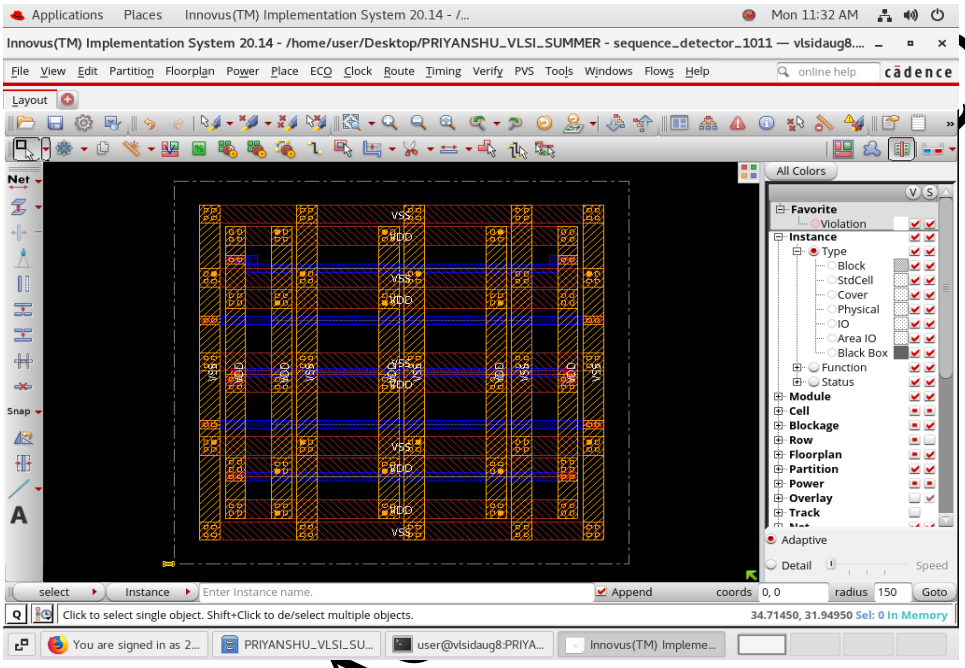
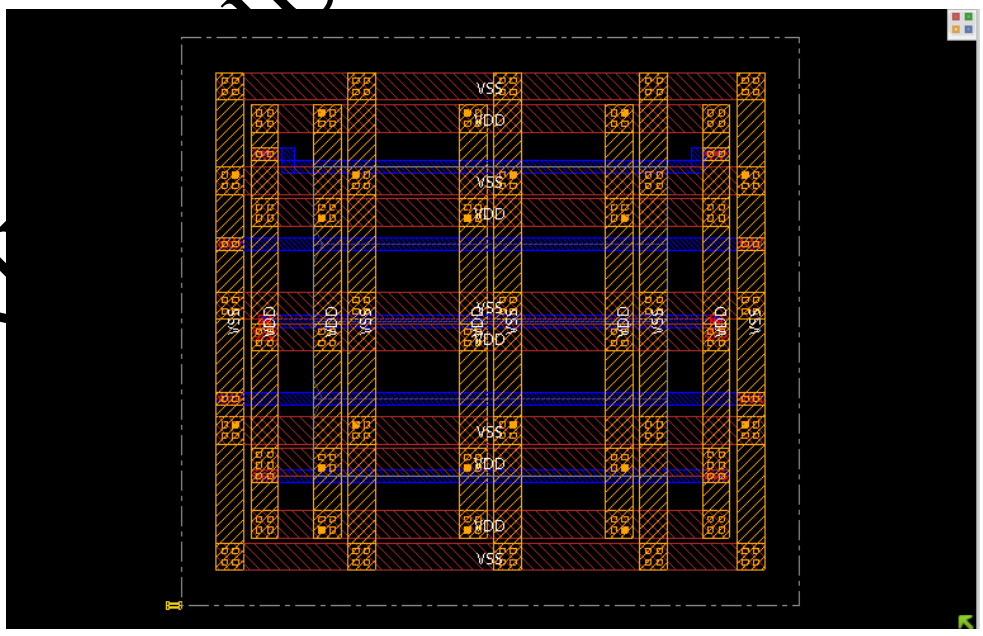
VLSI DESIGN AND AUTOMATION SUMMER INTERNSHIP

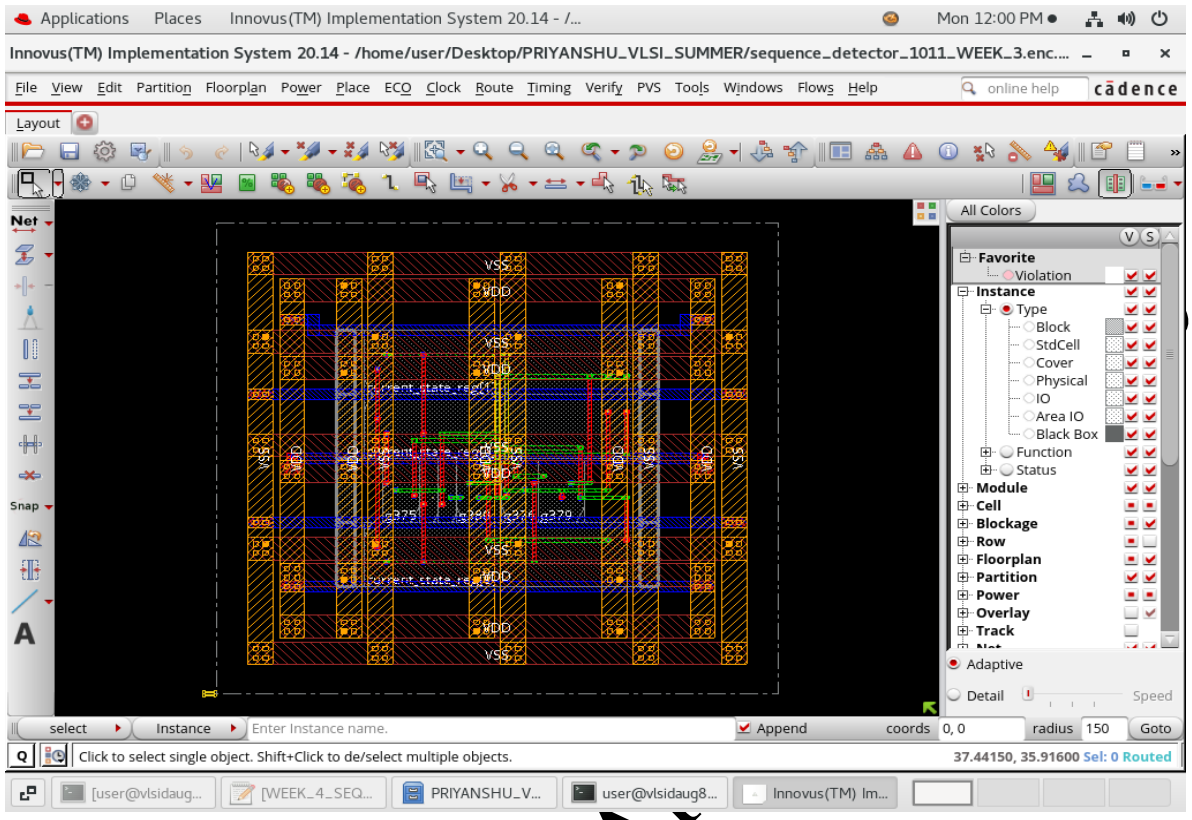
WEEK 4 SUBMISSION

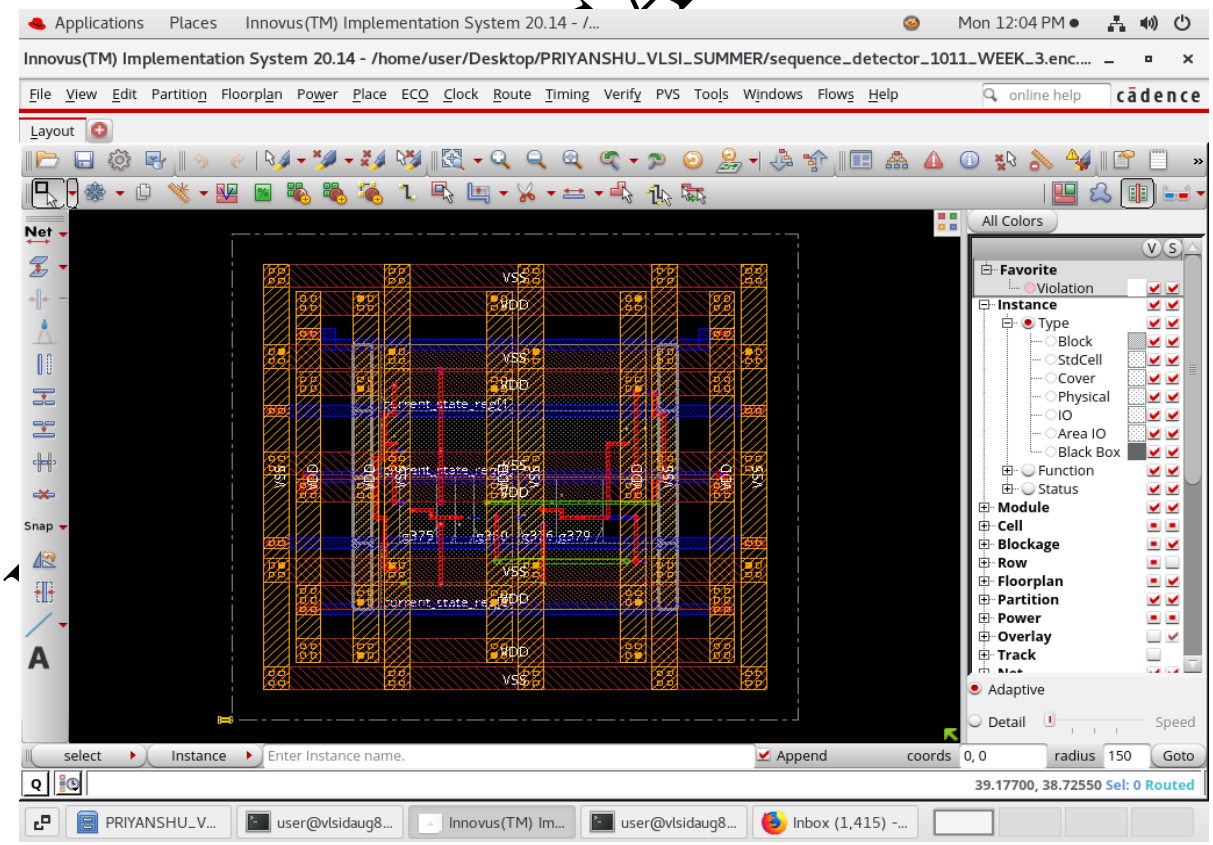
RESOURCE : WEEK 4 (ENC,NETLIST and DATA files are here)

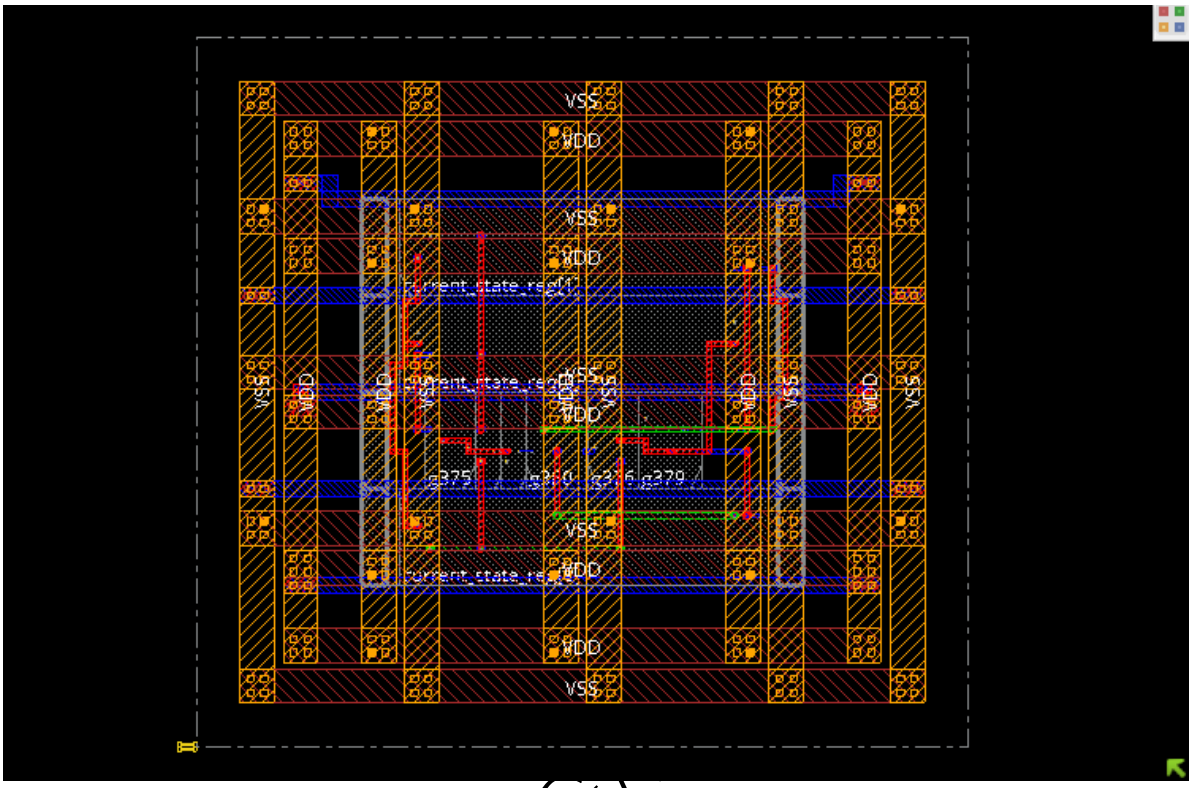
FSM (Finite State Machine) – Sequence Detector 1011

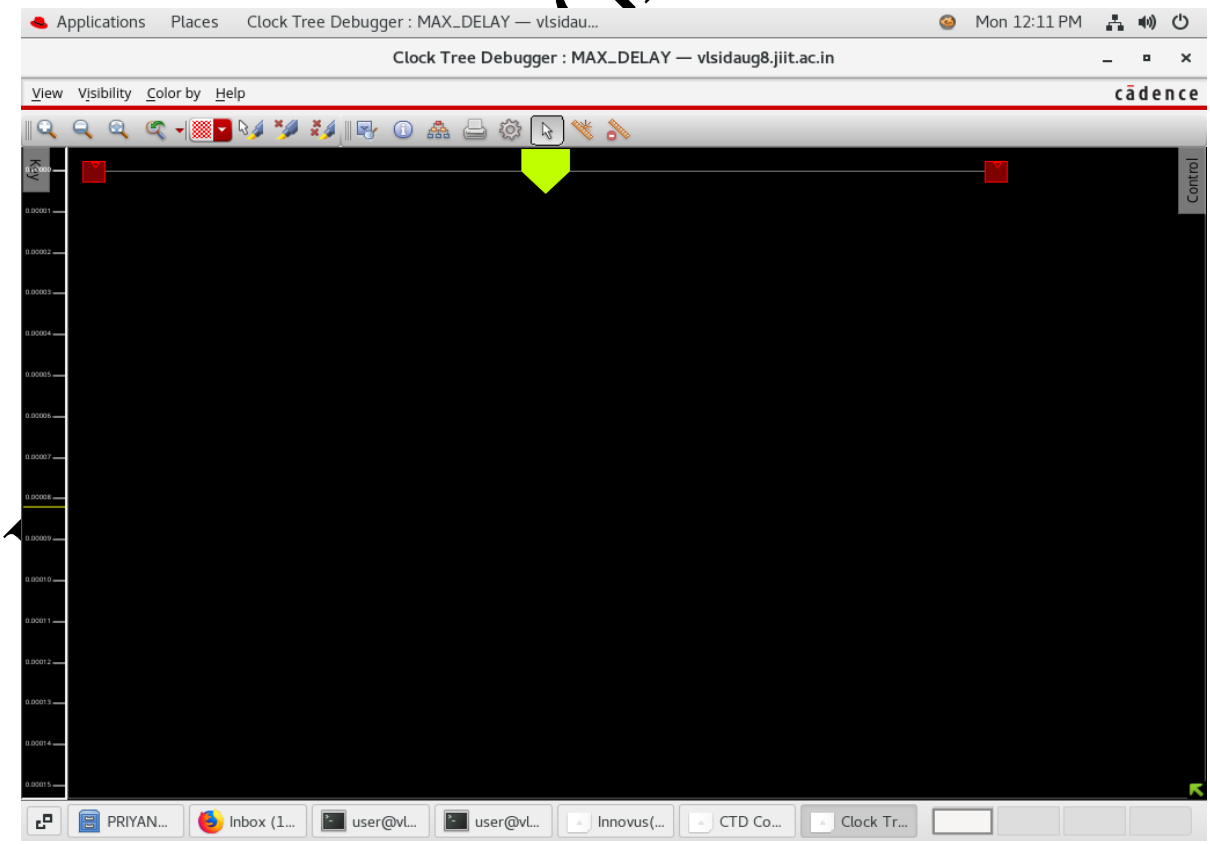




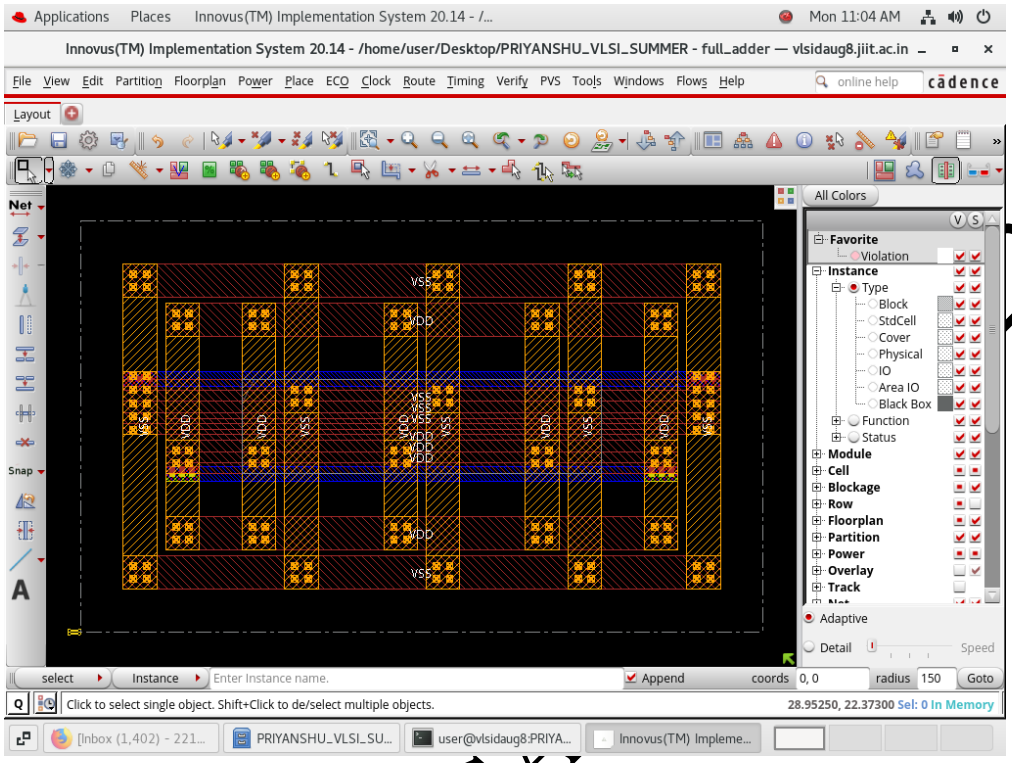

Applications Places Innovus(TM) Implementation System 20.14 - /... Mon 12:00 PM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/PRIYANSHU_VLSI_SUMMER/sequence_detector_1011_WEEK_3.enc....
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Net
Snap
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords 0, 0
radius 150
Goto
Click to select single object. Shift+Click to de/select multiple objects.
37.44150, 35.91600 Sel: 0 Routed
[user@vlsidaug...
[WEEK_4_SEQ...
PRIYANSHU_V...
user@vlsidaug8...
Innovus(TM) Im...

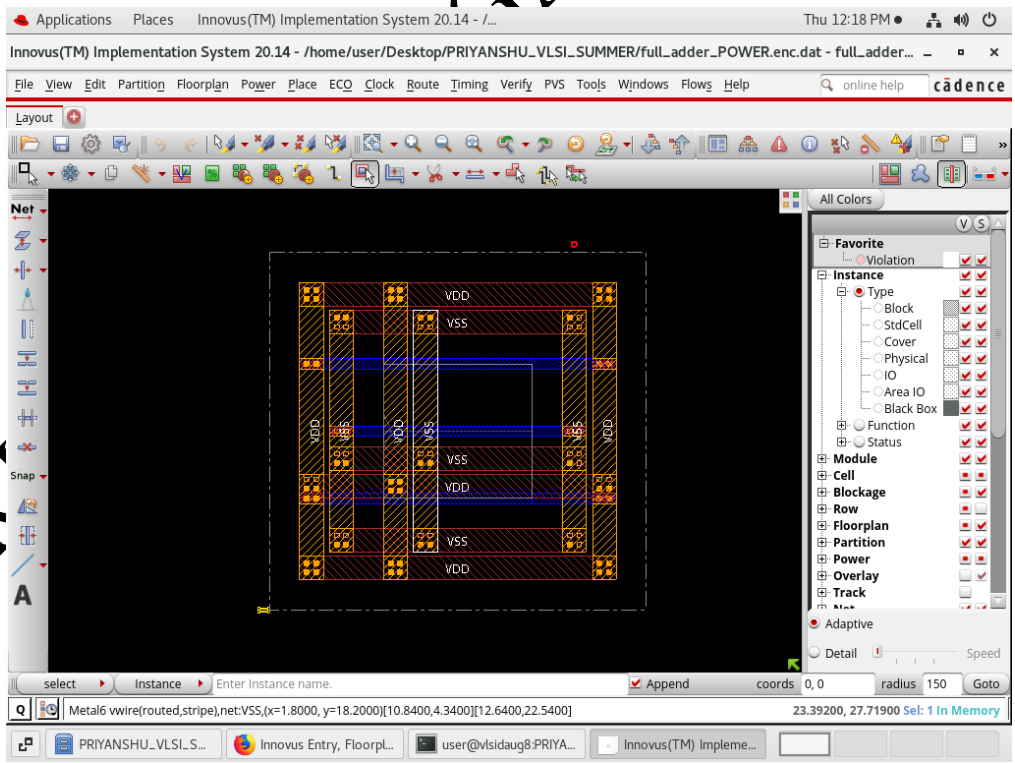

Applications Places Innovus(TM) Implementation System 20.14 - /... Mon 12:04 PM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/PRIYANSHU_VLSI_SUMMER/sequence_detector_1011_WEEK_3.enc....
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Net
Snap
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords 0, 0
radius 150
Goto
39.17700, 38.72550 Sel: 0 Routed
PRIYANSHU_V...
user@vlsidaug8...
Innovus(TM) Im...
user@vlsidaug8...
Inbox (1,415) -...

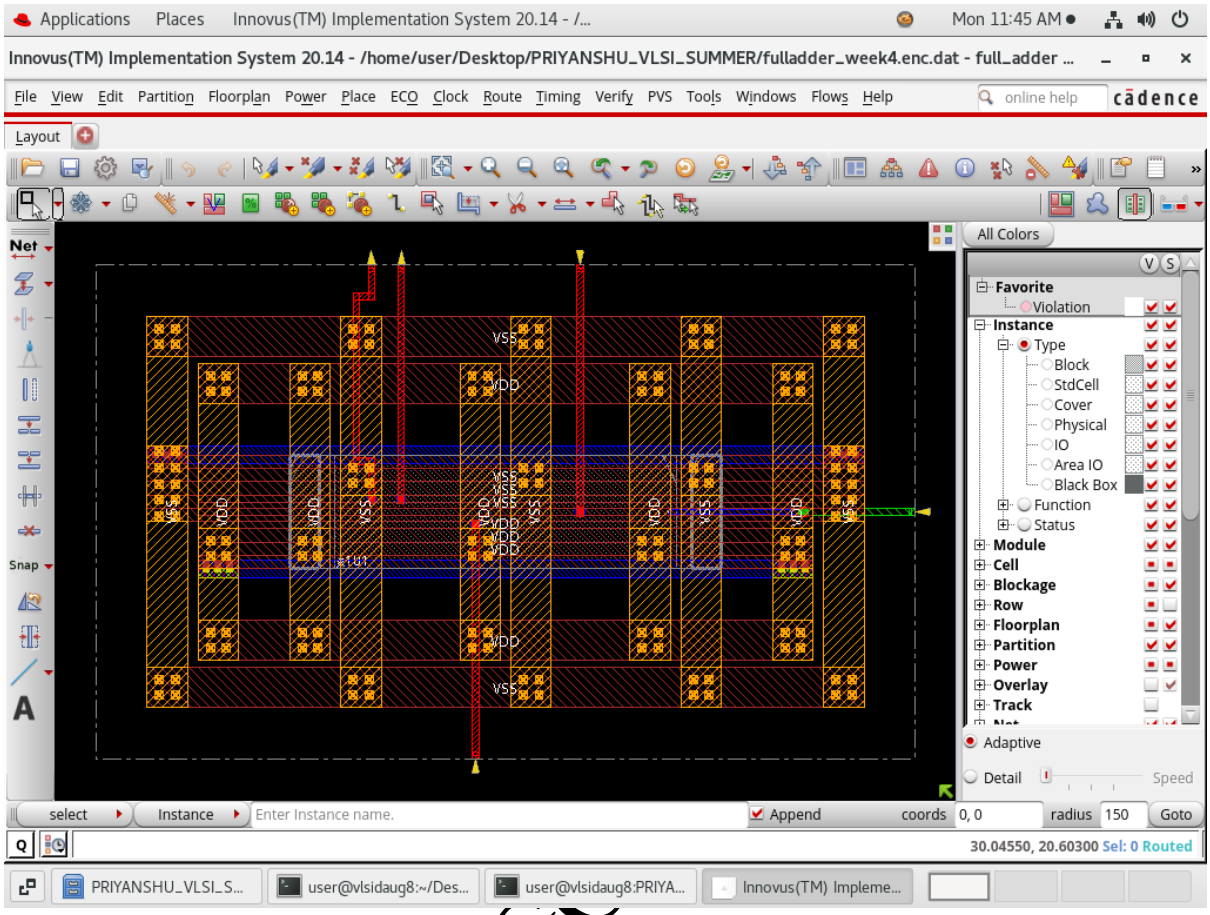

VSS
VDD
VSS
VDD
current_state_reg[1]
current_state_reg[0]
current_state_reg[2]
g375
g279
VSS
VDD
VSS
VDD

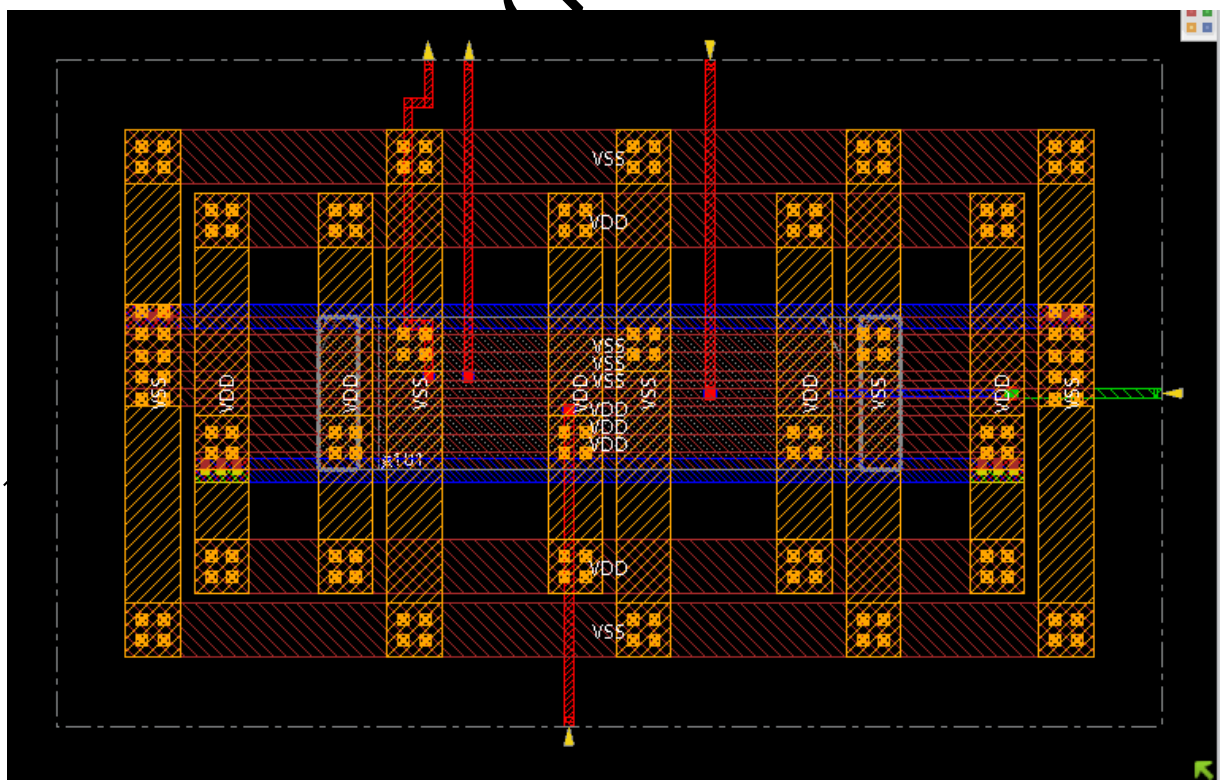

Applications
Places
Clock Tree Debugger : MAX_DELAY — vlsidau...
Mon 12:11 PM
Clock Tree Debugger : MAX_DELAY — vlsidaug8.jiit.ac.in
View
Visibility
Color by
Help
cadence
Control
PRIYAN...
Inbox (1...
user@vl...
user@vl...
Innovus(...
CTD Co...
Clock Tr...

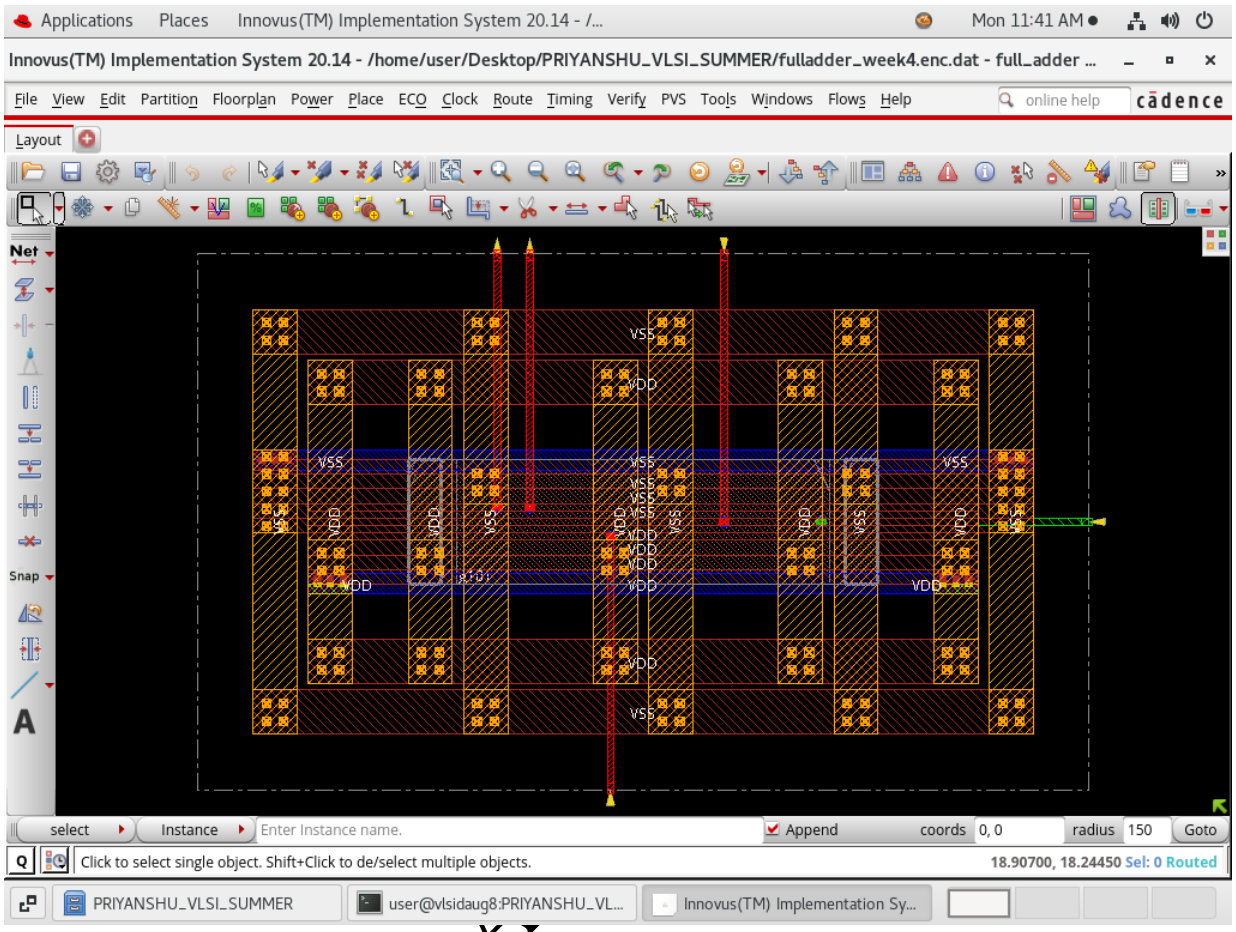
Combination Circuit – Full Adder

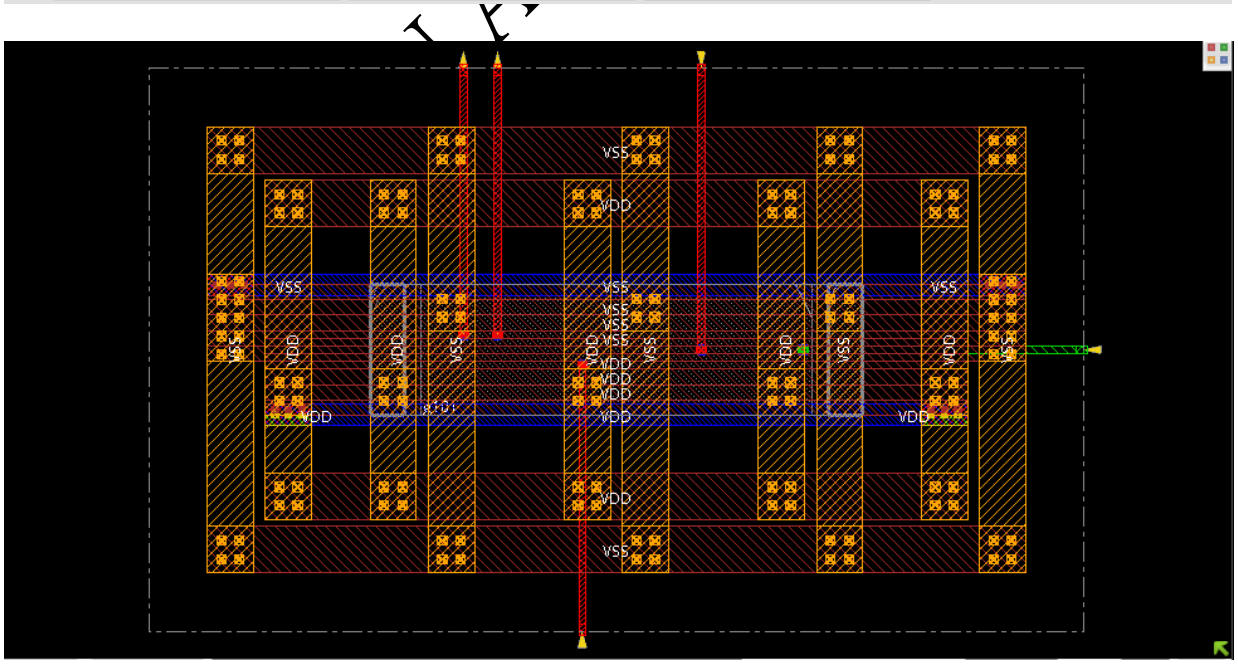




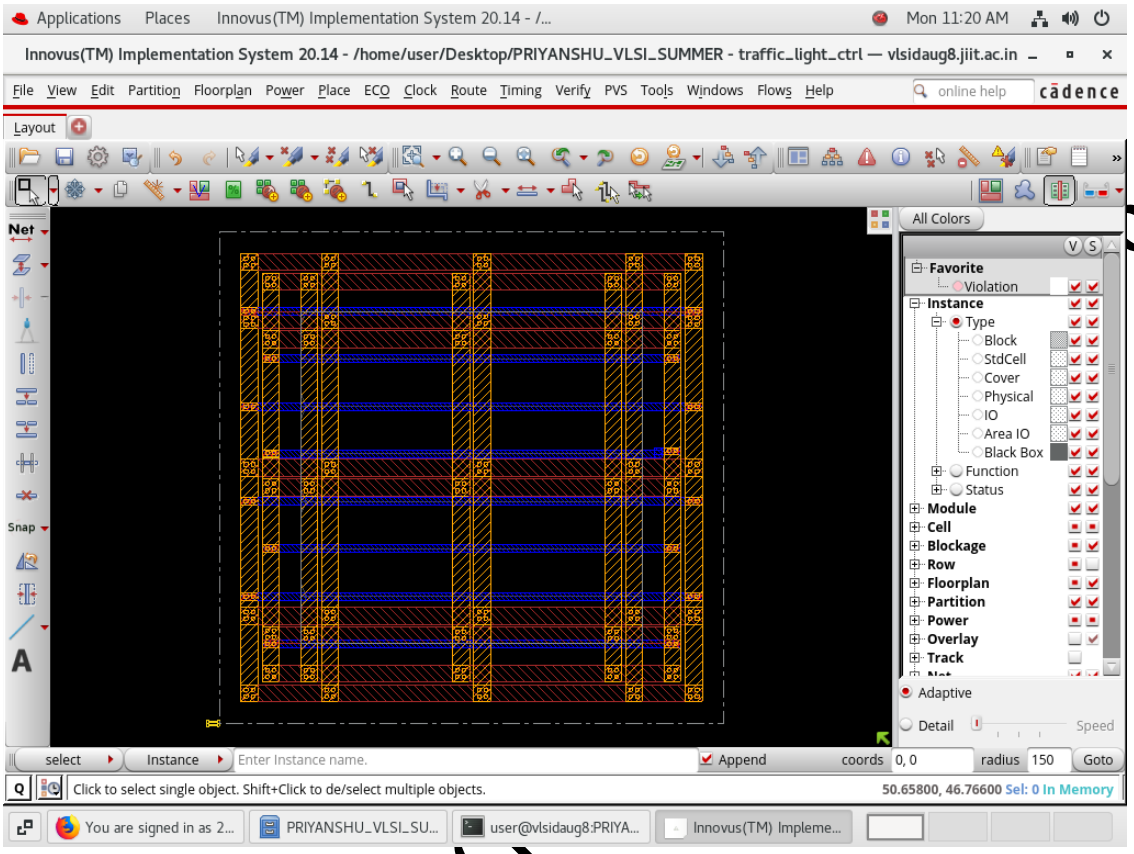

Applications
Places
Innovus(TM) Implementation System 20.14 - /...
Mon 11:45 AM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/PRIYANSHU_VLSI_SUMMER/fulladder_week4.enc.dat - full_adder ...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Net
Snap
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords
0, 0
radius
150
Goto
30.04550, 20.60300 Sel: 0 Routed
PRIYANSHU_VLSI_S...
user@vlsidaug8:~/Des...
user@vlsidaug8:PRIYA...
Innovus(TM) Impleme...
VSS
VDD
xfu1

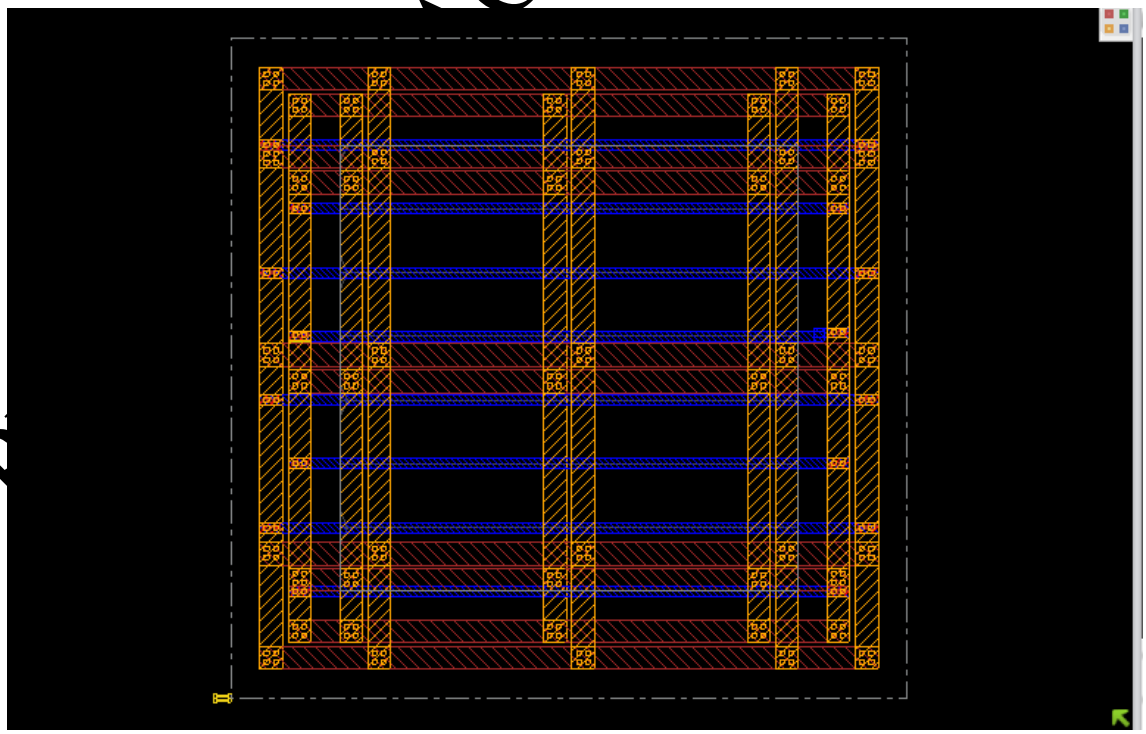

VSS
VDD
xfu1

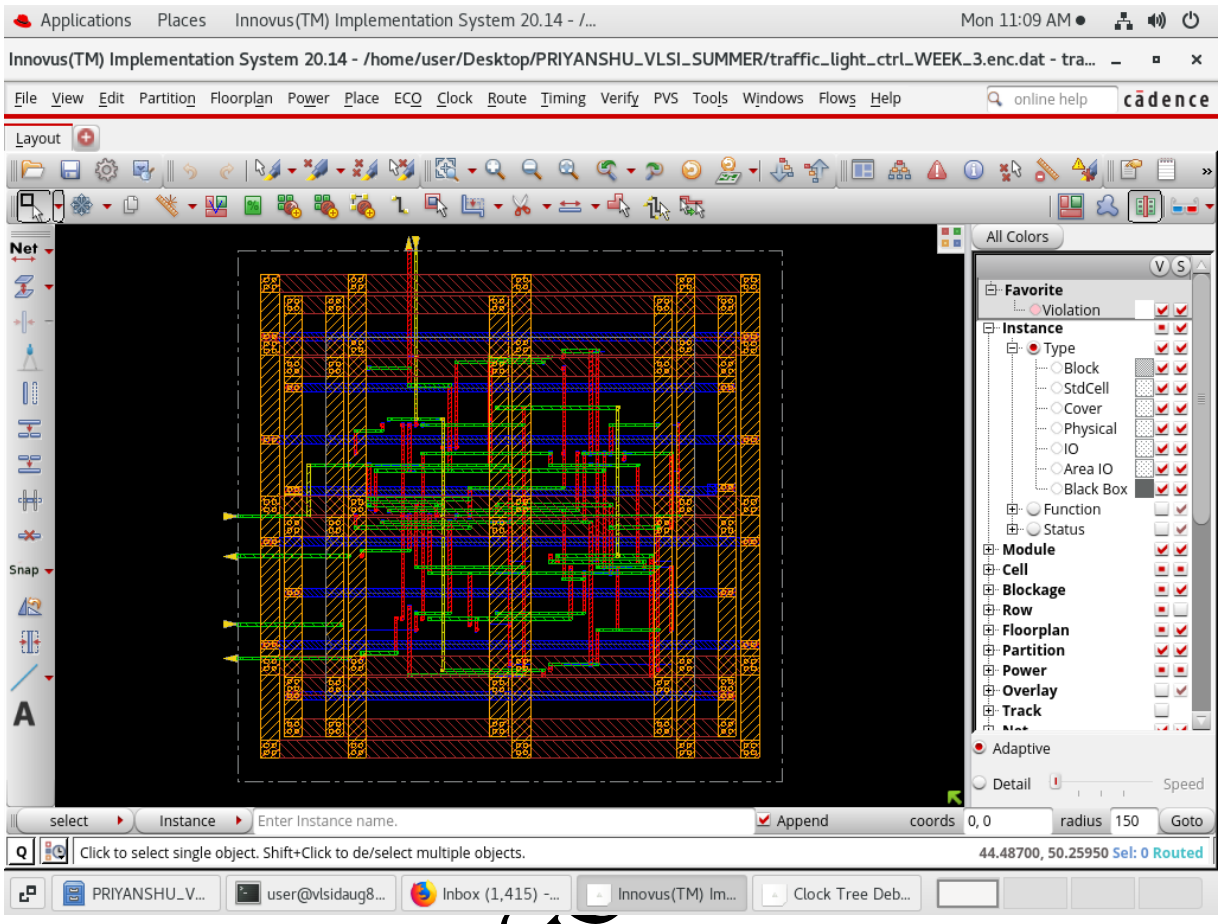

Applications
Places
Innovus(TM) Implementation System 20.14 - /...
Mon 11:41 AM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/PRIYANSHU_VLSI_SUMMER/fulladder_week4.enc.dat - full_adder ...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
Net
Snap
A
VSS
VDD
select
Instance
Enter Instance name.
Append
coords 0, 0
radius 150
Goto
Click to select single object. Shift+Click to de/select multiple objects.
18.90700, 18.24450 Sel: 0 Routed
PRIYANSHU_VLSI_SUMMER
user@vlsidaug8:PRIYANSHU_VL...
Innovus(TM) Implementation Sy...


VSS
VDD

Sequential Circuit – Traffic Light Control






Applications
Places
Innovus(TM) Implementation System 20.14 - /...
Mon 11:09 AM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/PRIYANSHU_VLSI_SUMMER/traffic_light_ctrl_WEEK_3.enc.dat - tra...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
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Area IO
Black Box
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Blockage
Row
Floorplan
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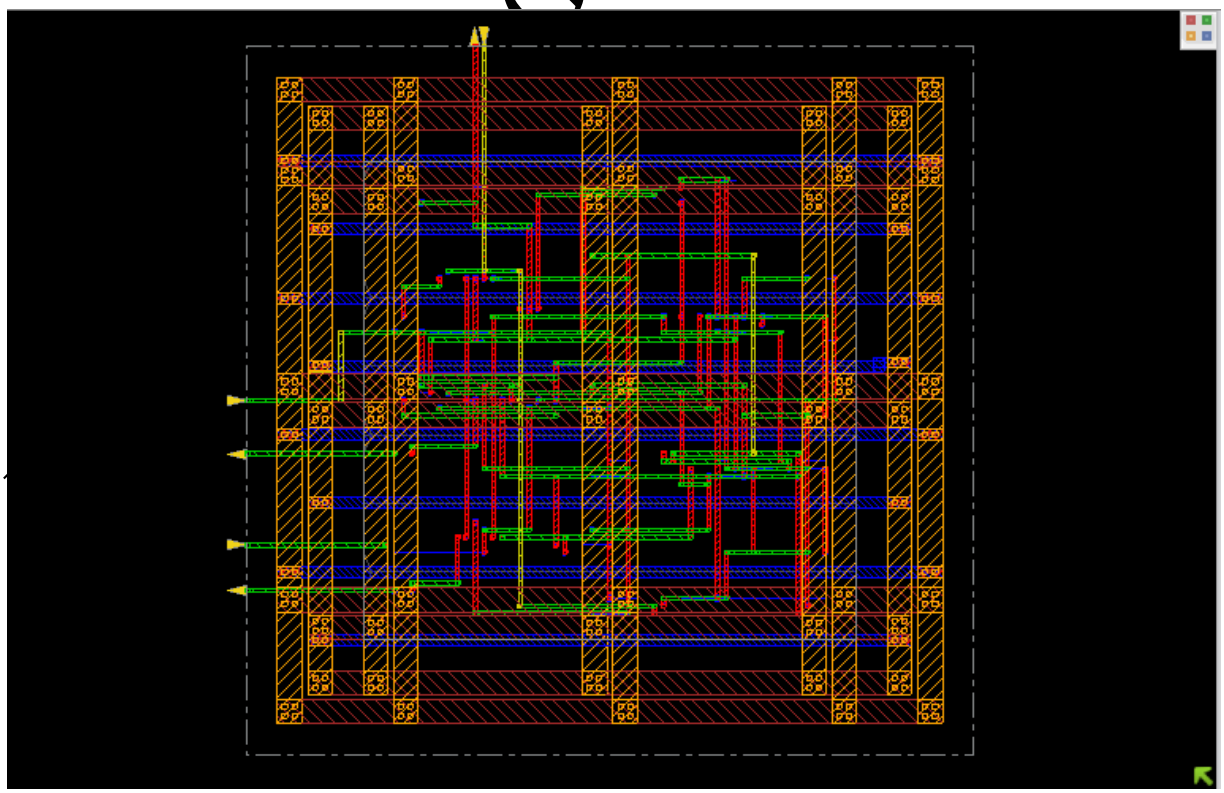
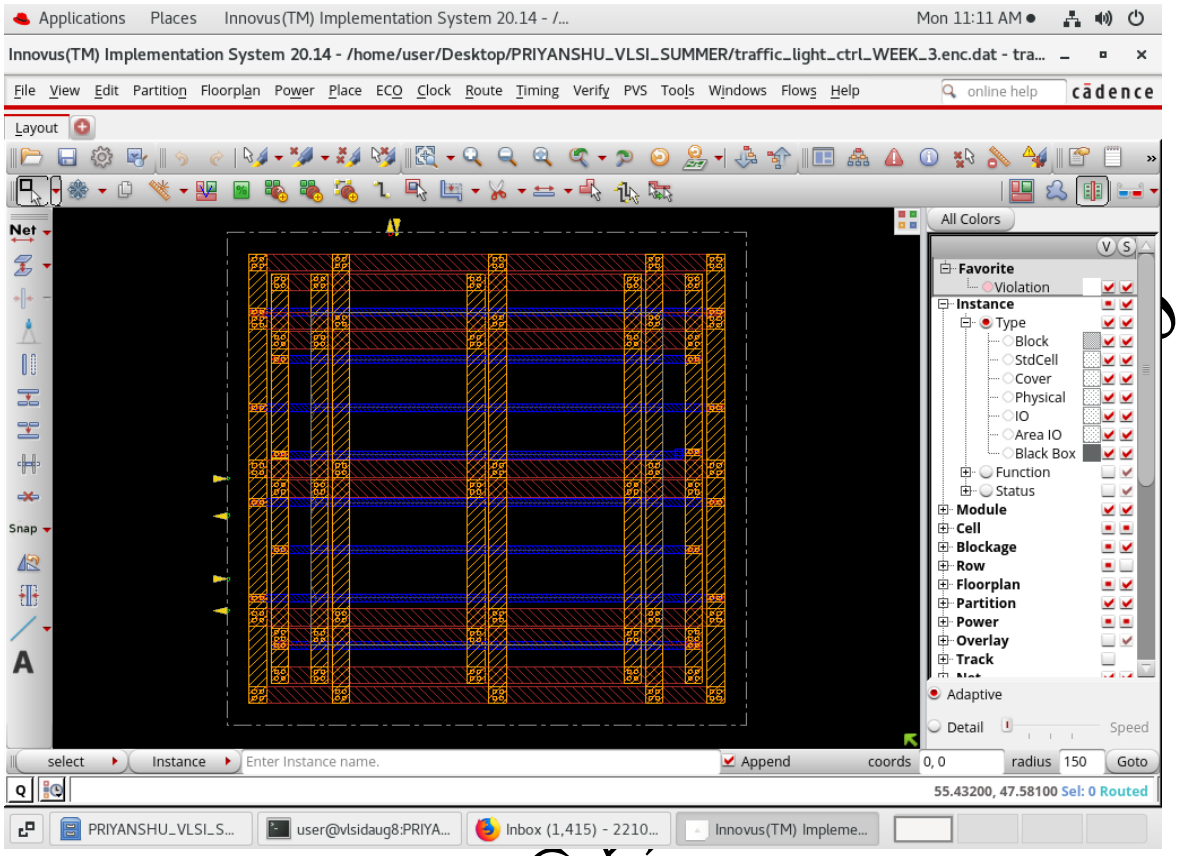
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords
0, 0
radius
150
Goto
Click to select single object. Shift+Click to de/select multiple objects.
44.48700, 50.25950 Sel: 0 Routed
PRIYANSHU_V...
user@vlsidaug8...
Inbox (1,415) -...
Innovus(TM) Im...
Clock Tree Deb...




Applications Places Innovus(TM) Implementation System 20.14 - /... Mon 11:11 AM
Innovus(TM) Implementation System 20.14 - /home/user/Desktop/PRIYANSHU_VLSI_SUMMER/traffic_light_ctrl_WEEK_3.enc.dat - tra...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
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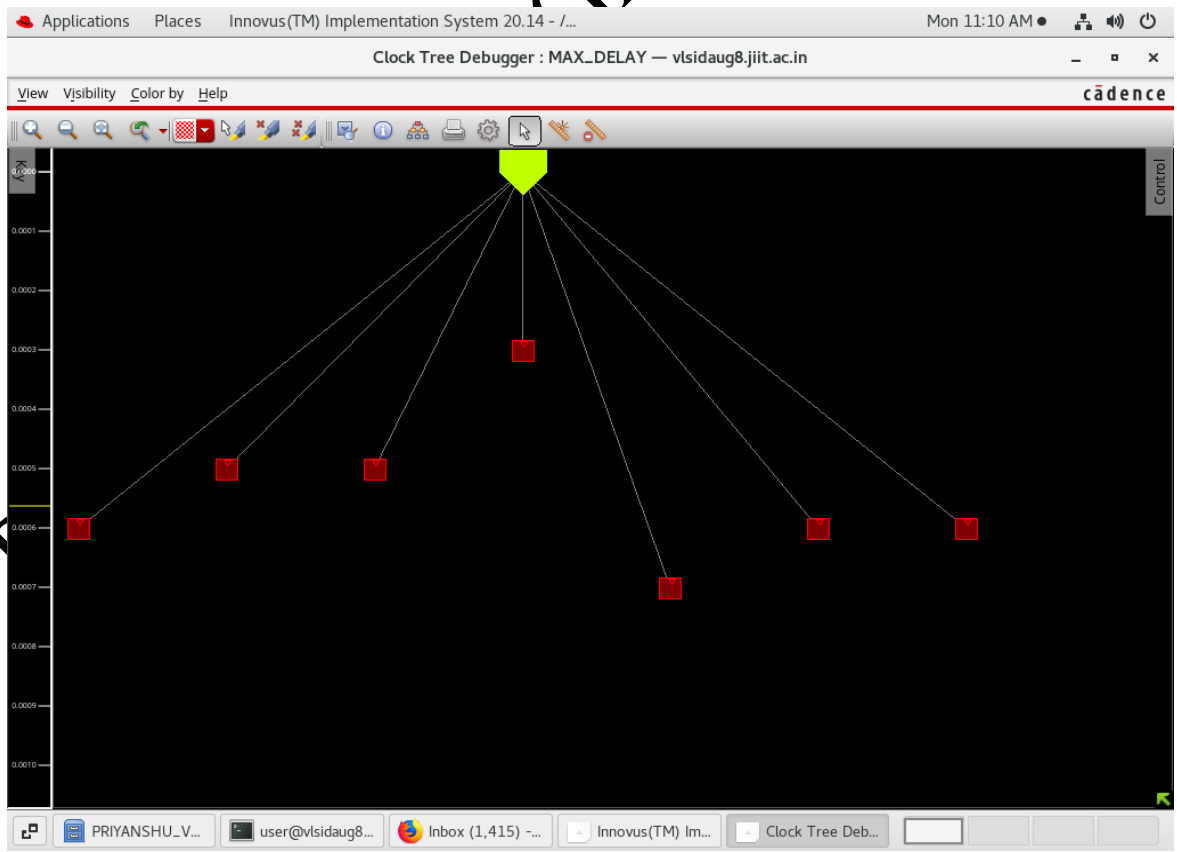
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Adaptive
Detail
Speed
select
Instance
Enter Instance name.
Append
coords
0, 0
radius
150
Goto
55.43200, 47.58100 Sel: 0 Routed
PRIYANSHU_VLSI_S...
user@vlsidaug8:PRIYA...
Inbox (1,415) - 2210...
Innovus(TM) Impleme...


Applications Places Innovus(TM) Implementation System 20.14 - /... Mon 11:10 AM
Clock Tree Debugger : MAX_DELAY — vlsidaug8.jiit.ac.in
View Visibility Color by Help
cadence
Control
PRIYANSHU_V...
user@vlsidaug8...
Inbox (1,415) -...
Innovus(TM) Im...
Clock Tree Deb...

PRIYANSHU AGGARWAL 2210236