

## BASIC DETAILS

Enrollment No. : ..... 22102236 .....

Name : ..... Polyonkhu Aggarwal .....

Department : ..... F.C.P. ..... Mob. 828717464

E-mail ID : ..... aggarwal.polyonkhu.902.6@gmail.com .....

Name of the Organisation : ..... J.I.I.T., Noida .....

Address : ..... A-10, Sector-62 .....

.....  
Noida, U.P. .....

Training Period (with date) : From ..... 9 June To 21 July .....

Training In-charge : Name : Dr. Shreuti Kalra .....

Designation : ..... Associate Professor .....

Signature of the Student : ..... Aneesh .....

Signature of the Training In-charge : .....

(With date and seal on the day student joins training)

# REPORT/REMARKS OF TRAINING INCHARGE

Remarks of Training In-charge :

Priyanshu has done good work with dedication. He was able to complete given project within allotted time frame.

Given below is the list of topics covered during the training.

*Sunita Karki  
for 12/9/25*

Signature of the Training In-charge

(With date and seal on the last day of the training)

Week -1

Date: 10/1 June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

The first two days were dedicated to setting up the Cadence stimulation environment and revising working HDL basics, I implemented around 15 Combinational Circuits such as adders, multiplexers and encoders writing corresponding test benches for each design.

Careful debugging helped me understand error patterns and improve accuracy; observing waveforms reinforced the connection between HDL coding and hardware behaviour. These exercises not only refreshed my digital logic foundation but also gave me a confidence in handling the tools like Cadence Xcellium. The process was challenging but manageable, and it prepared me for more complex designs.

Signature of Student :

Date: 12 / June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

During the next two days, I focused on sequential circuits and Fsm, I did - flip-flops, counters, shift registers, and traffic light controllers, verifying each through detailed test benches and waveform simulations. By the end of day 4, I had nearly completed ~~flame~~ <sup>6</sup> additional designs, raising my total to about 38. Debugging these circuits taught me the importance of initialization, clocking and state transitions, working with Fsm's gave me practical insights into how real-world systems are modelled digitally. The workload was intense but rewarding as I learned to balance speed and precision. These tasks further improved my coding discipline and problem solving.

Signature of Student :

Date: 14 / June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

The final day of week 1 continued on integrating concepts into larger projects, I designed as a bit Psm. using counters and many more, writing their testbenches and underlying waveforms allowed me to validate correctness across multiple operations. Additionally, I completed the remaining set of Odds, bringing the total to over fifty verilog designs with verified testbenches and simulations by the end of week 1. A brief introduction to synthesis helped me understand how RTL translates into gate-level hardware. This was the end of first week of my internship.

Signature of Student :

## Week-2

Date: 17 June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

The second week marked the beginning of synthesis, shifting from simulation towards, circuits for synthesis, including a traffic light controller, ring counter, and 4:1 mux. This days were spent setting up the synthesis environment and learning to apply constraints such as clock definitions, input/output delays, and technology library paths, carefully checked functional correctness before proceeding with synthesis. This phase helped me realize how design constraints and coding styles influence the overall implementation, preparing me for deeper exploration of performance and optimization in digital systems.

Signature of Student :

Date: 11 June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

These two days were dedicated to synthesizing sequential designs like the JK flip flop, binary to gray converter, and both 4-bit up and down counters. After simulation, each circuit was synthesized into a gate-level netlist. I analyzed synthesis reports to study area, timing and power for each design. Comparing results, gave me insight into how sequential circuits are more resource-intensive and timing sensitive compared to simple modules. I also noticed how clean coding improved synthesis outcomes, including warnings and improving efficiency. The experience emphasized on the importance of writing optimized RTL, as even a small change had noticeable impact on performance and results.

Signature of Student :

Date: 21 June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

The last day of the week focused on arithmetic circuits, including a 4-bit Comparator, full adder and 4-bit adder. Each design was synthesized after verification, and I carefully studied the generated reports. I observed that arithmetic modules, though small in scale, significantly affected timing and area utilization. Analyzing these results taught me about the balance between functionality and resource cost in hardware implementation. By the end of this day, I had successfully synthesized all four chosen designs, completing the week's target. This gave me a solid understanding of how simulation results translate into hardware-level implementations through synthesis.

Signature of Student :

Week - 3

Date: 24/June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

This week began with floor planning, which is the foundation of physical design. My first target was the full adder, drawn as the Combinational circuit without clock. I defined the die and cell area, allocated space for standard cells, and placed Input Output pins logically. The main focus was to create a layout that minimised congestion and ensured routing feasibility. Floor planning was then added by defining the power rings and straps, ensuring uniform power distribution. Though simple, this exercise helped me understand the link between logical synthesis and physical layout. It introduced me to practical chip implementation challenges.

Signature of Student :

Date: 26/June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

In next two days were devoted to the sequential design - the traffic light controller. Unlike the full adder, this design included flip-flops and required a clock definition. I worked on place planning the design carefully, leaving space for clock tree structures, and signal integrity. Power planning was more demanding here, as design needed a reliable power grid, to support state transitions, achieving how sequential circuit demanded greater attention to clock and power distribution gave me deeper insight into the physical design flow. This task highlighted why timing closure and power planning are essential in general VLSI projects.

Signature of Student :

Date: 28/Jan.

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

On the final day of the week, I worked on the fsm design, a sequence detector. This task was more complex, involving multiple states and control logic, along with floorplanning, focusing on efficient placement of logic clusters to reduce wire length. Next, I planned the power network, ensuring even distribution to avoid IR drops. The fsm design tested my ability to manage both control logic and sequential elements. This exercise gave me a strong sense of how abstract Verilog code translates into physical design. Week 3 concluded with valuable exposures to floor planning and power planning.

Signature of Student :

**JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY**  
 (Declared Deemed to be University u/s 3 of the UGC Act, 1956)  
**A-10, Sector-62, Noida, U.P.**

Date : 30/June/2024

**Feedback Form for Initial Assessment related to students' performance in 1st Month of Summer Internship**

**ATTRIBUTES:**

		<b>On a scale of 1 to 5 (5 is the highest and 1 is the lowest)</b>
1	<b>General:</b>	
	Etiquette (Appearance, Body Language, Attitude, etc)	5
	Willingness to learn	5
	Verbal / Written Communication	5
2	<b>Knowledge / Skills :</b>	
	Fundamentals	5
	Domain / Subjective	5
	Overall	5

Co. Officer's Name:

(Supervisor/Manager)

Mobile No.: 98176 8476

Email ID: Shanti.Kalra@jpit.ac.in

Signature

Week - 4

Date: 21 June

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

This week began with placement of standard cells for three designs, starting with the full adder, placement was straight forward since it was a small combinational design without clocks, for the traffic light controller and sequence detector, cell placement require more careful consideration to minimize congestion and wirelength. After placement, I performed clock tree synthesis for the sequential and fsm, knowing proper distribution of clock signals, understanding the importance of placement quality and clock synthesis was an eye opener, as both directly affect timing, power and overall chip performance in physical design.

Signature of Student :

Date: 1 July

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

The next phase involved routing the three designs, I routed all signal nets and clock connections, ensuring minimum delay, and crosstalk. Special attention was given to the sequence detector since fsm, typically involve dense control logic. Once routing was complete, I performed RC extraction to capture parasitic effects of wires and interconnects. This analysis gave me accurate estimates of delay and pause, beyond the values from synthesis. Comparing extracted results with pre-routing timing reports highlighted the impact of parasitics in real layout. These two days made me appreciate how routing and RC extraction define the practical feasibility of a design.

Signature of Student :

Date: 31 July

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

The final day of the week concluded with GDSII generation, the last step before fabrication. I verified design rules and checked for layout vs schematic (Lvs) consistency to ensure correctness. Generating the final GDSII, file for the full adder, traffic light controller, and sequence detector gave me immense satisfaction, as it represented a complete transition from Verilog RTL to fabrication ready layout. This step showed how every stage - simulation, synthesis, floor planning, placement, CIS, routing and extraction contributes to building the actual chip. Ending weekly, I had a holistic view of the physical design flaws and its practical significance in ULSI.

Signature of Student :

# Week 5

Date: 6 July

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

This week focused on Mealy-type Fsm that generate the sequencing of a vending machine. I began by thoroughly reviewing the RTI to problems state encoding, inputs/outputs, and expected behaviors. After functional re-simulation to ensure correctness, I synthesized the fsm to a gate-level netlist using an industry-standard synthesis tool while applying time constraints per the target clock. I defined primary (clock, input) output, delays, and slack paths as appropriate. The synthesis reports gave initial area and timing estimates. Then steps converted the abstract fsm into a physical representation ready for timing verification and generated early optimization opportunities.

Signature of Student :

Date: 8 July..

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

I performed static timing analysis (STA) on the synthesized netlist using pulsetime to validate timing at the specified clock (target frequency applied as timing constraint). I generated full timing reports, slack histograms, and found the worst fan paths. I identified multiple critical paths that showed combinational logic between State elements and through complex next-state logic. I analyzed these paths to determine constraints - long logic depth, large fanout, or heavy switching loads. Based on the reports, I experimented with synthesis directives, de-synthesis, buffer/inverter insertion, logic retiming, and drive-strength adjustments to reduce delay on critical nets.

Signature of Student :

Date: 10 July

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

The final day was dedicated to setup / hold analysis and remediation, I inspected setup violations (negative slack on launch → capture paths) and hold gisks (too-small path delays past -gate). For setup issues I applied retiming, pipeline simplification and localized logic simplification, for hold violations I added small delay buffers or adjusted clock insertion timing. I also checked margin across PUF corners and ensured constraints reflected realistic wire parasitics. After iterative fixes, STA showed most critical paths meeting with acceptable clock and no functional hold failures. The exercise taught me how STA-driven optimizations bridge RTL intent and reliable silicon behaviour.

Signature of Student :

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

I started the week 6 by converting the problem statement into clear Specifications and architecture. Requirements (4-8 digit pincode, master setup mode, doors code, 3-strike lockout, 8 minute timeout : Salmaid Central, door & sensor) were finalized, I designed a mealy fsm Central, Separated from the datapath, that handles (all storage, Comparison, Counter, timers and non-volatile memory modelling). I prepared state diagrams for idle, input, compare, grant, deny, lockout, doors, setup and test states. I defined interfaces (key pad, master, door, sensor, salmaid LFPs) and timing constraints. I also listed test scenarios and planned testbench structure for exhaustive verification.

Signature of Student :

Date: 15 July

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

These days were devoted to RTL implementation and functional verification. I wrote fully synthesizable Verilog modules, a mealy Control fsm, a datapath for digit buffering, And comparison, A secure passcode memory block, Counters for failed attempts and lockout timer, and salinity LFP devices. I ensured no combinational loops and kept control and datapath separate. I created directed and randomised test benches to validate correct unlock, device behaviour, lockout enforcement, Setup and changes and door sensor interactions, various confirmed correct state transitions, timing for the 10s unlock and 5-minute lockout, and safe handling of edge cases like short during critical areas power bounces,

Signature of Student :

Date: 17 July

Student Report - (Report on the work carried out in at least 100 words. Every two days using one page for two days)

on the final day, I prepared the design for synthesis and Integration testing. I ran lint checks, ensured coding styles suitable for ASIC flow, and annotated timing constraint (clock, I/O delays, multi-cycle paths for keypad debounce). I synthesised the tap module to get area/timing estimates and iterated on RTL to remove critical-path sources. Integration tests covered repeated heartbeat cycles, dureus activation, setup-mode guard logic, and base sensor safety. I documented module intervals, state encoding, and test procedures for future physical design steps. Ending week, the safe lock system was functionally complete, verified, and ready for the full physical-design signoff pipeline.

Signature of Student :

# JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY

(Declared Deemed to be University u/s 3 of the UGC Act, 1956)

A-10, Sector-62, Noida, U.P.

Date : 28 | July | 2023

## Feedback Form for Final Assessment related to students' performance in 2nd Month of Summer Internship

### ATTRIBUTES:

1 General:		On a scale of 1 to 5 (5 is the highest and 1 is the lowest)
	Level of confidence/maturity	5
	Involvement in a Team	5
2 Knowledge / Skills :		
	Core competency	5
	Open to new ideas	5
	Usage of related technology	5
	Overall	5

Co. Officer's Name:

Signature

(Supervisor/Manager)

Mobile No.: 9811768476

Email ID: Sheanti.Kalra@jiit.ac.in