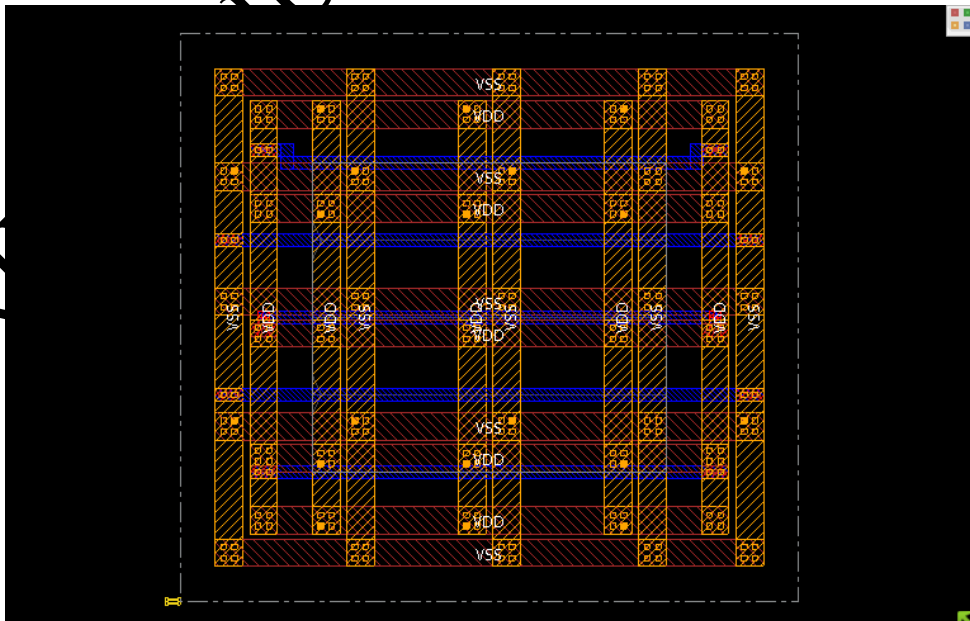
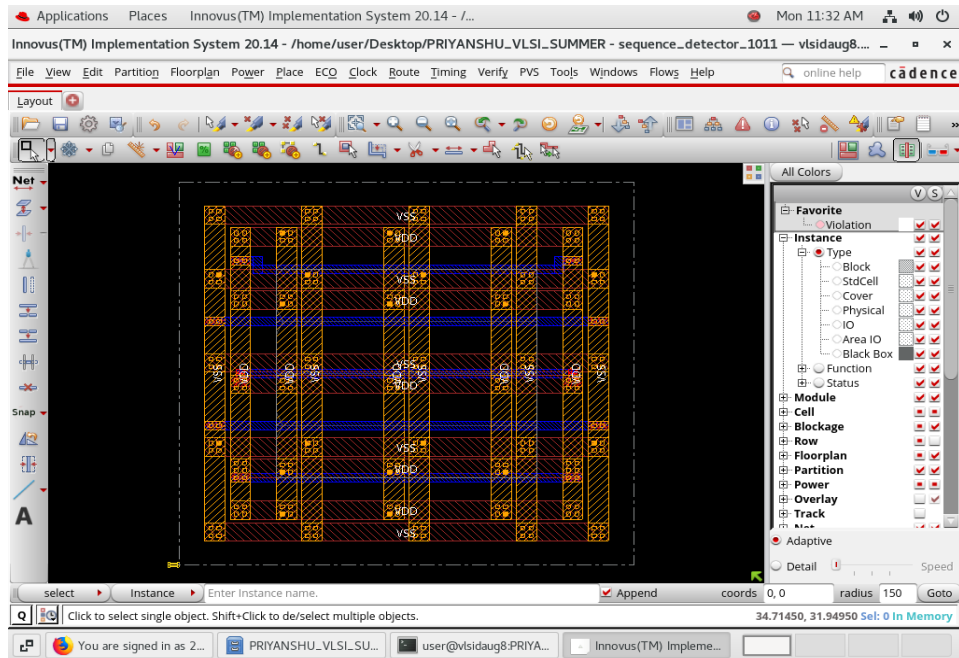


VLSI DESIGN AND AUTOMATION SUMMER INTERNSHIP

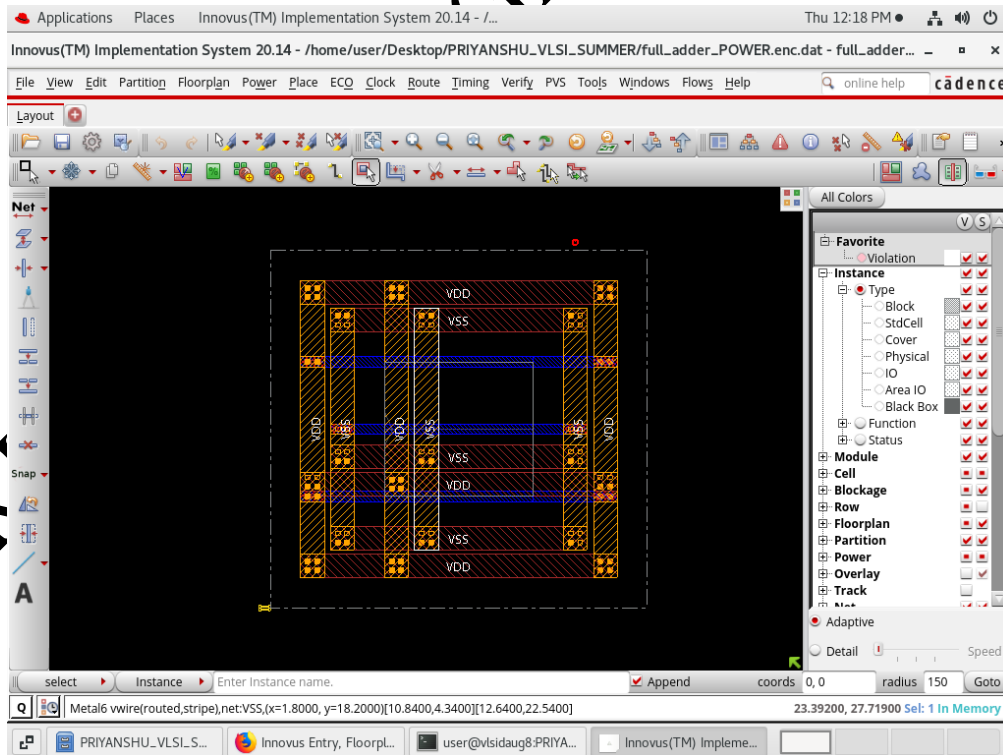
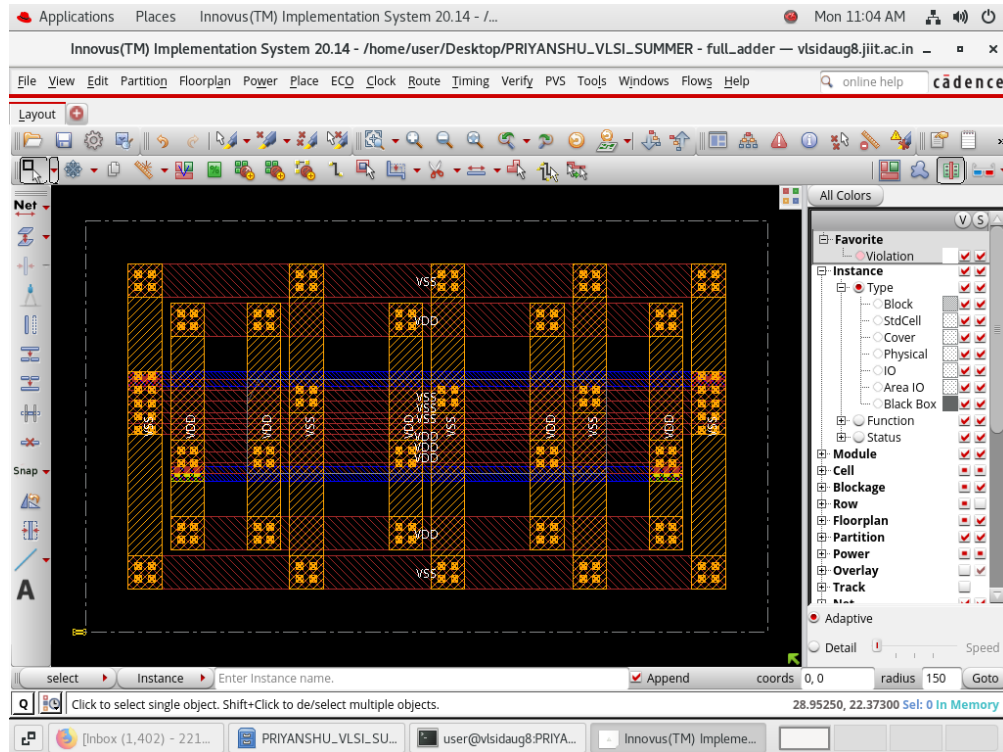
WEEK 3 SUBMISSION

RESOURCE : [WEEK 3](#) (ENC and NETLIST files are here)

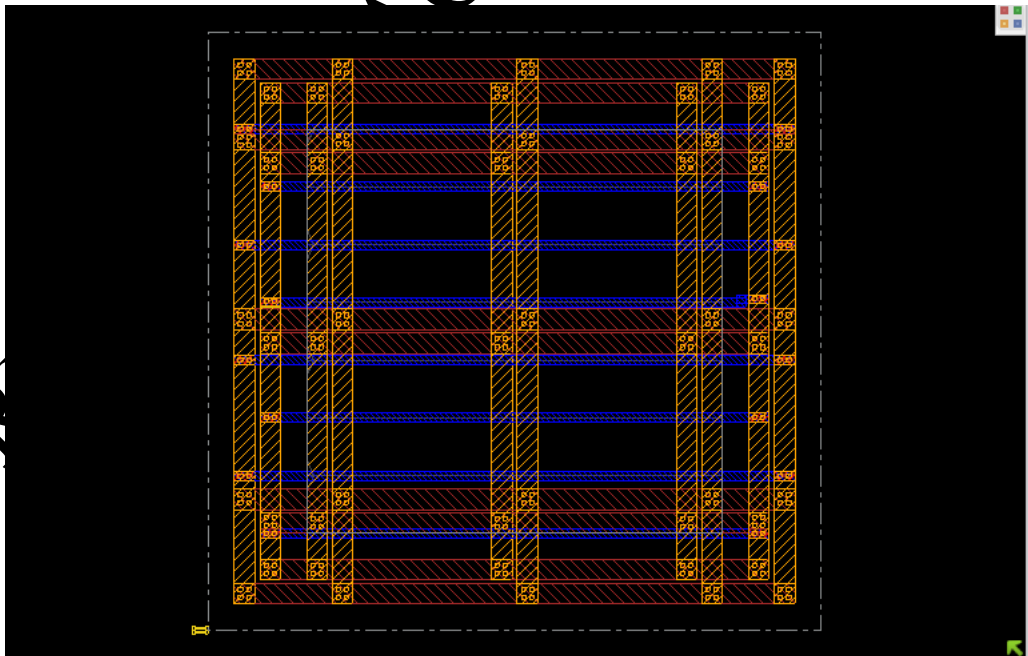
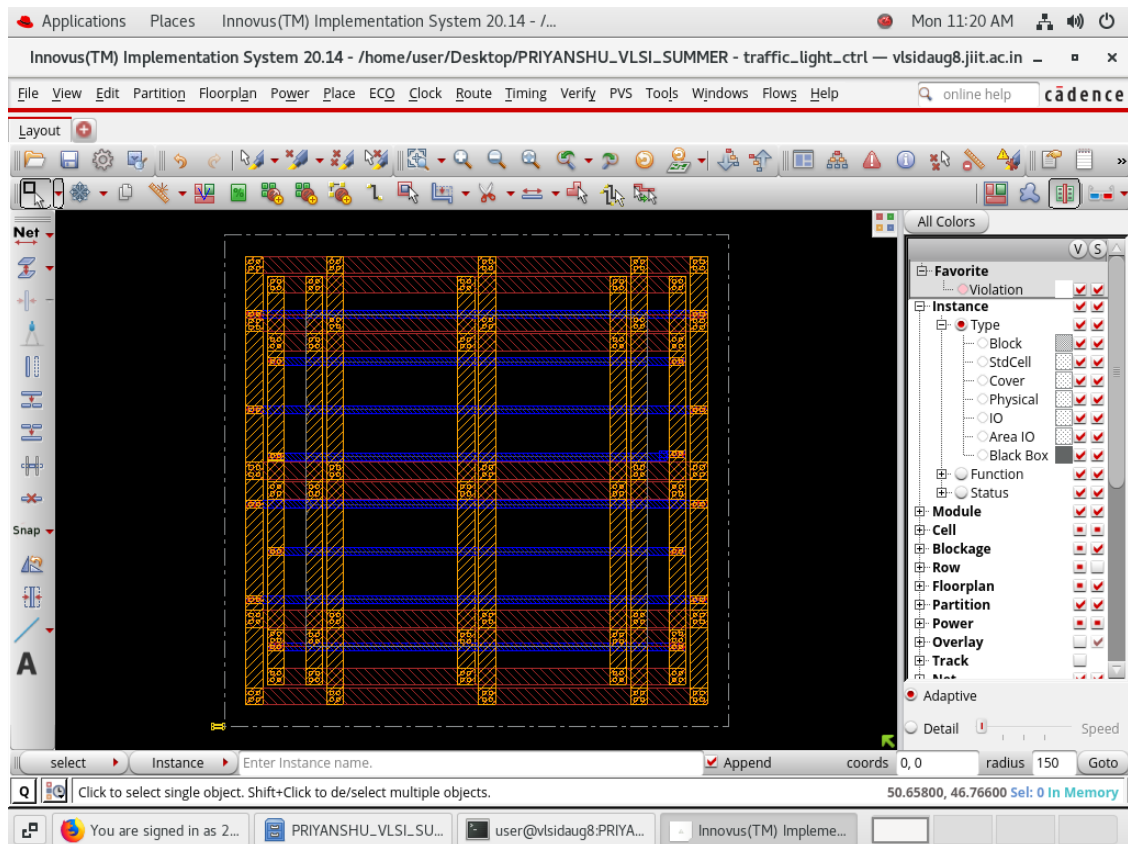
FSM (Finite State Machine) – Sequence Detector 1011



Combination Circuit – Full Adder



Sequential Circuit – Traffic Light Control



PRIYANSHU AGGARWAL 22102236