

# VLSI DESIGN AND AUTOMATION SUMMER INTERNSHIP

## WEEK 5 SUBMISSION

RESOURCE HERE : [WEEK 5](#) ( ENC and NETLIST files are here )

### BEFORE FILE TEXT :

```
tempus 5> report_timing -late
```

```
#####
```

```
#####
```

```
# Generated by: Cadence Tempus 20.20-p001_1
```

```
# OS: Linux x86_64(Host ID: wlsdaug9.jiit.ac.in)
```

```
# Generated on: Mon Jul 14 13:51:23 2025
```

```
# Design: leading_machine
```

```
# Command: report_timing -late
```

```
#####
```

```
#####
```

```
Path 1: MET Setup Check with Pin out_reg/CK
```

```
Endpoint: out_reg/SE (v) checked with leading edge of 'clk'
```

```
Beginpoint: in[0] (v) triggered by leading edge of 'clk'
```

```
Path Groups: {clk}
```

```
Analysis View: WORST
```

```
Other End Arrival Time 0.000
```

```
- Setup 0.230
```

```
+ Phase Shift 10.000
```

```
- Uncertainty 0.200
```

= Required Time 9.570  
 - Arrival Time 0.448  
 = Slack Time 9.123  
 Clock Rise Edge 0.000  
 + Input Delay 0.300  
 = Beginpoint Arrival Time 0.300

+-----+						
Instance	Arc	Cell	Delay	Arrival	Required	
			Time	Time		
+-----+						
	in[0] v		0.300	9.423		
g411	A v -> Y ^	INVX1	0.023	0.324	9.446	
g409	A0 ^ -> Y v	Q4121XL	0.124	0.448	9.570	
out_reg	SE v	SDFFTRX1	0.000	0.448	9.570	
+-----+						

tempus 4> tempus 4> report\_timing -early

#####

#####

# Generated by: Cadence Tempus 20.20-p001\_1

# OS: Linux x86\_64(Host ID vlsidaug9.jiit.ac.in)

# Generated on: Mon Jul 14 13:49:51 2025

# Design: vending\_machine

# Command: report\_timing -early

#####  
#####

Path 1: VIOLATED Hold Check with Pin present\_state\_reg/CK

Endpoint: present\_state\_reg/D (v) checked with leading edge of 'clk'

Beginpoint: next\_state\_reg/Q (v) triggered by leading edge of 'clk'

Path Groups: {clk}

Analysis View: BEST

Other End Arrival Time 0.000

+ Hold 0.031

+ Phase Shift 0.000

+ Uncertainty 0.200

= Required Time 0.231

Arrival Time 0.116

Slack Time -0.116

Clock Rise Edge 0.000

+ Clock Network Latency (Ideal) 0.000

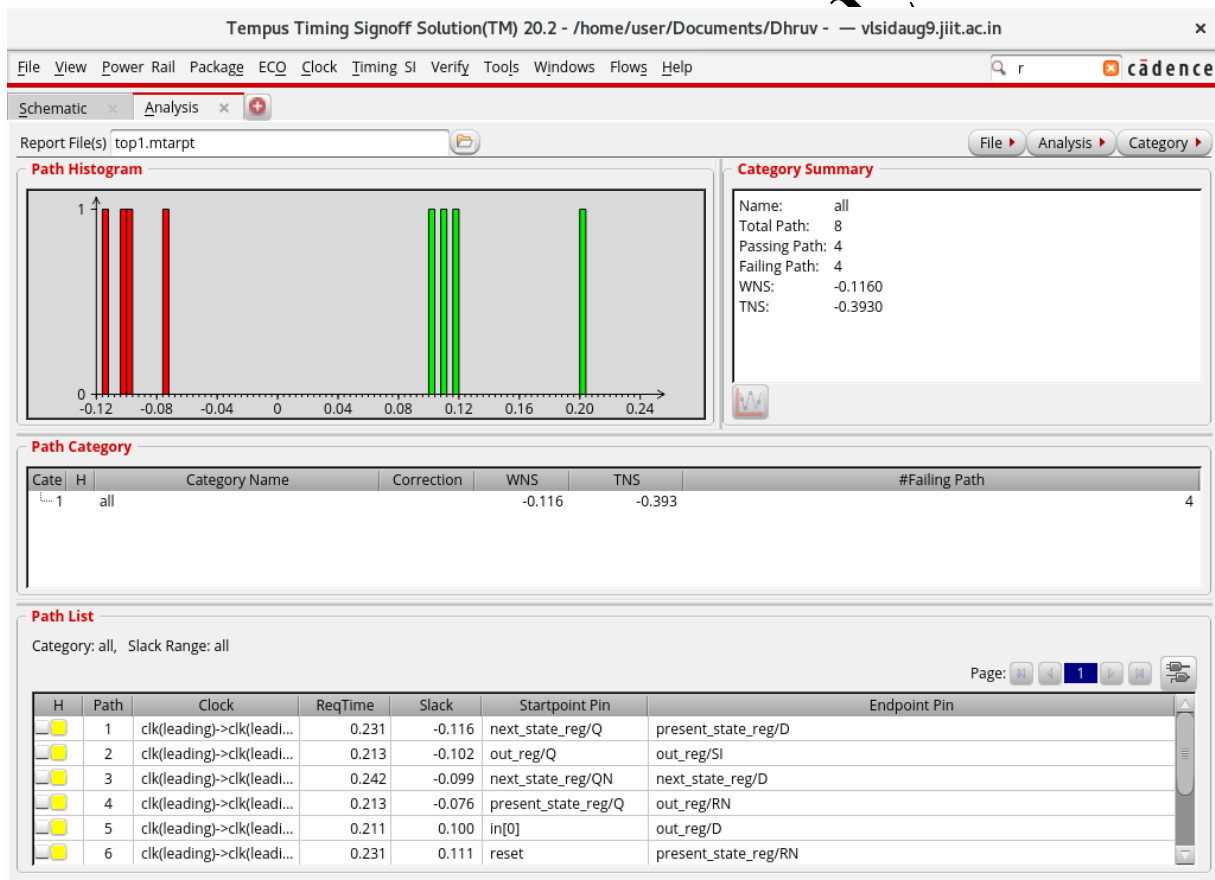
= Beginpoint Arrival Time 0.000

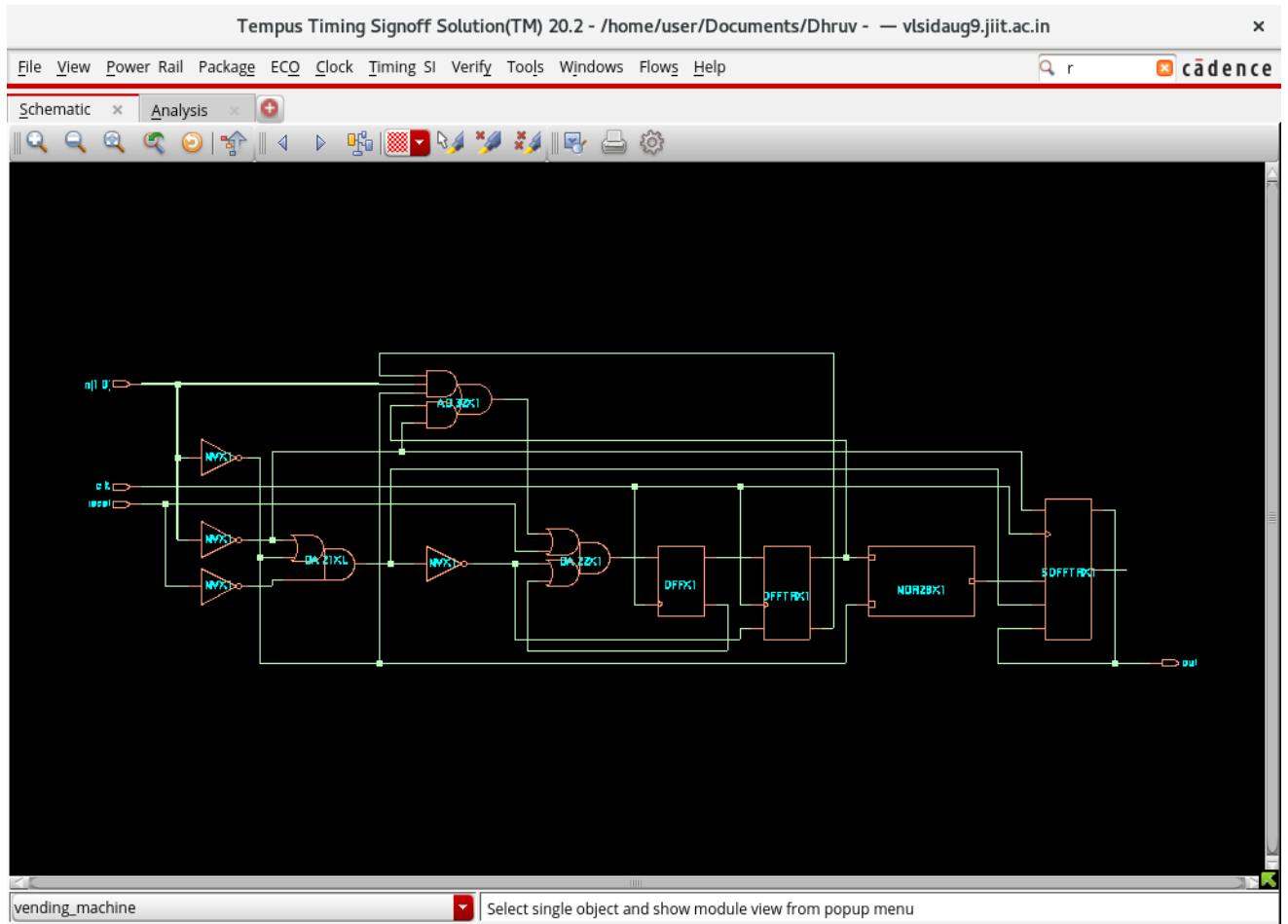
+-----+

Instance	Arc	Cell	Delay	Arrival	Required
			Time	Time	

+-----+-----+-----+-----+-----+-----+					
next_state_reg	CK ^			0.000	0.116
next_state_reg	CK ^ -> Q v	DFFX1	0.116	0.116	0.231
present_state_reg	D v	DFFTRX1	0.000	0.116	0.231
+-----+-----+-----+-----+-----+-----+					

## SCREENSHOTS :





PRIYANSHU AG