# Simulation Outputs in Ternary Logic Simulator

## I. Outputs of 14 to 3 Balanced Ternary Priority Encoder Simulated in Ternary Logic Simulator

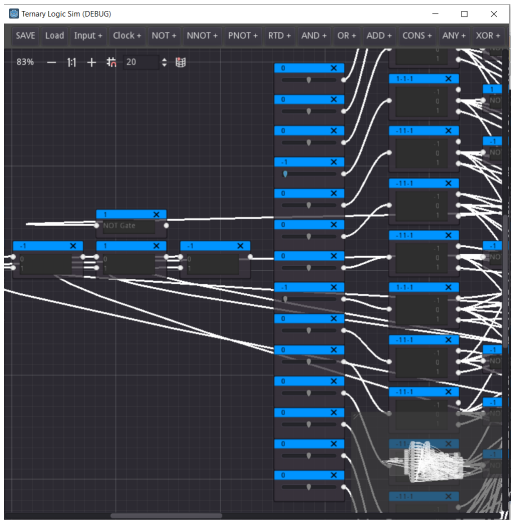


Fig. 1. Output when I7=-1 and I3=-1

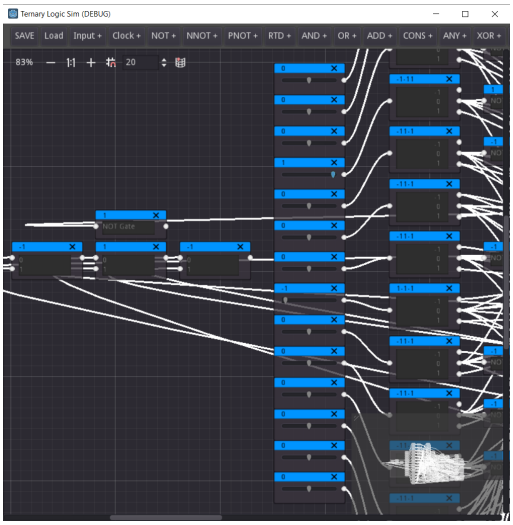


Fig. 3. Output when I7=-1 and I3=1

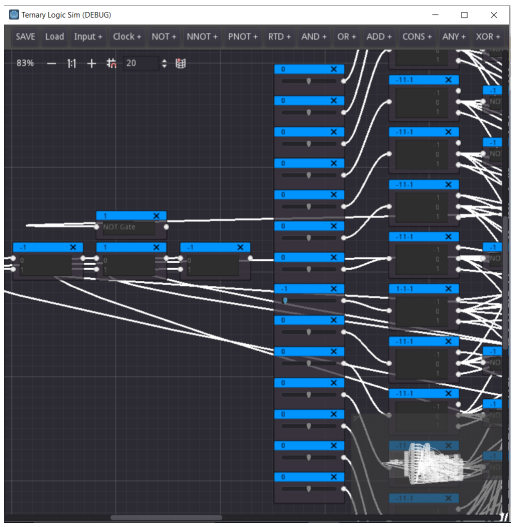


Fig. 2. Output when I7=-1 and I3=0

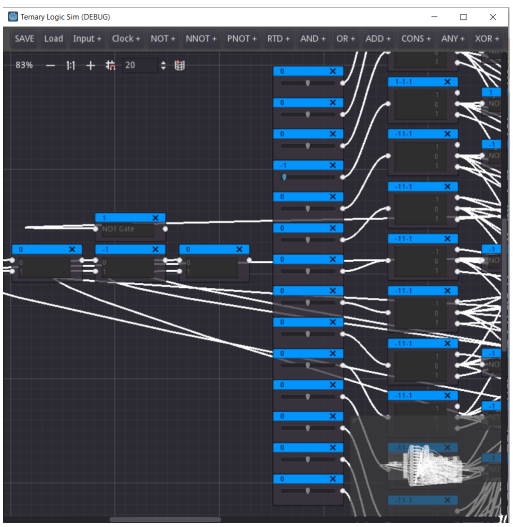


Fig. 4. Output when I7=0 and I3=-1

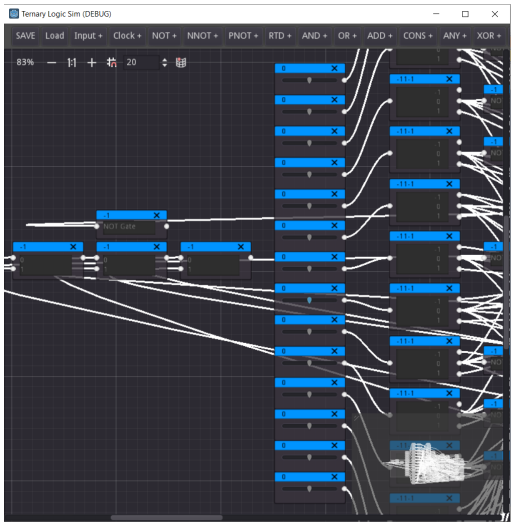


Fig. 5. Output when I7=0 and I3=0

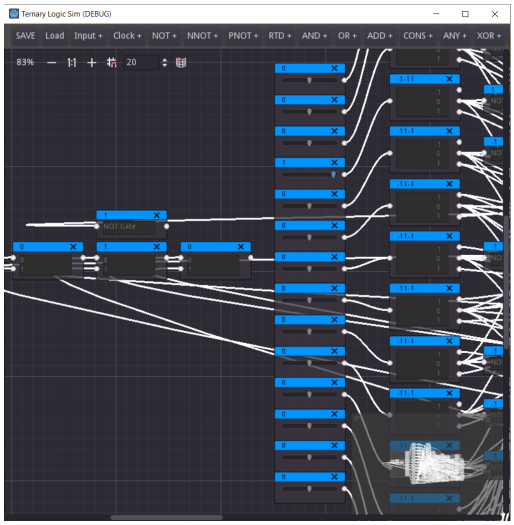


Fig. 6. Output when I7=0 and I3=1

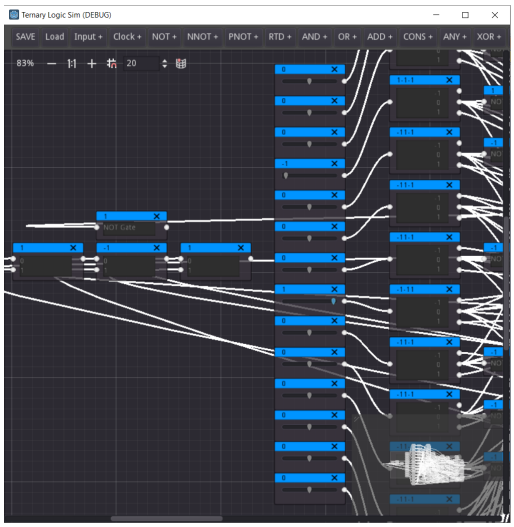


Fig. 7. Output when I7=1 and I3=-1

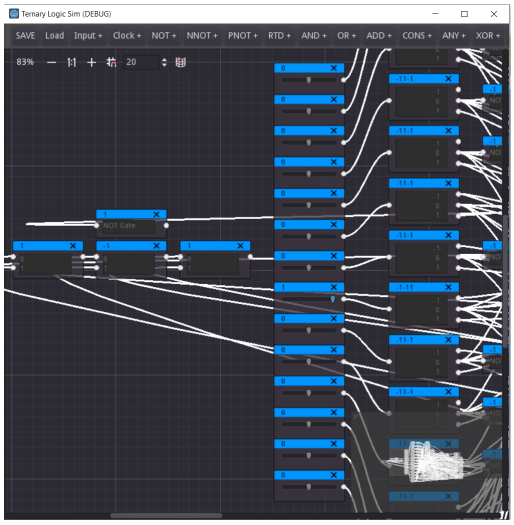


Fig. 8. Output when I7=1 and I3=0

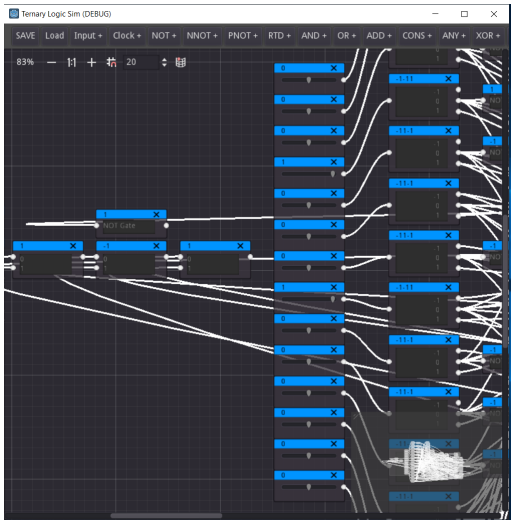


Fig. 9. Output when I7=1 and I3=1

## II. Outputs of Full Adder Simulated in Ternary Logic Simulator

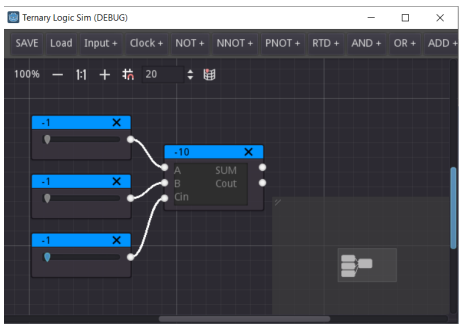


Fig. 10. Output of full Adder when -1, -1 and -1 are the inputs

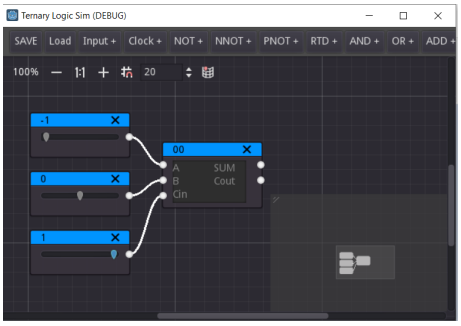


Fig. 11. Output of full Adder when -1, 0 and 1 are the inputs

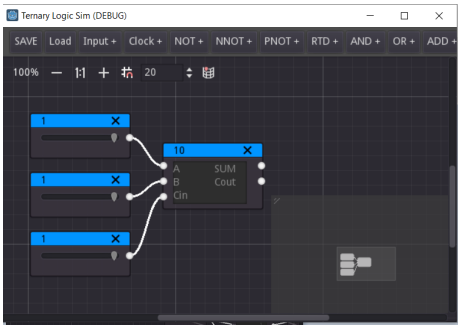


Fig. 12. Output of full Adder when 1, 1 and 1 are the inputs

## III. Outputs of Input Decoder Simulated in Ternary Logic Simulator

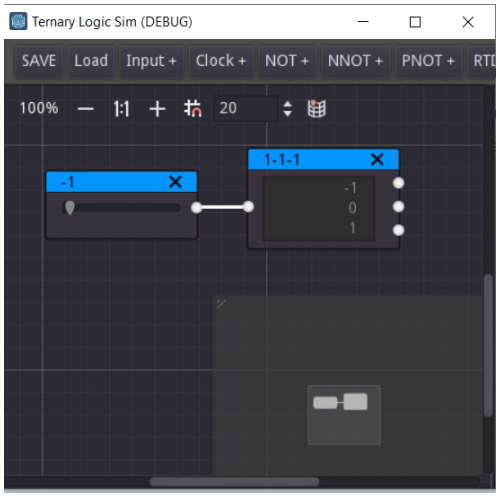


Fig. 13. Output of Input Decoder when -1 is the input

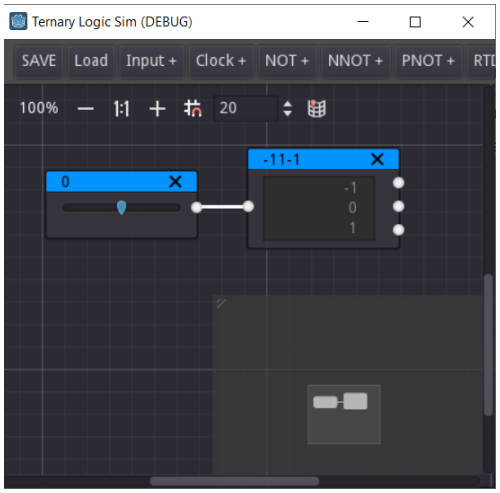


Fig. 14. Output of Input Decoder when 0 is the input

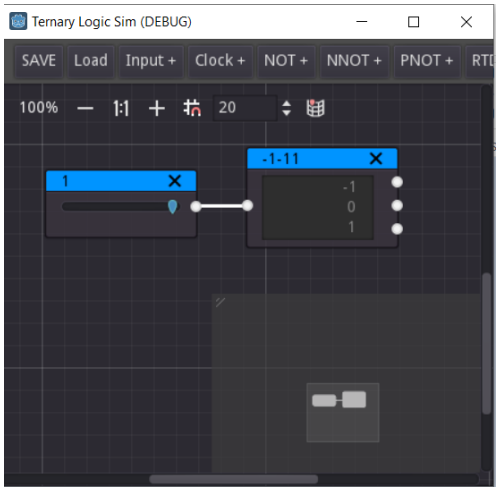


Fig. 15. Output of Input Decoder when 1 is the input