

# TD6336F

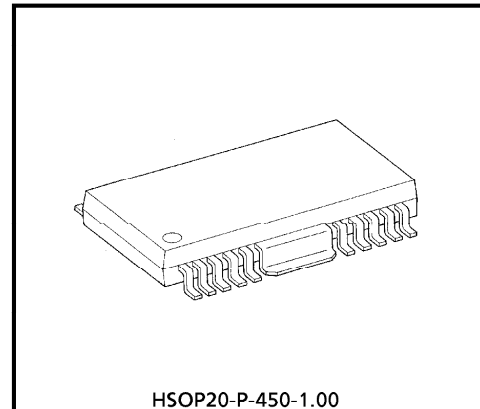
## 8-BIT SERIAL-IN PARALLEL-OUT DRIVER

The TD6336F is an automotive 8-bit SI/PO driver IC using a Bi-CMOS process characterized by high output withstand voltage.

The shift registers share a common clock and a common reset signal. Data is shifted on the leading edge of the clock. The IC also has  $\overline{\text{LATCH}}$  and ENABLE inputs. Its output is an N-channel open-drain output, and  $I_{\text{sink}}$  is up to 100mA. When the supply voltage becomes low, the output turns off.

### FEATURES

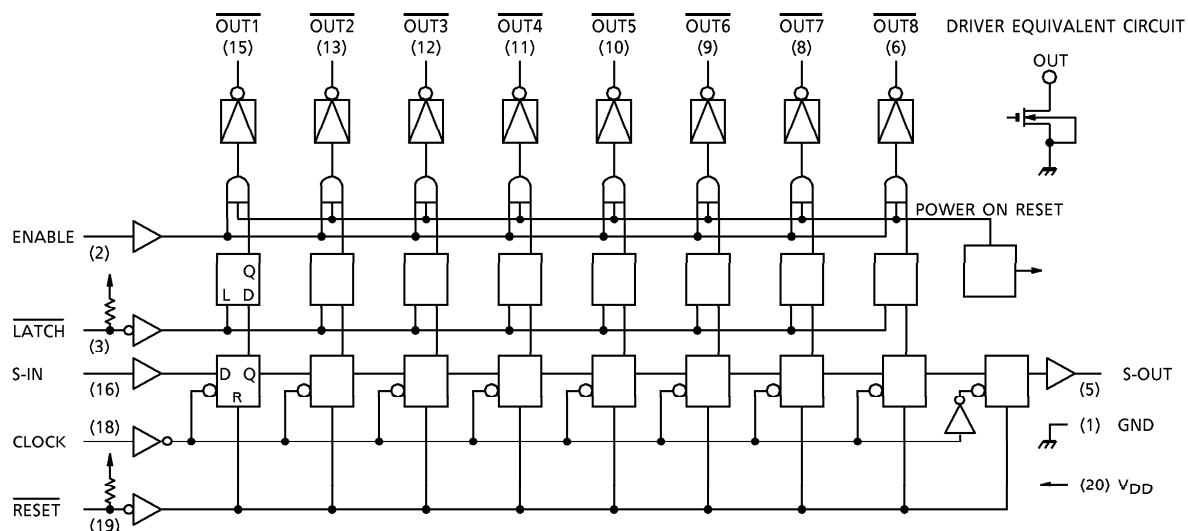
- Serial input and 8-stage parallel/serial output
- Serial output allows cascade expansion.
- ENABLE input for output control
- Large output current : 100mA (Max.)
- High output withstand voltage : 80V (Max.)
- Power detection circuit incorporated : The output is disabled when  $V_{\text{DD}} < 3\text{V}$  (Typ).



HSOP20-P-450-1.00

Weight : 0.79g (Typ.)

### BLOCK DIAGRAM AND PIN LAYOUT









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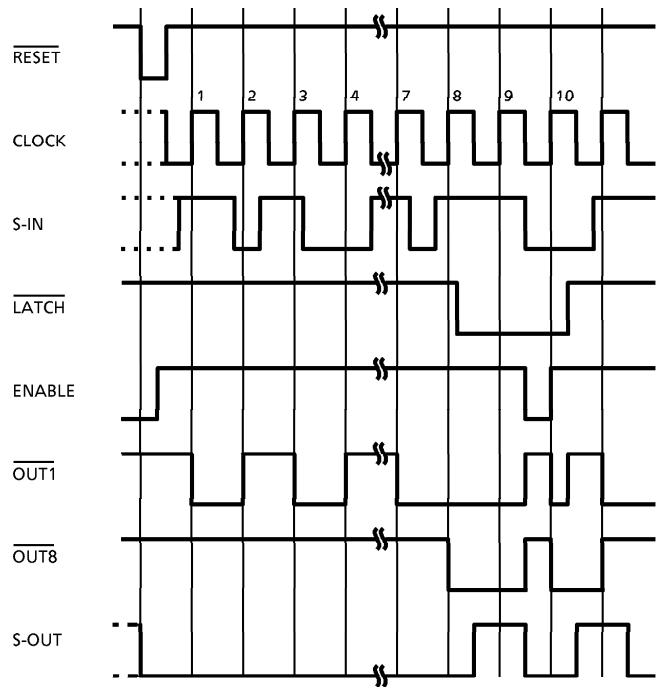
## PIN DESCRIPTION

PIN No.	SYMBOL	DESCRIPTION
1	GND	Grounded. Must be connected to the FIN pin.
2	ENABLE	Data is output when this signal is high ; all output buffers turn off when the signal goes low.
3	$\overline{\text{LATCH}}$	Data is held when this signal is low ; data is rewritten when the signal goes high. When the pin is open, the signal is high.
5	S-OUT	Serial output pin allowing easy bit addition. To prevent malfunction, this pin has a function for a half-bit delay output.
6 ~15	$\overline{\text{OUT8}}$ $\sim\overline{\text{OUT1}}$	Supplies shift register data or latch data. The signal is an N-channel MOS open-drain output.
16	S-IN	Serial data input pin.
18	CLOCK	Clock input pin for shift registers. The register acts at the leading edge of the clock.
19	$\overline{\text{RESET}}$	Clears data in the shift registers. The shift registers do not change when this signal is high ; they are reset when the signal goes low. When the pin is open, the signal is high.
20	V <sub>DD</sub>	Power supply pin.
4, 7, 14, 17	NC	Not connected.
FIN	GND	Ground pin serving also as a heat sink. This pin must be connected to pin 1.

## TRUTH TABLE

CK	E	$\overline{\text{R}}$	$\overline{\text{LATCH}}$	S-IN	OUT		S-OUT	CK = CLOCK E = ENABLE $\overline{\text{R}}$ = $\overline{\text{RESET}}$ S-IN = SERIAL IN OUT-PARALLEL OUT S-OUT = SERIAL OUT * = DON'T CARE NC = NO CHANGE L = LOW LEVEL H = HIGH LEVEL
					$\overline{\text{Q1}}$	$\overline{\text{Qn}}$		
	H	H	H	L	OFF	$\overline{\text{Qn-1}}$	Q7	
	H	H	H	H	ON	$\overline{\text{Qn-1}}$	Q7	
	H	H	L	*	NC	NC	Q7	
	L	H	*	*	NC	NC	Q7	
	*	*	*	*	NC	NC	Q7	
*	*	L	H	*	OFF	OFF	L	
*	H		L	*	NC	NC	L	

TIMING CHART



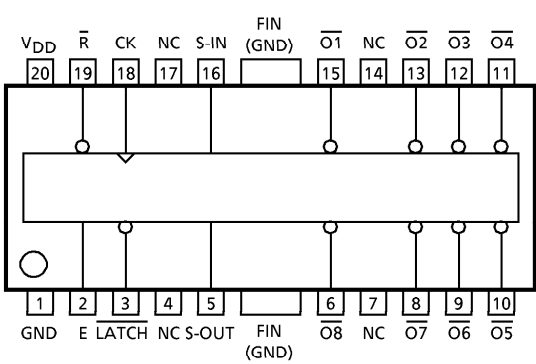
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	- 0.3~7	V
Input Voltage	V <sub>IN</sub>	- 0.3~V <sub>DD</sub> + 0.3	V
Output Voltage	V <sub>OUT1</sub> (Note 1)	- 0.3~V <sub>DD</sub> + 0.3	V
	V <sub>OUT2</sub> (Note 2)	- 0.3~80	
Output Current	I <sub>OUT</sub>	100	mA
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>stg</sub>	- 55~150	°C
Lead Temperature-time	T <sub>sol</sub>	260 (10s)	°C

(Note 1) S-OUT

(Note 2)  $\overline{\text{OUT1}} \sim \overline{\text{OUT8}}$

PIN CONFIGURATION



## RECOMMENDED OPERATING CONDITIONS (Ta = -40~105°C)

CHARACTERISTIC			SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage			V <sub>DD</sub>	—	—	4	5.0	6	V
Input Voltage			V <sub>IN</sub>	—	—	0	—	V <sub>DD</sub>	V
Output Current	High	S-OUT	I <sub>OH</sub>	—	—	0	—	− 1.0	mA
Output Voltage	High	$\overline{Qn}$	V <sub>OH</sub>	—	—	0	—	60	V
Output Current	Low	S-OUT	I <sub>OL</sub>	—	—	0	—	1.0	mA
		$\overline{Qn}$	I <sub>OL</sub>	—	—	0	—	70	mA
Clock Frequency			f clock	—	—	0	—	1.0	MHz
Clock Pulse Width			t <sub>w</sub> clock	—	—	500	—	—	ns
Data Setup Time			t <sub>setup</sub>	—	—	500	—	—	ns
Data Hold Time			t <sub>hold</sub>	—	—	500	—	—	ns
Maximum Clock Time	Rise Time	t <sub>r</sub>	—	—	—	—	—	70	μs
	Fall Time	t <sub>f</sub>			—	—	—	70	μs

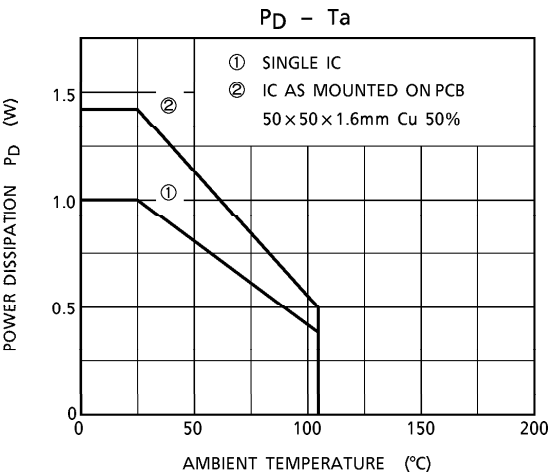
ELECTRICAL CHARACTERISTICS (Ta = -40~105°C, V<sub>DD</sub> = 4~6V)

CHARACTERISTIC			SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage		High	V <sub>IH</sub>	—	—	0.8 × V <sub>DD</sub>	—	—	V
		Low	V <sub>IL</sub>	—	—	—	—	0.2 × V <sub>DD</sub>	
Input Current	$\overline{R}$ , $\overline{LATCH}$		I <sub>IN</sub>	—	V <sub>IN</sub> = 0~V <sub>DD</sub>	—	—	± 100	μA
	CK, S-IN, E		I <sub>IN</sub>	—	V <sub>IN</sub> = 0~V <sub>DD</sub>	—	—	± 1	
Output Voltage	High	S-OUT	V <sub>OH</sub>	—	I <sub>OH</sub> = - 1mA	V <sub>DD</sub> - 0.4	—	—	V
Output Current	High	$\overline{Qn}$	I <sub>OH</sub>	—	V <sub>OH</sub> = 80V	—	—	100	μA
Output Voltage	Low	S-OUT	V <sub>OL</sub>	—	I <sub>OL</sub> = 1mA	—	—	0.4	V
		$\overline{Qn}$	V <sub>OL</sub>	—	Ta = 25°C, I <sub>OL</sub> = 100mA	—	—	1.2	V
Static Current Consumption			I <sub>DD</sub> (1)	—	V <sub>DD</sub> = 5V, f = 0Hz	—	—	1	mA
Dynamic Current Consumption			I <sub>DD</sub> (2)	—	V <sub>DD</sub> = 5V, f = 1MHz	—	—	5	mA

SWITCHING CHARACTERISTICS (Ta = - 40~105°C, VDD = 4~6V)

CHARACTERISTIC			SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Delay Time	High	CK-S-OUT	t <sub>pLH</sub>	—	R <sub>L</sub> S-OUT = 2kΩ R <sub>L</sub> $\overline{Qn}$ = 150Ω C <sub>L</sub> = 15pF V <sub>IH</sub> = 3.0V, V <sub>IL</sub> = 0V Duty = 50%	—	0.1	0.5	μs
		CK- $\overline{Qn}$	t <sub>pLH</sub>			—	0.5	2.5	
	Low	CK-S-OUT	t <sub>pHL</sub>			—	0.1	0.5	
		CK- $\overline{Qn}$	t <sub>pHL</sub>			—	0.3	1.5	
Maximum Clock Frequency			f <sub>max</sub>			—	10	—	MHz
Maximum Data Setup Time			t <sub>setup</sub>			—	5	25	ns
Minimum Data Hold Time			t <sub>hold</sub>			—	5	25	ns
Maximum Clock Time	Rise Time	t <sub>r</sub>	—			70	—	μs	
	Fall Time	t <sub>f</sub>	—			70	—		

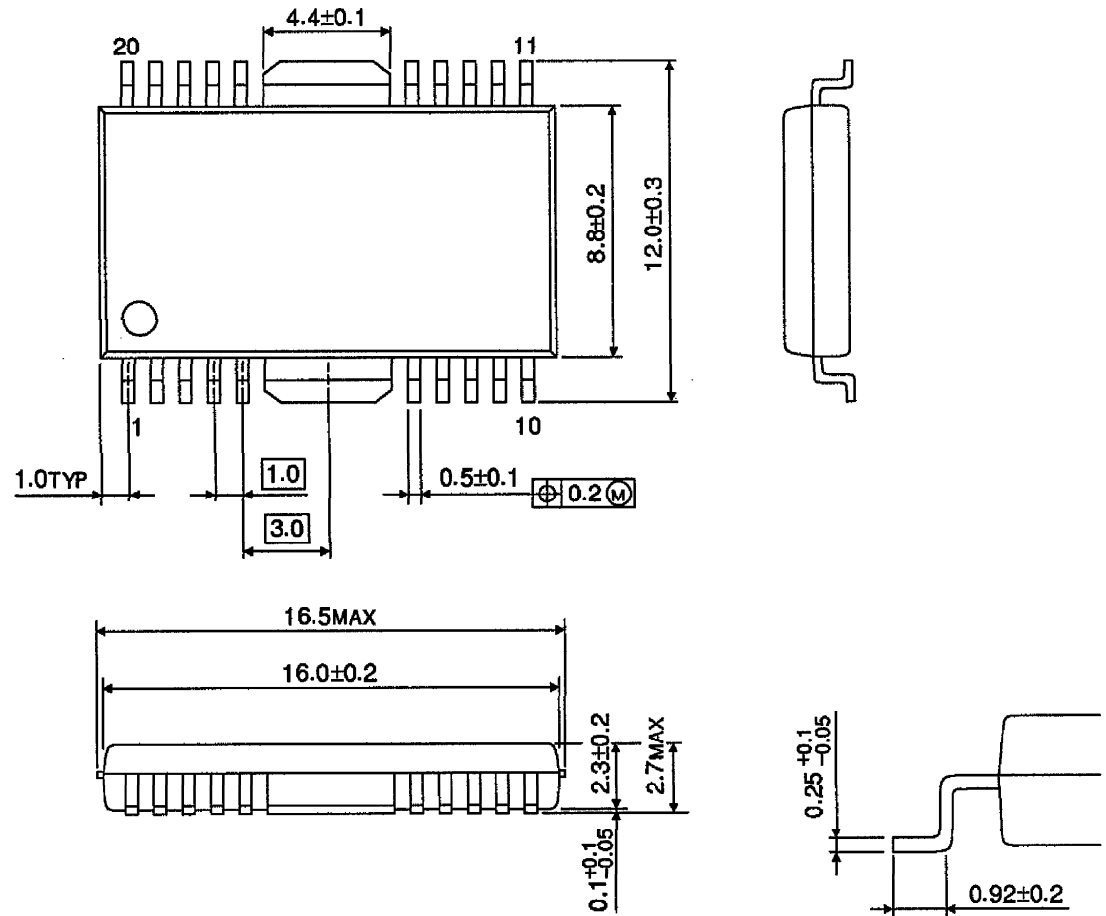
C<sub>L</sub> : Includes the capacitances of the measuring instrument and probe.



OUTLINE DRAWING

HSOP20-P-450-1.00

Unit : mm



Weight : 0.79g (Typ.)