MILESTONE 1 WORK:

Tuesday 8, 2024:

- Reviewed design and example programs [1 hr]
- Met with team and add instruction description [1 hr]

Tasks for milestone 2 has not decided yet.

I did not do much work for milestone 1 because other team members used Teams during the break and I did not received notification from Teams until I check Teams Group when I come back from break. I will ask for more work to do on the following milestones.

MILESTONE 2 WORK:

Thursday, January 11:

- Met with Ethan to understand the processer logic and his prototype in a simulator [1 hr]
- Explore and deploy jupyter notebook to run the assembler Ethan has built. [30 minutes]
- Agnay and I were to split the RTL insrtuction breakdown while Emma and Ethan were to work on jump + return and the RTL component list. [30 minutes]

Saturday, January 13:

- Agnay and I met and discussed homework 13 to understand RTL better and assigned the exact workload split for milestone 2. [3 hrs]

Sunday, January 14:

- Ethan commited the initial push for the quartus files and discussed the rough breakdown of how we would work through the verilog + unit testing on quartus on teams. [1 hr]
- Finished the second pass of the RTL instructions [2 hrs]

Monday, January 15:

- Met with team members to correct RTL instructions and finalize the document. [1 hrs]

MILESTONE 3 WORK:

Friday, January 19:

- Reviewed design document and started working on spliting single cycle RTL to 17 categories regaring with ALU implementation. [1 hr]

Saturday, January 20:

- Started working on multicycle RTL with Srivasa. [1.5 hrs]

Sunday, January 21:

- Finished multicycle RTL. [2 hrs]

Monday, January 22:

- Cleaned up multicycle RTL instruction table. Make them in a good format. [2 hrs]
- Met with team. Discussed how we are going to do test, and how to split work. [1 hr]
- Check and fix multicycle RTL instruction problems. [1.5 hrs]

MILESTONE 4 WORK:

Tuesday, January 23:

- Studyed on Verilog and started implement on module T_ALU_Complex logic, which is a decoder and a control unit. [1 hr]

Wednesday, January 24:

- Completed module T_ALU_Complex logic. [4 hrs]
- Completed skeleton of T_ALU_Complex test bench. [2 hrs]

Thurday, January 25:

- Met with team to discuss work assigment. [30 mins]

Sunday, January 28:

- Updated the new Signle Cycle RTL table and Multi Cycle RTL table since we greatly changed our design and instruction categories are affected. [1 hr]

work! why?

Monday, January 29:

- Started writting test bench skeleton for L_Control, which is the new decoder control unit. (We greatly changed our design) [2 hrs]

Tuesday, January 30:

- Met with Ethan to discuss about new design. [45 mins]
- Partially completed test bench skeleton for L_Control. [3.5 hrs]