Ethan Liu, Work Log

M1

December 29, 2023 - January 3, 2024 [20 Hours]

Draft and test instruction set
Draft hardware resources available to the hardware
Draft calling convention
Draft psuedo-instructions
Optimize procedure calling
Create proof-of-concept circuit for program testing
Create assembler
Write single input implementation of relprime

January 8, 2024
[1 hour]
Remodel instructions to have fixed length opcode and different func codes. Create instruction types.

January 9, 2024
[2 hours]
Create and test some example operations
[15 minutes]
Revise processor to have input and output lines 16 bits wide. Add instructions for read and write
[15 minutes]
Plan and create memory map

Why? Explain design reasons!

M2

January 11, 2024
[30 minutes] Update instruction format table for greater visibility
[1 hour] Update overall document structure for pulling information easier

Thank you!

January 12, 2024
[2 hours] Cleaned up assembled instructions for better visibility, fixed some examples with errors.
[1 hour] Review and update verilog code to a more usable format

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January 13, 2024
[3 hours] Update Veilog code into format usable for our design, create the logic component as proof-of-concept for writing verilog.

January 15, 2024
[2 hours] Clean up and fix RTL, plan & create components for the processor

What was wrong?