# EE 586 Final Project: Comparative Performance Evaluation of Dynamic and Static Flip-flops

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*Abstract*
***On the standpoint of delay and energy, designing the Flip-flops and Latches are very important parts [1] In this project. We compared 4 types of flip-flops, including implicit-pulsed, data-close-to-output, semi dynamic hybrid flip-flop (ip-DCO), hybrid latch flip-flop (HLFF), semi-dynamic edge-triggered flip-flop, and time borrowing master-slave flop-flop(tb-SMS). We implemented the circuit and evaluated them in terms of D-Q delay, energy, and energy delay product. We found tb-SMS has the fastest speed while HLFF is the most energy efficient flip-flop.***

*Keyword*
***Clocking, flip-flops, latches, edge-triggered, low power***

## 1. INTRODUCTION

When transmitting a digital data to the input node and calculating logic algorithms, it certainly required delay time to process the signal. In dynamic circuits, the output is not changed with the input every time. Whether to work the circuit is defined by the clock signal. In some devices, it required different clock signals that were pursued by other logic function circuits, such as using an inverter for CLK-not. Changing clock signal to control the time to process the circuit is important for defining setup time and hold time of the input data. If the processing time could be fit to the clock to Q delay, the energy would be decreased. Then, with proper controlling data signals and clock period, power, and time for transmitting the data could be also decreased. For example, HLFF could even have negative setup time of data and even could borrow time from the next stage [2]. Hence, to realize the devices with high energy efficiency, not only decreasing the processing time to output, but it is also necessary to set modified clock signals.

Flip-flop is the type of circuit and usually used in memory storage. In the flip-flop design, the state of the circuit, such as set and reset (SR) or data (D) and delay, would be changed through the logic level of the clock signal. However, the latency for switching the devices could not be ignored in the full device. For example, taking a device with 20 gate delays, the total delay cost of flip-flops could be up to 15% time in one cycle [3]. Although flip-flops would decrease the performance, they could also prevent processing unnecessary data inputs on the time not using the output signal from the device. Hence, in the modern system, combining with more than ten thousand flip-flops is very common, and the number of flip-flops is still increasing. Thus, a flip-flop with high energy efficiency would be important.

Latches is the device for transmitting the data in the specific clock signal. If the data arrive input node on other clock signal, the latch looks transparent, and the data would not be used. The main advantages of latches are having a soft clock edge for slack passing and minimizing the effects of clock skew on cycle time [2]. Flip-flops and latches are similar, and could both be used in memory storage, but they are different in the time to sample data. In latches, the range of time for transmitting is long and soft. If the clock skew, different arriving time to each device, happened, latches would still be able to work. Flip-flops are also thought as clocking or synchronous because they are designed for synchronizing the full system. Hence, data just could be sent to flip-flops on the time of the specific change of the clock signal.

To produce the devices with both high performance and power efficiency, it is important to pay attention to the latches and flip-flops. In this paper,

## 2. Related Work

J. Tschanz et al. [1] implemented ip-DCO and compared it with explicit-pulsed semi dynamic hybrid flip-flop(ep-DCO), explicit pulsed hybrid static flip-flop (ep-SFF), and time-borrowing static master-slave (tb-SMS) [1]. They set clock to Q delay of different devices to 60 ps. as the standard. Then, they compare energy (E), energy delay product (E*D), and energy per cycles. The result showed that compared with current designs, ip-DCO really have better energy efficiency in the same clock to Q delay.

H. Partovi et al. [2] introduced Hybrid Latch Flip-Flop (HLFF) that is designed for decreasing the latch latency and clock load. The authors went through the HLFF design and explained the function of each part of HLFF. The authors also showed the wave to illustrate the HLFF working status.

Klass et al. [3] introduce semi dynamic and dynamic flip-flops for high-speed application. The authors discussed the advantages of semi dynamic and dynamic flip-flops compare to single-phase flip-flops; they explained the prior flip-slops are faster.

Tam et al. [4] introduced a design of D-type flip-flop with simpler circuit structure and enhanced energy efficiency called double edge-triggered half-static clock-gated D-type flip-flop. In their design, the flip-flop is edge-triggered by $\mathrm{CLK} - \overline{\mathrm{CLK}}$ in order to remove the pulse generator.

Klass [5] introduced embedded logic semi-dynamic and dynamic flip-flops. Klass found those flip-flops have lower clock load and their latency is low. In the situation of incorporating logic functions, semi-dynamic and dynamic flip-flops have less extra delay, by reducing gate delay in the critical path, this aspect makes it suitable for high performance designs.

Padure et al. [6] introduced semi-dynamic flip-flops with embedded threshold logic functions. The authors successfully designed a Threshold Logic flip-flop (TLFF) with up to 16 data inputs. After simulation, the authors tested and adjusted their design. The authors found embedded AND function TLFF is faster than embedded OR function TLFF.

## 3. Methodology

In this project, we used Cadence to figure out and simulate the schematics of all the flip-flop's circuits. All schematics of circuits would be combined with instances in the 65 nm technology node. All the circuits are working under 2 GHz frequency.

To scale the total size for analyzing delay and energy, we decided the proportion of sizes between different parts in the circuit at first, such as the sizing of master latch and inverters of positive feedback.

Pulse width is critical for the pulse triggered Flip-Flops working with a lower energy. To size the circuit and make it work properly, we started by sizing the circuit to have equal rise and fall time as the 2:1 inverter. After a few adjustments, we found the pulse width is close to half of the clock cycle, which is not ideal for the circuit's energy optimization. In order to reduce the pulse width, we size down the pull up devices and size up the pull-down devices. With adjustments of the delayed clock path's inverters' sizing the size ratio of the first stage, we reduce the pulse width within 60p second and work properly.

In those fundamental sizes, the instance should not be skewed, and we reduce the glitch in the results as much as possible. The result graph needs to be accurate, such as small glitches and rectangular waves. We multiply the sizing of every transistor by the variable "x" to set up different sizes for the circuit. We collect data by adjusting "x" to analyze the relationship between the total sizes, energy consumption, and D to Q delay.

To evaluate the relationship between those data, we started by the smallest transistors' size we can get the circuit working. Then we size up the circuit by increasing the "x". After each time we modify the "x" we collect the D-Q delay and the energy of the circuit running for 2n Seconds. We increase "x" until we find the D-Q delay no longer reduces with the x increasing. We repeat this process on all four circuits and collect data we need.

## 4. Flip-Flop Circuit

In this part we discussed the operation of each circuit and explain our sizing method for each circuit.

### 4.1 Implicit-pulsed, data-close-to-output, semi dynamic hybrid flip-flop (ip-DCO)

The IP-DCO circuit has two stages and positive feedback circuits in the output of both stages. First stage is the dynamic inverter gate driven by a clock signal, and the second stage is the CMOS inverter gate with one Clock controlling signal in NMOS. The main features of ip-DCO are high energy-consumption and time-borrowing capability (more negative setup time) [1]. The main reason is that the transistor driven by data is close to the output signal, and it increases the sampling speed. To make the output of stage 1 into a pulse signal. We set the input of data before the clock signal changed to zero, the end of evaluation phase in evaluation phase. To pull down and pull up output nodes in a short time, we increase the sizes of pull-down transistors in the first stage. Size up NMOS transistors make them significantly larger than other transistors, letting the first stage have high gate capacitance. To maintain the pulse, we set the lower size to the two inverters in positive feedback. Then, the positive feedback would have more delay and less power to charge the output of the first stage. Finally, we modified the sizes in the second stage for the rectangular wave form at QB node.

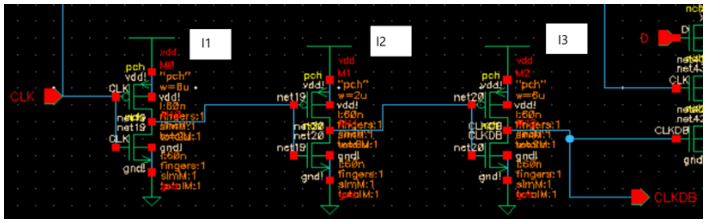


**Fig. 1. Ip-DCO Delay circuit**

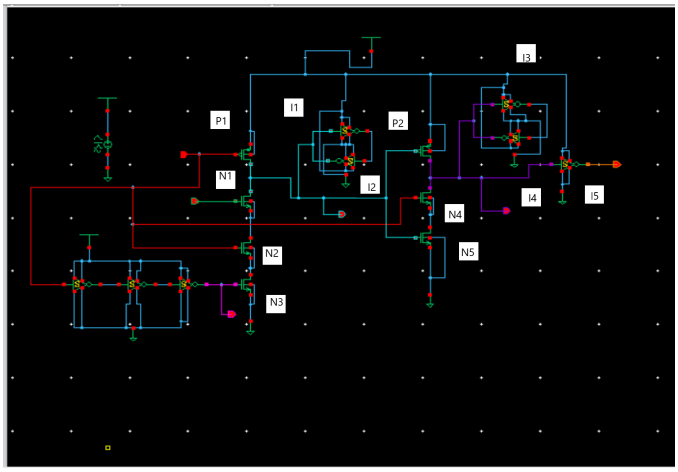


**Fig. 2. Ip-DCO circuit**

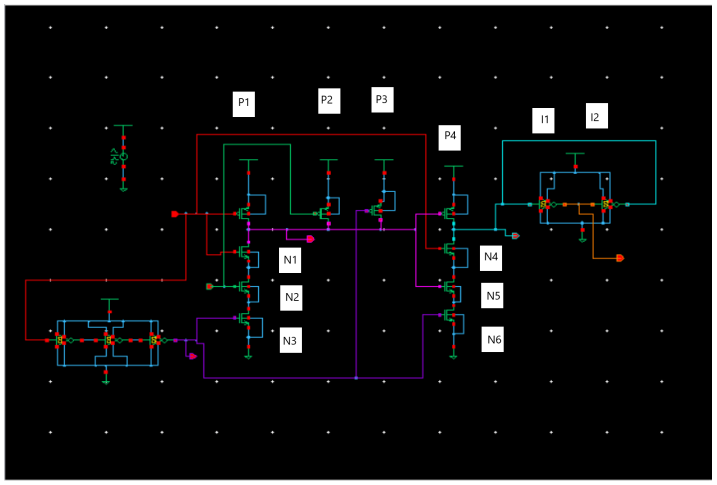


**Fig. 4 HLFF circuit**

### 4.2 Hybrid Flip-Flop Latch

The Hybrid Latch Flip-Flop has two stages. The first stage generates a pulse as a sample window based on data input. Three inverters delay the clock signal and the propagation time between clock and delayed clock determines the pulse width. According to Nedovic and Oklobdzija [7] the second stage functions as capturing the pulse from the first stage, the output sets to 0 if the pulse does not arrive when clock switching to 1. The circuit is designed to reduce the energy [2] by using less width pulse instead of clock to pass the data to the second stage of the circuit. To generate the pulse, we use the delayed clock path to generate a delayed clock while sizing down the pull-up devices to make the pulse wide enough to pass the data. We keep the pull-down devices not too high to prevent creating a pulse that is too wide to save energy.

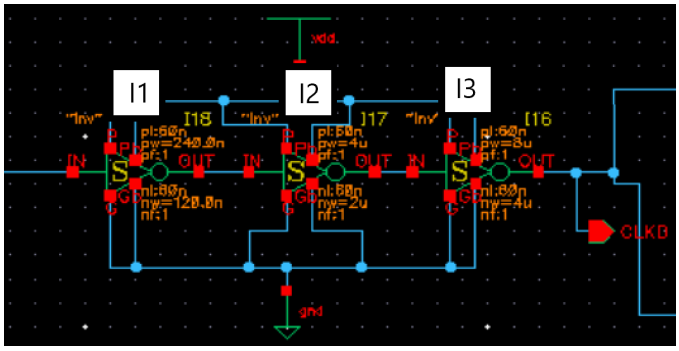


**Fig. 3. HLFF Delay circuit**

### 4.3 Semi Dynamic Edge-Triggered Flip-Flop

The circuit has two stages, the first stage is dynamic, and the second stage is static [5]. The first stage pre-charge the Node X to VDD when the clock is in the pre-charge phase. Then, to make the pulse in the node X, we make input D switch to logic 1 at the end of the evaluation phase, the NMOSs in the first stage will pull down node X and trigger the transistors in the second stage to transmit the signal. When the clock signal changes to logic 0 again, the first stage would switch to pre-charge phase for charging node X to $V_{DD}$ again, and the stage 2 would be closed. The level restorer at the second stage will maintain the logic of output so the first stage only needs a narrow pulse to pass the data.

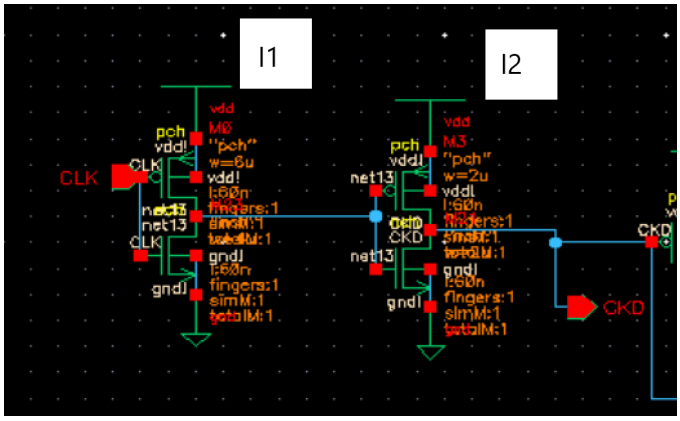


**Fig. 5. Semi Dynamic Edge-Triggered Flip-Flop Delay circuit**

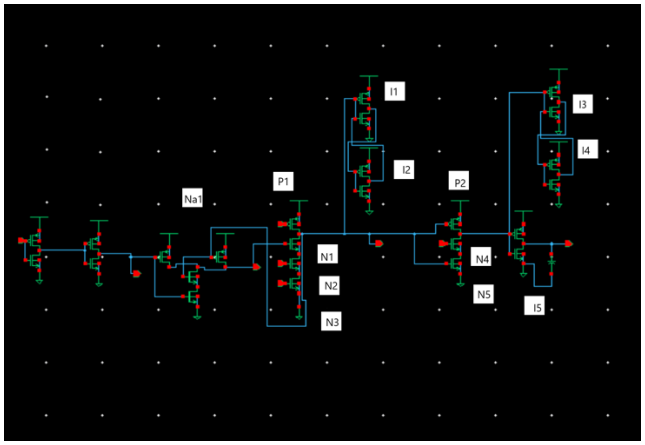


**Fig. 6. Semi Dynamic Edge-Triggered Flip-Flop circuit**

### 4.4 Time Borrowing master-slave flip-flop (tb-SMS)

Time Borrowing master-slave flip-flop is a type of implicit-pulsed static flip-flop design. It is combined with the two stages of transmission gates and positive feedback with controlling signal in the output of both two stages. The main difference between ip-DCO is that there is a delay between the first and second stage. Then, the times when transmitting in the first and second stages would be different. Moreover, the positive feedback would be driven by clock signal and maintain the logic level of the output when the transmission gate switches off. These designs provide the circuit ability of time borrowing. It means that the first stage could keep processing transmission before the gate switch on again. Then, after the delay of processing, the second stage switches on and begins processing the transmission to node Q.

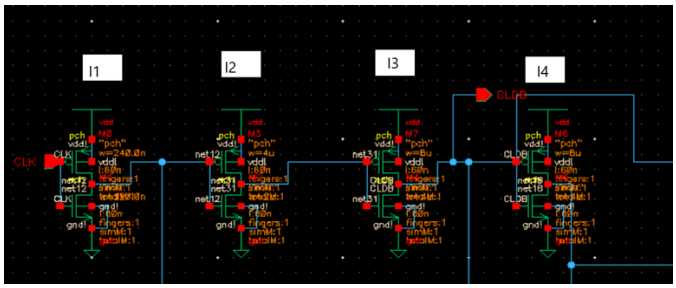


**Fig. 7. Tb-SMS Delay circuit**

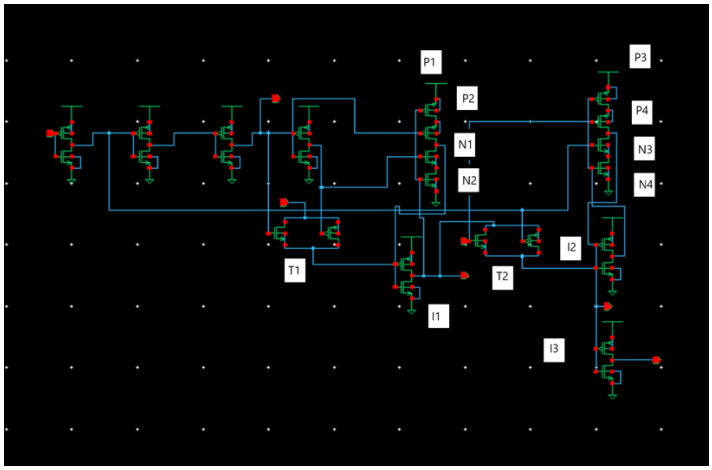


**Fig. 8. Tb-SMS circuit**

## 5. Results

This part presents the results and evaluation of the circuit according to those data. Although the relationship between energy per cycle and delay time is similar to Tschanz et al.'s work [1], the amounts of energy and ED product in our designs is different. The main reason would be the fundamental proportion of all transistors in our designs. When defining the sizes, we paid more attention on whether the specific node needs pulling up or pulling down and set the sizes into very high and very low amounts. However, it is required to be considered that the glitch and delay would usually happen on skewed gates and gates with unbalanced effective capacitances. For those reasons, we increased the sizes for higher leakage tolerance and noise immunity.

### 5.1 ip-DCO

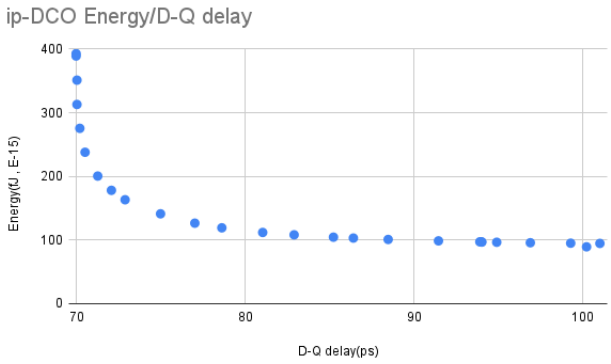


**Fig. 9. Ip-DCO Energy**

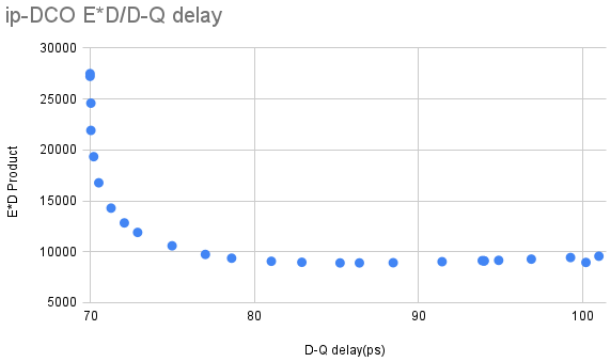


**Fig. 10. Ip-DCO Energy Delay Product**

The ip-DCO has a higher energy consumption with a higher delay compared to other 3 designs. In our tests, ip-DCO did not save energy compared to other 3 designs while it has a higher D-Q delay.

### 5.2 Hybrid Flip-Flop Latch

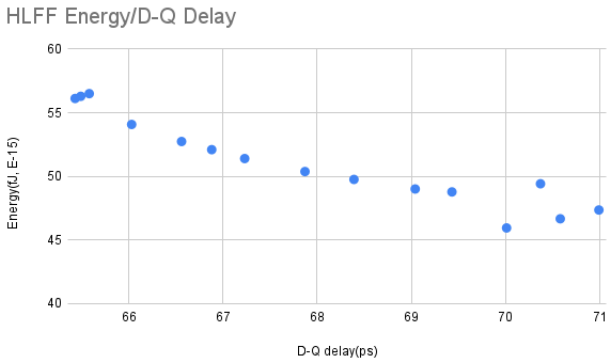


**Fig. 11. HLFF Energy**

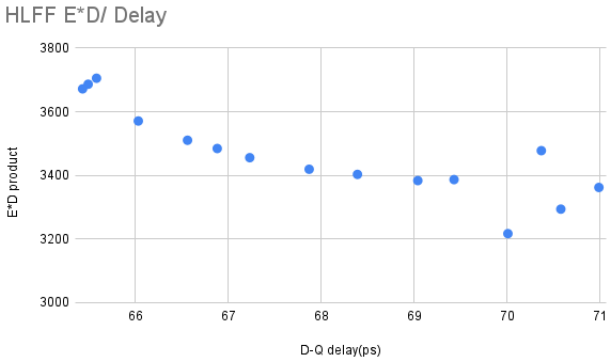


**Fig. 12. HLFF Energy Delay Product**

HLFF consumes lowest energy in 4 designs. Although the delay is higher than semi dynamic edge triggered flip-flop and tb-SMS, HLFF has a much lower energy consumption. This results HLFF has the lowest Energy Delay Product showing it is the most energy efficient design among the circuits we tested.

### 5.3 Semi Dynamic Edge-Triggered Flip-Flop

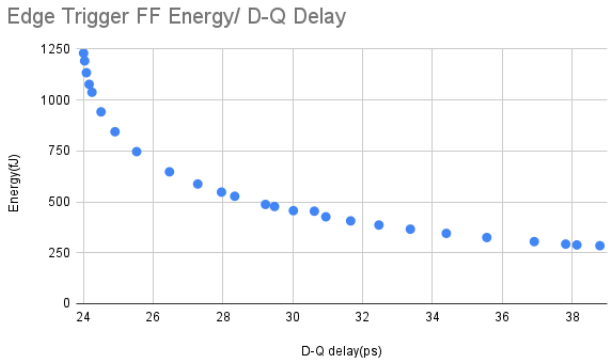


**Fig. 13. Semi Dynamic Edge-Triggered Flip-Flop Energy**

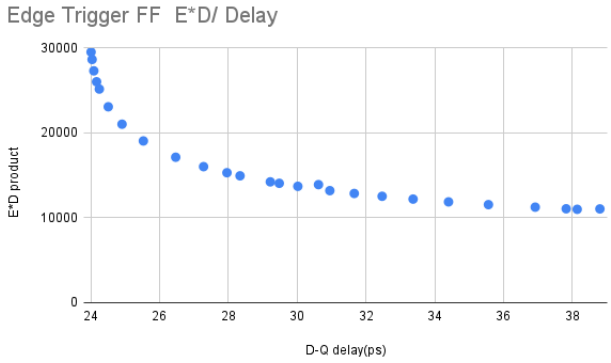


**Fig. 14. Semi Dynamic Edge-Triggered Flip-Flop Energy Delay Product**

Semi Dynamic Edge-Triggered Flip-Flop has a very low latency in terms of D-Q delay. This design reaches similar delay to tb-SMS with a much lower energy cost. Although it is around 0.75p second slower than tb-SMS it cost about 1/10 energy of tb-SMS with a similar delay.

### 5.4 Time Borrowing master-slave flip-flop (tb-SMS)

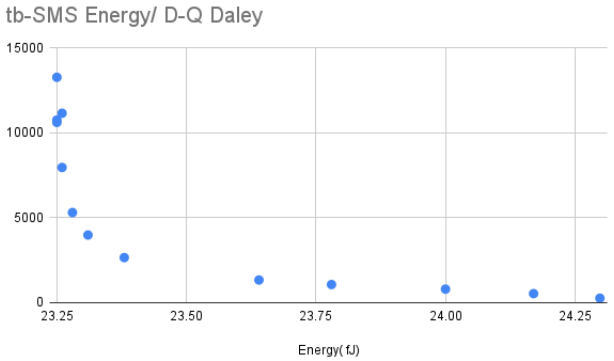


**Fig. 15. Tb-SMS Energy**

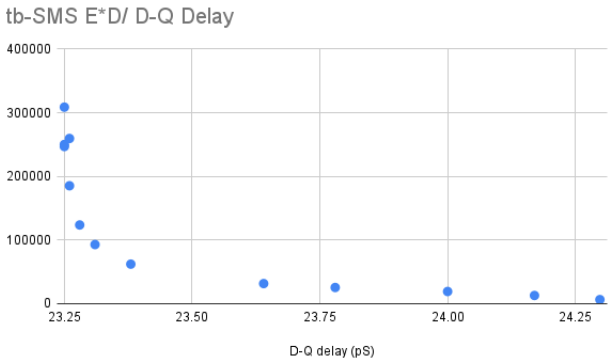


**Fig. 16. Tb-SMS Energy Delay Product**

According to data, tb-SMS has the least D-Q delay. The energy cost of tb-SMS is relatively high compared to Semi Dynamic Edge-Triggered Flip-Flop. ED product also indicates that tb-SMS is not as energy efficient as Semi Dynamic Edge-Triggered Flip-Flop.

| Minimal | Ip-DCO | HLFF | Edge triggering FF | Tb-SMS |
|---|---|---|---|---|
| Delay (pS) | 70.19 | 65.43 | 24.01 | 23.25 |
| Energy (fJ) | 275.5 | 56.12 | 1230 | 10620 |
| ED (pS*fJ) | 19337 | 3671.93 | 29532.3 | 246915 |

**Table 1. Minimal delay comparison**

For all four circuits, as we increase the total size of the transistors, delay reduces at before we reached the lowest D-Q delay. After the lowest delay point, the delay increases as the total size goes up. The energy keeps increasing as we increase the total size.

## 6. Conclusion

The pulse triggered flip-flops have advantages compare to static flip-flop in terms of saving energy. This design can reach a low energy cost without increase too much latency, resulting a low ED product. We found tb-SMS is the fastest design in these four circuits, but it is not the most energy efficient design. In our opinion, Semi Dynamic Edge-Triggered Flip-Flop should be used in high-speed operations because it has a low delay without adding too much energy cost. HLFF should be used for majority of the data paths because it has the highest energy efficiency according to ED product.

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