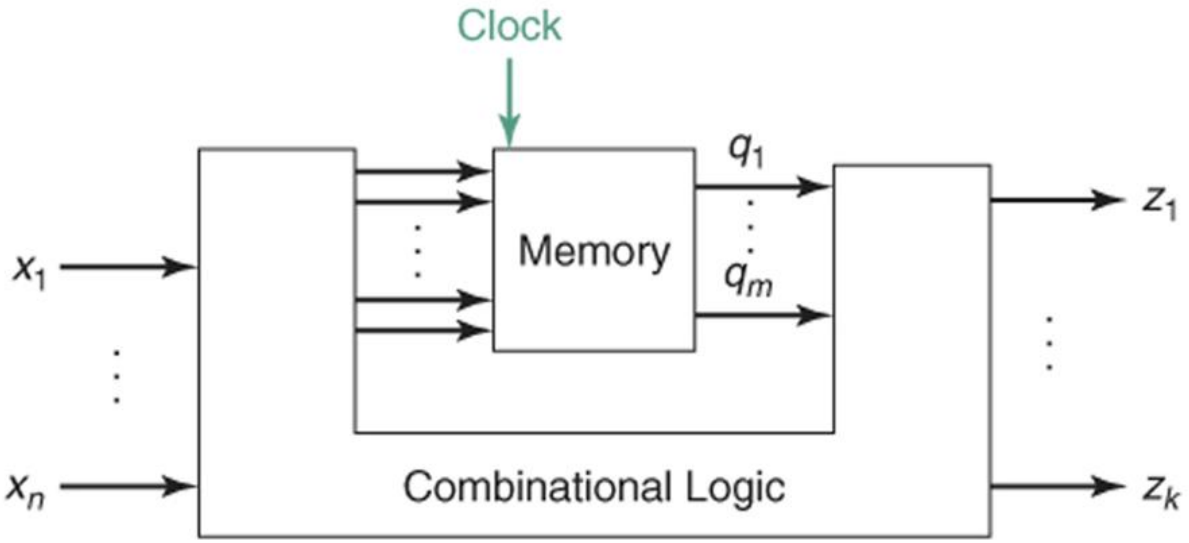
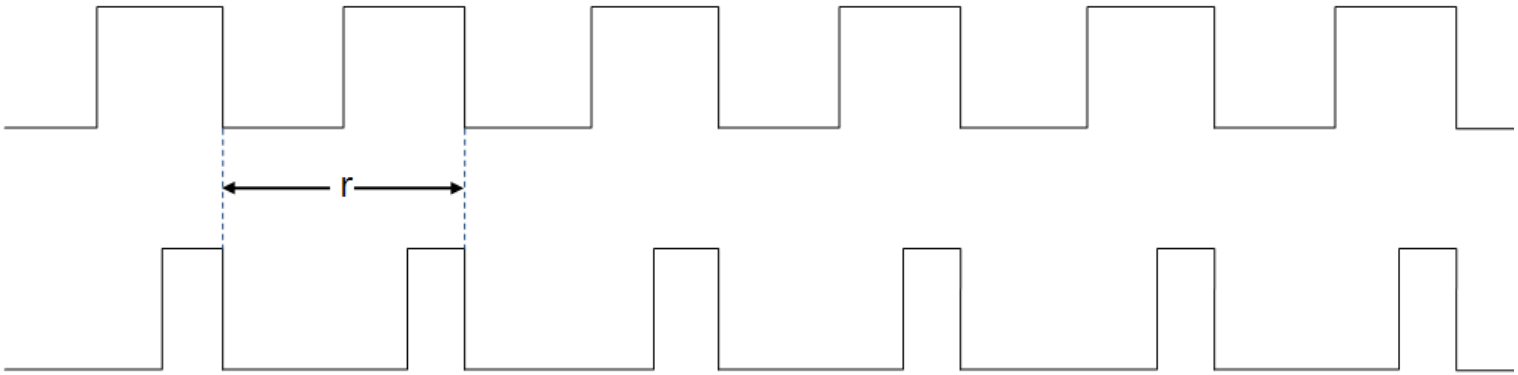
Chapter 5 Analysis of Sequential Systems

Figure 5.2 Conceptual view of a sequential system.

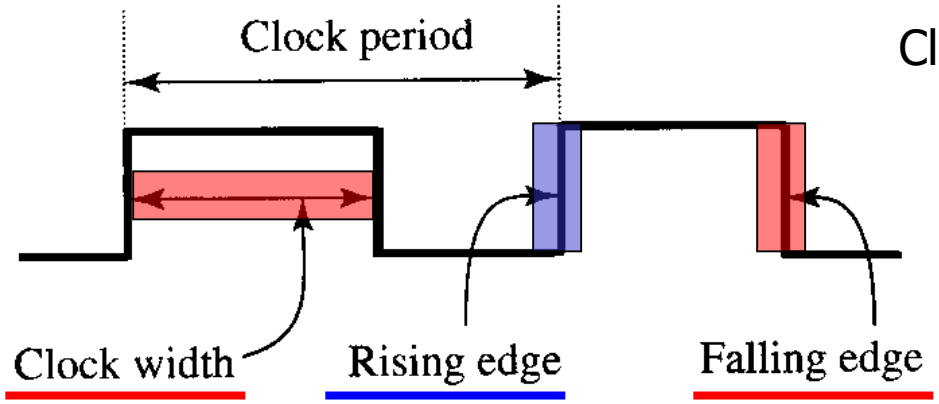


- Sequential systems (finite state machine)
  - systems with memory
  - Output depends on present input and past history
- Synchronous systems
  - Clock signal regulates input, internal, and output signal

Clock



- Alternating sequence of 0 and 1 at a regular rate
  - Two kinds: 0 and 1 in same length, 0 longer than 1



Clock period T = 1/clock_rate

Moore machine

- A system with one input x and one output z such that z = 1 iff x has been 1 for at least three consecutive clock times

Trace 5.1 Three consecutive 1's.

x	0	1	1	0	1	1	1	0	0	1	0	1	1	1	1	1	0	0			
z	?	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0

  - Output depends only on state of the system after the desired input pattern has occurred (not the present input).
  - Such system is called Moore machine (Moore model)
  - Output of the first input is unknown because no history

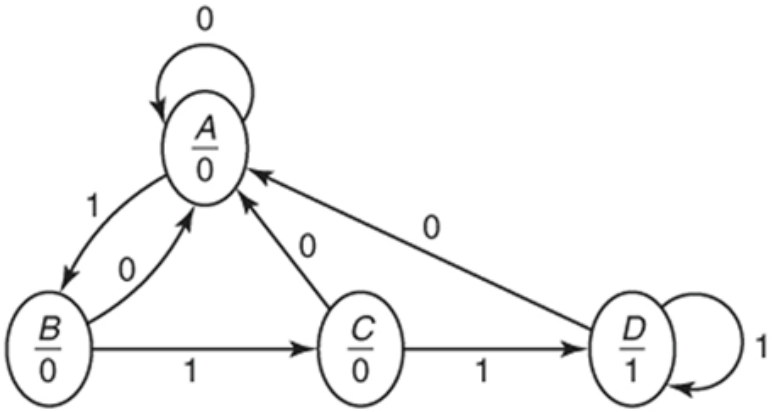
- Moore machine (finite state machine): output values are determined solely by its current state

Moore machine (state table, state diagram)

Table 5.1 A state table.

Present state	Next state $x = 0$	Next state $x = 1$	Output
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

Figure 5.3 A state diagram.

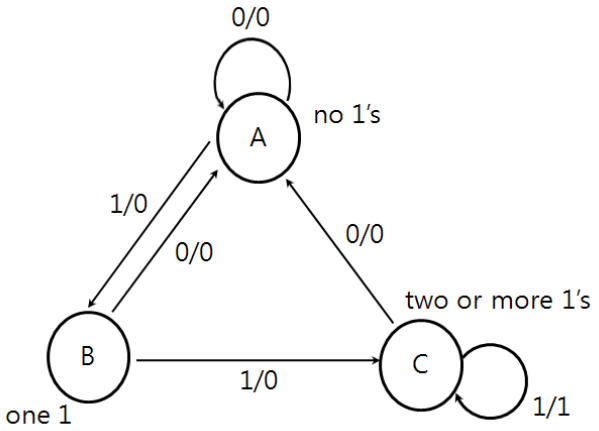


x	0	1	1	0	1	1	1	0	0	1	0	1	1	1	1	1	0	0		
q	?	A	B	C	A	B	C	D	A	A	B	A	B	C	D	D	D	A	A	?
z	?	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0

Mealy machine

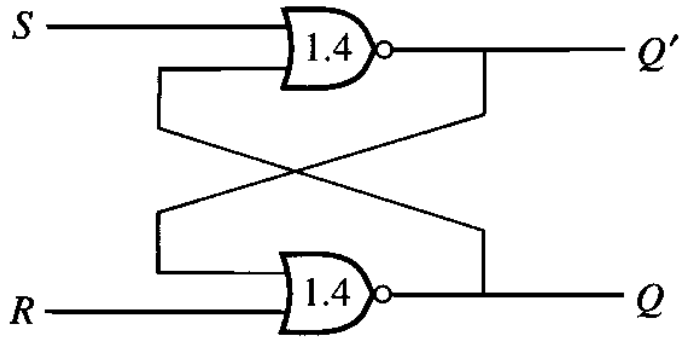
- Output depends on not only on the present state of the machine but also on the present input.

q	q*		z	
	x=0	x=1	x=0	x=1
A	A	B	0	0
B	A	C	0	0
C	A	C	0	1



x	0	1	1	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	0	0	
q	?	A	B	C	A	B	C	C	A	A	B	A	B	A	B	C	C	C	C	A	A
z	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Latch



(a) Logic schematic

S	R	Q	Q(next)	Q′(next)
0	0	0	0	1
0	0	1	1	0
0	1	X	0	1
1	0	X	1	0
1	1	X	0	0

(b) Truth table

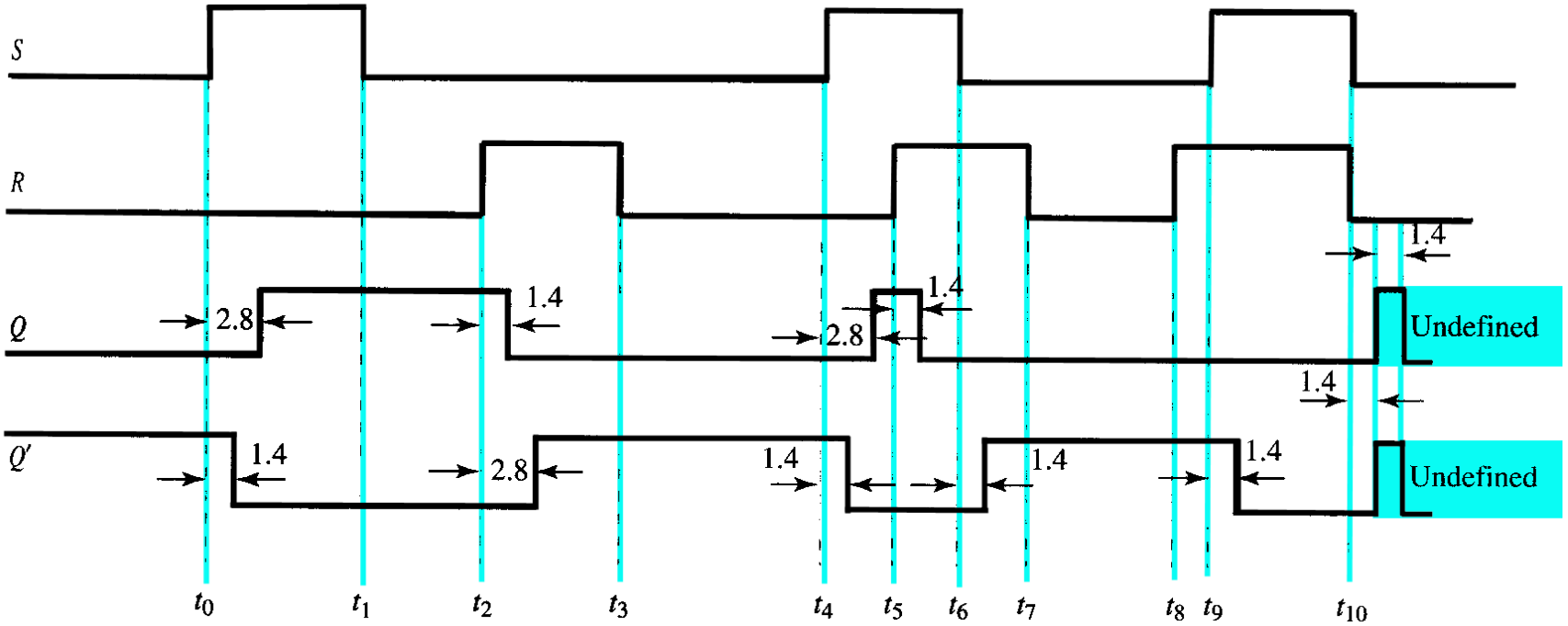
- SR latch is the simplest memory element
  two cross-coupled **NOR** gates

- Q′ = (S + Q)′
- Q = (R + Q′)′

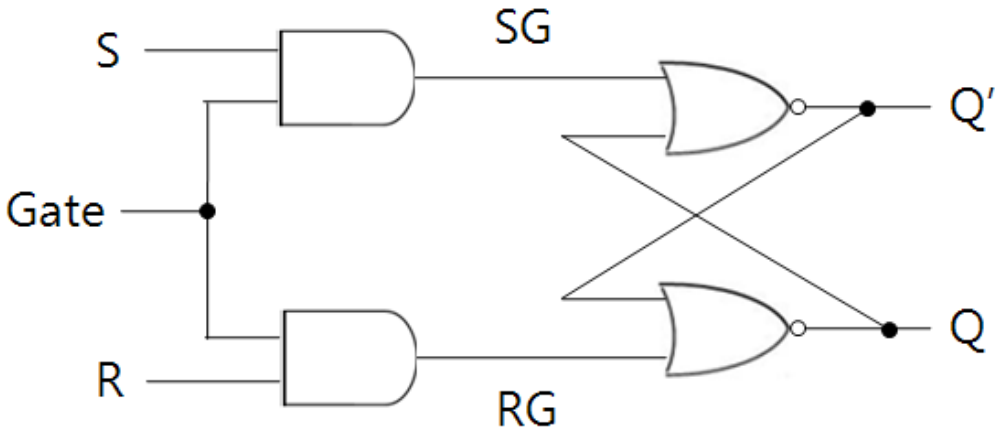
- two input signals
  - **the set signal** → ***S***, **the reset signal** → R
- two output signals
  - **set state** → ***Q=1 (Q`=0)***, **reset state** → ***Q=0, (Q`=1)***

SR Latch timing

S and R signal overlapping problem



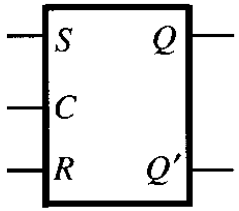
Gated latch



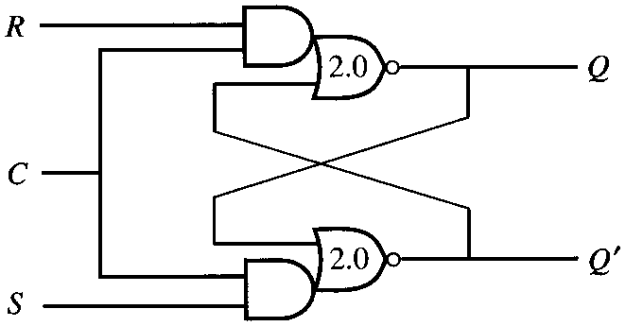
- Gate signal is inactive (= 0)
  - SG, RG are both 0. Latch remains unchanged.

- Gate signal is active (= 1)
  - Latch stores 0 or 1.

Clocked SR latch



(a) Graphic symbol



(b) Logic schematic

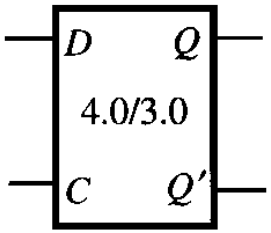
C	S	R	Q	Q(next)
0	X	X	0	0
0	X	X	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	X	0
1	1	0	X	1
1	1	1	X	NA

(c) Truth table

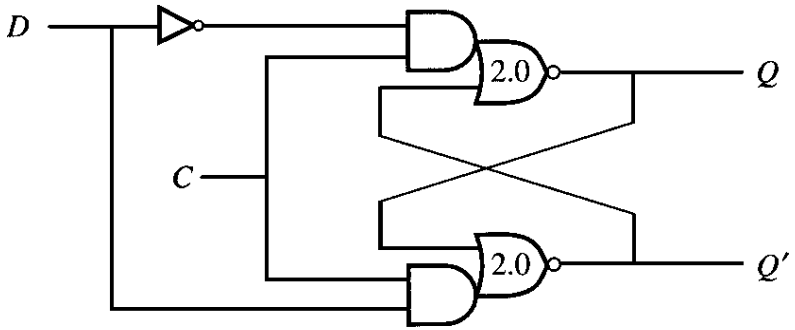
- two input and a third control input ***C***
- ***C=1*** $\rightarrow$ operate as **SR latch**, ***C=0*** $\rightarrow$ **setting or resetting**
- **The gated SR latch** is called **a clocked SR latch**

Gated D latch

- only one input ***D*** and a control input ***C***
- ***D*** input to the ***S*** input and ***D`*** to the ***R*** input of the ***SR*** latch
- ***S*** and ***R will never equal 1 at same time***
- ***C=1*** → same values as **input D**, ***C=0*** → **last value of D**



(a) Graphic symbol

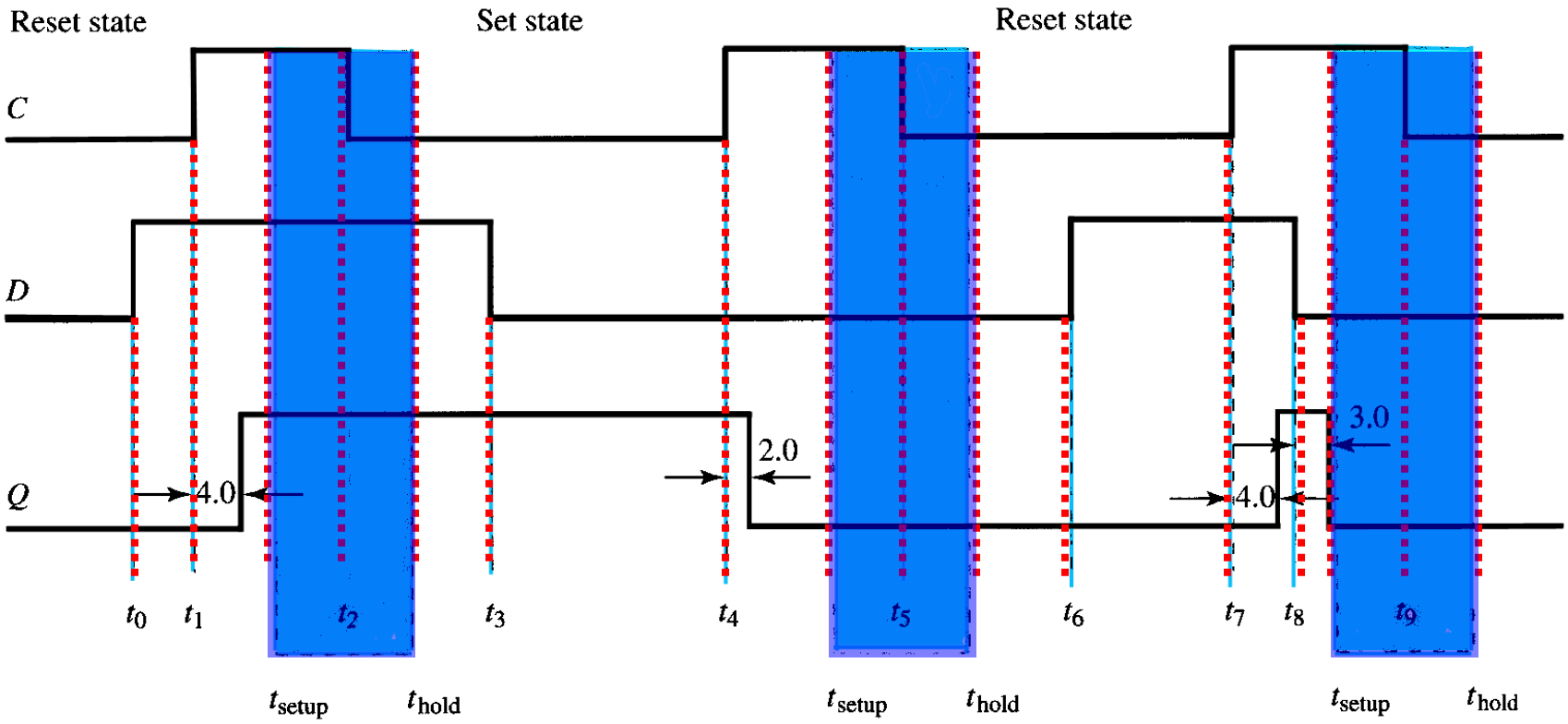


(b) Logic schematic

C	D	Q	Q(next)
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

(c) Truth table

Gated D latch timing



Flip Flops

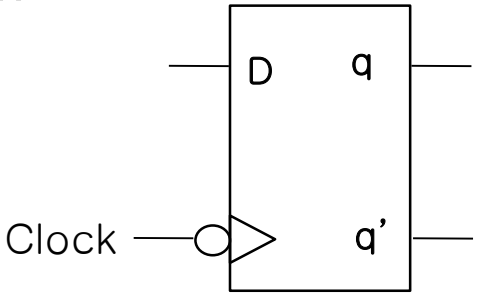
- A flip flop is a clocked binary storage device, that is, a device that stores either 0 or 1. The value will change on the appropriate transition of the clock.

- Trailing edge triggered (falling) or Leading edge triggered (rising) by clock signal

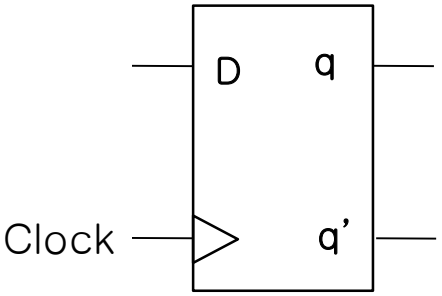
- D flip flop
- SR flip flop
- JK flip flop
- T flip flop

D flip flop

- Output is just the input delayed until the next active clock transition. The next state of the D flip flop is the value of D before the clock transition

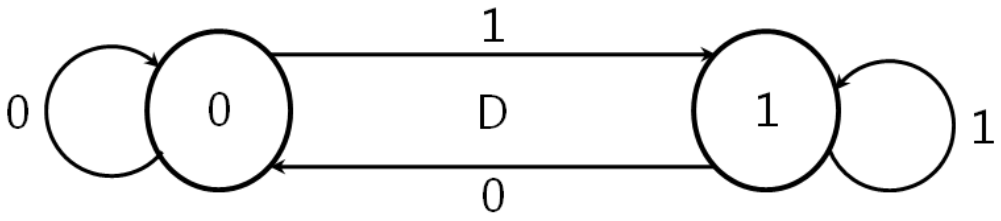


Trailing-edge Triggered

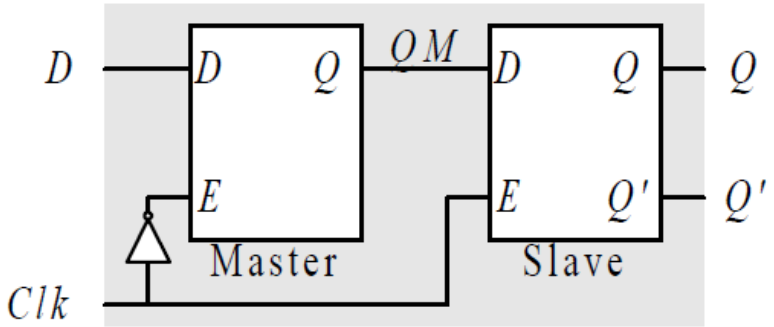


Leading-edge Triggered

D	q*
0	0
1	1



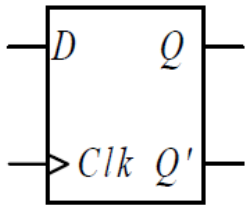
D flip flop using two D latches



(a)

Clk	D	Q	Q_{next}	Q_{next}'
0	×	0	0	1
0	×	1	1	0
1	×	0	0	1
1	×	1	1	0
↓	0	×	0	1
↓	1	×	1	0

(b)

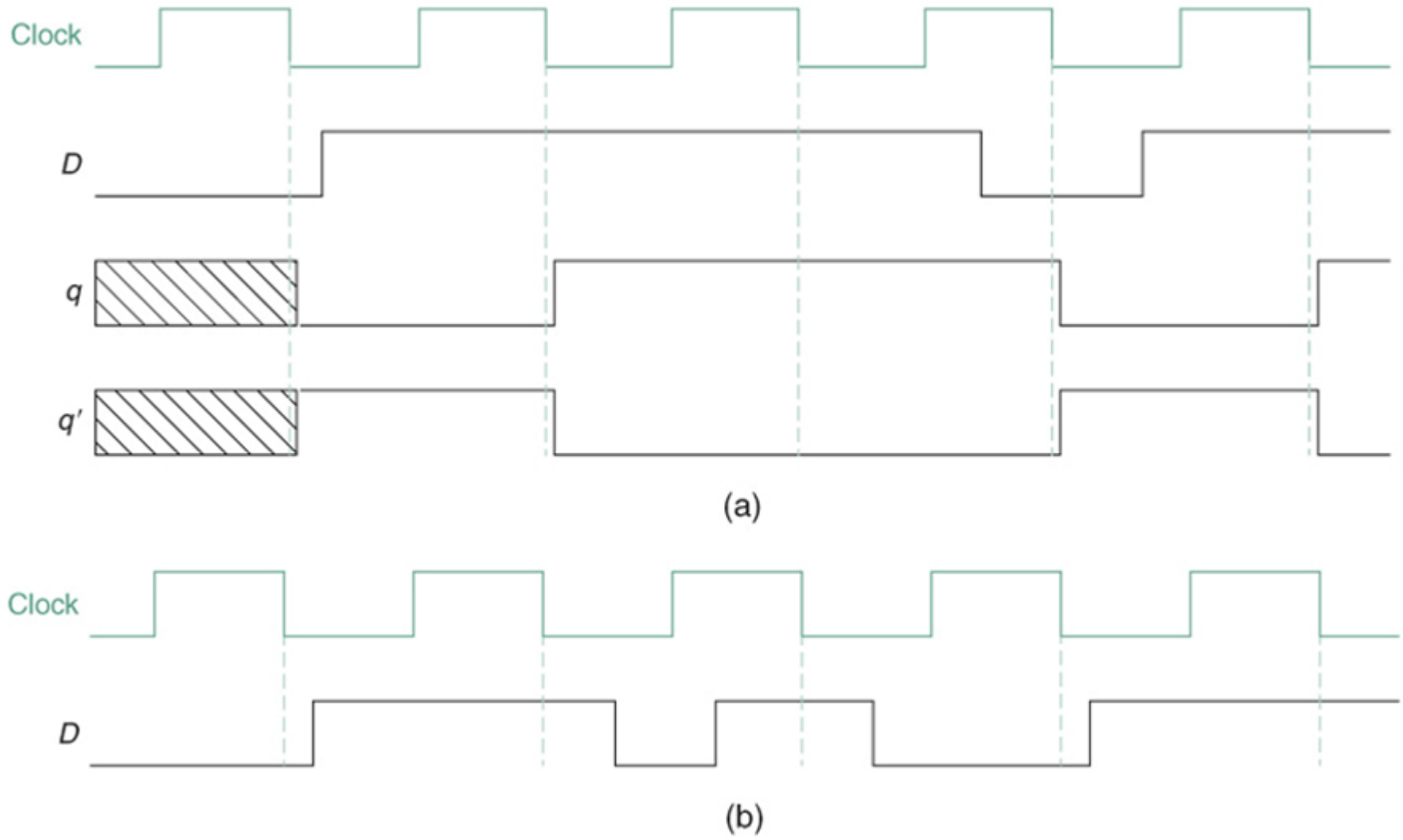


(c)

Clock and D of (a) and (b) results same q

(negative edge triggered)

Figure 5.9 *D* flip flop timing diagram.



Master-slave flip flops

- By connecting two D flip flops

Figure 5.11 Two flip flops.

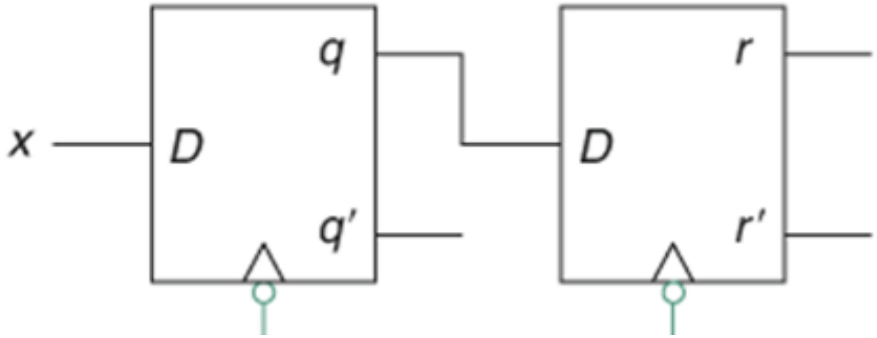
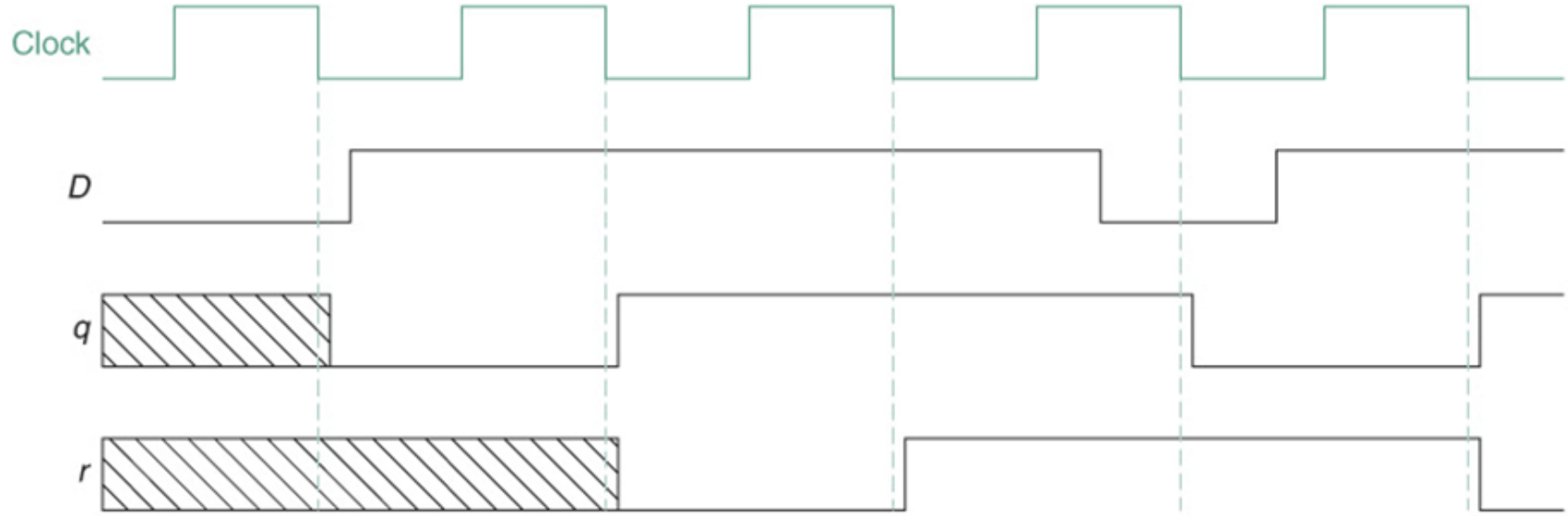


Figure 5.12 Timing for two flip flops.



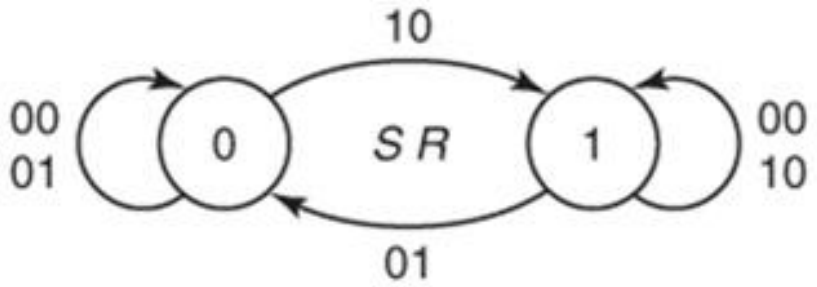
SR flip flop

Table 5.5 *SR* flip flop behavioral tables.

S	R	q	q^*	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	—	not
1	1	1	—	allowed

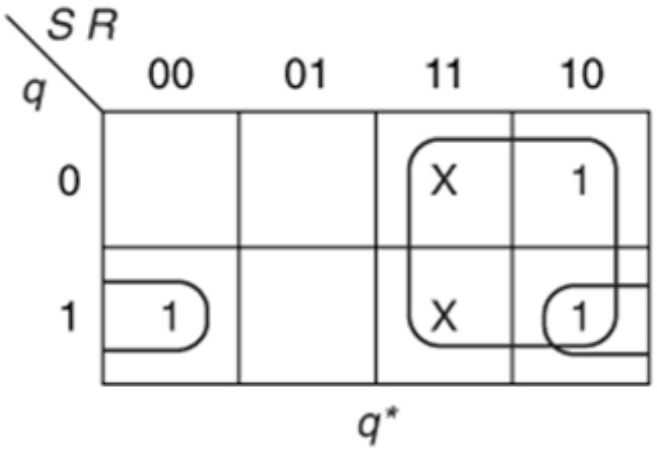
S	R	q^*	
0	0	q	
0	1	0	
1	0	1	
1	1	—	not allowed

Figure 5.15 *SR* flip flop state diagram.



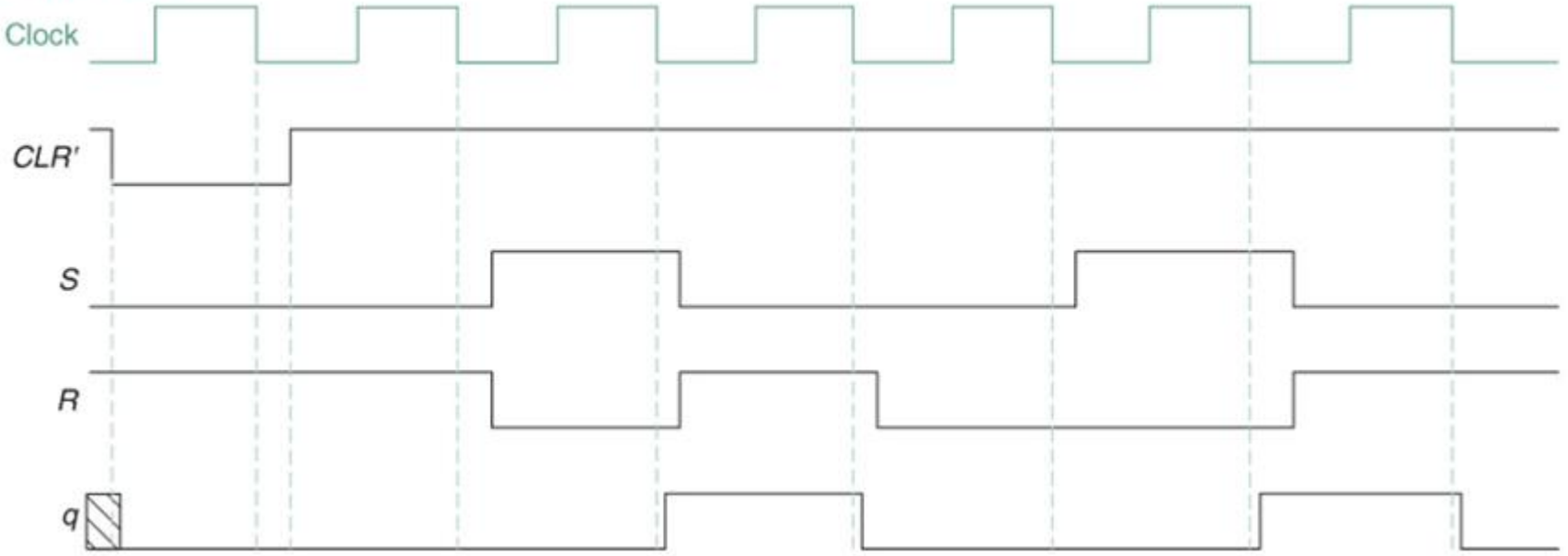
SR flip flop

Map 5.1 *SR* flip flop behavioral map.

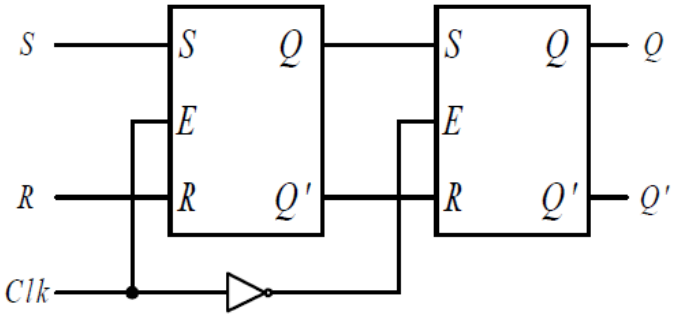


$q^* = S + R'q$

Figure 5.16 *SR* flip flop timing diagram.



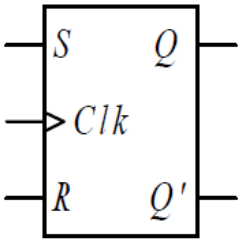
SR flip flop



(a)

S	R	Q	Q_{next}	Q_{next}'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	×	×
1	1	1	×	×

(b)



(c)

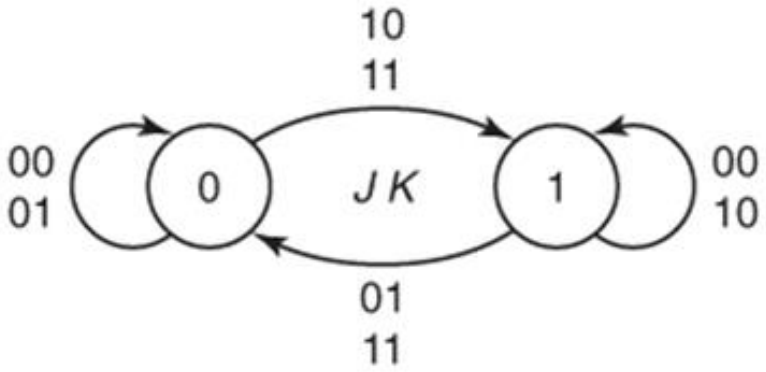
JK flip flop

Table 5.7 *JK* flip flop behavioral tables.

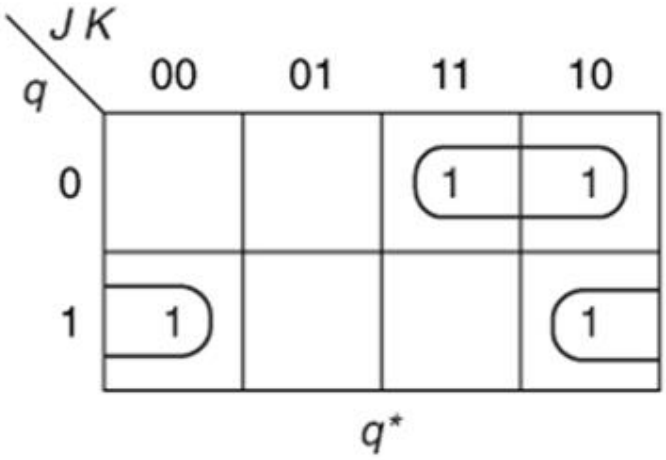
J	*K*	*q*	*q**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J	*K*	*q**
0	0	*q*
0	1	0
1	0	1
1	1	*q′*

Figure 5.19 *JK* flip flop state diagram.

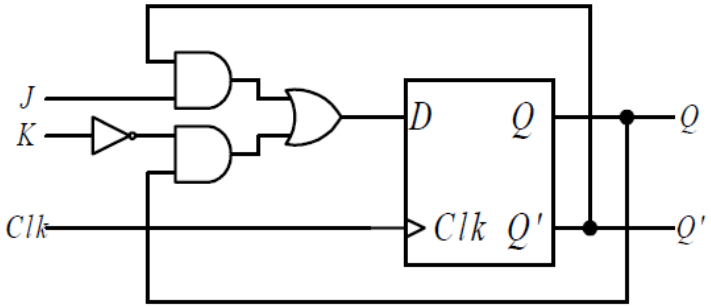


Map 5.2 *JK* flip flop behavioral map.



$q^* = Jq' + K'q$

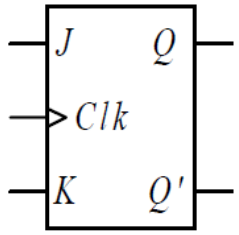
JK flip flop



(a)

J	K	Q	Q_{next}	Q_{next}'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

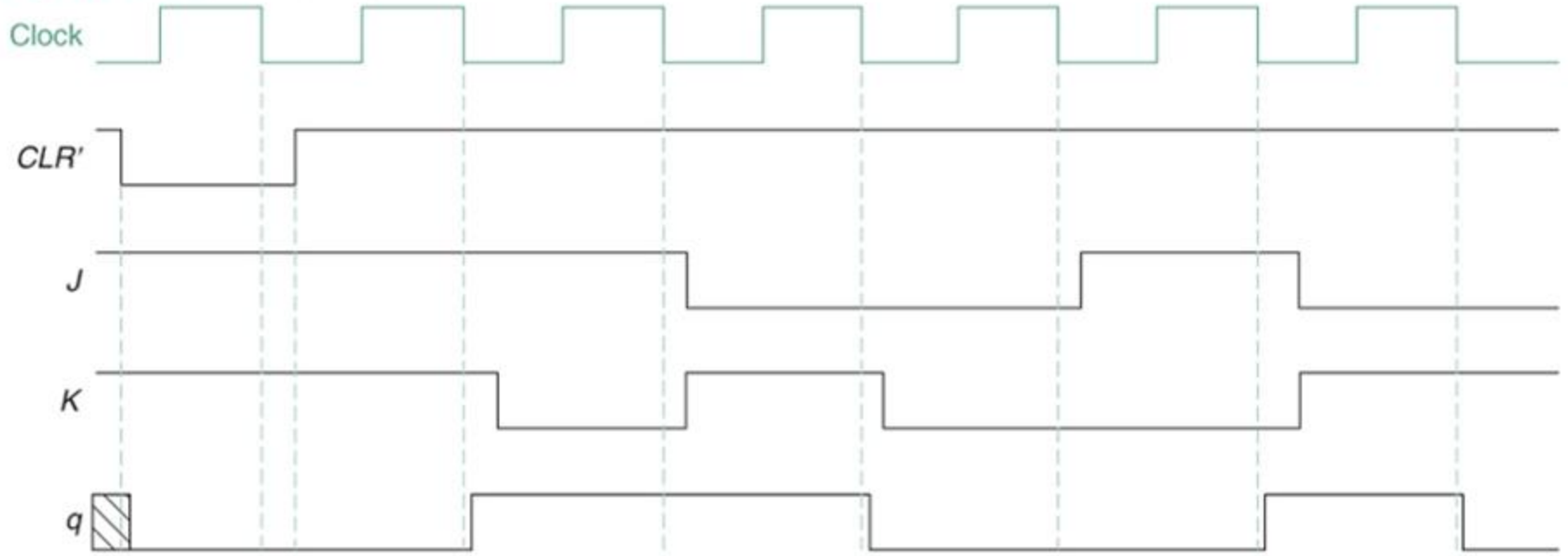
(b)



(c)

JK flip flop timing

Figure 5.20 Timing diagram for *JK* flip flop.



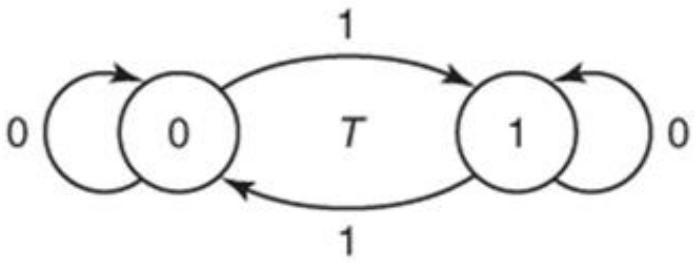
T flip flop

Table 5.6 *T* flip flop behavioral tables.

T	q	q^*
0	0	0
0	1	1
1	0	1
1	1	0

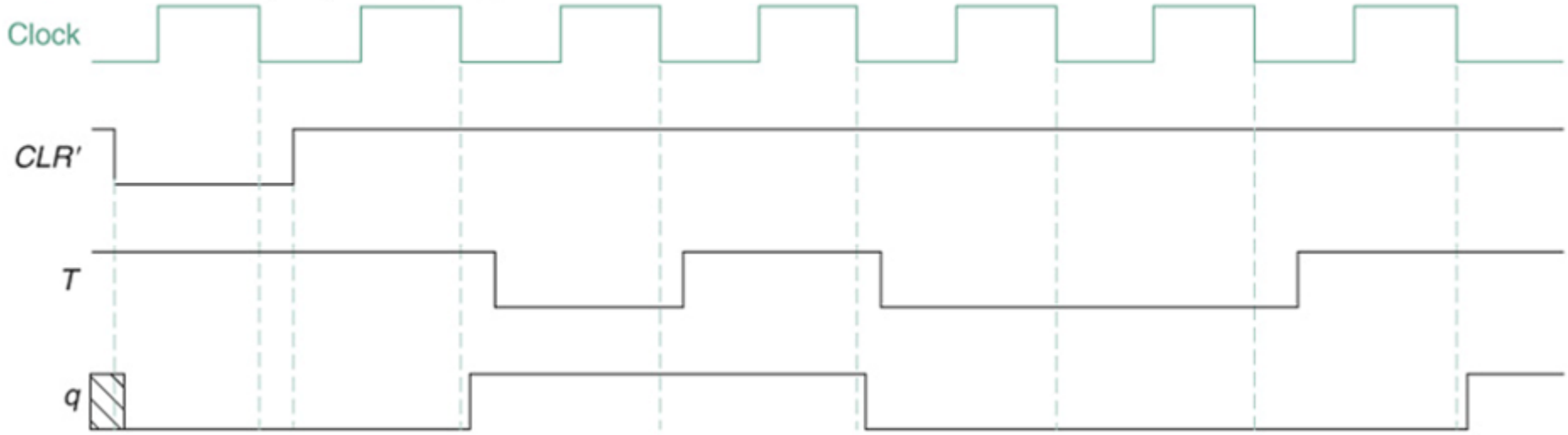
T	q^*
0	q
1	q'

Figure 5.17 *T* flip flop state diagram.

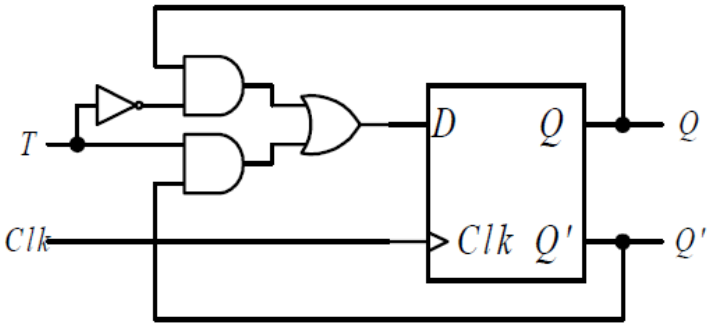


$q^* = T \oplus q$

Figure 5.18 *T* flip flop timing diagram.



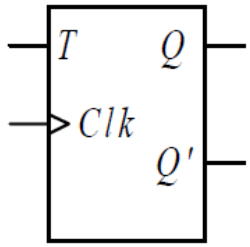
T flip flop



(a)

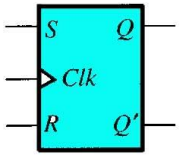
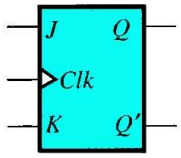
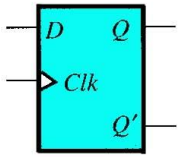
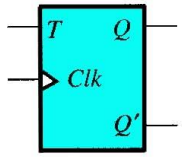
T	Q	Q_{next}	Q_{next}'
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

(b)

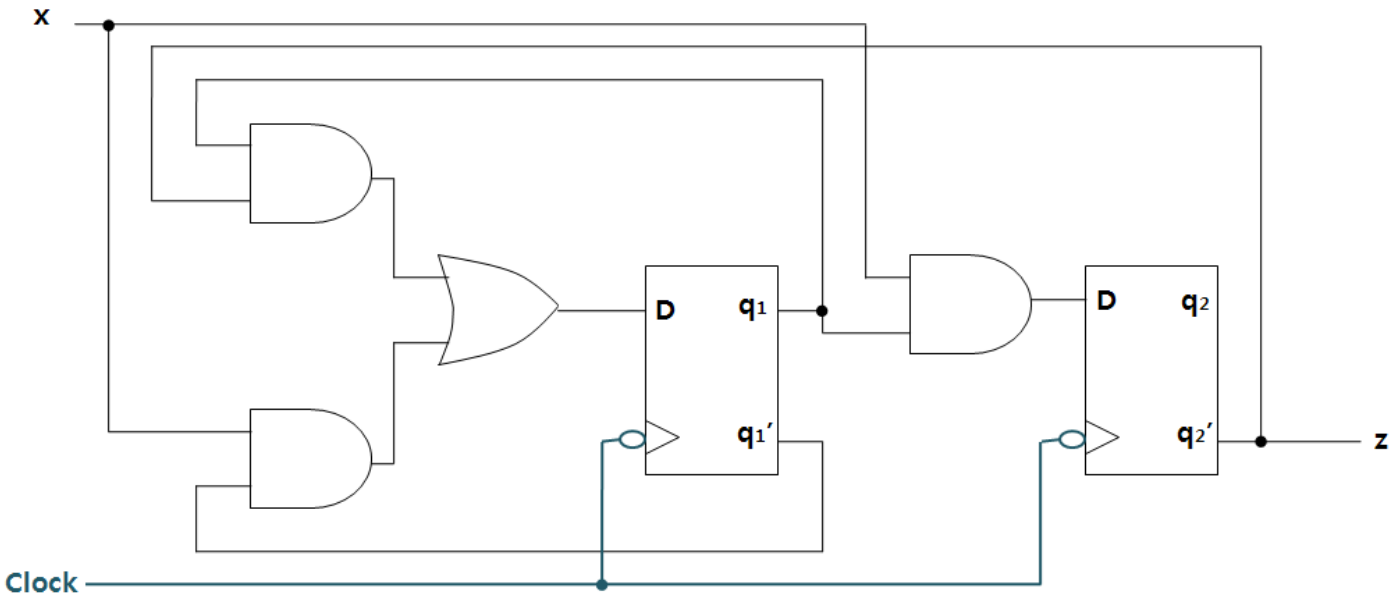


(c)

Summary of flip flop

FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE
SR		S R $Q(next)$ 0 0 Q 0 1 0 1 0 1 1 1 NA	$Q(next) = S + R'Q$ $SR = 0$	Q $Q(next)$ S R 0 0 0 X 0 1 1 0 1 0 0 1 1 1 X 0
JK		J K $Q(next)$ 0 0 Q 0 1 0 1 0 1 1 1 Q′	$Q(next) = JQ' + K'Q$	Q $Q(next)$ J K 0 0 0 X 0 1 1 X 1 0 X 1 1 1 X 0
D		D $Q(next)$ 0 0 1 1	$Q(next) = D$	Q $Q(next)$ D 0 0 0 0 1 1 1 0 0 1 1 1
T		T $Q(next)$ 0 Q 1 Q′	$Q(next) = TQ' + T'Q$	Q $Q(next)$ T 0 0 0 0 1 1 1 0 1 1 1 0

D flip flop Moore model circuit



- Equation

$D_1 = q_1q_2' + xq_1'$

$D_2 = xq_1$

$z = q_2'$

Construct (1) state table and
(2) state diagram from the circuit

Table 5.8a Partial state table.

q_1q_2	$q_1^* q_2^*$ $x=0$	$x=1$	z
0 0	0	1	1
0 1	0	1	0
1 0	1	1	1
1 1	0	0	0

Table 5.8b Complete state table.

q_1q_2	$q_1^* q_2^*$ $x=0$	$x=1$	z
0 0	0 0	1 0	1
0 1	0 0	1 0	0
1 0	1 0	1 1	1
1 1	0 0	0 1	0

- Equation

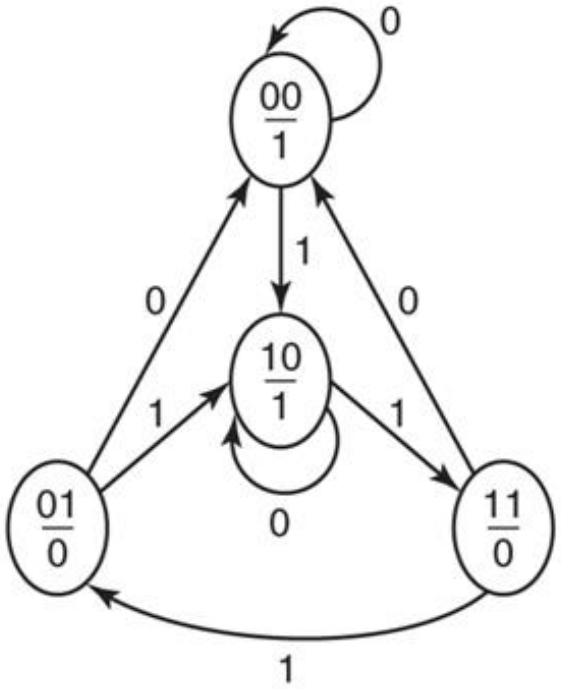
$D_1 = q_1q_2' + xq_1'$

$D_2 = xq_1$

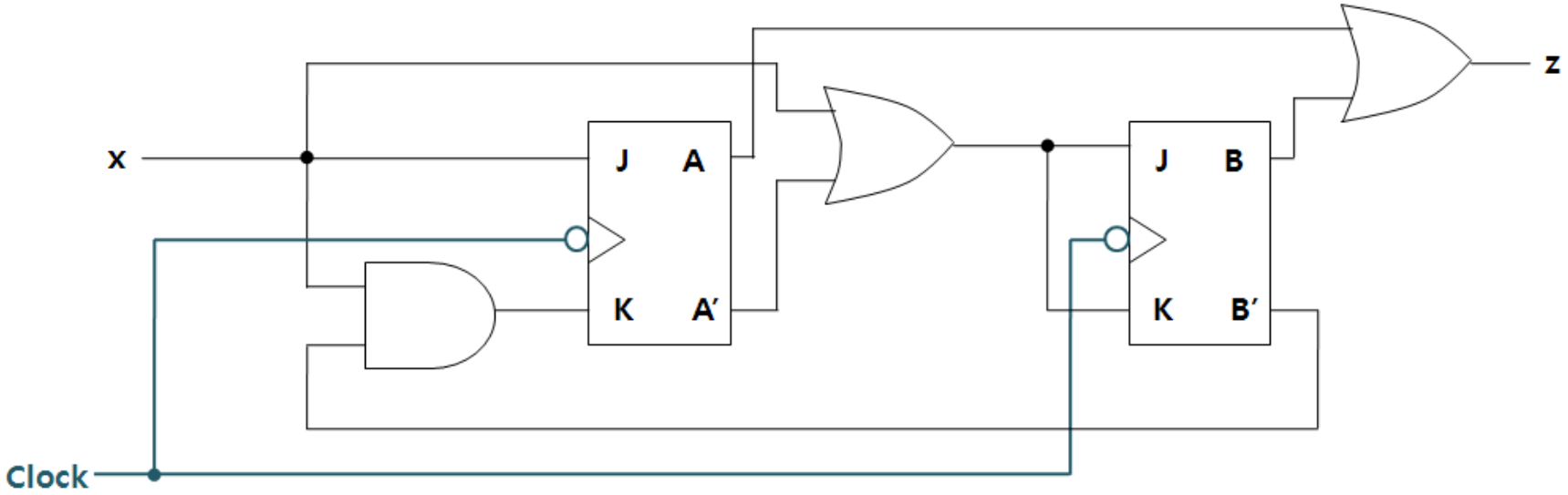
$z = q_2'$

For next state q* = D
q1* = D1
q2* = D2

Figure 5.22 A Moore state diagram.



JK flip flop Moore model circuit



- Equation

$J_A = x \quad K_A = xB'$

$J_B = K_b = x + A'$

$z = A + B$

Construct (1) state table and
(2) state diagram from the circuit

Table 5.7 *JK* flip flop behavioral tables.

J	K	q	q*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J	K	q*
0	0	q
0	1	0
1	0	1
1	1	q'

- Equation

$J_A = x \quad K_A = xB'$

$J_B = K_b = x + A'$

$z = A + B$

Table 5.9a State table with first two entries.

A B	A* B* x = 0	A* B* x = 1	z
0 0	0 1		0
0 1	0 0		1
1 0			1
1 1			1

Table 5.9b State table with A^* entered.

A B	A* B* x = 0	A* B* x = 1	z
0 0	0	1	0
0 1	0	1	1
1 0	1	0	1
1 1	1	1	1

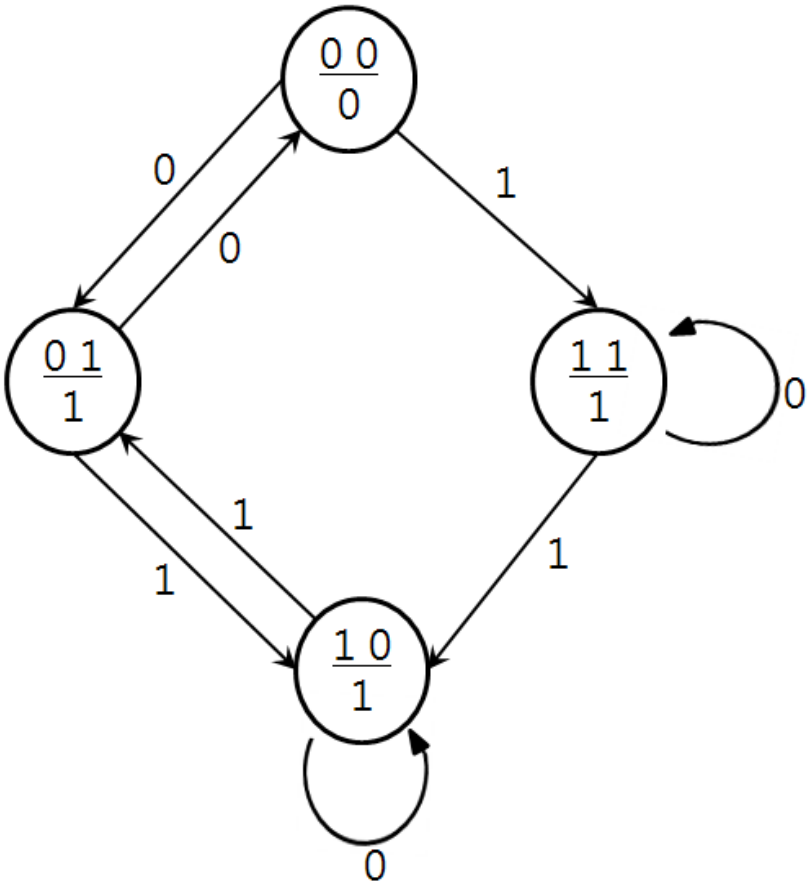
Table 5.9c Completed state table.

A B	A* B* x = 0	A* B* x = 1	z
0 0	0 1	1 1	0
0 1	0 0	1 0	1
1 0	1 0	0 1	1
1 1	1 1	1 0	1

State diagram

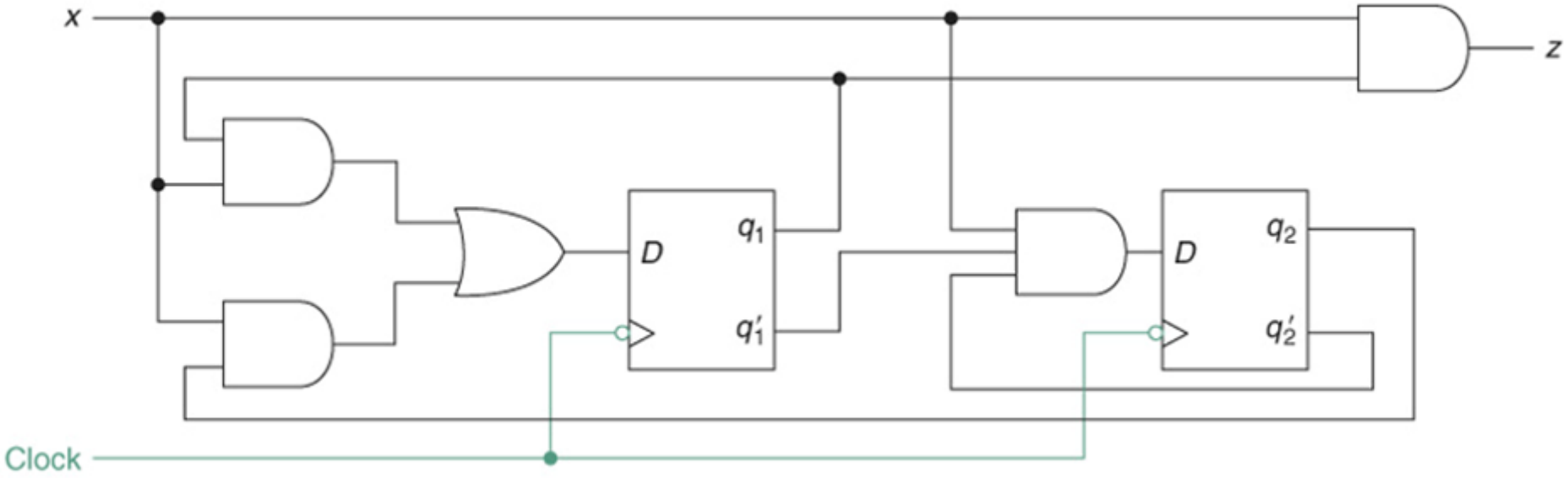
Table 5.9c Completed state table.

A B	$A^* B^*$ $x = 0$	$x = 1$	z
0 0	0 1	1 1	0
0 1	0 0	1 0	1
1 0	1 0	0 1	1
1 1	1 1	1 0	1



A Mealy Model

Figure 5.26 A Mealy model.



$$D_1 = xq_1 + xq_2$$
$$D_2 = xq_1'q_2'$$
$$z = xq_1$$

analysis

$$D_1 = xq_1 + xq_2$$
$$D_2 = xq_1'q_2'$$
$$z = xq_1$$

In D flip flops, q* = D
q1* = xq1 + xq2
q2* = xq1'q2'

Table 5.10 State table for the Mealy system.

q	q^* $x=0$	q^* $x=1$	z $x=0$	z $x=1$
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1
1 1	0 0	1 0	0	1

Figure 5.27 State diagram for a Mealy model.