Chapter 7 selected topics

- Circuit technology
- ASIC and CAD
- Circuit classification
- Circuit design and fabrication
- Design flow
- Design Constraints
  - Performance
  - Power

Circuit technology

- First Generation: Vacuum Tube
- Second Generation: Transistor
  - invented in 1947
  - smaller, faster, cheaper
  - IBM-709TX in 1958
- Third Generation: IC (Integrated Circuit)
  - many tiny transistors on a single chip
  - IBM-360 in 1964
- Fourth Generation: LSI (Large Scale Integrated), VLSI (Very ~)
  - millions of transistors on a single chip
  - DEC's minicomputer, PDP-11 and IBM-370 mainframe in 1970, 1971
  - Today's personal computers

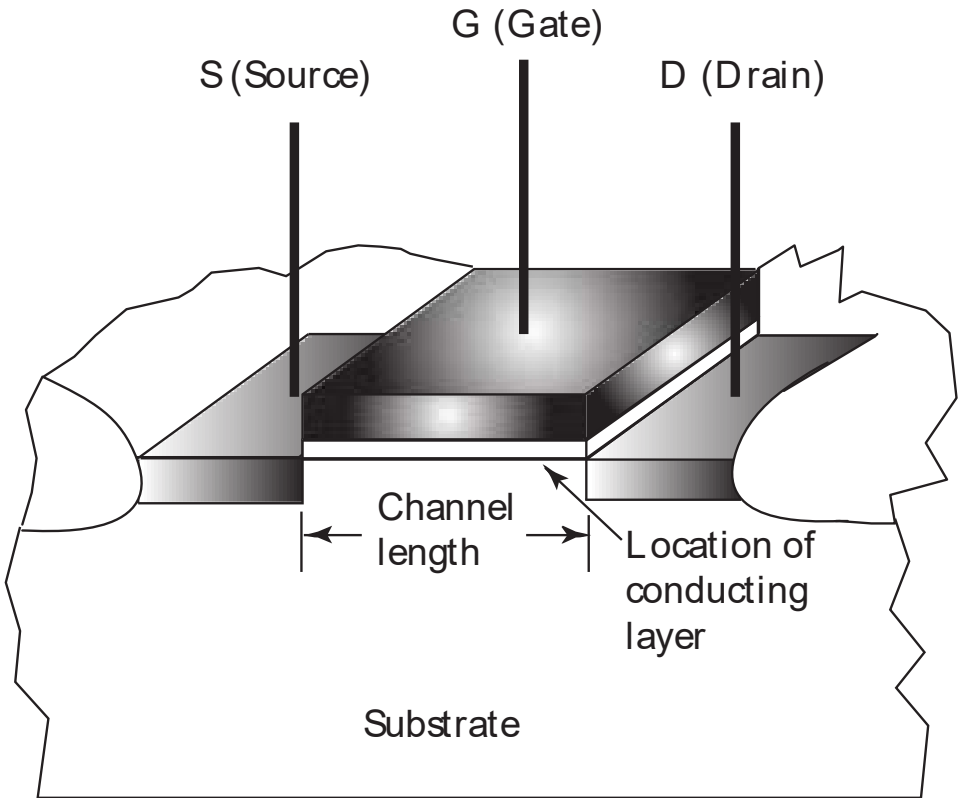
Small transistor technology makes faster and cheaper

Integrated circuits

- Integrated circuit (informally, a "chip") is a semiconductor crystal (most often silicon) containing the electronic components for the digital gates and storage elements which are interconnected on the chip.

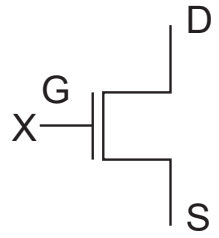
- Terminology - Levels of chip integration
  - *SSI* (*small-scale integrated*) - fewer than 10 gates
  - *MSI* (*medium-scale integrated*) - 10 to 100 gates
  - *LSI* (*large-scale integrated*) - 100 to thousands of gates
  - *VLSI* (*very large-scale integrated*) - thousands to 100s of millions of gates

MOS Transistor



Switch Models for MOS Transistors

- n-Channel – Normally Open (NO) Switch Contact

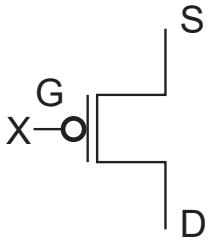


Symbol

Switch Model:

Simplifed
Switch Model

- p-Channel – Normally Closed (NC) Switch Contact



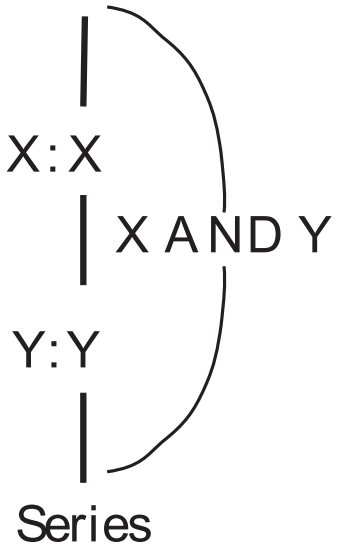
Symbol

Switch Model

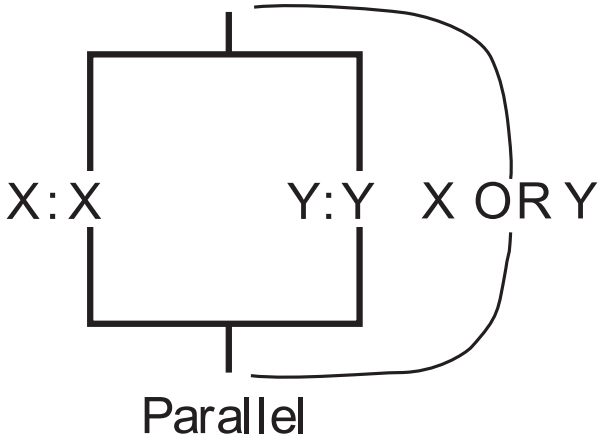
Simplified
Switch Model

Circuits of Switch Models

- Series

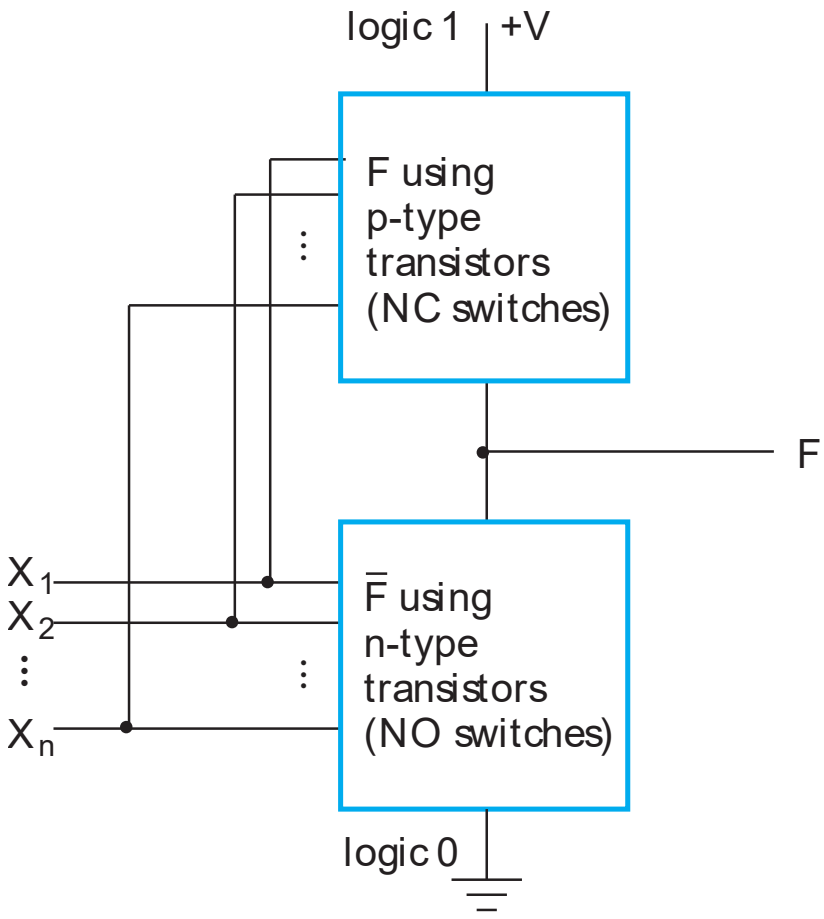


- Parallel



Fully-Complementary CMOS Circuit

- Circuit structure for fully-complementary CMOS gate



General Structure

CMOS Circuit Design Example

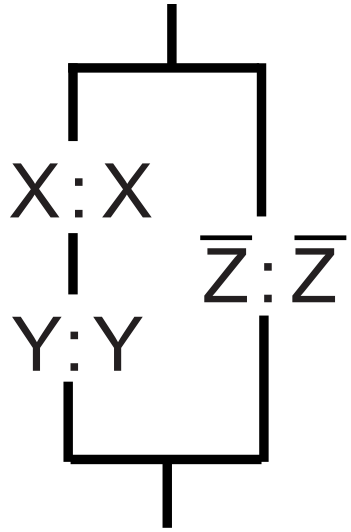
- Find a CMOS gate with the following function:

$$F = \overline{X}\,Z + \overline{Y}\,Z = (\overline{X} + \overline{Y})Z$$

- Beginning with F0, and using F'

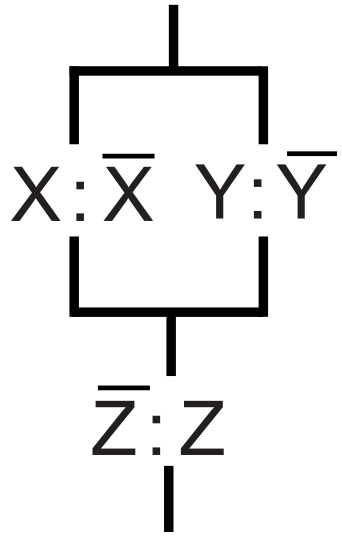
$$F0\ \text{Circuit:}\ \overline{F} = X\,Y + \overline{Z}$$

- The switch model circuit in terms of NO switches:



CMOS circuit design example

- The switch model circuit for F1 in terms of NC contacts is the dual of the switch model circuit for F0:



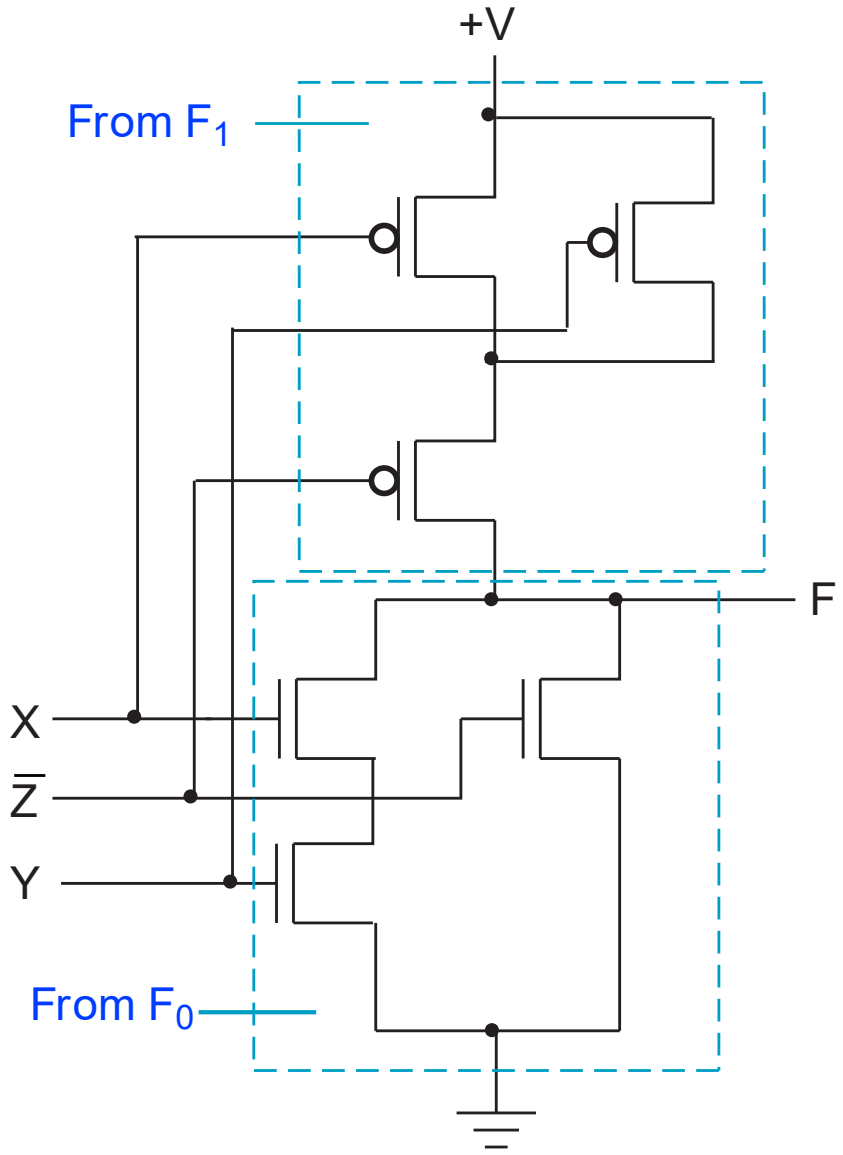
- The function for this circuit is:

$$F1\ \text{Circuit}: F = (\overline{X} + \overline{Y})\, Z$$

which is the correct F.

CMOS circuit design example

- Replacing the switch models with CMOS transistors; note input Z' must be used.



ASIC (Application Specific Integrated Circuit) and CAD

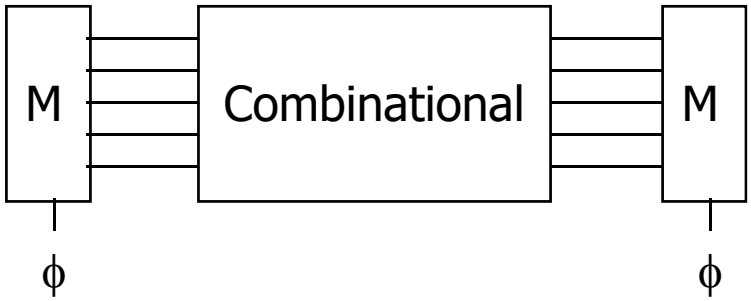
- integrated circuit (IC) components performing a specialized task or a limited set of tasks
- large market sharing
- issues
  - volume of sales
  - fast design time
  - low design cost
  - design quality measured by performance and manufacturing yield
- Computer-Aided Design (CAD) techniques
  - reduction of design time
  - optimization of design quality : optimization of large-scale circuits (millions of transistors) is a complex problem

Circuit Classifications

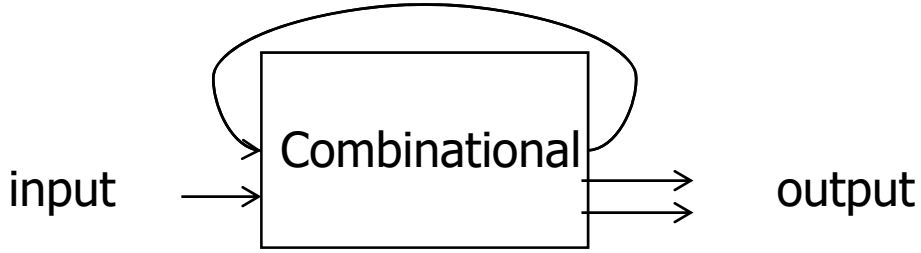
- semiconductor materials :
  - Silicon on sapphire, or p-well and n-well
  - Gallium-arsenide
- electronic device types :
  - Complementary Metal Oxide Semiconductor (CMOS) : PMOS and NMOS
  - Bipolar
  - Combination of CMOS and Bipolar : BiCMOS
- analog and digital
  - Analog circuit : information is related to the value of a continuous electrical parameter such as voltage or current (power amplifier for an audio system)
  - Digital circuit : information is related to the range of voltages at circuit internal nodes having binary values (logic 0 and 1)

Circuit classification

- Digital circuits in mode of operation : synchronous and asynchronous circuits
  - Synchronous circuit : a global clock controls the timing of the circuit, dominating digital circuit design, needs clock distribution

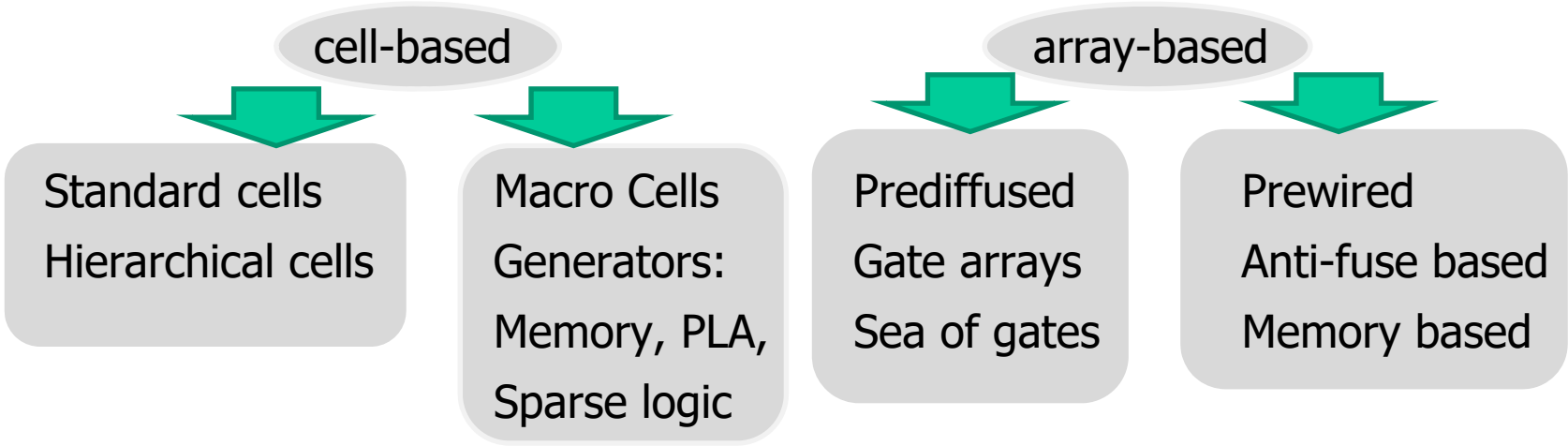


  - Asynchronous circuit : No global clock signal



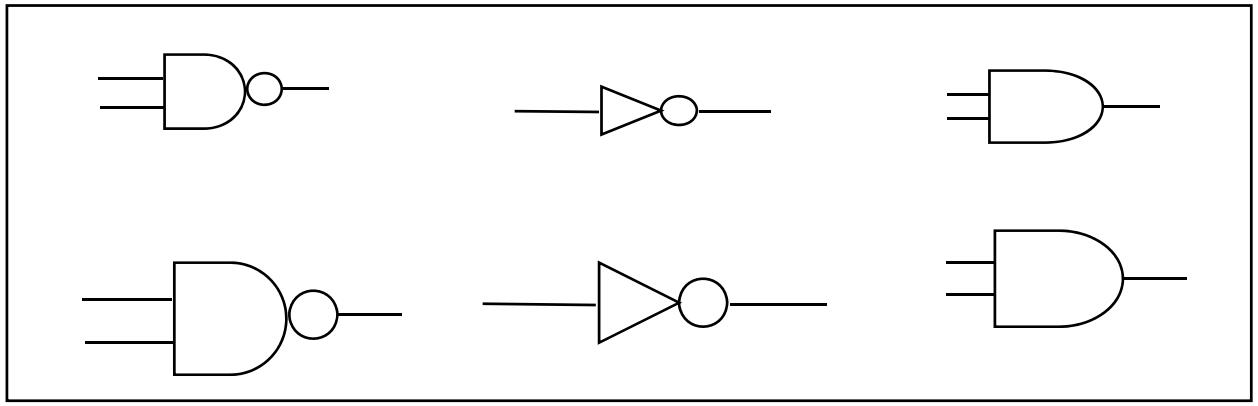
Circuit classification

- Microelectronic Design Styles
  - custom design: functional and physical design are hand-crafted, requiring an extensive effort of a design team to optimize each detailed feature of the circuit
    - expensive
    - large design time
    - high density, performance design
  - semi-custom design:



Cell based design

– Standard-cell design

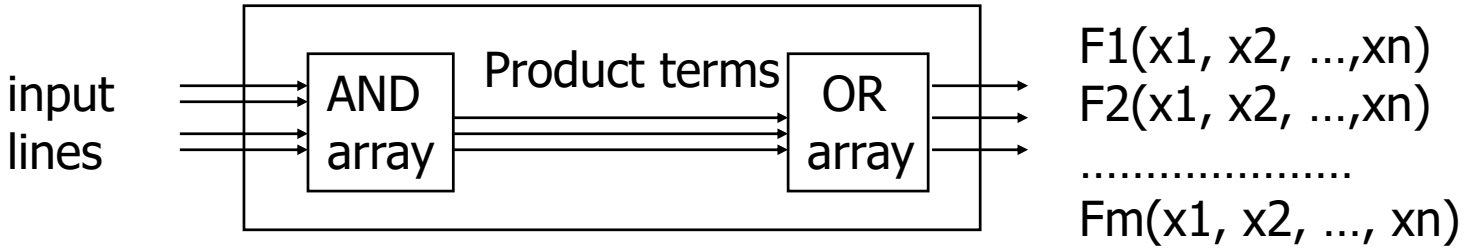


- fundamental cells are designed by *cell generators* and stored in the *library*
- updates are necessary as semiconductor technology progresses
- *library binding* or *technology mapping* from the library

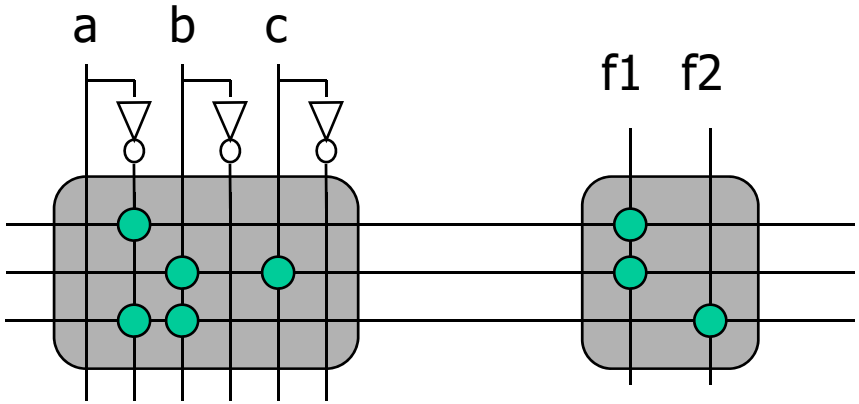
– Hierarchical standard-cell design: larger cells are derived by combining smaller cell

Macro-cell based design

- Macro-cell based design
  - automatic synthesis of memory arrays
    - RAM : read/write memory (random access)
    - ROM : read-only memory
  - programmable logic arrays (PLA) : a regular layout structure for implementing sum of products.



ex) f1 = a' + bc, f2 = a'b



Array based design

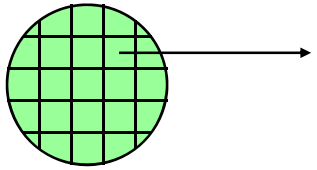
- Prediffused (mask programmable) based design
  - Gate arrays
- Prewired (field programmable gate arrays) based design
  - Anto-fuse based
  - memory based

Comparison of design styles

	Custom	Cell-based	prediffused	prewired
Density	Very high	High	High	Low
Performance	Very high	High	High	Low
Flexibility	Very high	High	Medium	Low
Design time	Very long	Short	Short	Very short
Manufacturing time	Medium	Medium	Short	Very short
Cost(low volume) Cost(high volume)	Very high Low	High Low	High Low	Low High

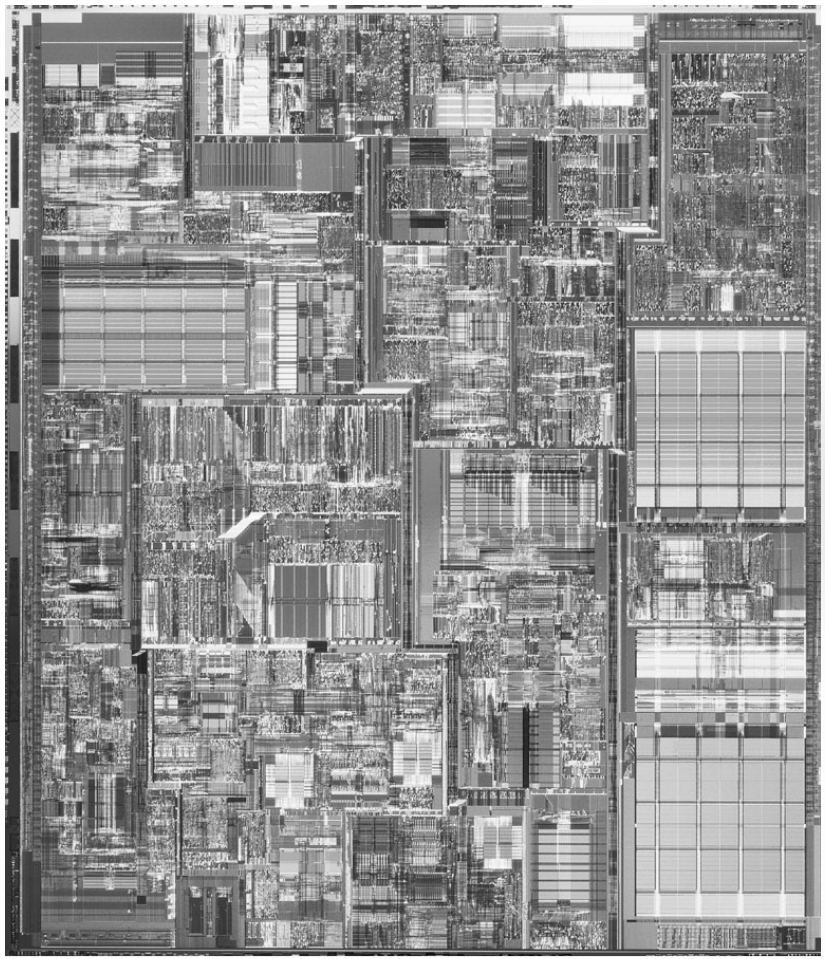
Circuit design

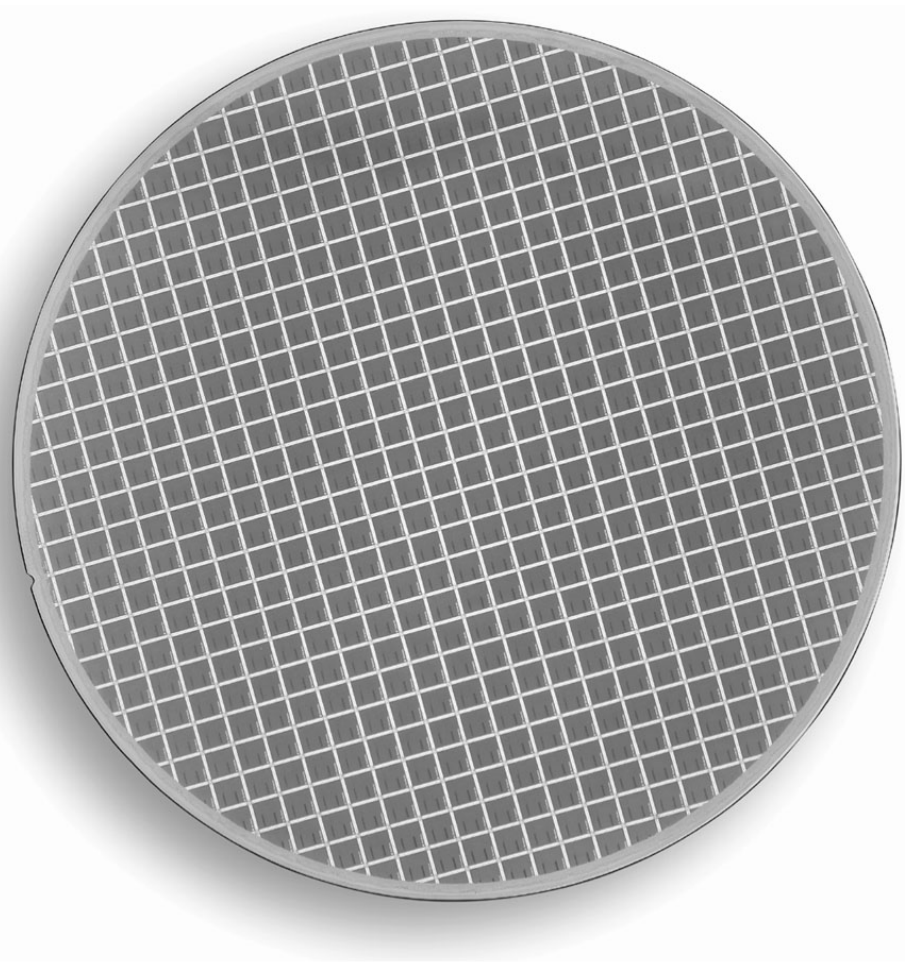
- design
  - modeling: representing ideas, modeling by *Hardware Description Languages*
  - synthesis and optimization: detailed model of the circuit and performance enhancement for speed, area, and power
  - validation: simulation and verification
- fabrication:
  - start with lightly doped silicon wafers 150~300 mm diameter & 1 mm thick



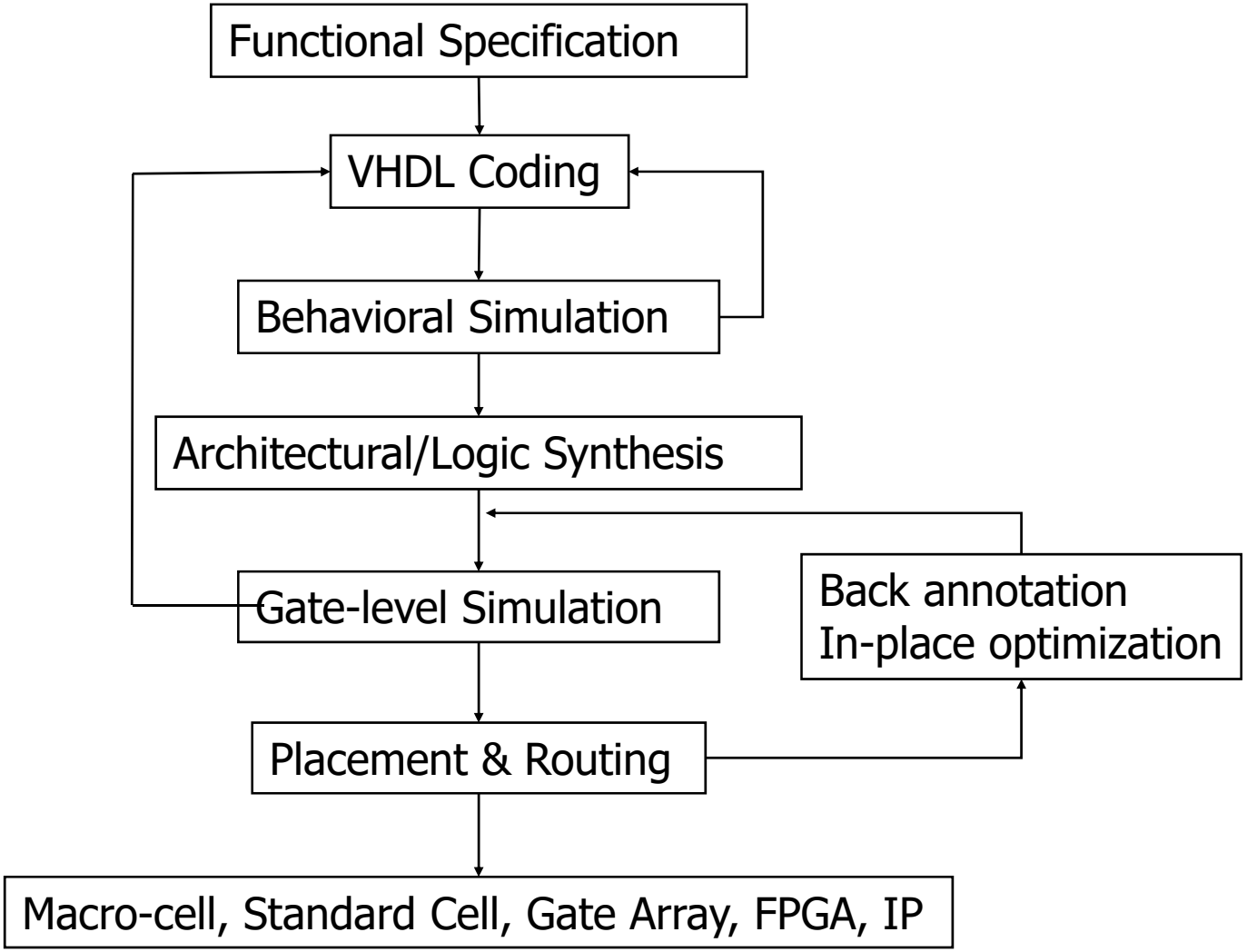
  - 4 categories of processes:
    1. Pattern transfer (lithograph)
    2. Selective removal of material (etching)
    3. Addition of material layers
    4. Addition & activation of impurities

Pentium 4 microprocessor die and 8-inch wafer

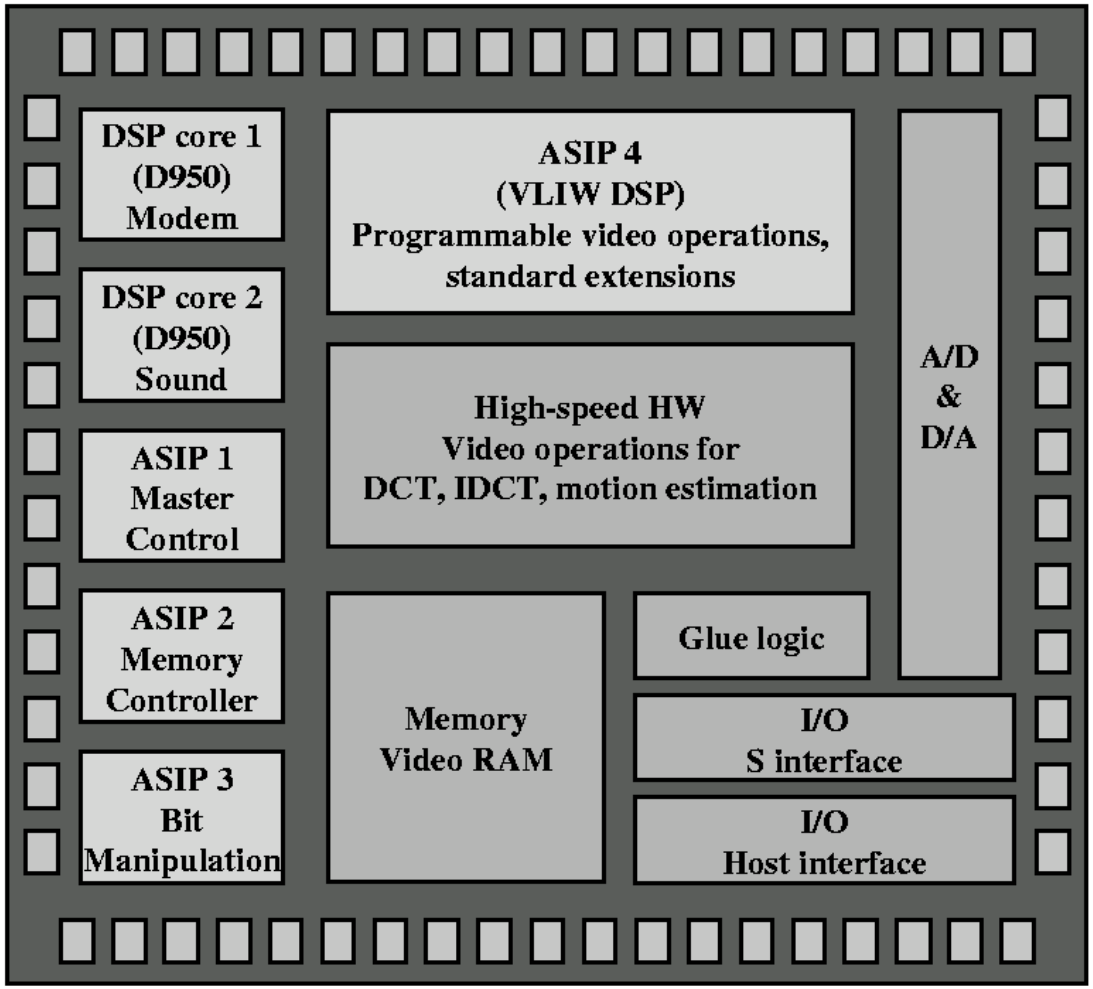




Design Flow Example



System-On-Chip



Circuit Design Constraints

- Performance
  - Timing models (RC delay, table model, non-linear equations)
- Area
  - Size shrinks due to technology improvement
- Power
  - 3 types of power consumption
    - Dynamic
    - Short circuit
    - Leakage
- Testability
- Design time
- Cost
- Yield

Performance constraint

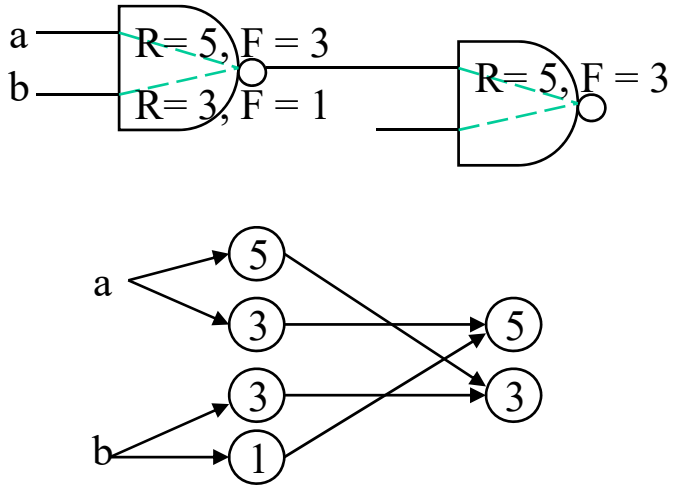
- Timing analysis
  - Entire chip
  - Critical path
  - Block
  - Latch (setup and hold time)
- 3 levels of analysis
  - Transistor(Switch)-Level , Logic(Gate)-Level, High-Level

- High Level Analysis
  - directly operate on the internal representation of the behavioral specifications, so it is quite obvious that the chosen formulation style has a lasting effect to later design steps and to the final result.

Performance analysis – Gate level

Finding circuit delay from input pin to output pin

- Graph-based formulation
  - Convert circuit into a graph
  - One node per pin
  - Weight is delay from pin in to pin out



Power

Hot chips

DEC Alhpa 72W, Pentimum Pro 40W

Next Generation uP chip - 100W

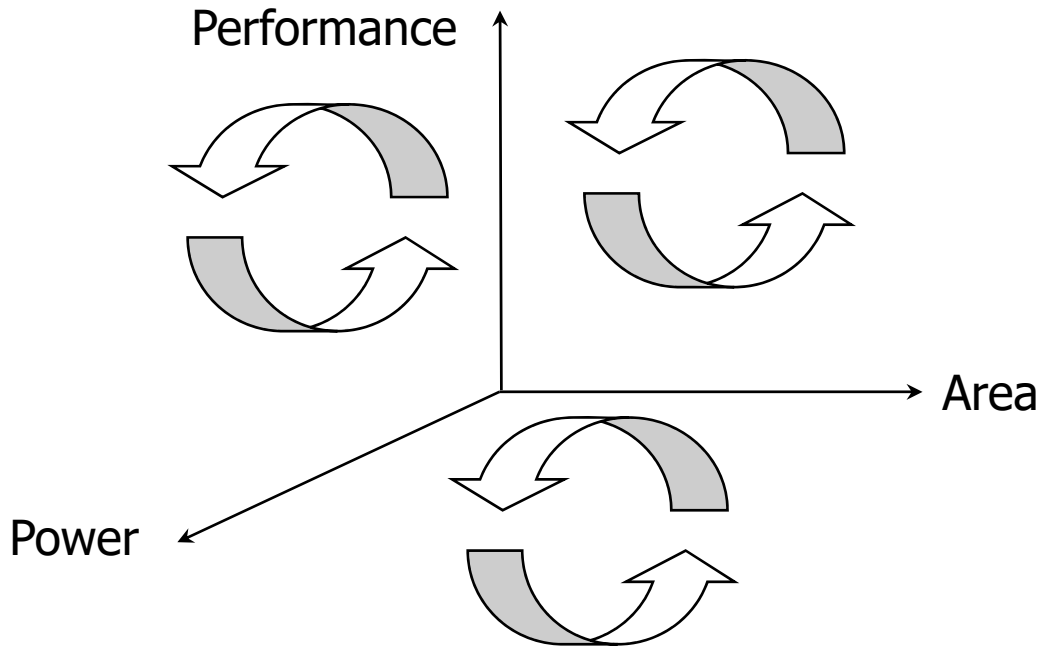
- Performance degradation
- Reduction in chip lifetime
- Cost of specialized sinks/packaging

Portable Electronics

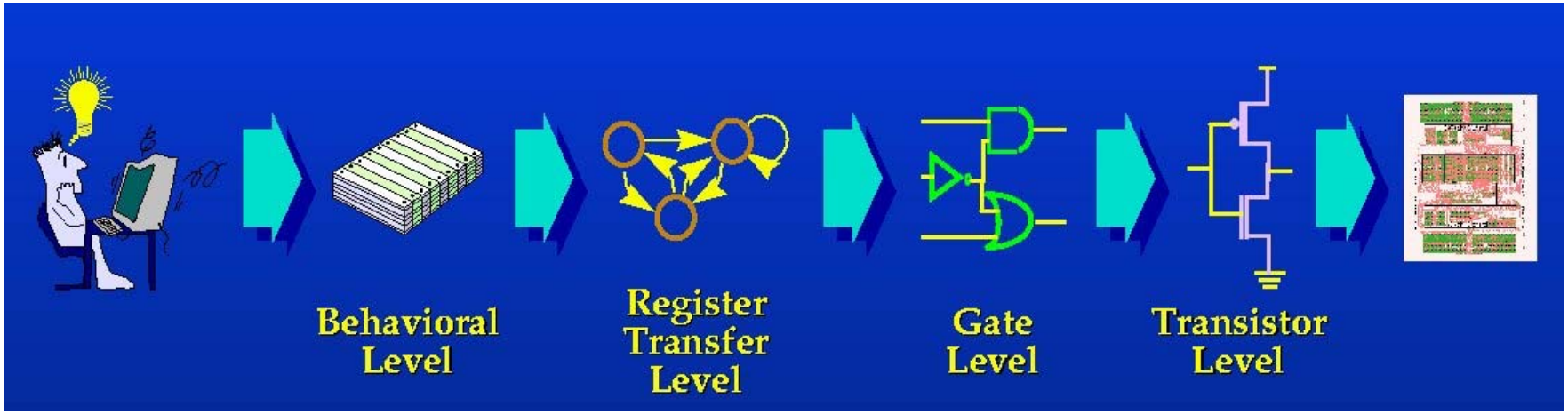
- Low battery life
- Reliability and performance issues
- Expensive packaging required

Power

Power as a design constraint in mobile embedded system



Computer aided design for power



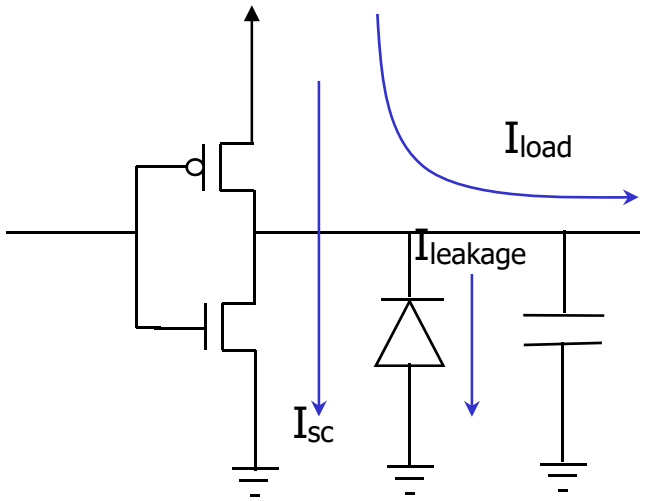
Power oriented design philosophy.

- Estimation
- Optimizaiton

Techniques for estimation and optimization at every stage of design flow.

Source of power consumption

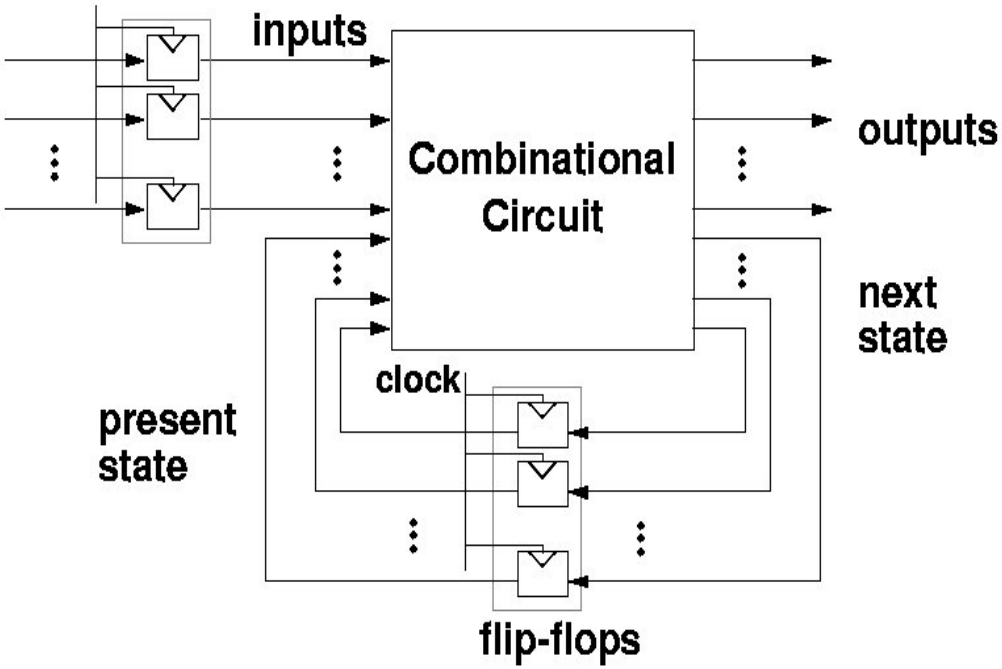
- Dynamic Power Consumption
  - Charging and Discharging Capacitors
- Short Circuit Currents
  - short circuit path between supply rails during switching
- Leakage
  - Leaking diodes and transistors



$$P = 0.5\, C\, V_{DD}^2\, f\, N + Q_{SC}\, V_{DD}\, f\, N + I_{leak}\, V_{DD}$$

F : frequency of clocking
N: number of times gate switches in a clock cycle

Gate-level power estimation



Dynamic power estimation

$$\text{Power} = \text{Energy/transition} * \text{transition rate}$$

$$= C_L * V_{dd}^2 * f_{0\to1}$$

$$= C_L * V_{dd}^2 * P_{0\to1} * f$$

$$= C_{EFF} * V_{dd}^2 * f$$

Power Dissipation is Data Dependent
Function of *Switching Activity*

$$C_{EFF} = \text{Effective Capacitance} = C_L * P_{0\to1}$$