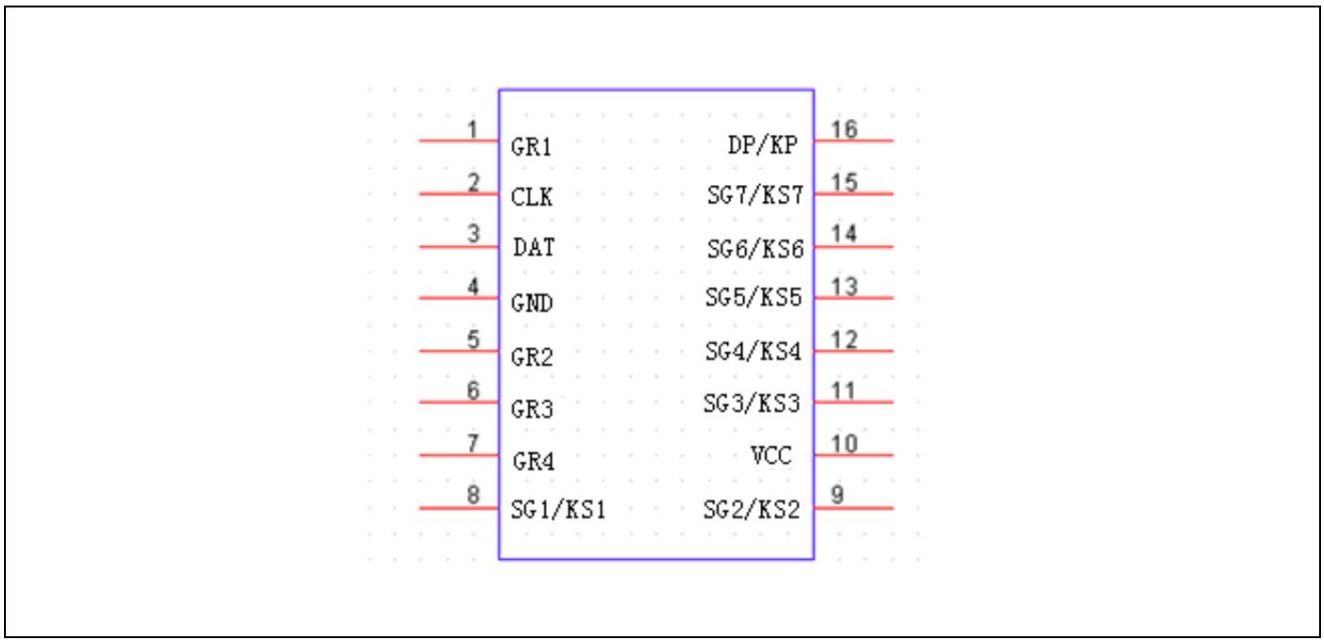
LED driver control/keyboard scanning ASIC

Overview

UMW ET6226M is a special circuit for LED drive control with keyboard scanning circuit interface. Internal integrated MCU input and output control Circuits for digital interface, data latch, LED driver, keyboard scan, brightness adjustment, etc. The chip has stable performance, reliable quality, and strong anti-interference ability, and can be adapted to applications that work continuously for 24 hours for a long time.

Features

z Display mode: 8 segments × 4 bits z segment drive current not less than 25mA, word drive current not less than 150mA z Provide 8-level brightness control z Keyboard scanning: 7 × 4bit z High-speed two-wire serial interface z Built-in clock oscillator circuit z Built-in power-on reset circuit, support 3V-5.5V power supply voltage, provide DIP16 (UMW ET6226P) and SOP16 (UMW ET6226M) package pin layout



Pin Description

symbol	pin name	illustrate
SG1/KS1~ SG7/KS7	Segment Drive Output/Key Scan Input	LED segment driver output, active high, Also used as key scan input, active high, built-in pull-down
GR1ÿGR4	Bit/Key Scan Output	LED bit driver output, active low, Also used as keyboard scan output, active high
DP/KP	Segment/Bit	LED segment output, also used as keyboard logo output
CLK	Output Clock	Data clock input for I2C serial interface, built-in pull-up resistor
WHICH	Input Data Input/	I2C serial interface data input and output, built-in pull-up open-drain mode
VCC	Output Power	3ÿ5.5V
GND	Ground	ground

Function Description

I ^{2}C bus interface

Through the DAT and CLK serial signals, it is possible to transmit signals to and from the MCU. Therefore, DAT and CLK constitute UMW6226

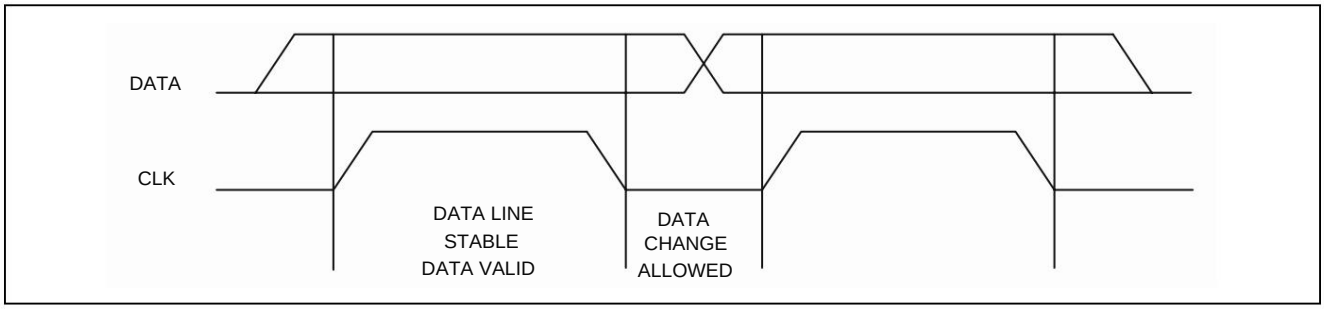
I ^{2}C bus interface.

Data Signal

When the CLK signal is high, the signal on DAT is considered to be a correct and stable signal. And when the CLK signal is low,

The signal on DAT can do high and low level conversion.

As shown below:

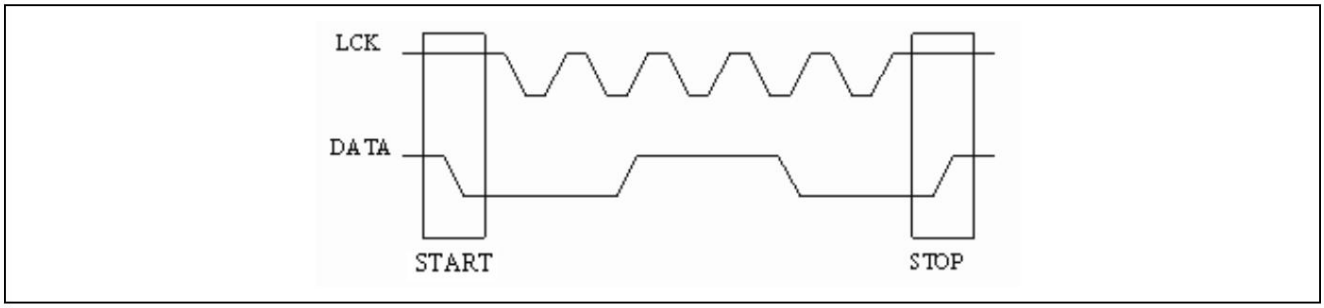


Start and End Conditions

Serial signal transfer "starts" when the CLK signal is high and the DAT signal transitions from high to low.

When the CLK signal is high and the DAT signal is switched from low to high, the serial signal transmission is "end".

As shown below:



Command signal format

The command signal format of the DAT line has eight bits (bit), and each command signal needs to be followed by a "confirmation" signal, and the maximum symbol is used.

The number bit "MSB" is sent out first.

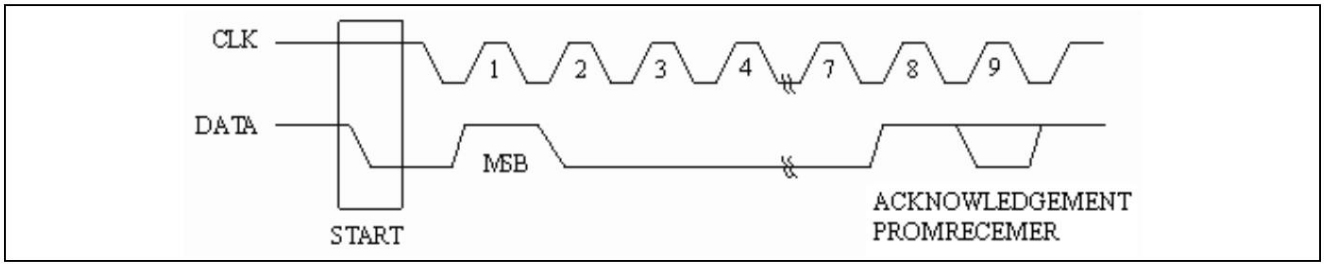
"Acknowledge" signal format (Acknowledge)

In the ninth clock cycle, the MCU first sets the DAT bus to a high-impedance state. If the UMW ET6226M confirms this signal, the DAT bus

It will be pulled low by UMW ET 6226M to keep the DAT bus in a stable low state. As shown below:

UMW ET6226M will generate an "acknowledgment" signal after receiving each command signal, otherwise, at the ninth clock pulse

(CLOCK) time will remain high.



Transmission without "Acknowledge"

Signal If you want to omit the detection of "Acknowledge" signal by UMW ET6226M, a simple transmission method can be used. The method is that after UMW ET6226M receives a group of command signals, it waits for a clock pulse without confirmation. If this method is used, it is likely to cause transmission input error, and will reduce the anti-interference ability.

UMW ET6226M control program format

The UMW ET6226M control program format is shown in the figure below, and the command shown in the figure below is SYSON.

Start 0		1	0 0 1	0 0 0 Ack	0 0 0	0 0 0 0											1 Ack	Stop		

The specific control instructions are shown in the table

below. upper **8** bits	lower **8** bits	Function
48	00	off display on
48	01	display (eight-segment mode) on
48	09	display (seven-segment mode)
48	04	enable sleep
48	X1	Turn on display, keyboard, X-level brightness X=1, first-level brightness; X=4, fourth-level brightness; X=0, eight-level brightness, The rest are like this
68	XX	Digital tube bit 0 is displayed, XX is 8-bit data, and the highest bit is punctuation
6A	XX	Digital tube bit 1 display, XX is 8-bit data, the highest bit is punctuation
6C	XX	Digital tube position 2 display, XX is 8-bit data, the highest bit is punctuation
6E	XX	Digital tube position 3 display, XX is 8-bit data, the highest bit is punctuation
4F	-	Get key, return key code

key code

	GR1	GR2	GR3	GR4
SG1/KS1	44H	45H	46H	47H
SG2/KS2	4 ONLY	4DH	4 EH	4FH
SG3/KS3	54H	55H	56H	57H
SG4/KS4	5CH	5DH	5EH	5FH
SG5/KS5	64H	65H	66H	67H
SG6/KS6	6CH	6DH	6EH	6FH
SG7/KS7	74H	75H	76H	77H

Limit parameters (Ta = 25ÿ)

Parameters	symbol	scope	unit
Supply voltage	VCC	-0.5 ÿ +6.5	IN
Input voltage	WE	-0.5 ÿ VCC + 0.5	IN
Operating	Top	-40 ÿ +85	ÿ
temperature Storage temperature	Tstg	-55 ÿ +125	ÿ

Electrical parameters (test conditions: Ta = 25°C, VCC = **5V)**

Parameters	Symbol	Minimum	Typical	Maximum	Unit
Supply voltage	VCC	3		5	5.5 IN
Supply current	IC			80	150 mA
Quiescent current (CLK, DAT, KP high) Sleep current	ICs			0.3	0.6 mA
(CLK, DAT, KP high)	ICslp			0.05	0.1 mA
CLK and DAT pins low-level input voltage	WILL	-0.5			0.8 IN
CLK and DAT pins high input voltage	HIV	2.0			VCC+0.5 IN
KS pin low level input voltage	WOLVES	-0.5			0.5 IN
KS pin high level input voltage	WHICH	1.8			VCC+0.5 IN
GR pin low level output voltage (-200mA)	VIOLENT				1.2 IN
GR pin low level output voltage (-100mA)	VIOLENT				0.8 IN
GR pin high level output voltage (5mA)	VOHdig	4.5			IN
KS pin low level output voltage (-20mA)	Volki				0.5 IN
KS pin high level output voltage (20mA)	VOHk	4.5			IN
KS pin input pull-down current	IDN1	-30		-50	-90 uA
CLK pin input pull-up current	IUP1	100		200	300 uA
DAT pin input pull-up current	IUP2	150		300	400 uA
KP pin output pull-up current	IUP3	500		2000	5000 uA
default voltage threshold for power-on reset	VR	2.3		2.6	2.9 IN

Internal timing parameters (test conditions: Ta = 25°C, VCC = 5V)

parameter	symbol	minimum	typical	Maximum	unit
Reset time TPR generated by power-on detection Display scan		10	25	60	ms
period	TP	4	8	20	ms
Keyboard scan interval, key response time TKS Note: The timing		20	40	80	ms

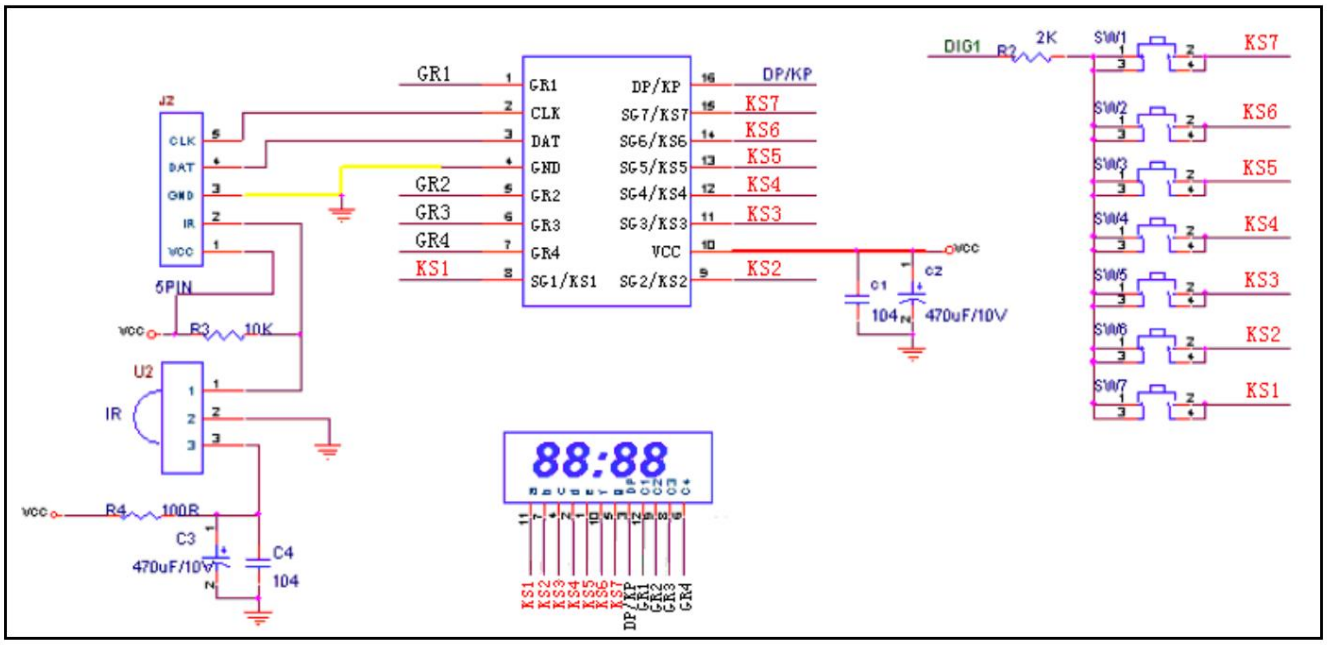
parameters of this table are multiples of the built-in clock cycle, and the built-in clock frequency decreases with the decrease of the power supply voltage.

Interface Timing Parameters (Test Condition: Ta = 25ÿ, VCC =5V) Parameters

	Symbol Minimum	Typical Maximum	Unit		
DAT falling edge start signal setup time	TSSTA	100			ns
DAT falling edge start signal hold time	THSTA	100			nS
DAT rising edge stop signal setup time	TSSTO	100			ns
DAT rising edge stop signal hold time	THSTO	100			ns
Low level width of CLK clock signal	TCLOW	100			nS
High level width of CLK clock signal	TCHIG	100			nS
DAT input data to CLK rising edge setup time TSDA		30			nS
DAT input data hold time THDA to the rising edge of CLK		10			nS
DAT output data valid to CLK falling edge delay TAA		2		30	nS
DAT Output Data Invalid Delay to CLK Falling Edge TDH Average Data Rate		2		40	nS
	Rate	0		4M	bps

Note: The measurement unit of this watch is 10-9 in nanoseconds. If the maximum value is not specified, the theoretical value can be infinite.

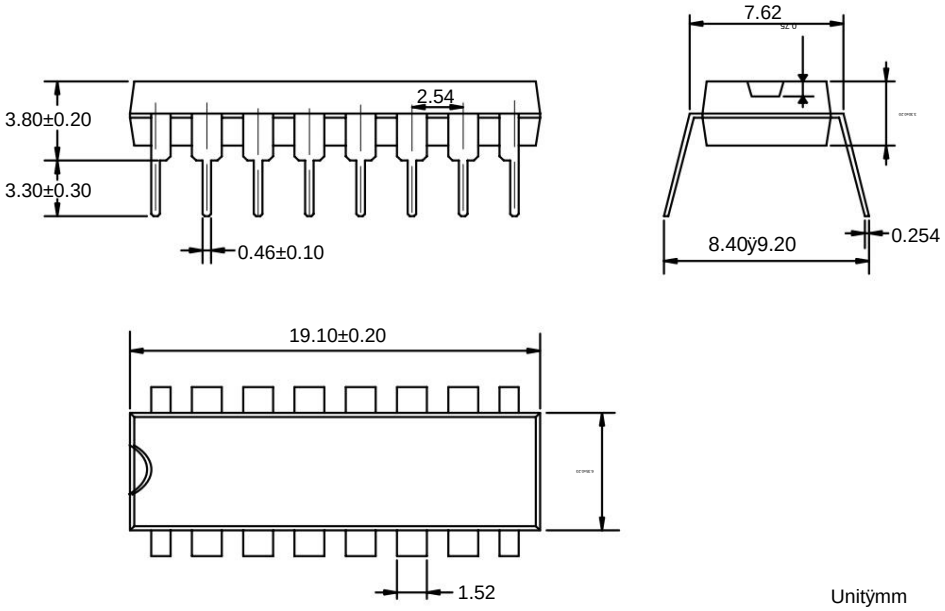
Refer to the application circuit diagram



*: This circuit is for reference only.

Package size

DIP16



SOP16