# CA-IS3050 Isolated CAN Transceiver

## 1 Product Features

• Compliant with ISO11898-2 standard • Up to 5000VRMS isolation withstand voltage • Logic side I/O voltage range supports 2.5V ~ 5 V • Signal transfer rate up to 1 Mbps • High common mode transient immunity: 100 kV/ÿs (typ. ) • –40 V to 40 V bus fault protection • Low loop delay: – 150 ns (typ) – 210 ns (max) • Drive (TXD) master dynamic timeout function • Thermal shutdown protection • Bus maximum Supports 110 nodes • Unpowered nodes do not interfere with the bus • Temperature range: –40°C to 125°C • Safety and Regulatory Approvals (pending): VDE Approval to 61010-1 – UL 1577 Compliant, 5 kVRMS for 1 minute – Certified according to IEC 60950-1, IEC 61010-1 and IEC 60601-1 – TUV 5kVRMS reinforced insulation according to EN/UL/CSA 60950-1 approval – CQC reinforced insulation according to GB4843.1-2011

## 2 applications

• CAN Data Bus • Industrial Field Networks • Building and Greenhouse Environment Control Automation • Security Systems • Transportation • Medical • Telecommunications

## 3 Overview

The CA-IS3050 is an isolated Control Area Network (CAN) physical layer transceiver that complies with the technical specifications of the ISO11898-2 standard. This device uses Using on-chip silicon dioxide (SiO2) capacitors as an isolation layer creates a fully isolated interface between the CAN protocol controller and the physical layer bus, used with isolated power supplies to isolate noise and interference and prevent damage to sensitive circuits.

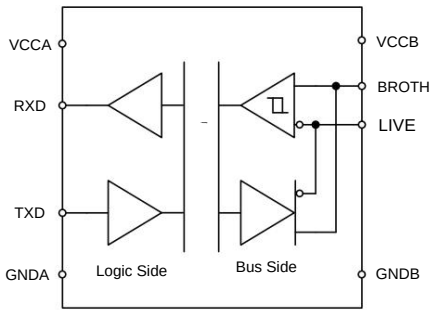
CA-IS3050 can provide differential receiving and differential transmitting capabilities for CAN protocol controller and physical layer bus respectively, and the signal transmission rate can reach up to 1 Mbps. The device features current-limiting, overvoltage and ground loss protection (–40 V to 40 V), thermal shutdown to protect against output short circuits, and a common-mode voltage range of –12 V to 12 V.

The CA-IS3050 is rated from –40°C to 125°C and is available in wide-body SOIC8 and wide-body SOIC16 packages.

Device Information

| Part number | Package | Package size (nominal) |
|---|---|---|
| CA-IS3050 | SOIC8-WB(G) | 5.85 mm × 7.50 mm |
| | SOIC16-WB(W) | 10.30 mm × 7.50 mm |

Simplified functional block diagram



## 4Ordering Guide

Table 4-1 Valid Ordering Part Numbers

| model | VCC1ÿVÿ | VCC2ÿVÿ | transfer speed ÿKbpsÿ | Rated withstand voltage (V) | package |
|---|---|---|---|---|---|
| CA-IS3050G | 2.5~5.5 | 4.5~5.5 | 1000 | 5000 | SOIC8-WB |
| CA-IS3050GE | 2.5~5.5 | 4.5~5.5 | 1000 | 2500 | SOIC8-WB |
| CA-IS3050W | 2.5~5.5 | 4.5~5.5 | 1000 | 5000 | SOIC16-WB |
| CA-IS3050WE | 2.5~5.5 | 4.5~5.5 | 1000 | 2500 | SOIC16-WB |

Table of contents

**5** -pin configuration and functional description

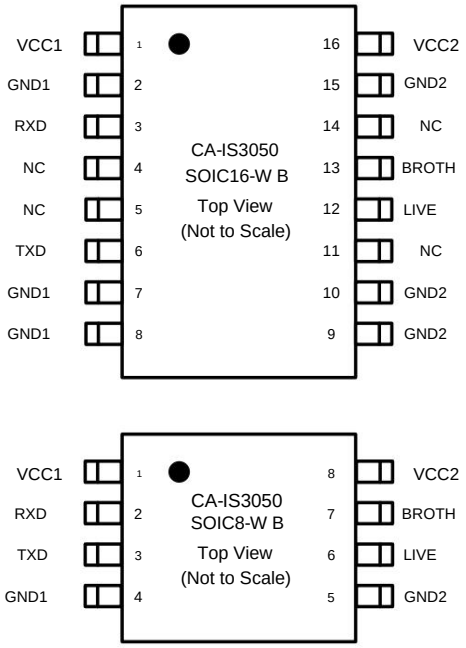



Figure **5-1** Pin Configuration

Table **5-1** Pin function description

| pin name | pin number | | type | describe |
|---|---|---|---|---|
| | SOIC16 | SOIC8 | | |
| VCC1 | 1 | 1 | power | Logic side power input |
| GND1 | 2 | - | | ground, logic side |
| RXD | 3 | 2 | ground | receiver output data |
| NC | 4 | - | output | Do not connect, do not connect this pin |
| NC | 5 | - | no | Do not connect, do not connect this pin |
| TXD | 6 | 3 | input | drive input data |
| GND1 | 7 | 4 | | ground, logic side |
| GND1 | 8 | - | | ground, logic side |
| GND2 | 9 | 5 | | ground, bus side |
| GND2 | 10 | - | | ground, bus side |
| NC | 11 | - | ground no | Do not connect, do not connect this pin |
| LIVE | 12 | 6 | Input/output low level CAN voltage input/output | |
| BROTH | 13 | 7 | Input/output high level CAN voltage input/output | |
| NC | 14 | - | | Do not connect, do not connect this pin |
| GND2 | 15 | - | | ground, bus side |
| VCC2 | 16 | 8 | groundless power | Bus side power input |

## 6.1 Absolute Maximum **Ratings1**

| parameter | | Min Max Unit | | |
|---|---|---|---|---|
| VCC1 or VCC2 | Supply Voltage | –0.5 | 6.0 | IN |
| WE | 2 Logic Side Input Voltage (TXD) Bus | –0.5 | VCC1 + 0.53 | IN |
| VCANH or VCANL | Side Voltage (CANH, CANL) Receiver Output | –40 | 40 | IN |
| IO | Current Junction Temperature Storage | –15 | 15 | mA |
| TJ | Temperature Range | | 150 | °C |
| TSTG | | –65 | 150 | °C |

Remark:

1. Equal to or exceeding the above absolute maximum ratings may cause permanent damage to the product. These are rated maximum values only and should not be used at these conditions or at any other

   It is inferred that the product will operate normally under the conditions of the specifications shown in the Operational Section. Exposure to conditions beyond the maximum ratings for extended periods of time may affect product reliability.

2. All input/output logic voltages are measured with respect to logic side ground GND1, and differential bus voltages are measured with respect to bus side ground GND2.

3. The maximum voltage must not exceed 6 V.

## 6.2 **ESD** rating

| | | Numerical unit | |
|---|---|---|---|
| VESD electrostatic discharge | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pin 1 Device Charge Model | ±4000 | IN |
| | (CDM), per JEDEC specification JESD22-C101, all pin 2 | ±1500 | |

Remark:

1. JEDEC document JEP155 specifies that 500V HBM can be manufactured safely with standard ESD control procedures.

2. JEDEC document JEP157 specifies that 250V CDM allows safe manufacturing using standard ESD control processes.

## 6.3 Recommended working conditions

| parameter | | | Min Typ Max Units | | | |
|---|---|---|---|---|---|---|
| VCC1 | Logic Side Supply Voltage | | 3 | 3.3 | 5.5 | IN |
| VCC2 | Bus Side Supply Voltage | | 4.5 | 5 | 5.5 | IN |
| VI or VIC | Bus Pin Voltage (Single-Ended or Common | | –12 | | 12 | IN |
| HIV | Mode) Input High Voltage Input Low Voltage | Drive (TXD) Drive | 2 | | VCC1 + 0.3 | IN |
| WILL | Differential Input Voltage | (TXD) | –0.3 | | 0.8 | IN |
| AT | | | –7 | | 7 | IN |
| John | output high level current | Driver Receiver Driver | –70 | | | mA |
| | | Receiver | –2 | | | |
| IOL | output low level current | | | | 70 | mA |
| | | | | | 2.5 | |
| PER | Ambient temperature | | –40 | | 125 | °C |
| TJ | Junction temperature | | –40 | | 150 | °C |
| PD | Total power | VCC1 = 5.5VўVCC2 = 5.25VўTA = 125°Cў | | | 200 | mW |
| PD1 | consumption Logic side | RL = 60ў, TXD input signal is 500 kHz square | | | 25 | mW |
| PD2 | power consumption Bus | Wave (50% duty cycle) | | | 175 | mW |
| side power consumption TJ(shutdown) Thermal shutdown temperature | | | 155 | 165 | 180 | °C |

1 Note:

1. Operation beyond thermal shutdown temperature may affect device reliability.

## 6.4 Thermal properties

| Heat Meter | | SOIC8-WB | SOIC16-WB unit | |
|---|---|---|---|---|
| RўJA | Chip Junction to Ambient Thermal Resistance Chip | 110.1 | 86.5 | °C/W |
| RўJC(top) | Junction to Case (Top) Thermal Resistance Chip | 51.7 | 49.6 | °C/W |
| RўJB | Junction to Board Thermal Resistance Chip Junction | 66.4 | 49.7 | °C/W |
| ўJT | to Top Characteristics Chip Junction to Board | 16.0 | 32.3 | °C/W |
| ўJB | Characteristics Chip Junction to Case (Bottom) | 64.5 | 49.2 | °C/W |
| RўJC(bottom) | Thermal Resistance | n/a | n/a | °C/W |

## 6.5 isolation characteristics

**6.5.1** Isolation characteristics: **5 kVRMS** class

| parameter | Test Conditions | Numerical value | unit |
|---|---|---|---|
| **IEC 60664-1** | | | |
| CLR External Air Gap (Gap) 1 | Measure the input end to the output end, the shortest distance from | 8 | mm |
| CPG external creepage distance1 | the input end to the output end, and the shortest distance along the | 8 | mm |
| DTI isolation distance | housing Minimum internal clearance (internal distance) | 14 | ym |
| CTI Relative Leakage Index Materials Group | DIN EN 60112 (VDE 0303-11); IEC 60112 according to IEC | > 600 | IN |
| | 60664-1 Rated mains voltage ÿ 300 VRMS Rated mains voltage | | |
| IEC 60664-1 Overvoltage Category | ÿ 400 VRMS Rated mains voltage ÿ 600 VRMS | I-IV | |
| | | I-IV | |
| | | I-III | |
| **DIN V VDE V 0884-10 (VDE V 0884-10):2006-122** | | | |
| VIORM Maximum Repetitive Peak Isolation Voltage | AC voltage (bipolar) | 1414 | VPK |
| VIOTM maximum transient isolation voltage | VTEST = VIOTM,<br>t = 60 seconds (authentication);<br>VTEST = 1.2 × VIOTMÿ<br>t = 1 second (100% production tested) | 7070 | VPK |
| qpd Characterizing Charge 3 | Method b1, routine testing (100% production tested) and pre-processing (sampling<br>sample test)<br>Vini = 1.2 × VIOTMÿ tini = 1 s<br>Vpd(m) = 1.875 × VIORM, tm = 1 second | ÿ 5 | pC |
| CIO Gate Capacitance, Input to Output 4 | VIO = 0.4 × sin (2ÿft),f = 1MHz VIO = 500 V,TA = | 2 | pF |
| RIO insulation resistance 4 | 25°C | > 1012 | Oh |
| | VIO =500Vÿ100°C ÿ TA ÿ 125°C | > 1011 | |
| | VIO = 500 V at TS = 150°C | > 109 | |
| Pollution degree | | 2 | |
| **UL 1577** | | | |
| VISO maximum isolation voltage | VTEST = VISO, t = 60 seconds (authentication);<br>VTEST = 1.2 × VISO, t = 1 second (100% production tested) | 5000 | VRMS |

Remark:

1. Apply creepage and clearance requirements according to the application-specific equipment isolation criteria. Care should be taken to maintain board design creepage and clearance distances to ensure isolators on the printed circuit board mounting pads will not reduce this distance. Creepage distances and clearances on printed circuit boards become equal in some cases. Techniques such as inserting grooves in printed circuit boards are used to help help increase these specifications.
2. This isolator is suitable for basic electrical isolation within the safety limit data, and safety ratings must be ensured by appropriate protective circuitry.
3. The characterizing charge is the discharge charge (pd) caused by partial discharge.
4. All pins on both sides of the gate are connected together to form a two-terminal device.

## 6.5.2 Isolation Characteristics : 2.5 kVRMS level

| parameter | Test Conditions | Numerical value | unit |
|---|---|---|---|
| **IEC 60664-1** | | | |
| CLR External Air Gap (Gap) 1 | Measure the input end to the output end, the shortest distance from | 8 | mm |
| CPG external creepage distance1 | the input end to the output end, and the shortest distance along the | 8 | mm |
| DTI isolation distance | housing Minimum internal clearance (internal distance) | 14 | ÿm |
| CTI Relative Leakage Index Materials Group | DIN EN 60112 (VDE 0303-11); IEC 60112 according to IEC | > 600 | IN |
| | 60664-1 Rated mains voltage ÿ 300 VRMS Rated mains voltage | | |
| IEC 60664-1 Overvoltage Category | ÿ 400 VRMS Rated mains voltage ÿ 600 VRMS | I-IV | |
| | | I-IV | |
| | | I-III | |
| **DIN V VDE V 0884-10 (VDE V 0884-10):2006-122** | | | |
| VIORM Maximum Repetitive Peak Isolation Voltage | AC voltage (bipolar) | 707 | VPK |
| VIOTM maximum transient isolation voltage | VTEST = VIOTM,<br>t = 60 seconds (authentication);<br>VTEST = 1.2 × VIOTMÿ<br>t = 1 second (100% production tested) | 3535 | VPK |
| qpd Characterizing Charge 3 | Method b1, routine testing (100% production tested) and pre-processing (sampling<br>sample test)<br>Vini = 1.2 × VIOTMÿ tini = 1 s<br>Vpd(m) = 1.875 × VIORM, tm = 1 second | ÿ 5 | pC |
| CIO Gate Capacitance, Input to Output 4 | VIO = 0.4 × sin (2ÿft),f = 1MHz VIO = 500 V,TA = | 2 | pF |
| RIO insulation resistance 4 | 25°C | > 1012 | Oh |
| | VIO =500Vÿ100°C ÿ TA ÿ 125°C | > 1011 | |
| | VIO = 500 V at TS = 150°C | > 109 | |
| Pollution degree | | 2 | |
| **UL 1577** | | | |
| VISO maximum isolation voltage | VTEST = VISO, t = 60 seconds (authentication);<br>VTEST = 1.2 × VISO, t = 1 second (100% production tested) | 2500 | VRMS |

Remark:

1. Apply creepage and clearance requirements according to the application-specific equipment isolation criteria. Care should be taken to maintain board design creepage and clearance distances to ensure isolators on the printed circuit board mounting pads will not reduce this distance. Creepage distances and clearances on printed circuit boards become equal in some cases. Techniques such as inserting grooves in printed circuit boards are used to help help increase these specifications.
2. This isolator is suitable for basic electrical isolation within the safety limit data, and safety ratings must be ensured by appropriate protective circuitry.
3. The characterizing charge is the discharge charge (pd) caused by partial discharge.
4. All pins on both sides of the gate are connected together to form a two-terminal device.

## 6.6 Relevant safety certification

| VDE (pending) | CSA (pending) | UL (pending application) | CQC (applying) | TUV (pending application) |
|---|---|---|---|---|
| according to DIN V VDE V 0884-11:2017-01 Certification | certified according to IEC60950-1, IEC 62368-1 and IEC 60601-1 certificate | UL1577 Device Certification Program Certification | according to GB4843.1-2011 Certification | according to EN61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013 Certification |
| | | | | |

## 6.7 Microelectronics Co., Ltd.

All voltages are referenced to their respective grounds, 3 V ÿ VCC1 ÿ 5.5 V, and 4.5 V ÿ VCC2 ÿ 5.5 V, unless otherwise noted. All min/max specifications apply over the entire recommended operating range. unless otherwise stated

Note, all typical specifications are measured at TA = 25°C, VCC1 = VCC2 = 5 V.

| parameter | | Test Conditions | Min Typ Max Units | | | |
|---|---|---|---|---|---|---|
| **Supply current** | | | | | | |
| ICC1 logic side supply current | | VI = 0 V or VCC1, VCC1 = 3.3 V VI = 0 V or | | 1.8 | 2.8 | mA |
| | | VCC1, VCC1 = 5 V | | 2.3 | 3.6 | |
| ICC2 bus side supply current | main dynamic | VI = 0 VÿRL = 60 ÿ | | 52 | 73 | mA |
| | passive dynamic | VI = VCC1 | | 8 | 12 | |
| **driver** | | | | | | |
| VO(D) bus output voltage (main dynamic) | BROTH | VI = 0 V, RL = 60 ÿ; see Figure 7-1 Figure 7-2 | 2.9 | 3.4 | 4.5 | IN |
| | LIVE | | 0.8 | | 1.5 | |
| VO(R) bus output voltage (passive) | | VI = 2 V, RL = 60 ÿ; see Figure 7-1 Figure 7-2 | 2 | 2.5 | 3 | IN |
| VOD(D) differential output voltage (main dynamic) | | VI = 0 V, RL = 60 ÿ; see Figure 7-1 Figure 7-2 Figure 7-3 | 1.5 | | 3 | IN |
| | | VI = 0 V, RL = 45 ÿ; see Figure 7-1 Figure 7-2 Figure 7-3 | 1.4 | | 3 | IN |
| VOD(R) differential output voltage (passive) | | VI = 3 V, RL = 60 ÿ; see Figure 7-1 Figure 7-2 | –12 | | 12 | mV |
| | | VI = 3 V, no load | –0.5 | | 0.05 | IN |
| VOC(D) common mode output voltage (main dynamic) | | See Figure 7-7 | 2 | 2.5 | 3 | IN |
| VOC(pp) common mode output voltage peak-to-peak | | | | 0.3 | | IN |
| IIH high level input current, TXD input | | VI = 2V | | | 5 | µA |
| IIL low level input current, TXD input | | VI = 0.8 V | –5 | | | µA |
| IOS(SS) short-circuit steady-state output current | | VCANH = –12 V, CANL open; see Figure 7-10 VCANH = 12 | –105 | –72 | | mA |
| | | V, CANL open; see Figure 7-10 VCANL = –12 V, CANH open; | | 0.36 | 1 | |
| | | see Figure 7-10 VCANL = 12 V, CANH open; see Figure 7-10 | –1 | –0.5 | | |
| | | VI = 0 V or VCC1; see Figure 7-11 | | 71 | 105 | |
| CMTI Common Mode Transient | | | | 100 | | kV/µs |
| **Immunity Receiver** | | | | | | |
| VIT+ positive input threshold voltage | | | | 0.8 | 0.9 | IN |
| VIT - Negative Input Threshold Voltage | | | 0.5 | 0.65 | | IN |
| VHYS input voltage hysteresis window | | | 100 | 125 | | mV |
| VOH output high voltage, VCC1 = 5 V | | IOH = –4 mA; see Figure 7-6 IOH = | VCC1 – 0.8 | 4.6 | | IN |
| | | –20 µA; see Figure 7-6 IOH = –4 mA; | VCC1 – 0.1 | 5 | | |
| VOH output high voltage, VCC1 = 3.3 V | | see Figure 7-6 IOH = –20 µA; see | VCC1 – 0.8 | 3.1 | | IN |
| | | Figure 7-6 IOH = 4 mA; see Figure | VCC1 – 0.1 | 3.3 | | |
| VOL output low voltage | | 7-6 IOH = 20 µA; Figure 7-6 TXD is | | 0.2 | 0.4 | IN |
| | | 3V, VI = 0.4 × sin (2ÿft) + 2.5 V, | | 0 | 0.1 | |
| theme CANH, CANL input capacitance to ground | | f = 1MHz | | 13 | | pF |
| CID Input Differential Capacitor | | TXD is 3V, VI = 0.4 × sin (2ÿft) , f = 1MHz TXD is 3V TXD is 3V | | 5 | | pF |
| RIN CANH, CANL input resistance | | | 15 | 30 | 40 | kÿ |
| RID differential input resistance | | | 30 | | 80 | kÿ |
| RI(m) input resistance matching (1 – [RIN(CANH) / RIN(CANL)]) | | VCANH = VCANL | –5% | 0% | 5% | |
| CMTI Common Mode Transient Immunity | | VI = 0 V or VCC1; see Figure 7-11 | | 100 | | kV/µs |

## 6.8 Timing Characteristics: Devices

All voltages are referenced to their respective grounds, 3 V ÿ VCC1 ÿ 5.5 V, and 4.5 V ÿ VCC2 ÿ 5.5 V, unless otherwise noted. All min/max specifications apply over the entire recommended operating range. unless otherwise stated

Note, all typical specifications are measured at TA = 25°C, VCC1 = VCC2 = 5 V.

| | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| tloop1 total loop delay, driver input to receiver output, passive to active tloop2 total loop | See Figure 7-8 | 110 | | 210 | ns |
| delay, driver input to receiver output, active to passive | | 110 | | 210 | ns |

## 6.9 Timing Characteristics: Drivers and Receivers

Unless otherwise noted, all voltages are referenced to their respective grounds, 3 V ÿ VCC1 ÿ 5.5 V, and 4.5 V ÿ VCC2 ÿ 5.5 V. All min/max specifications apply over the entire recommended operating range. unless otherwise stated

Note that all typical specifications are measured at TA = 25°C, VCC1 = VCC2 = 5 V.

| parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| driver | | | | | |
| tPLH propagation delay, the output changes from passive to active | See Figure 7-4 | 35 | 75 | 130 | ns |
| tPHL propagation delay, output changes from active to passive tr | | 35 | 55 | 100 | |
| differential output signal rise time tf differential output signal fall time | | | 40 | 60 | |
| tTXD_DTO1 master dynamic timeout time | | | 40 | 60 | |
| | CL = 100 pF; see Figure 7-10 | 300 | 450 | 700 | µs |
| | | | | | |
| tPLH propagation delay, output from low to high | See Figure 7-6 | 70 | 110 | 140 | ns |
| tPHL propagation delay, the output changes from high level to low level | | 55 | 80 | 100 | |
| tr output signal rise time tf output signal fall time Remarks: | | | | 6 | |
| | | | | 6 | |

1. Once the driver enters the main dynamic for more than tTXD_DTO, the main dynamic timeout function will turn off the driver to release the bus into the passive dynamic, preventing the bus from being locked locally.

on the main dynamic. The drive can only resume the function of transmitting the main dynamic after entering the passive dynamic.

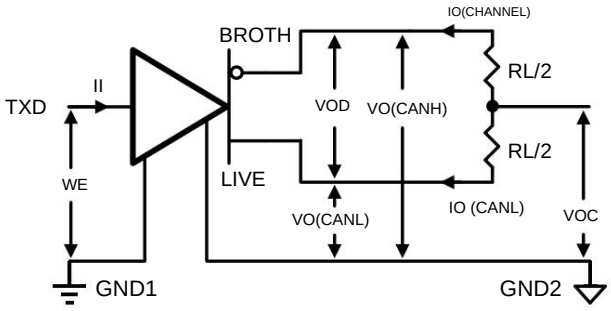



Figure **7-1** Definition of driver voltage and current

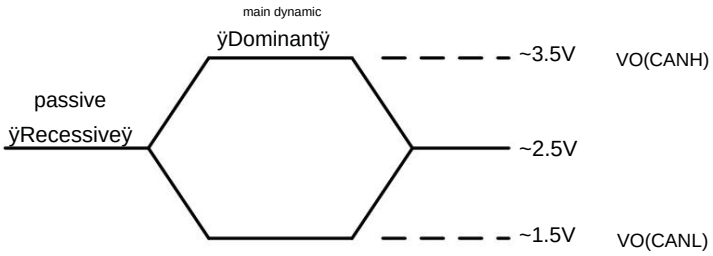



Figure **7-2** Definition of bus logic state voltage

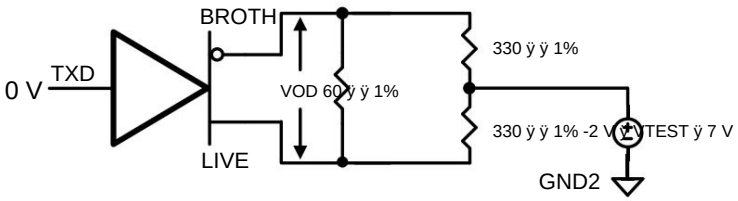
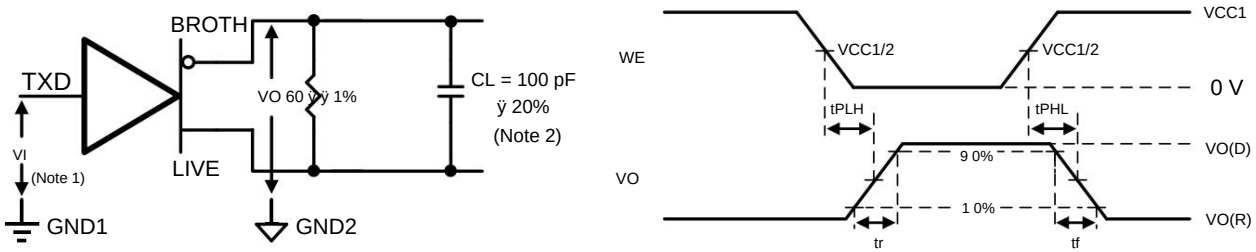



Figure **7-3** Driver **VOD** voltage measurement circuit with common mode load




Remarks: 1. The input pulse generated by the signal source has the following requirements: pulse repetition rate PRR ÿ 125 kHz, 50% duty cycle, rise time tr ÿ 6 ns, fall time tf ÿ 6 ns, output impedance ZO = 50 ÿ; 2 . Load capacitance CL includes the parasitic capacitance of the instrument and fixture.

Figure **7-4** Driver measurement circuit and voltage waveform

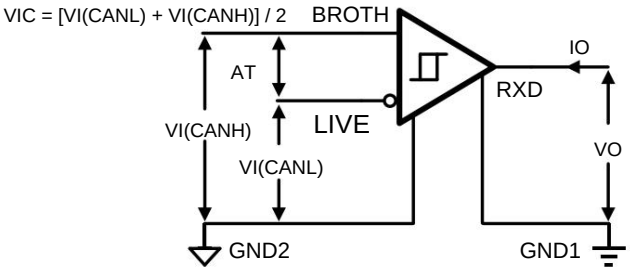
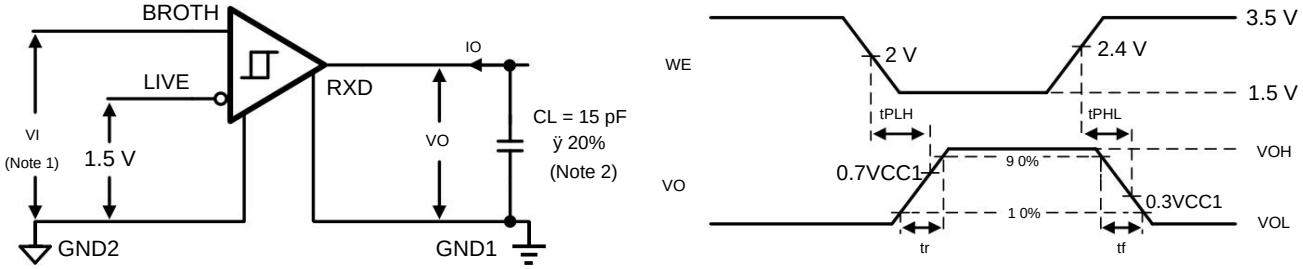



Figure **7-5** Receiver Voltage and Current Definitions




Remarks: 1. The input pulse generated by the signal source has the following requirements: pulse repetition rate PRR ÿ 125 kHz, 50% duty cycle, rise time tr ÿ 6 ns, fall time tf ÿ 6 ns, output impedance ZO = 50 ÿ; 2 . Load capacitance CL includes the parasitic capacitance of the instrument and fixture.

Figure **7-6** Receiver Measurement Circuit and Voltage Waveforms

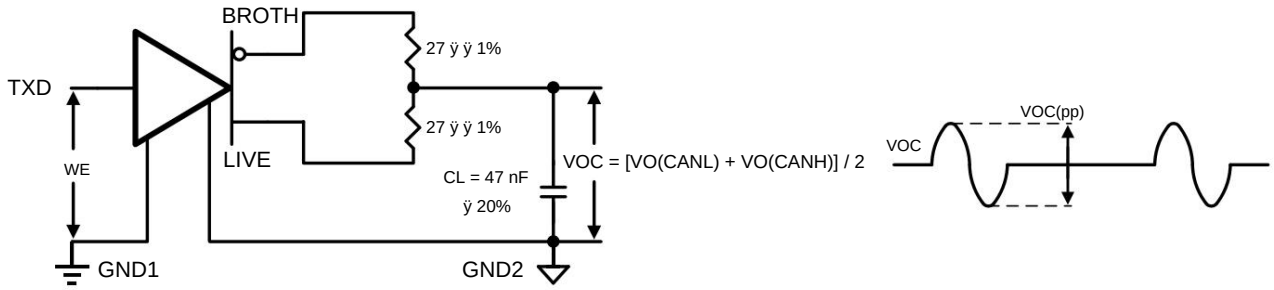



Figure **7-7** Common mode output voltage peak-to-peak measurement circuit and waveform

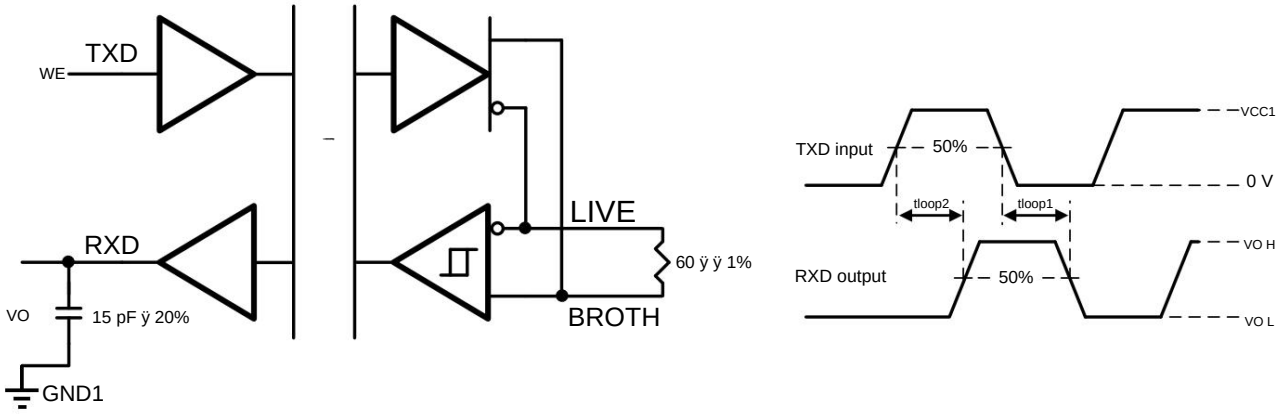
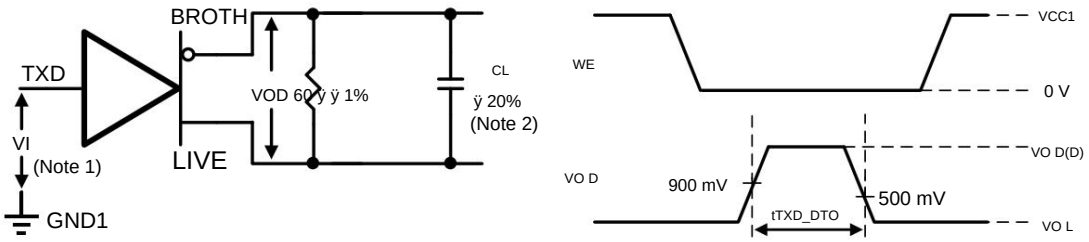



Figure **7-8 tloop** measurement circuit and voltage waveform




Remarks:

1. The input pulse generated by the signal source has the following requirements: the rise time tr ÿ 6 ns, the fall time tf ÿ 6 ns, and the output impedance ZO = 50 ÿ; 2. The load capacitance CL includes the instrument.

Figure **7-9** Main Dynamic Timeout Function Measurement Circuit and Voltage Waveforms

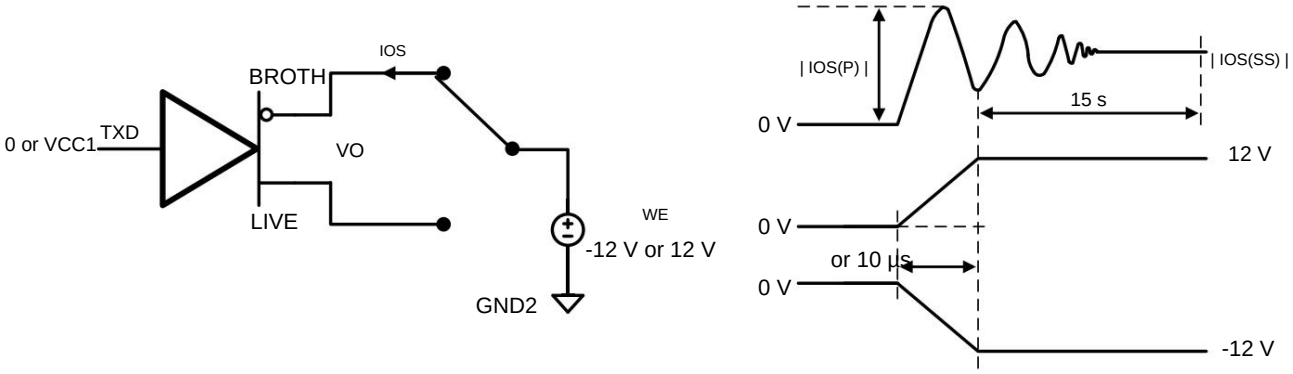



Figure **7-10** Output short circuit current measurement circuit and waveform

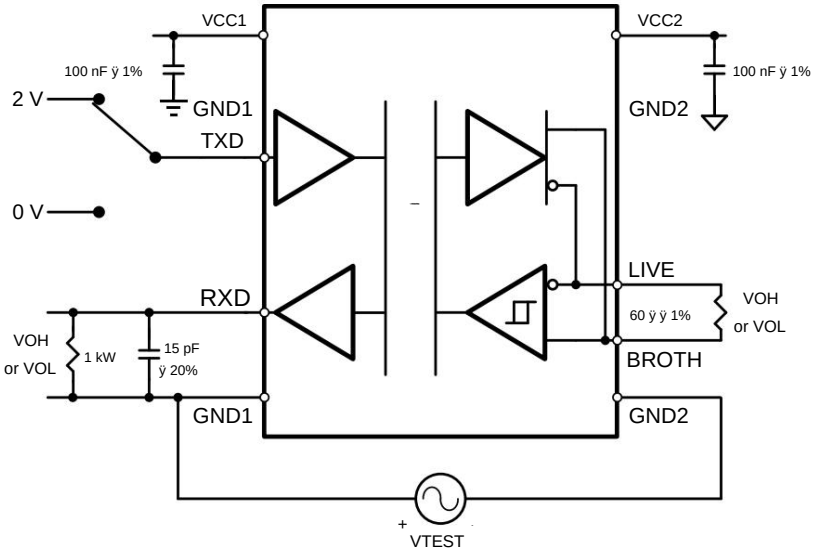



Figure **7-11** Common mode transient immunity measurement circuit

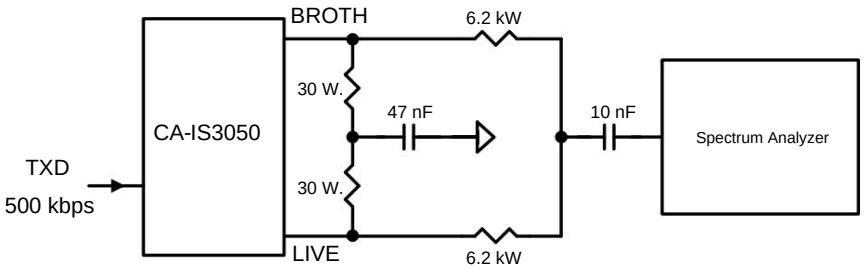



Figure **7-12** Electromagnetic radiation measurement circuit

**8** Function Description of Shanghai Chuandu Microelectronics Co., Ltd.

## 8.1 Overview

The CA-IS3050 is an isolated controller area network (CAN) physical layer transceiver that supports 5 kVRMS isolation withstand voltage level, common-mode transient immunity greater than 100 kV/ÿs, integrated master dynamic timeout function and thermal shutdown break protection. The logic side of the device can be powered by 3.3 V power supply, and the bus side is powered by 5 V power supply, which is very suitable for industrial control occasions with harsh environments. Because in industrial control applications, the logic side generally uses a 3.3 V power rail to power low-voltage devices such as microcontrollers to save power consumption, while the bus side usually uses a 5 V power rail to ensure a high signal-to-noise ratio.

## 8.2 **CAN** bus status

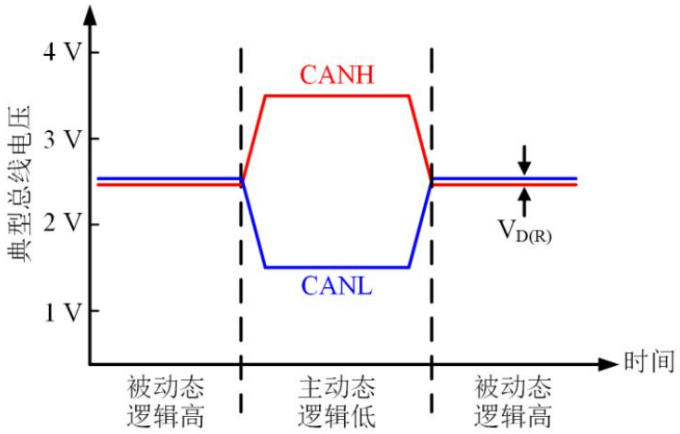



Figure **8-1** Typical waveform of CAN bus status

The CAN bus has two states: active and passive: when the differential voltage between CANH and CANL is greater than 0.9 V, the bus is active; when the differential voltage between CANH and CANL is less than 0.5 V, the bus is passive. When the bus is active, the CANH pin is in a high-level state, and the CANL pin is in a low-level state; when the bus is in a passive state, both CANH and CANL pins are in a high-impedance state. A typical bus voltage waveform is shown in Figure 8-1.

## 8.3 Protection function

### **8.3.1** Signal isolation

The signal isolation of CA-IS3050 is realized by the digital isolator based on the capacitive isolation scheme. On the logic side, the digital isolator adopts the On-Off Key (OOK) modulation method to modulate the input signal to high frequency and then isolate the signal through the digital isolator. The on-chip silicon dioxide capacitor with the function of withstand voltage, the digital isolator part of the circuit on the bus side restores the received signal and then converts it into a standard level and outputs it to the CAN bus. In the same way, the level on the bus side is processed by the bus side circuit and also modulated to high frequency by the digital isolator and then transmitted back to the logic side, and then demodulated on the logic side to restore the output to RXD. The grounds of the logic side and the bus side can be completely separated, and the isolation withstand voltage level of up to 5 kVRMS is achieved through the on-chip silicon dioxide capacitor , which ensures the integrity and safety of signal transmission between the microcontroller and the high-voltage bus in actual use.

### **8.3.2** Main Dynamic Timeout Function

The CA-IS3050 has the main dynamic timeout function to prevent TXD from being pulled down to a low level due to software or hardware failures, causing the bus to continuously enter the main dynamic and thus be locked (blocking the entire network communication). The main dynamic time-out function is triggered during the negative edge of the TXD input signal by using a counter. When the low level of TXD is longer than the main dynamic time-out time tTXD_DTO , the transceiver is turned off, at which time the bus is released and Enter passive. During the positive edge of the TXD input signal, the counter is set.

### **8.3.3** Thermal shutdown protection

CA-IS3050 integrates thermal shutdown protection function, which can protect the internal circuit of the device under over-temperature conditions. If the junction temperature of the device exceeds the thermal shutdown temperature TJ (shutdown), the driver will be shut down, thus blocking the signal transmission path from TXD to the bus, the typical thermal shutdown temperature is 165°C. When the device junction temperature falls below the thermal shutdown temperature, the driver is re-enabled.

**8.3.4** Current limiting protection

CA-IS3050 integrates the current-limiting protection function, which can prevent the output of the bus side from being short-circuited to the power supply or the instantaneous overcurrent to the ground, which may cause damage to the device. Note that once the current-limiting protection occurs

A larger current will be generated, resulting in larger losses.

## 8.4 Device Functional Truth Table

Table **8-1** Truth Table Abbreviations

| letter | describe |
|---|---|
| H | high level |
| L | low level |
| X | irrelevant |
| mow | Hi-Z (Off) |
| ? | uncertain |
| Open | open circuit |

Table **8-2** Driver function truth table

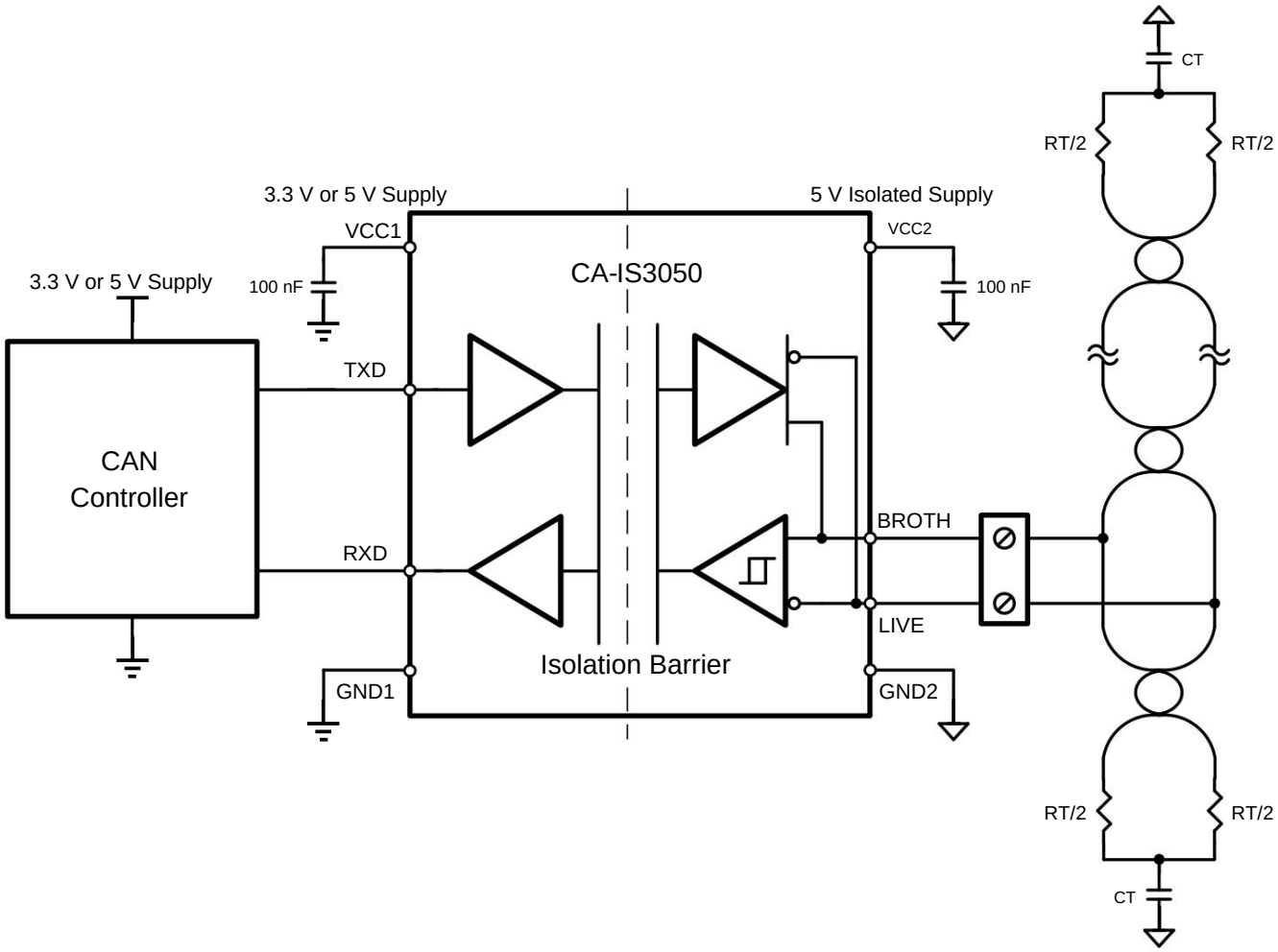
| enter | output | | bus status |
|---|---|---|---|
| TXD | BROTH | LIVE | |
| L | H | L | main dynamic |
| H or Open | mow | mow | passive |

Table **8-3** Receiver Function Truth Table

| CAN bus differential input<br>WID = VCANH – VCANL | bus status | RXD |
|---|---|---|
| 0.9 V ÿ VID | main dynamic | L |
| 0.5 V < VID < 0.9 V VID ÿ 0.5 V | ? | ? |
| Open (VID ÿ 0 V) | passive | H |
| | Open | H |

Table **8-4** Transceiver Functional Truth Table

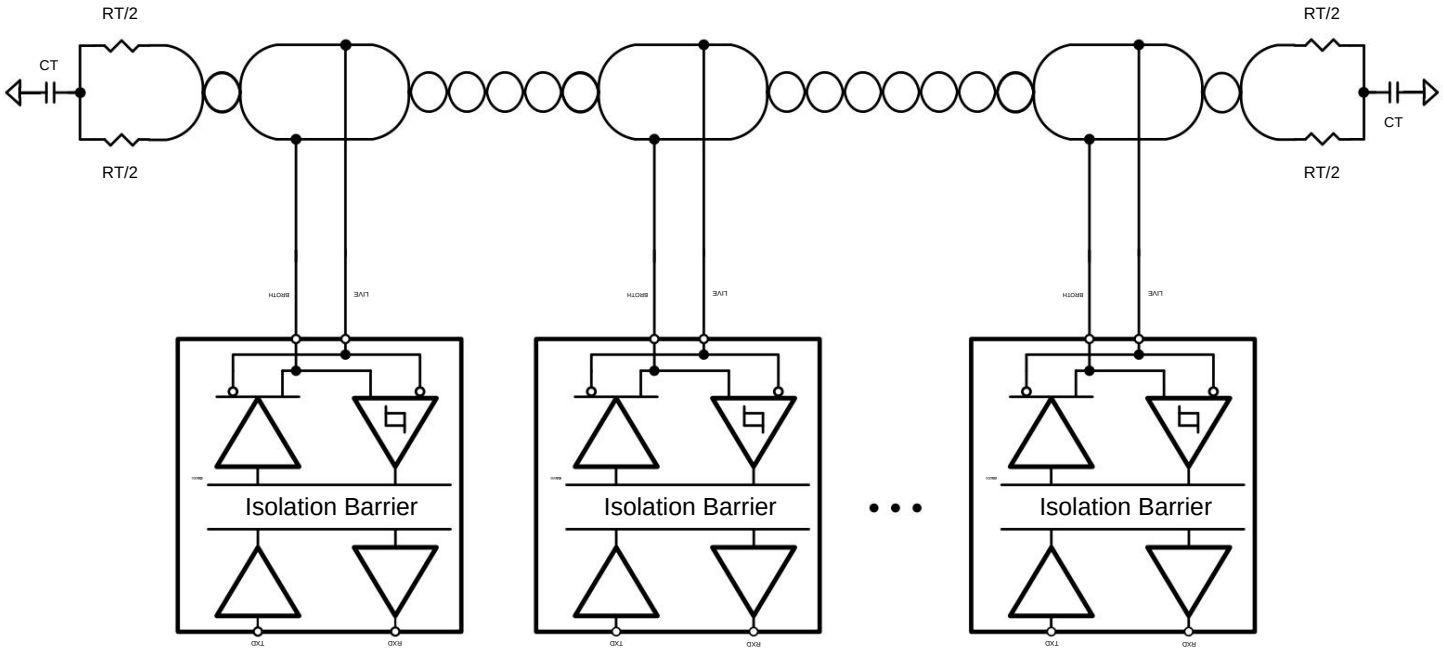
| driver output | | | | receiver | | |
|---|---|---|---|---|---|---|
| enter | | | bus status | Differential input<br>WID = VCANH – VCANL | RXD output bus status | |
| TXD | BROTH | LIVE | | | | |
| L 1 | H | L | main dynamic | 0.9 V ÿ VID passive | L | main dynamic |
| H | mow | mow | 0.5 V < VID < 0.9 V passive passive | | ? | ? |
| Open | mow | mow | | VID ÿ 0.5 V | H | passive |
| X | mow | mow | | Open | H | passive |




Remark:

1. The termination resistance RT should be equal to the characteristic impedance of the cable.

Figure **9-1** Typical isolated **CAN** node based on **CA-IS3050**



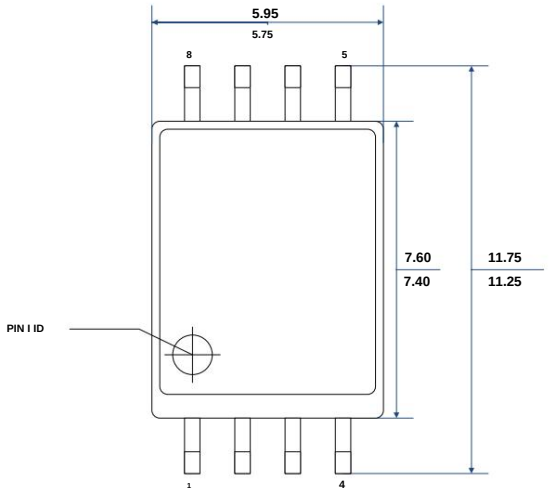

Remark:

1. The terminal resistance RT should be equal to the characteristic impedance of the cable;
2. CA-IS3050 can support up to 110 nodes.

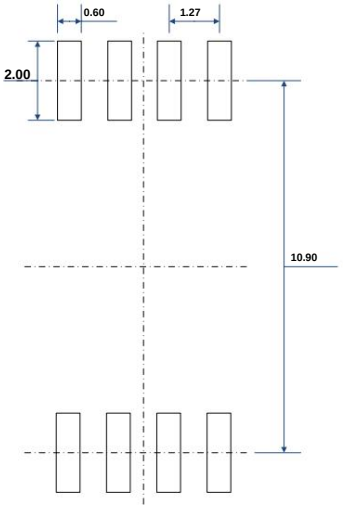
Figure **9-2** Typical **CAN** bus based on **CA-IS3050**

## 10.1 **SOIC8** Wide Body Dimensions

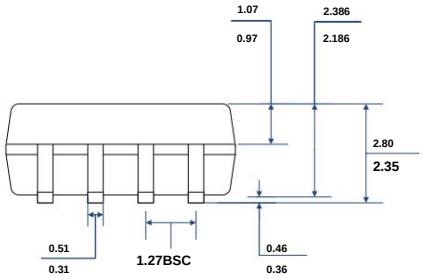
The following figures illustrate the SOIC8 wide-body package size diagram and recommended land size diagram for the CA-IS3050 series of isolated CAN transceivers. Dimensions are in mm unit.



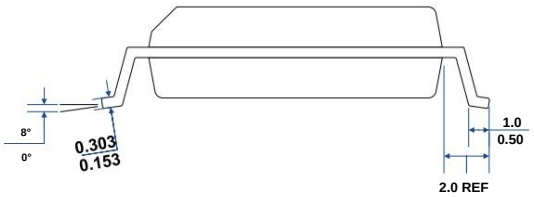

**TOP VIEW**




**RECOMMENDED LAND PATTERN**



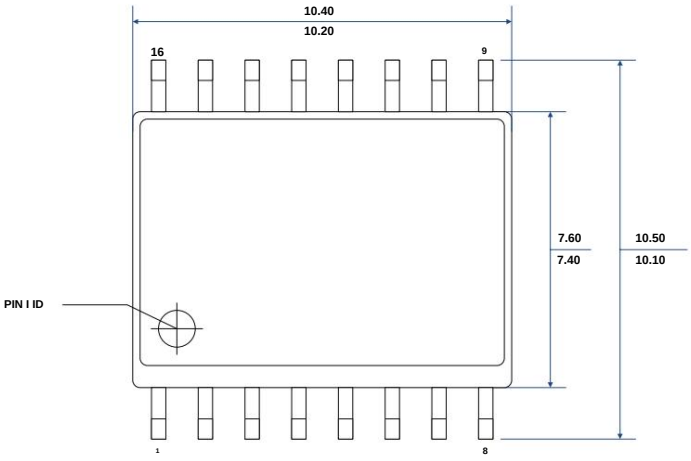

**FRONT VIEW**



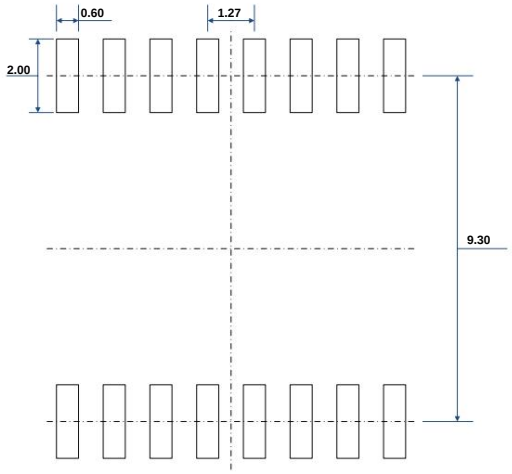

**LEFT-SIDE VIEW**

## 10.2 SOIC16 wide body dimensions

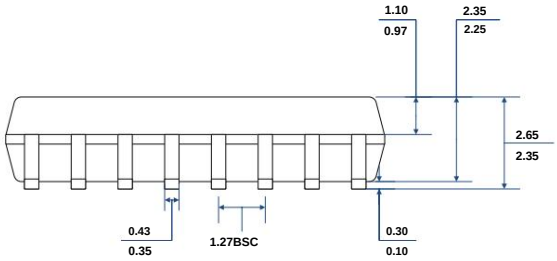
The figure below illustrates the SOIC16 wide-body package size and recommended land dimensions for the CA-IS3050 series of isolated CAN transceivers. Dimensions are in mm unit.



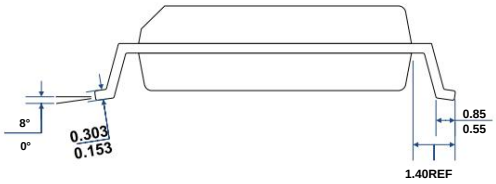

TOP VIEW




RECOMMENDED LAND PATTERN



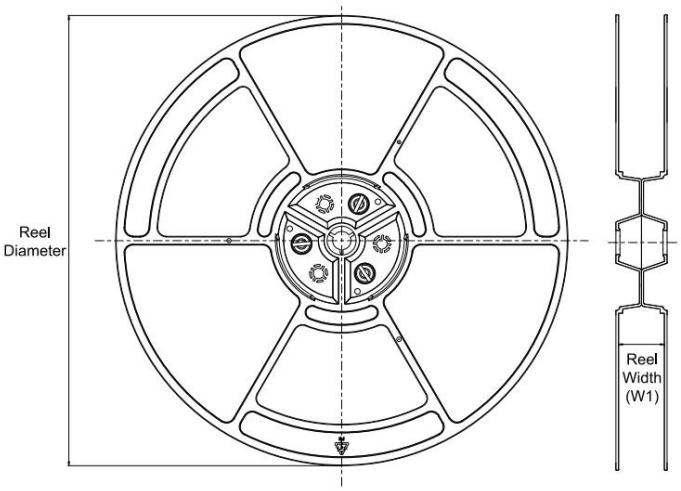

FRONT VIEW



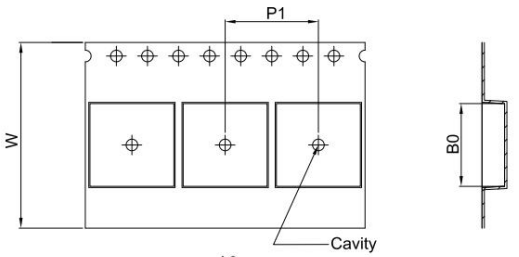

LEFT-SIDE VIEW

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

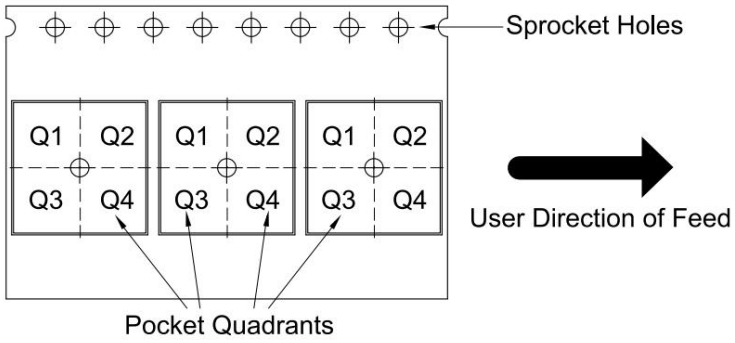



**TAPE DIMENSIONS**




| |
|---|
| A0 Dimension designed to accommodate the component width |
| B0 Dimension designed to accommodate the component length |
| K0 Dimension designed to accommodate the component thickness |
| W Overall width of the carrier tape |
| P1 Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins SPQ | | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | In (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA-IS3050WR | SEC W 16 | | | 1000 | 330 | 16.4 | 10.8 | 10.7 | 2.9 | 12.0 | 24.0 | Q1 |
| CA-IS3050WER | SEC W 16 | | | 1000 | 330 | 16.4 | 10.8 | 10.7 | 2.9 | 12.0 | 24.0 | Q1 |
| CA-IS3050GR | SEC | G | 8 | 1000 | 330 | 16.4 | 12.05 6.15 | | 3.3 | 16.0 | 16.0 | Q1 |
| CA-IS3050GER | SEC | G | 8 | 1000 | 330 | 16.4 | 12.05 6.15 | | 3.3 | 16.0 | 16.0 | Q1 |

Important Notice

The above information is for reference only and is used to assist Chipanalog customers in design and development. Chipanalog reserves the right, without prior notice, to reserves the right to change the above information due to technological innovation.

Chipanalog products are all factory tested. For specific practical applications, customers are responsible for their own evaluation and determine whether it is applicable. Chipanalog Customer's authorization to use said resources is limited to the development of related applications for the Chipanalog products involved. Other than that, the said resources may not be reproduced or displayed, such as Chipanalog is not responsible for any claims, damages, costs, losses, liabilities, etc., arising out of the use of said resources.

Trademark Information

Chipanalog Inc.®, Chipanalog® are registered trademarks of Chipanalog.

**http://www.chipanalog.com**