1. Overview and Motivation

Purpose and Context:

This ISA is tailored for a custom RISC-V processor aimed at AI-powered mobile financial services in Lesotho. It targets low-cost mobile devices, empowering users with intelligent, secure, and accessible digital banking capabilities. These services are crucial for enhancing financial inclusion in regions with limited resources.

Key Application Domains:

1. Voice-Driven Financial Transactions (VDFT) – perform banking using spoken commands.
2. Signal Strength Prediction – anticipate mobile connectivity quality.
3. Voice and Biometric Authentication – secure identity verification via voice and face.
4. Geo-Location and Fencing Tracking – determine the user's location to ensure secure transactions.

Design Goals:

- Deliver cost-effective and power-efficient processing.
- Enable local, on-device AI for voice, signal, and biometric tasks.
- Maintain compatibility with open-source RISC-V toolchains.
- Enable non-interuptable instructions for security.
- Optimize for wireless communication environments.

Suitability of ISA:

Built on the RISC-V RV32I base, this ISA offers:

- A clean, reduced instruction set with straightforward decoding.
- Flexibility to integrate custom AI and Digital Signal Processing (DSP) instructions.
- Extensions such as M, F, P, A, V, Zicsr, and Zk for efficient computation, parallelism, control, and security.

This makes the ISA ideal for developing smart, secure, and responsive financial services tailored to Lesotho's 4IR ambitions.

2. Architectural Design Choices

Feature	Choice	Justification
Instruction Style	RISC	Easy to customize and ensures simple control logic and fast execution.
Registers	32 × 32-bit general-purpose	Standard configuration supports AI and Digital Signal Processing operations that work on raw data.
Data Types	32-bit integer, optional float/vector	Covers all workloads including voice and biometrics.
Addressing Modes	Register + immediate offset	Simple and efficient hardware implementation.
Memory Model	Little-endian, word-aligned	The workloads require a robust software stack (OS, drivers, libraries), so these choices ensure compatibility with the dominant software ecosystem, including operating systems and development tools,
Instruction Formats	Fixed 32-bit (R, I, S, B, U, J, Custom)	Uniform layout simplifies instruction decoding.

3. Instruction Set Summary

Voice Authentication and Driven Transactions Processing

Mnemonic	Operands	Description
MATCHSTR	rd, rs1, rs2	Detects command keywords like "SEND"
PARSEAMT	rd, rs1, rs2	Converts spoken numbers into integers
TXVERIFY	rd, rs1, rs2	Ensures funds are sufficient for transfer
MFCCX	rd, rs1	Extracts MFCC(feature extraction technique that reduces raw voice data into a compact set of numbers) features for voice recognition
FFT32	rd, rs1	Performs First Fourier Transform on input signal

Signal Processing

Mnemonic	Operands	Function
AVGSMPL	rd, rs1, rs2	Computes average of signal samples
NOISERED	rd, rs1, rs2	Reduces signal noise

Biometric Authentication

Mnemonic	Operands	Description
INITAUTH	-	Initializes the biometric system
AUTHUSER	rd, rs1, rs2	Verifies user via biometric input
UPDSAMPLE	rd, rs1	Updates stored fingerprint/voice sample
FPVERIFY	rd, rs1	Matches fingerprint template

Transaction Tracking and Fencing

Mnemonic	Operands	Description
GETLOC	rd	Retrieves GPS coordinates
CHKZONE	rd, rs1	Verifies if user is in authorized area
LOCVERIFY	rd, rs1, rs2	Validates location before a transaction

4. Instruction Encoding Summary

R-Type Format

Field	Bits
opcode	[6:0]
rd	[11:7]
funct3	[14:12]
rs1	[19:15]
rs2	[24:20]
funct7	[31:25]

- Custom instructions use a reserved opcode (e.g., `0b1111011`) with unique `funct7` values for decoding.

Other Formats:

- **I-type**: Used for immediate ops and loads.
- **S-type**: For stores.
- **B-type**: Conditional branches.
- **U/J-type**: For constants and jumps.

Regularity:

- All instructions are 32-bit fixed length.
- Uniform structure eases hardware design and pipelining.
- Custom extensions preserve base ISA structure.

5. Design Rationale & Trade-offs

Consideration	Design Choice & Rationale
Simplicity vs Features	A reduced instruction set keeps hardware minimal and specialized tasks are handled via carefully chosen custom instructions.
Compactness vs Performance	32-bit fixed-width instructions enable predictable execution. Compressed RVC can be optionally adopted to reduce memory use.
Hardware Impact	The base ISA is minimal; custom instructions for AI, biometrics, and location add modest complexity while offering big performance gains.
Extendability	Designed to support future growth. Additional instructions (e.g., for facial recognition or 5G prediction) can be integrated seamlessly.