Analizing GF180 process Manual for ESD design.

- Using regular devices data to construct the ESD window.
  - Oxide Breakdowns.
  - NMOS max operation voltages.
  - PMOS max operation voltages.

  - Look at Chapter 5 on the following Link. GF180MCU process Manual.
  - https://gf180mcu-pdk.readthedocs.io/en/latest/physical_verification/design_manual/drm_15.html

- Understanding ESD special devices.
- Understanding TLP data for each of them.
  - Sizing the devices correctly.

  - Look for Chapter 14 for GF180MCU process manual.
  - https://gf180mcu-pdk.readthedocs.io/en/latest/physical_verification/design_manual/drm_14.html

Real World Exercise:

- **Use GF180 Manual Specs.**
- **Our Chip is a 5 pin part. VCC, GND, IO1, I02, IO3.**
  - **VCC is 3V +/- 10%. 100uA ICC consumption. Max reverse rating = -0.5V.**
  - **IO1 is Digital, Push Pull inverter Outputs. +/- 1mA , 100mV (100ohm).**
  - **IO2 is a GATE INPUT pin. 3V rated. +/-100nA current.**
  - **IO3 is an OPEN Drain Nmos Output. +1mA, 100mV, 5V rated. (100ohm).**
  - **Need to Pass 2Kv HBM spec for all Pins expect IO3 that must pass 4Kv.**
- Draw the PAD RING equivalent Circuit and define an ESD Protection Architecture using a Power Clamp + Local Protections.
- Calculate the ESD window for a VCC-GND discharge.
  - Digital Circuits Gates connected between VCC-GND.
- Describe the Current Path for ESD event IF no protection is given.
- Propose a Power Clamp for it.
  - Draw the Characteristic over the ESD Window graph.
  - Consider effect of Metallization.
  - Define the Star-VCC and Star-GND concept Nodes.

Exercise 2:

- Consider IO1 now.
  - Analize Events to GND. Positive and Negative.
  - Analize Events to VCC. Positive and Negative.
  - Draw the ESD Window.
  - Consider an Architecture that will Share the Power Clamp on VCC-GND.
    - Draw the current path during ESD events IF protection is NOT place.
    - Same when protection is connected.
    - Consider effects of metallization.
- Consider I02 now.

Exercise 3:

- Consider I03 to GND now.
  - Draw the ESD window.
    - Figure the Current path for ESD event if No protection is available.
  - Find a ESD protection Solution:
    - A) Using an Isolated Protection.
      - Estimate the Size for the Protection.
      - Figure the Current Path during en ESD event.
    - B) Reusing the Power Clamp located in VCC-GND.
      - Figure the current path during ESD event.
      - Estimate the Size for the Local device.
      - Consider the effect of metallization.
    - C) Compare and discuss A) and B).
- Repeat for IO3 to VCC case.
- Discuss the 6 steps of ESD design Methodology.
- Discuss the usage of TLP measurements to verify the circuitry design.