# A design of flyback switched-mode power supply with softswitching using the UC3842 controller

# A design of flyback switched-mode power supply with soft-switching using the UC3842 controller

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**Abstract.** The flyback switched-mode power supply is widely used in various electrical equipments due to its high efficiency and small size. This article is used UC3842 as the core control chip to design a flyback switched-mode power supply. The design includes the input of 36~48V and an output of 12V and introduces a soft-switching design. The trigger signal of the next cycle arrives after the switching voltage drops to zero and realizes zero voltage switching (ZVS) to reduce switching losses. At the same time, single-ended flyback switching circuits, feedback circuits, and RCD clamp circuits are designed. The simulation result is shown the accuracy for the output voltage is within 1.08%, as well as the ripple factor is below 0.011%.

## 1. Introduction

With the ongoing development of power electronics techniques, the demands for better performance are getting stronger on the switched-mode power supply (SMPS). The conventional SMPS has a shortage in the process of switching that substantial losses have resulted when conducting. In our study, the soft-switching technique is introduced to realize zero-voltage switching (ZVS) for reducing power losses during the on-off switching process [1-3]. As the switching frequencies increasing from a few ten thousand hertz to many hundreds thousand hertz, it is getting practical for the SMPS to realize the desired characteristics, like high-frequency switching, small size, and high converting efficiency [4-6]. However, with the increase in switching frequency, the switching losses are piling up to a substantial level. In order to convert the power efficiently for a better transfer rate, it is desirable to apply soft-switching techniques to remove or eliminate the switching losses. The flyback convert circuit is widely used in the multiple outputs power supply application due to its simple topology, electrical isolation between the input and the output, wide voltage ranges for step-up or step-down, and the load balancing among multiple outputs [7-9]. In the flyback converter, the transformer plays two parts as the inductor and the transformer. Since the magnetic core of the transformer is DC biased, the core is air-gapped to prevent magnetic flux saturation that introduces more magnetic flux leakage [10-11]. When the power transistor is cutting off, there will be a big voltage pike that exerts voltage stress on the transistor to cause damages possibly. Therefore, the resistor-capacitor-diode (RCD) clamp circuit is involved to control the voltage(current) level in the inductor while conducting.

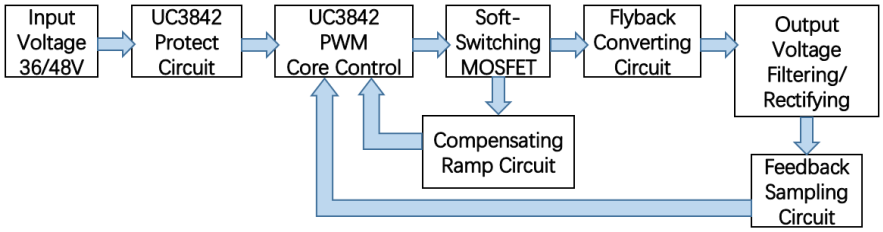


**Figure 1.** Functional block diagram.

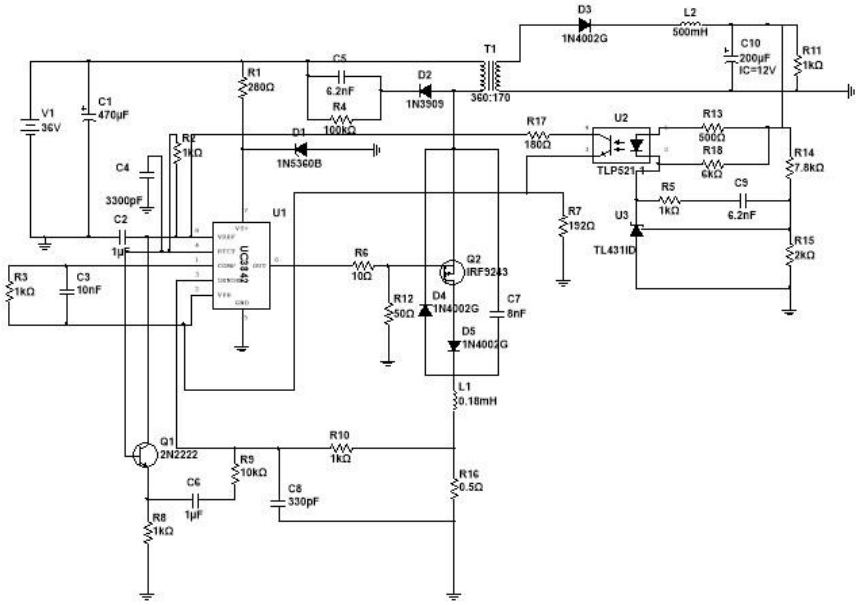


**Figure 2.** Flyback SMPS circuit schematic diagram.

## 2. Method

### *2.1. SMPS performance design indicator*

The current specification for the input voltage is set to 36/48V because it is the most commonly used battery output ratings for electrical vehicles. The normal working voltage for components of electrical vehicles is usually 12V. Therefore, the SMPS in our proposed design converts the 36/48V input to the 12V output with less than 50% duty ratio at the switching frequency of 200kHz.

### *2.2. Block diagram and system schematic*

Figure 1 is the functional block diagram of our proposed flyback SMPS system. The main functional blocks are the start-up protection circuit, the core control circuit, the soft-switching driving circuit, the compensating ramp generating circuit, the flyback converting circuit, the output rectifier circuit, and the feedback sampling circuit. The complete circuit schematic diagram is depicted in Figure 2.

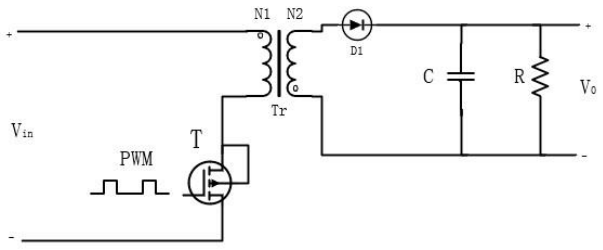


**Figure 3.** Isolated single switch flyback topology.

### *2.3. Flyback SMPS with the soft-switching design procedure*

*2.3.1. Flyback converting basic operation and soft-switching method.* The topology of the basic isolated single switch flyback inverter is demonstrated in Figure 3. When the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as a switch *T* is turned on, the input voltage $V_{in}$ puts on the primary side windings $N_1$ transferring the electrical energy as the magnetic energy stored in the transformer. In the meantime, the opposite secondary side windings $N_2$ makes the diode $D_1$ reversely biased to stop energy transfer to the load. When the MOSFET *T* is turned off, the energy stored in the primary side windings $N_1$ is transferred to the secondary side windings $N_2$ through the coupling of the transformer when the diode $T_1$ is forward biased to deliver energy to the load with the filtering capacitor *C* stabilizing the output voltage. In our design, the mode of the flyback converting circuit is the current mode control which the current is not reduced to zero when the MOSFET is turned on[10].
The output voltage can be calculated by equation 1 below:

$$v_o = v_{in} \cdot \frac{N_2}{N_1} \cdot \frac{D}{1-D} \tag{1}$$

where $N_2/N_1$ is the reciprocal of the transformer's turn ratio (TR), and *D* is the duty ratio.
The UC3842 current mode pulse width modulation (PWM) controller is capable to output 200*kHz* frequency pulses to drive the MOSFET. Therefore, the high-speed switching of the MOSFET results in some part of energy loss which is the conduction loss. The conduction loss $E_{on}$ is calculated by

$$E_{on} = \int_{T_{on}} p(t)dt \tag{2}$$

where $T_{on}$ is the conduction duration and $p(t) = v_{DS}(t) \cdot i_{DS}(t)$.
Quasi-resonant converter (QRC) circuit is a relatively early and practical soft-switching method. It is efficient and stable when the load changes. In our study, the zero-voltage-switched (ZVS) QRC is applied. After the MOSFET T is turned off, the circuit generates a resonant pulse between inductor *L* and capacitor $C_1$ that can counter the sudden changes in voltage and current at both ends of the MOSFET. Therefore, the MOSFET turns on when the voltage goes to zero to avoid switching loss. The resonant frequency can be calculated by

$$f_\gamma = \frac{1}{2\pi\sqrt{C_1 L}} \tag{3}$$

In the design phase of soft switching, usually, the switching frequency is larger than the LC resonant frequency. Hence, the corresponding values for *L* and $C_1$ can be inferred with a certain switching frequency. Based on our simulation, the setup with the best outcome is to assign
0.18*mH* and 8*nF* to *L* and $C_1$, respectively, as indicated in Figure 4.

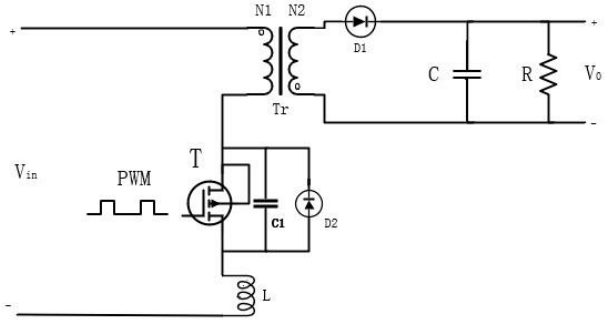


**Figure 4.** Soft switching quasi-resonant converter topology.

*2.3.2. Power-on circuit design.* The power-on circuit consists of a current-limiting resistance $R_5$ and a Zener diode $D_1$, as in Figure 5. Because the power-on voltage of the UC3842 PWM controller is greater than 16*V*, the Zener diode is part number 1N5360B to meet the specification. The current-limiting

resistor $R_5$ is obtained by calculation to lower the voltage at both ends of $R_5$ with less heat loss. With the Zener diode being used, the UC3842 controller can be powered on with stabilized source voltage.

*2.3.3. RCD clamping protection circuit*

Due to the flux leakage of the transformer and other distributed characteristics, the flyback converter will generate a high voltage spike at the moment of switching off that can adversely affect the normal operation of the MOSFET switch. Certain measurements should be taken in order to suppress the voltage spike. Most of the flux energy leakage will transfer on the capacitor $C_5$ of the clamping circuit instantly at the moment of switching off. Then, the energy stored in the capacitor will be consumed later by the clamping resistor $R_4$. In this way, the stress on the MOSFET switch is notably relieved. The RCD clamping circuit is widely used because of its simple structure and low cost [12-13].

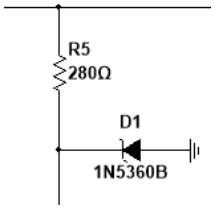


**Figure 5.** Power-on circuit.

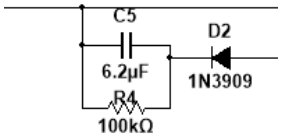


**Figure 6.** RCD clamping circuit.

*2.3.4. Output rectifying filter circuit.* After being rectified by the diode $D_3$, the output voltage is stabilized at 12$V$ with subsequent serial inductor $L$ and parallel capacitor $C$. The input DC voltage is conducting on and off by the high-frequency MOSFET switch. The electrical energy is converting through the high-frequency transformer. Therefore, there will be interference of high-frequency noise at the output side. The LC low-pass filter serves the purpose of eliminating high-frequency noise.

*2.3.5. Feedback voltage-sampling circuit.* The feedback circuit is designed with the TL431 and the TLP521 in focus. The output voltage ($V_o$) passing through the voltage divider of $R_{14}$ and $R_{15}$ is connected to the voltage reference pin of the TL431. When the reference voltage is very near the level of 2.5$V$, the internal transistor works in the linear region, and a constant current is drawn from the voltage of the resistor $R_5$. The constant current flowing through the light-emitting diode (LED) will induce a current in proportion on the phototransistor at the opposite side for the TL521. The feedback loop passes the error signal from the optically coupled isolator to the PWM controller UC3842. The error signal is compared with the internal ramp signal to output the drive signals with the correct duty cycle. Therefore, the inverter can have a stable output voltage with different input voltages or output load situations. If the output voltage ($V_o$) of the SMPS needs to be increased, the duty cycle of the drive signal needs to increase accordingly. Hence, the feedback error signal needs to increase as well that the current flowing through the isolator LED needs to be reduced in consequence [14].

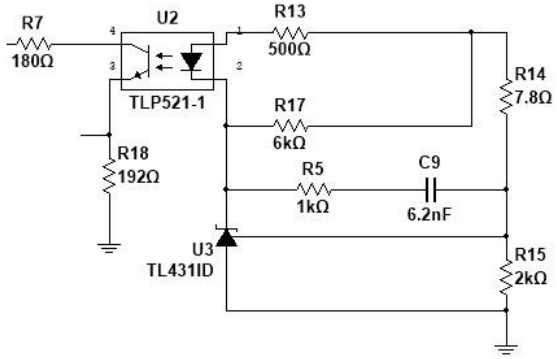


**Figure 7.** Feedback voltage-sampling circuit.

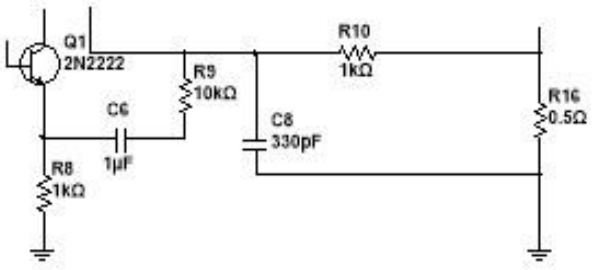


**Figure 8.** Compensating ramp generating circuit.

*(1) Calculate $R_{14}$ and $R_{15}$ resistors*

Owning to the reference voltage of TL431 is $V_{ref} = 2.5V$, $R_{14}$ and $R_{15}$ are calculated in proportion when $V_o$ is $12V$, and the current at the input is more than $2\mu A$. Considering the effect of the current at the input on the divider circuit, the current at $R_{14}$ and $R_{15}$ should be increased. Therefore, we have $R_{14} = 7.8k\Omega$ and $R_{15} = 2k\Omega$.

*(2) Calculate $R_{13}$ resistor*

According to the TLP521 datasheet, the input forward current $I_f$ is within the range of $0.1mA$ to $50mA$. In the meantime, the voltage drop for the optically coupled isolator is $1.2V$. Hence, we have $[(V_o - 1.2 - 2.5)/50 \times 10^{-3}] \times R_{13} \leq [(V_o - 1.2 - 2.5)/0.1 \times 10^{-3}]$. In our case, the resistor $R_{13}$ equals $500\Omega$.

*(3) Calculate $R_{17}$ resistor*

When the coupled isolator is turned off, to keep the TL431 active, the resistor $R_{17}$ is connected in parallel to provide the $1mA$ minimum current for the TL431. By $R_{17} \leq [(I_F R_{13} + 1.2)/(1 \times 10^{-3})]$, we get $R_{17} = 6k\Omega$.

*(4) Calculate $R_{18}$ and $R_7$ resistors*

The input voltage at the $V_{FB}$ pin is compared with the reference $2.5V$ by the differential amplifier circuit inside the UC3842. When the voltage at the $V_{FB}$ pin is $2.5V$, and the $I_F$ of the coupler is $10mA$, the CTR is about 130. So when the output current of the coupler is $13mA$, the resistor $R_{18}$ can be calculated by $R_{18} = 2.5V/0.013A = 192\Omega$.

The resistor $R_7$ which plays the role as the voltage divider is to lower the input voltage at the $V_{FB}$ pin. Since the differential input voltage range for the UC3842 is between $2.42V$ and $2.58V$, it is necessary to select the value properly for the resistor $R_7$ as well as the duty cycle to make the output voltage stable.

*2.4. Compensating ramp generating circuit*

During the switching process, the circuit parasitic capacitance and inductance will generate a sudden spike current running through the MOSFET switch. Therefore, the resistor $R_{10}$ and the capacitor $C_8$ are added as the filter. By introducing the emitter follower, the equivalent resistance is increased for the compensating circuit to reduce the effects due to the working frequency. The function of capacitor $C_6$ is to filter out the DC component from the sawtooth waveform [15].

## 3. Results and discussions

From Figures, 9 and Figure 10, when there is a trigger signal in the G level of the switch, the voltage at both ends of the switch are still at the maximum, and the current jumps from 0 to the conduction current $I_d$, immediately before it is turned on. In this process, when the voltage and current are not zero, the arrival of the trigger signal is bound to have a power loss. In the $200kHz$ high-frequency trigger switch used in this design, compared with the old $20kHz$ frequency. The conduction loss of the switch is multiplied by 100 times bigger, so the soft switch designed in this experiment is needed to improve this power loss.

From Figures 11 and Figure 12, it can be seen that before the trigger signal of the switch tube comes, the voltage at both ends of the switch tube is already zero, and zero voltage can be realized, but the current does not produce current immediately when it is turned on. It is because there is a certain phase difference between the charge and discharge of capacitor $C_7$ and inductor $L_1$. The design of adding a soft switch is in line with $P = V \cdot I$ ($V = 0$), which reduces the switching loss when the high frequency is turned on and achieves the expected design goal.

In our simulation experiments, the DC $36V$ voltage is used as the input power source. The output voltage is observed on the oscilloscope. From the experiment results, the output waveform is like a straight line with up-and-down ripples on the scope. The approximate output voltage level is at $12 \pm 0.01V$ which indicates the specification for our proposed design is satisfied. The experiment result is illustrated in Figure 13.

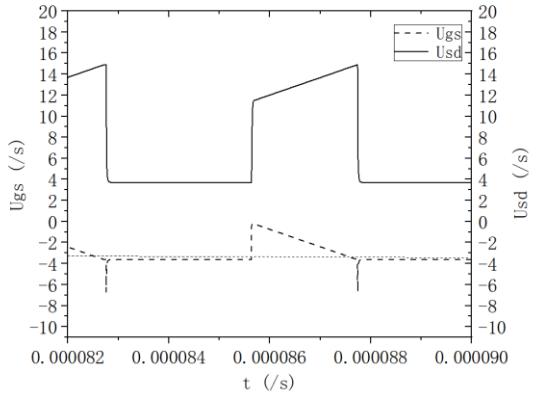


**Figure 9.** $U_{sd}$ and $U_{gs}$ with hard switching.

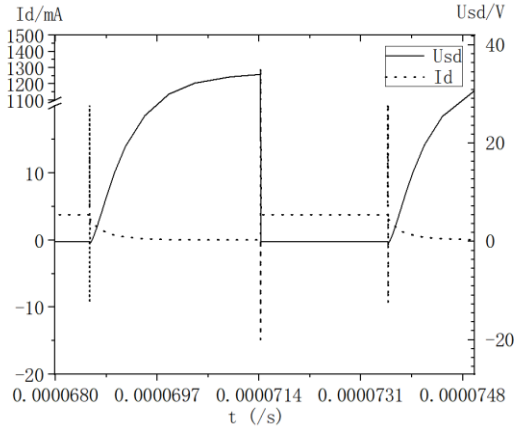


**Figure 10.** $U_{sd}$ and $I_d$ with hard switching.

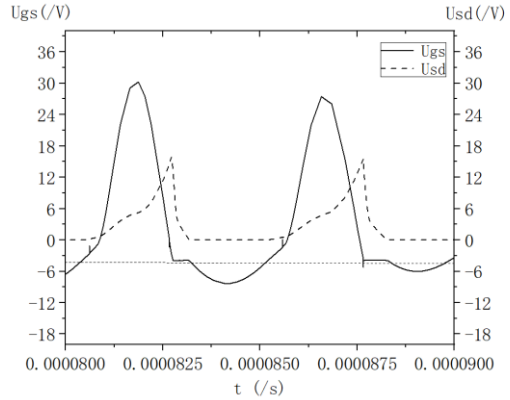


**Figure 11.** $U_{sd}$ and $U_{gs}$ with soft switching.

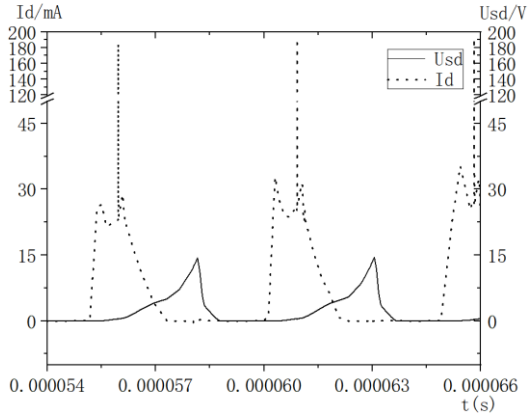


**Figure 12.** $U_{sd}$ and $I_d$ with soft switching.

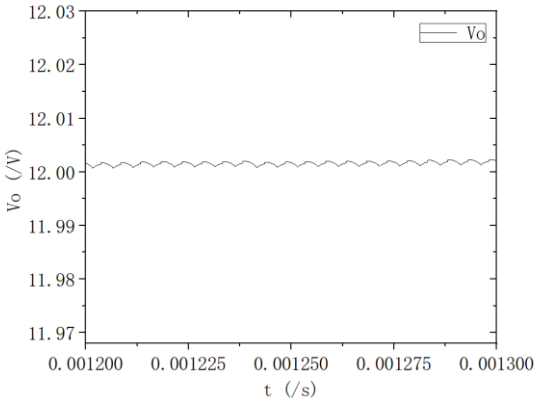


**Figure 13.** Output voltage waveform with 36*V* input.

Because the inductor and capacitor are added in the design for the soft switching to generate certain resonance, the voltage $U_{sd}$ and gate voltage $U_{gs}$ waveforms at both ends of the switch are not perfect, which is also in a reasonable range, and a little trade-off is needed in the design. Therefore, the desired effect is achieved in the design.

Because the feedback voltage of the UC3842 only varies from 2.42*V* to 2.58*V*, the interval that can be adjusted is very limited. The comparison of the effect of soft and hard switches in the process can only improve the efficiency of soft switches by changing the input value and the ratio of transformers. The experimental results of the corresponding output voltage of soft and hard switches are listed in Table 1.

As shown in Table 1, the output voltage with the soft-switching is significantly higher than that of hard-switching.

**Table 1.** Simulation measurement data summary (unit: *V*).

| Input Voltage ($V_{in}$) | Output Voltage (Soft-Switching) | Output Voltage (Hard-Switching) | ripple factor (Soft-Switching) |
|---|---|---|---|
| 48 | 12.130 | 12.067 | 0.0116 |
| 46 | 12.080 | 12.016 | 0.0097 |
| 44 | 12.063 | 11.995 | 0.0111 |
| 42 | 12.053 | 11.987 | 0.0092 |
| 40 | 12.126 | 12.059 | 0.01103 |
| 38 | 12.089 | 12.020 | 0.00647 |
| 36 | 12.001 | 11.930 | 0.00690 |

By applying the soft-switching, the accuracy of the output voltage is within 1.08%, and the ripple factor is kept below 0.011%.

## 4. Conclusion

In this study, a flyback converter circuit design is proposed based on the UC3842 controller with the duty cycle $D < 50\%$ for the MOSFET switch. With the topology of the quasi-resonant converter with zero-voltage switching, the zero-voltage conduction is implemented to achieve better conversion efficiency than the traditional hard switching. Introduction of the soft-switching reduces the loss during the on-off state transition at the high switching frequency. The accompany functional circuits of UC3842, i.e., the feedback circuit, power-on circuit, protection circuit, and harmonics compensation circuit, guarantee stability during operation. In accordance with the simulation waveforms and associated calculations, the proposed design in this study achieves our original expectation.

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