**EE-212 Electronic Circuits Design**

# Complex Engineering Problem

# Design, Simulation and Hardware Implementation of a Class AB Output Stage Amplifier

**BSEE 2022-2026**

**Semester 3**

**Fall 2023**

**Contribution in the Final Result: 20%**

**CLO Mapping: CLO3 & CLO4**

## Schedule:

- Assigned on 25-10-2023
- Approval of the design calculations till 15-11-2023
- Testing and validation in simulation till 30-11-2023
- Demonstration of the hardware implementation till 15-12-2023
- Submission of the final report till 30-12-2023

Work in a team of 2-3 students

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# 1. Background and Descriptions

Class AB output stage amplifiers are attractive for a variety of applications for their higher efficiency as compared to the class A amplifiers, and for their lower output distortion as compared to the class B amplifiers. The basic concept of biasing a class AB amplifier at a quiescent collector current well below the peak load current is realized in many different ways. This CEP focuses on designing a class AB output stage amplifier for a specific load to maximize power efficiency and minimize the total harmonic distortion.

# 2. The problem statement

## 2.1. Design Specifications

You are required to design, simulate and implement a class AB output stage amplifier with a op-amp based preamplifier for the following specifications.

- **Input:** Audio signal from the audio port of your cell phone
- **Load:** 4Ω/10W load speaker
- **The minimum power efficiency:** 60%
- **The maximum total harmonic distortion:** 0.5%
- **Output voltage:** to be calculated to ensure 10W power dissipation in the 4Ω load
- **Minimum input resistance:** 1kΩ
- **Maximum output resistance:** 0.1Ω
- **The maximum allowed power supply:** ±15V
- **Additional objectives:**
    - Maximize power efficiency
    - Maximize the input resistance
    - Minimize the output resistance
    - Minimize the power supply rating
    - Minimize total harmonic distortion (including Zero-cross-over distortion, saturation and asymmetry)
    - Minimize circuit complexity
- **The circuit topology:** any variant class AB amplifier of your choice
- **Simulation tool:** any of your choice including LTSpice, Multisim, Altium, Proteous, Psim etc.
- **Hardware implementation:**
    - Use TIP31 and TIP32 transistors along with any small signal transistors

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# 3. Grading

## 3.1. Grading Scheme

| Activity | Points | CLO Mapping |
|---|---|---|
| Design calculations | 25 | 3 |
| Working simulations | 25 | 4 |
| Demonstration of the working hardware and its evaluation | 25 | 4 |
| Written report with detailed testing and evaluation of the hardware, learning outcomes and conclusions | 25 | 4 |

## 3.2. Rubrics for Grading:

| **Activity** | **Points** | **CLO Mapping** | **Assessment method** | **Very Weak 20%** | **Weak 40%** | **Average 60%** | **Good 80%** | **Very Good 100%** |
|---|---|---|---|---|---|---|---|---|
| **Design calculations** | **25** | **3** | **Evaluation of the written report and oral questions** | Did not complete, OR copied/reproduced without understanding | Completed with errors and have poor understanding | Completed with good understanding BUT presentation of calculations in the report is ambiguous | Completed with good understanding, and the presentation in the written report is fairly good | Completed with very good understanding, and the presentation in the written report is very good including equations' numbering, referencing, and summary of the calculations in tables etc. |
| **Working simulations** | **25** | **4** | **Demonstration of the working simulation** | Incomplete circuit diagrams, OR simulations not working, OR inappropriate circuit's component models | Complete circuit with working simulations, BUT the results are unexpected (do not meet the design requirements) | Complete working simulations with expected results, HOWEVER the student finds it difficult to explain the results | Complete working simulations with expected results, and the student understands the results | Complete working simulations with expected results, and the student not only understand the results but have useful suggestions to improve the designs |

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| **Demonstration and evaluation of the hardware** | **25** | **4** | **Practical demonstrations in the lab** | The amplifier is not implemented properly | The amplifier is implemented BUT not working properly or not meeting the performance targets (deviation from the targets is more than ±10% for each of the targets or more than 20% for one of the targets) | The amplifier is working properly BUT meeting the performance targets marginally (deviation from the targets is less than 10% for each of the targets) | The amplifier is working properly meeting the performance targets. Demonstrated with a sinusoidal tone and audio signal from a cell phone. | The amplifier is working exceptionally resulting in performance above the specified targets (10% improvement in at least two of the targets). Demonstrated with a sinusoidal tone and audio signal from a cell phone. |
| **Written report** | **20** | **4** | **Evaluation of the written report and oral questions** | The design calculation, simulation, and hardware descriptions are poor. | The design calculation, simulation, and hardware descriptions are good BUT the results recorded are not presented properly. | The design calculation, simulation, and hardware descriptions are good. The results recorded are presented properly. However, the student demonstrated a poor understanding of the results. | The design calculation, simulation, and hardware descriptions are good. The results recorded are presented properly. The student demonstrated a good understanding of the results but failed to conclude the results or identify the causes and remedies for the issues faced during the development of the amplifier. | The design calculation, simulation, and hardware descriptions are good. The results recorded are presented properly. The student demonstrated a good understanding of the results with a good ability to conclude the results. Moreover, the student demonstrated a good understanding of the issues (unresolved/resolved) and knew how to fix the issues. |

# 4. Description of the attributes of the CEP

| | Attributes | General description of the attributes | Specific description for the CEP under consideration |
|---|---|---|---|
| | Preamble<br>Engineering problems which cannot be resolved without in-depth engineering knowledge, and have some or all of the characteristics listed below: | | The problem under discussion requires in-depth knowledge of output stage amplifiers, different topologies, and their trade offs. |
| | Range of conflicting requirements | Involve wide-ranging or conflicting technical, engineering, and other issues | There are several conflicting performance indicators in the design of the output stage amplifier such as the circuit complexity, power efficiency, and total harmonic distortion. A challenging set of conflicting targets is considered in this problem as given in section 2 of this document. |
| | Depth of analysis required | Have no obvious solution and require abstract thinking, and originality in analysis to formulate suitable models | It is not trivial to select a suitable topology for the given set of specifications and requires a good understanding followed by analytical analysis to finally choose a particular topology. |
| | Depth of knowledge required | Requires research-based knowledge much of which is at, or informed by, the forefront of the professional discipline and which allows a fundamentals-based, first principles analytical approach. | It requires a very clear understanding of the transistors' saturation and cut-off, and thorough calculations to find the biasing resistors to meet the given requirements of the load while maintaining the performance parameters. Along with the theoretical and analytical background, hardware implementation requires expertise in resolving generic hardware-related issues such as power supply noise, grounding, use of multiple power supplies, and limited current driving capabilities of the power supplies. |
| | Familiarity of issues | Involve infrequently encountered issues | The students would consider distortion and its measurement probably for the first time in this case. Moreover, there are several issues that the students are expected to face in the simulations and hardware implementations such as inappropriate/unmatched parameters of PNP and NPN transistors and diodes. The transient response of coupling capacitors may result in unexpected results at the start of the simulations. Moreover, specific issues |

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| | | | such as thermal run-away, mismatch of the transistors, and power derating need to be addressed. |
| | Extent of applicable codes | Are outside problems encompassed by standards and codes of practice for professional engineering | The students will have to work within the ratings of the transistors. The measurements, such as THD and power efficiency, will have to be measured, and minimized/maximized to meet the standards and general practices. The will work with standard audio outputs from a digital device such as cell phone. |
| | The extent of stakeholder involvement and level of conflicting requirements | Involve diverse groups of stakeholders with widely varying needs | |
| | Consequences | Have significant consequences in a range of contexts. | This activity has significant learning consequences in the domain of design of electronic circuits, and use of modern tools such as simulation software, and hardware implementation skills particularly reading the datasheets, choosing components for a specific set of specifications, measurement of harmonic distortion using FFT on a digital oscilloscope etc. |
| | Interdependence | Are high-level problems including many component parts or sub-problems | The overall system is expected to have a preamplifier stage followed by an output stage amplifier. The output stage amplifier will act as a load for the preamplifier. Moreover, the input to the preamplifier is from the audio port of a cell phone. Hence, the are multiple components of the required amplifier that are dependent on each other. |