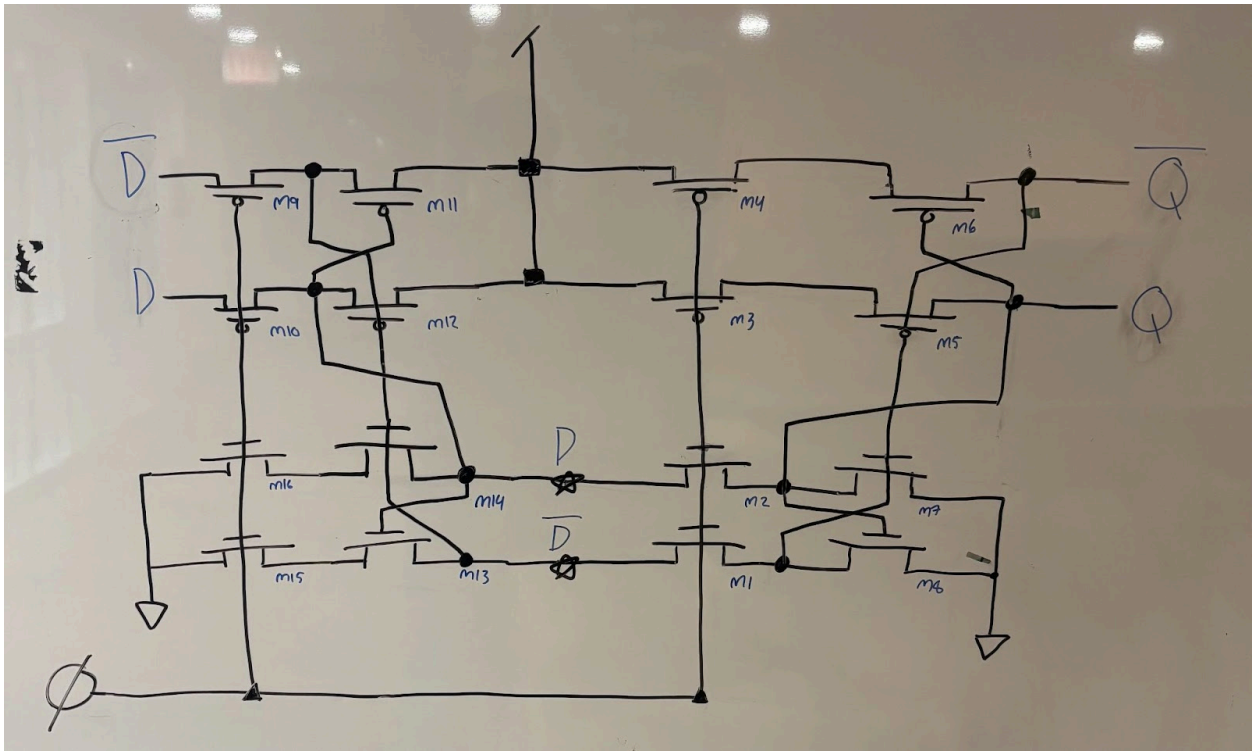
Miniproject 2

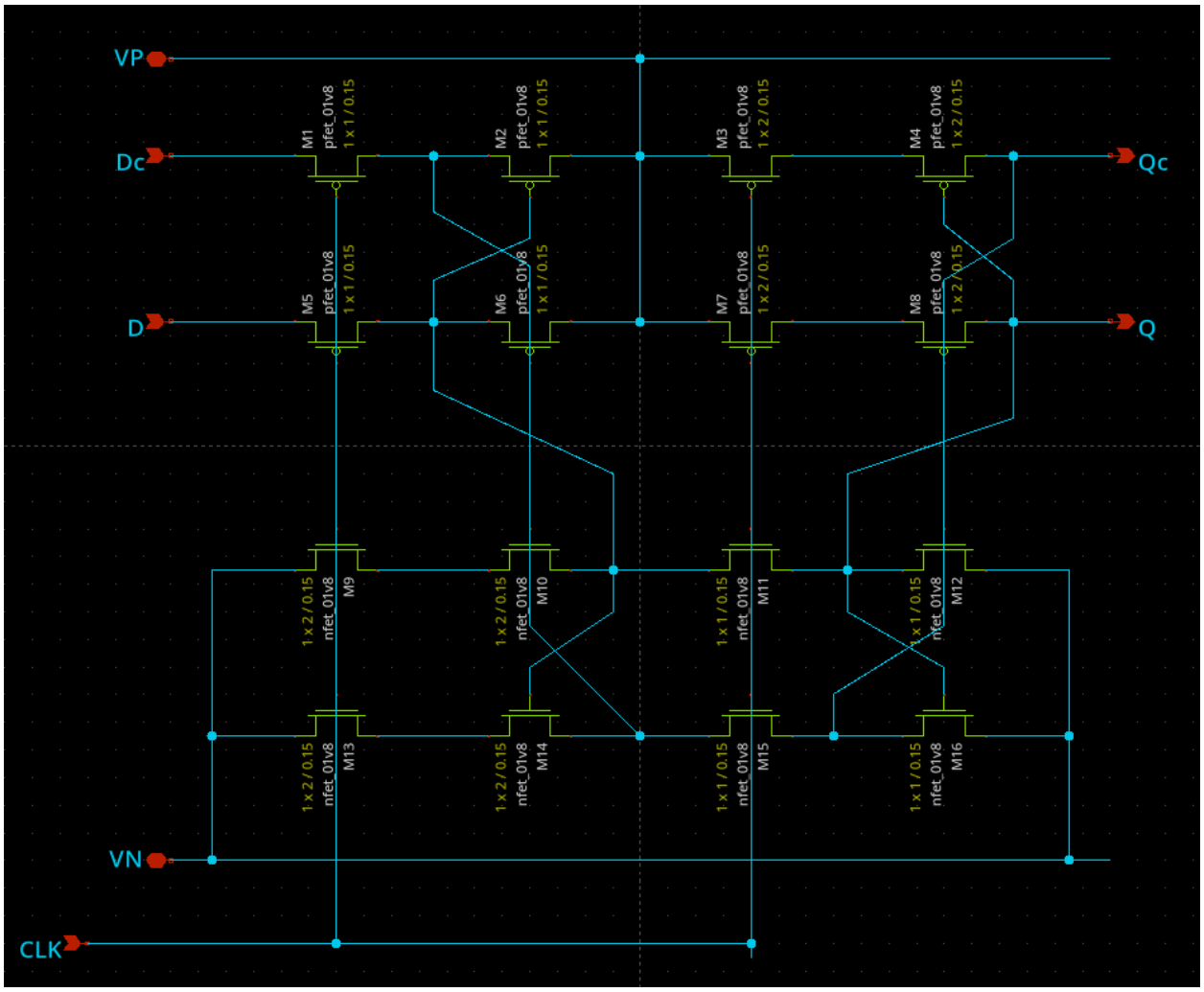
This report presents the design, simulation, and verification of a rising-edge triggered Complementary Set-Reset Logic (CSRL) D flip-flop and its integration into a four-bit shift register. It includes transistor-level schematics, Xschem transient simulations across all process corners (TT, FF, SS, FS, SF), and Magic layouts verified through DRC and LVS. The attached GitHub repository contains all schematic files, circuit symbols, layout cells, simulation test benches, and extracted netlists used for the project. Key screenshots throughout the project are displayed in the report.

Github Repository Link:
https://github.com/Ahan-Trivedi2/Mixed-Analog-Digital-VLSI/tree/main/Miniproject2

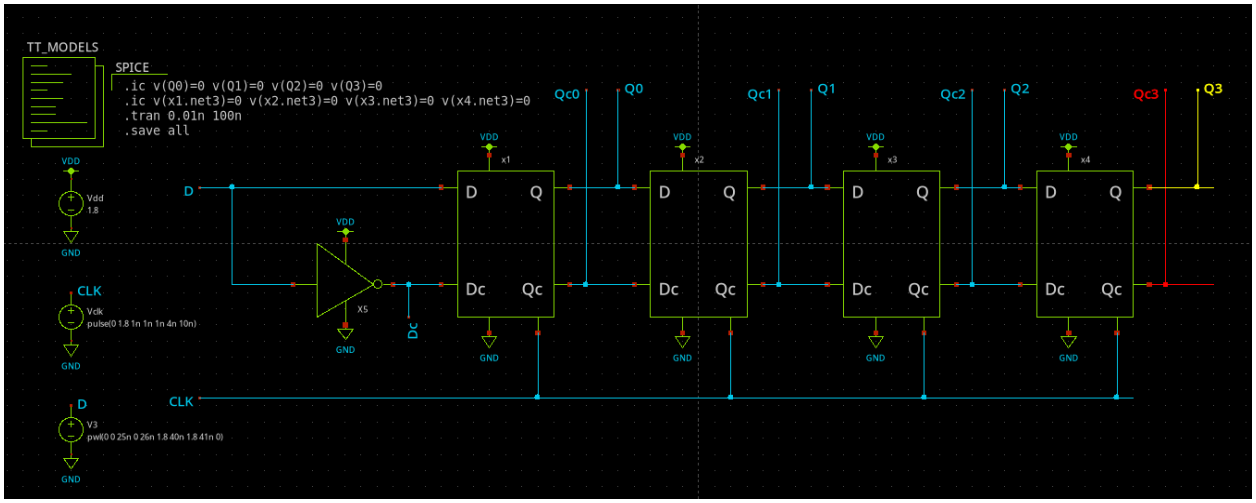
Schematic Capture and Simulation

D flip-flop transistor level schematic:




VP
Dc
D
VN
CLK
Qc
Q
M1 pfet_01v8 1 x 1 / 0.15
M2 pfet_01v8 1 x 1 / 0.15
M3 pfet_01v8 1 x 2 / 0.15
M4 pfet_01v8 1 x 2 / 0.15
M5 pfet_01v8 1 x 1 / 0.15
M6 pfet_01v8 1 x 1 / 0.15
M7 pfet_01v8 1 x 2 / 0.15
M8 pfet_01v8 1 x 2 / 0.15
M9 nfet_01v8 1 x 2 / 0.15
M10 nfet_01v8 1 x 2 / 0.15
M11 nfet_01v8 1 x 1 / 0.15
M12 nfet_01v8 1 x 1 / 0.15
M13 nfet_01v8 1 x 2 / 0.15
M14 nfet_01v8 1 x 2 / 0.15
M15 nfet_01v8 1 x 1 / 0.15
M16 nfet_01v8 1 x 1 / 0.15

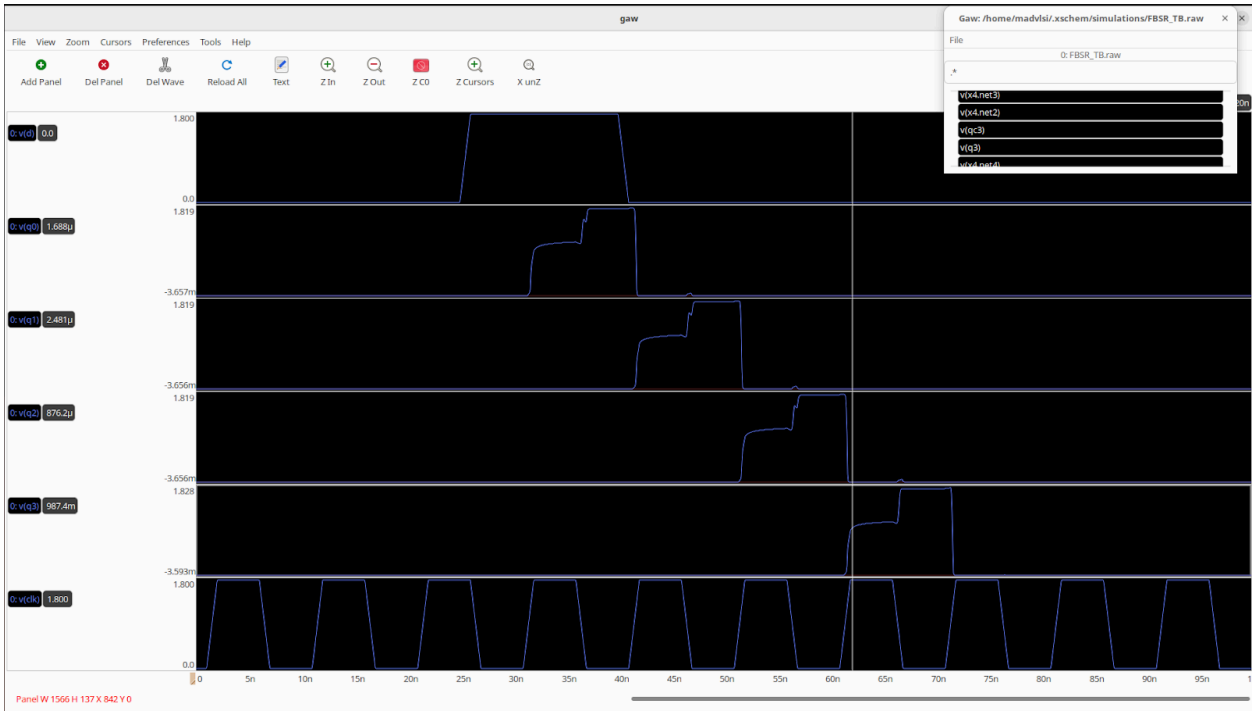
Simulation test harness:



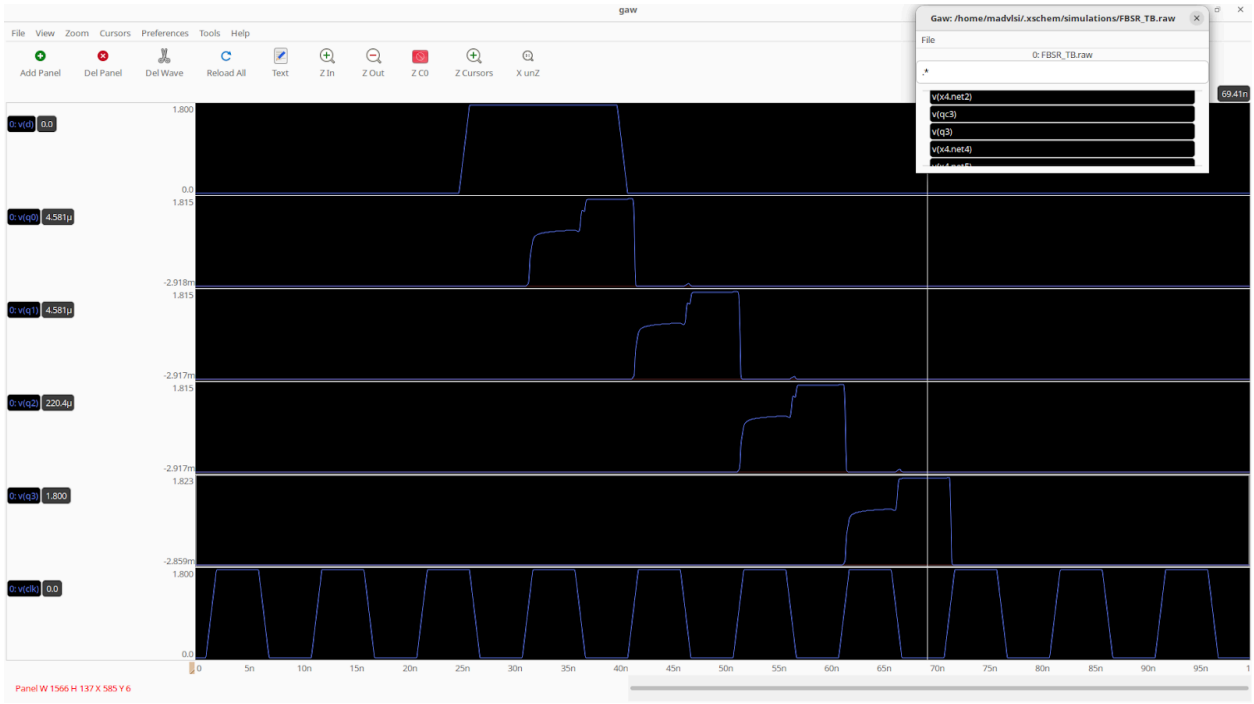
**In this picture, the TT_models from the MADVLSI library were used. I simply swapped out the transistor model type, but used the same test harness.*

Plots for transient simulations from TT, FF, SS, FS, and SF corner models:

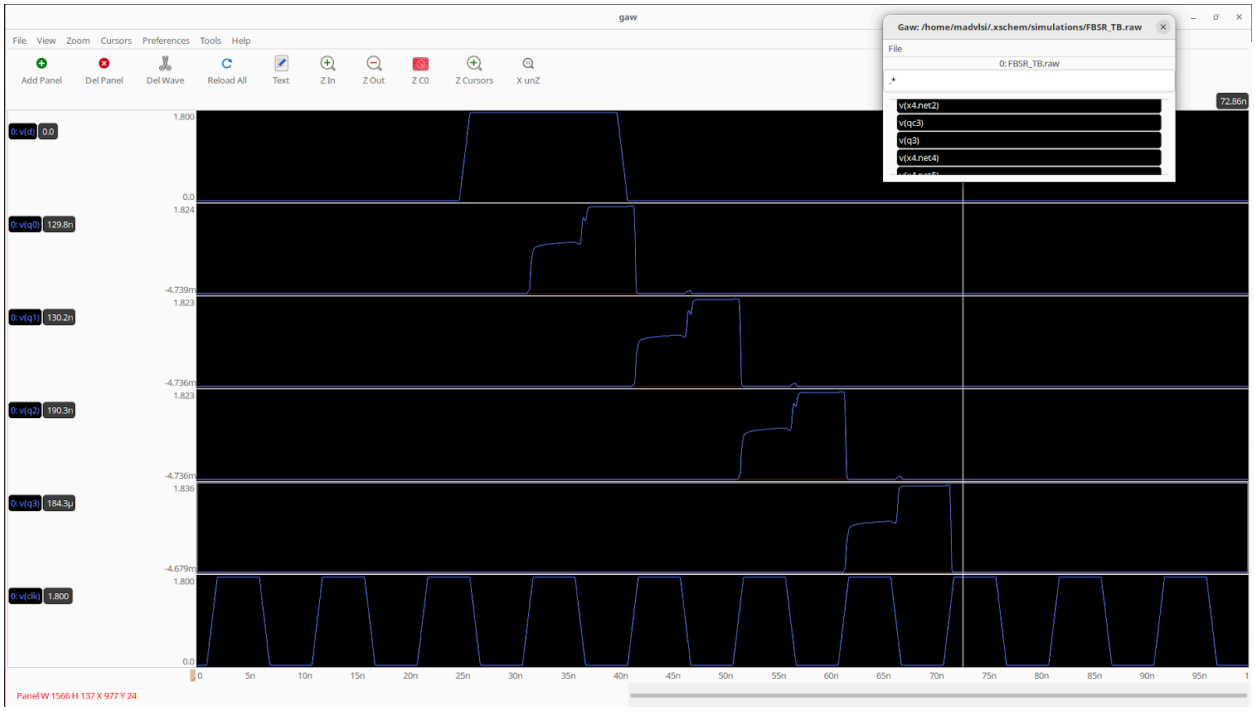
TT



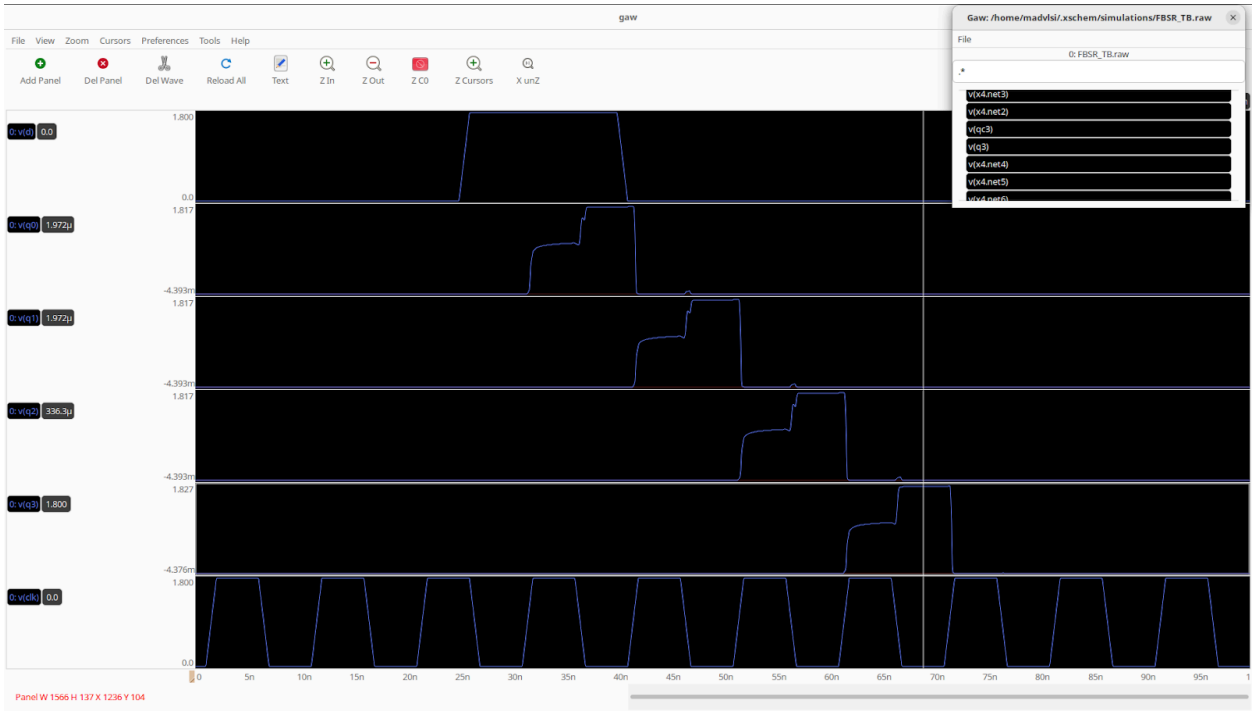
FF


gaw
File View Zoom Cursors Preferences Tools Help
Add Panel
Del Panel
Del Wave
Reload All
Text
Z In
Z Out
Z C0
Z Cursors
X unZ
Gaw: /home/madvlsi/.xschem/simulations/FBSR_TB.raw
File
0: FBSR_TB.raw
.*
v(x4.net2)
v(qc3)
v(q3)
v(x4.net4)
69.41n
0: v(d) 0.0
0: v(q0) 4.581µ
0: v(q1) 4.581µ
0: v(q2) 220.4µ
0: v(q3) 1.800
0: v(clk) 0.0
1.800
0.0
1.815
-2.918m
-2.917m
1.823
-2.859m
0 5n 10n 15n 20n 25n 30n 35n 40n 45n 50n 55n 60n 65n 70n 75n 80n 85n 90n 95n
Panel W 1566 H 137 X 585 Y 6

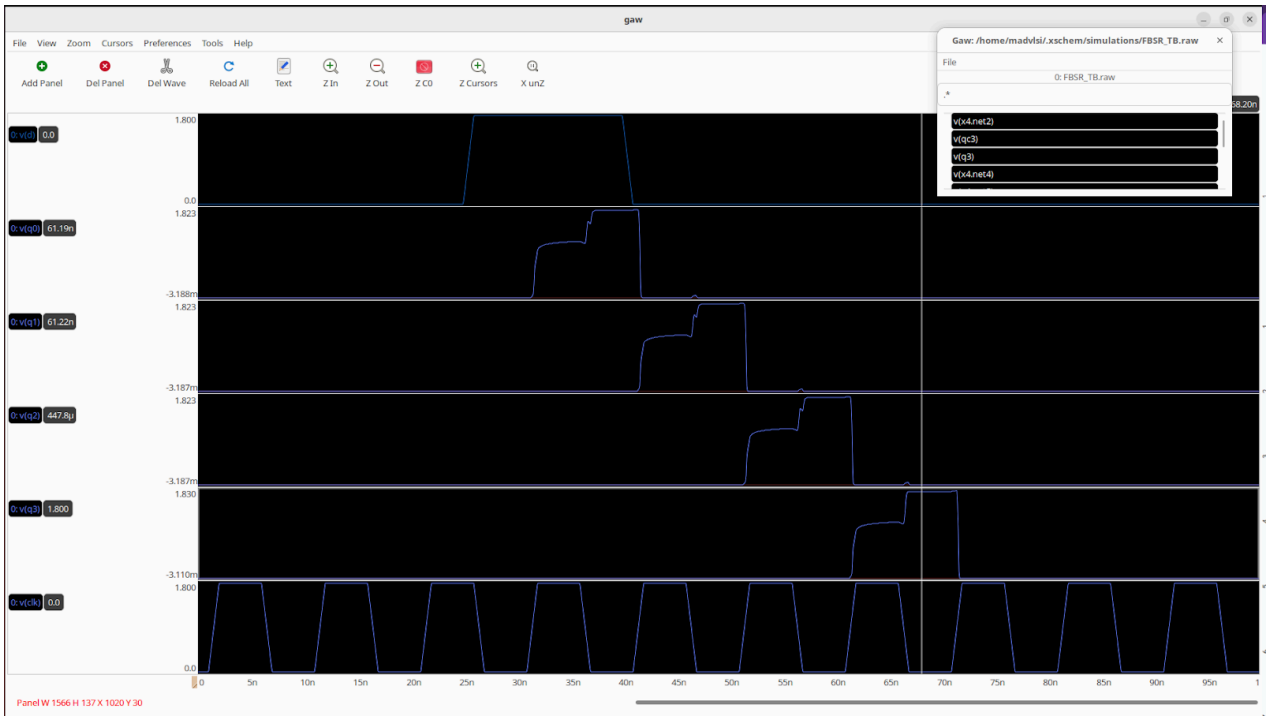
SS


gaw
File View Zoom Cursors Preferences Tools Help
Add Panel
Del Panel
Del Wave
Reload All
Text
Z In
Z Out
Z C0
Z Cursors
X unZ
Gaw: /home/madvlsi/.xschem/simulations/FBSR_TB.raw
File
0: FBSR_TB.raw
.*
v(x4.net2)
v(qc3)
v(q3)
v(x4.net4)
72.86n
0: v(d) 0.0
0: v(q0) 129.8n
0: v(q1) 130.2n
0: v(q2) 190.3n
0: v(q3) 184.3µ
0: v(clk) 1.800
1.800
0.0
1.824
-4.739m
1.823
-4.736m
1.836
-4.679m
0 5n 10n 15n 20n 25n 30n 35n 40n 45n 50n 55n 60n 65n 70n 75n 80n 85n 90n 95n
Panel W 1566 H 137 X 977 Y 24

FS


gaw
File View Zoom Cursors Preferences Tools Help
Add Panel
Del Panel
Del Wave
Reload All
Text
Z In
Z Out
Z C0
Z Cursors
X unZ
Gaw: /home/madvlsi/.xschem/simulations/FBSR_TB.raw
File
0: FBSR_TB.raw
.*
v(x4.net3)
v(x4.net2)
v(qc3)
v(q3)
v(x4.net4)
v(x4.net5)
0: v(d) 0.0
0: v(q0) 1.972µ
0: v(q1) 1.972µ
0: v(q2) 336.3µ
0: v(q3) 1.800
0: v(clk) 0.0
1.800
0.0
1.817
-4.393m
1.827
-4.376m
0 5n 10n 15n 20n 25n 30n 35n 40n 45n 50n 55n 60n 65n 70n 75n 80n 85n 90n 95n
Panel W 1566 H 137 X 1236 Y 104

SF

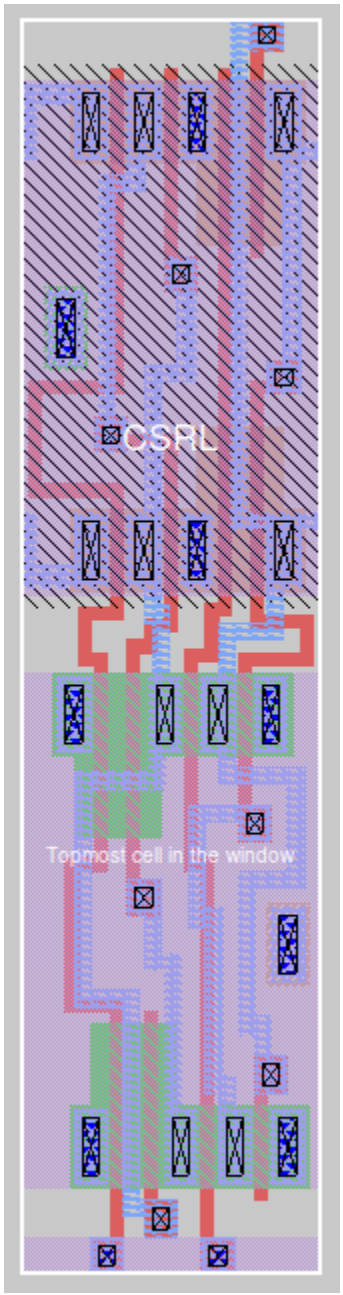

gaw
File View Zoom Cursors Preferences Tools Help
Add Panel
Del Panel
Del Wave
Reload All
Text
Z In
Z Out
Z C0
Z Cursors
X unZ
Gaw: /home/madvlsi/.xschem/simulations/FBSR_TB.raw
File
0: FBSR_TB.raw
.*
v(x4.net2)
v(qc3)
v(q3)
v(x4.net4)
0: v(d) 0.0
0: v(q0) 61.19n
0: v(q1) 61.22n
0: v(q2) 447.8µ
0: v(q3) 1.800
0: v(clk) 0.0
1.800
0.0
1.823
-3.188m
1.823
-3.187m
1.823
-3.187m
1.830
-3.110m
0 5n 10n 15n 20n 25n 30n 35n 40n 45n 50n 55n 60n 65n 70n 75n 80n 85n 90n 95n
Panel W 1566 H 137 X 1020 Y 30

Layout Design

Dimensions of D flip-flop layout:

Width: 3.650 micron
Height: 15.250 micron

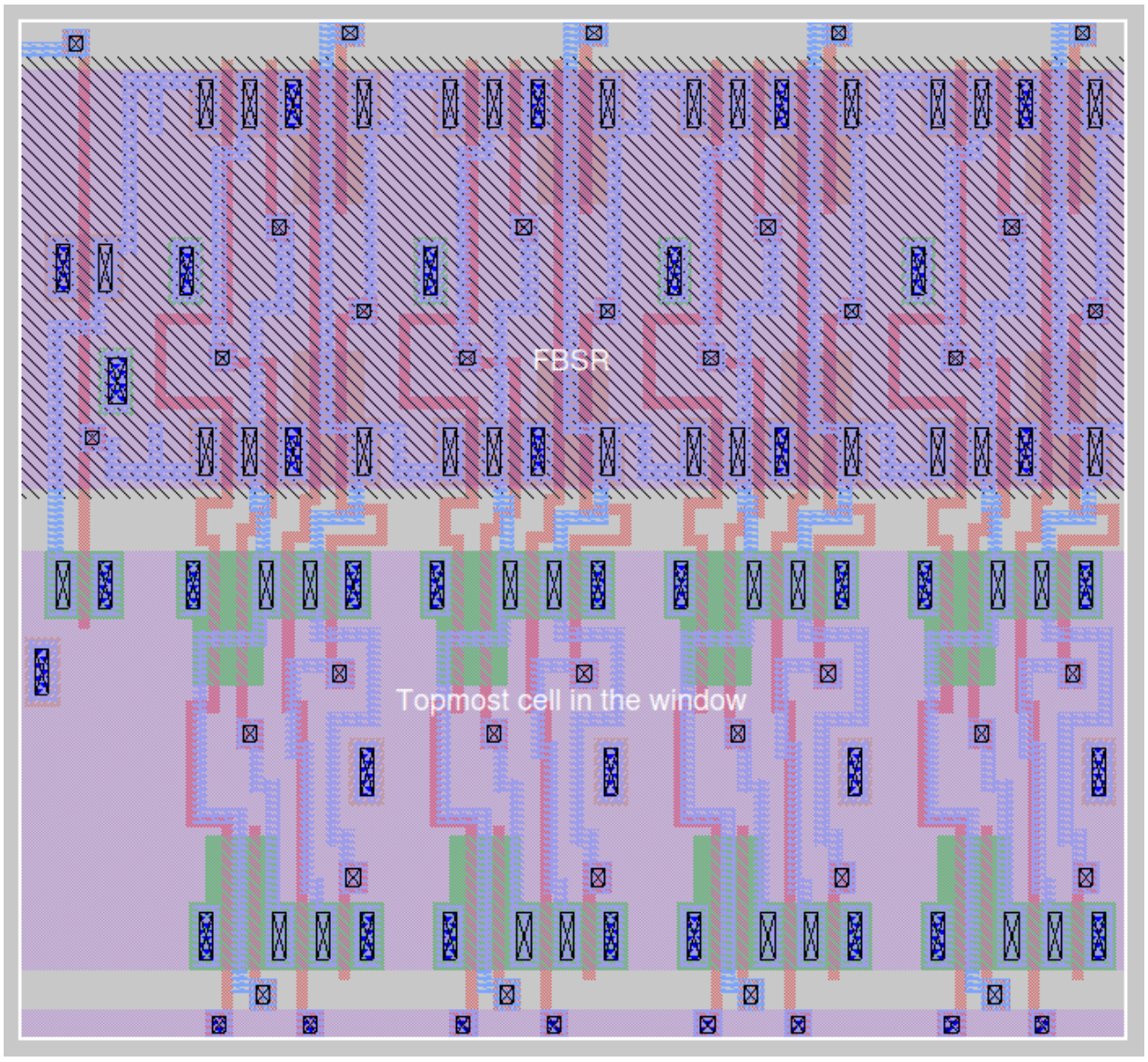
D flip-flop layout:



Dimensions of shift register layout:

Width: 16.550 micron
Height: 15.250 micron

Shift register layout:



Layout Versus Schematic

Terminal Output from LVS:

```
madvlsi@madvlsi-ubuntu-usb:~/Documents/Miniproject2/magic$ lvs FBSR.spice
FBSR_xschem.spice FBSR
Netgen 1.5.299 compiled on Sat Sep  6 02:50:48 PM EDT 2025
Warning: netgen command 'format' use fully-qualified name '::netgen::format'
Warning: netgen command 'global' use fully-qualified name '::netgen::global'
Reading netlist file FBSR.spice
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Reading netlist file FBSR_xschem.spice
Call to undefined subcircuit CSRL_D_FF
Creating placeholder cell definition.
Call to undefined subcircuit inverter
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.

Reading setup file /usr/local/share/pdk/sky130A/libs.tech/netgen/sky130A_setup.tcl

Model sky130_fd_pr__nfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__nfet_01v8
No property sa found for device sky130_fd_pr__nfet_01v8
No property sb found for device sky130_fd_pr__nfet_01v8
No property sd found for device sky130_fd_pr__nfet_01v8
No property nf found for device sky130_fd_pr__nfet_01v8
No property nrd found for device sky130_fd_pr__nfet_01v8
No property nrs found for device sky130_fd_pr__nfet_01v8
No property area found for device sky130_fd_pr__nfet_01v8
No property perim found for device sky130_fd_pr__nfet_01v8
No property topography found for device sky130_fd_pr__nfet_01v8
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
No property area found for device sky130_fd_pr__nfet_01v8
No property perim found for device sky130_fd_pr__nfet_01v8
No property topography found for device sky130_fd_pr__nfet_01v8
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__pfet_01v8
No property sa found for device sky130_fd_pr__pfet_01v8
```

```
No property sb found for device sky130_fd_pr__pfet_01v8
No property sd found for device sky130_fd_pr__pfet_01v8
No property nf found for device sky130_fd_pr__pfet_01v8
No property nrd found for device sky130_fd_pr__pfet_01v8
No property nrs found for device sky130_fd_pr__pfet_01v8
No property area found for device sky130_fd_pr__pfet_01v8
No property perim found for device sky130_fd_pr__pfet_01v8
No property topography found for device sky130_fd_pr__pfet_01v8
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property area found for device sky130_fd_pr__pfet_01v8
No property perim found for device sky130_fd_pr__pfet_01v8
No property topography found for device sky130_fd_pr__pfet_01v8
Comparison output logged to file comp.out
Logging to file "comp.out" enabled
Circuit sky130_fd_pr__pfet_01v8 contains no devices.
Circuit sky130_fd_pr__nfet_01v8 contains no devices.

Contents of circuit 1:  Circuit: 'FBSR'
Circuit FBSR contains 66 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  33
  Class: sky130_fd_pr__pfet_01v8 instances:  33
Circuit contains 37 nets.
Contents of circuit 2:  Circuit: 'FBSR'
Circuit FBSR contains 66 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  33
  Class: sky130_fd_pr__pfet_01v8 instances:  33
Circuit contains 37 nets.

Circuit 1 contains 66 devices, Circuit 2 contains 66 devices.
Circuit 1 contains 37 nets,    Circuit 2 contains 37 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
madvlsi@madvlsi-ubuntu-usb:~/Documents/Miniproject2/magic$
```