Ahan Trivedi

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Education

Olin College of Engineering *Bachelor of Science: Electrical and Computer Engineering* (GPA: 3.9/4.0) May 2027

- **Coursework:** Mixed Analog-Digital VLSI, Computer Architecture, Data Structures and Algorithms, Circuits, Machine Learning, Software Systems, Embedded Systems, Databases, Signals and Systems, Controls, Microelectronics, Data Science

Babson College *Certificate: Finance* May 2027

Software and Hardware Skills

Proficiencies: Analog & Mixed-Signal IC Design, CMOS Device Modeling, VLSI & RTL Design, FPGAs, Layout & Physical Verification (DRC/LVS), Semiconductor Manufacturing and Process, PDK Development, Testbench & Hardware Verification,

Languages: SystemVerilog, Verilog, VHDL, UVM, Perl, Python, TCL, C, C++, Linux, Bash, Powershell, MATLAB

Tools: Magic, Xschem, Skywater130, Vivado, LTSpice, Docker, Kubernetes, Oscilloscope, Multimeter, GTKWave, Netgen

Experience

Micron Technology *Process Integration Engineering Intern (APTD)* Summer 2025

- Led W2W fusion bonding **process integration** (CVD, back-grind, wet-process, CMP, bond) for **High-Bandwidth Memory** proposing a flow deviation that identified a film with **20%** higher bond energy, and presenting findings to **SVPs**.
- Evaluated bond energy across multiple integration modalities using the Maszara test, DCB, XPS, and other **metrology** steps.
- Built **OpenCV/NumPy** pipeline for automated wafer metrology, **cutting extraction time by 40%** via pixel-level analysis.

VdZ Design Automation Lab *Machine Learning Researcher* May 2024 - Present

- Built a **MySQL-Python** pipeline leveraging unsupervised **machine learning** and **NLP** to extract semantic meaning and analyze correlations between user communication patterns and team success in enterprise social networks.
- Deployed an **agentic AI** model via **Hugging Face** to generate and test simulated design team communication data.
- **First author** on accepted conference paper for ASME IDETC DM track; presented findings at the AAAS annual meeting.

Olin Electric Motorsports *Hardware/Firmware Engineer* August 2023 - August 2024

- Collaborated with a team of 30+ engineers to design and build a fully electric Formula SAE race car.
- Designed and **documented** high-voltage **power and sensing circuits** to meet FSAE safety and performance standards.
- Programmed microcontroller **firmware** to parse and transmit **CAN** data to a mobile interface for real-time diagnostics.

Velo3D Inc. *Product Engineering Intern* Summer 2023

- Designed and improved manufacturing methods in Laser Sinter 3D Print process, **decreasing failure rate by 40%**.
- Prototyped and assembled **custom monitoring circuits** to measure voltage and temperature in laser-beam fusion printers,
- Swift resolution of **electrical** issues with laser-beam fusion printers, addressing power delivery failure of **optical systems**.

Projects and Research Publications

7-Bit MOSFET-Based Digital-to-Analog Converter | *Mixed-Signal Design, Xschem, Magic, LVS, netgen, SPICE* November 2025

- Built a 7-bit current-steering **MOSFET DAC** using FVF cells, cascode CM's, and a bootstrap bias generator in **Skywater130**
- Simulated DNL/INL and Monte Carlo mismatch in **Ngspice** and analyzed results in MATLAB.
- Completed full layout with analog design practices (mirroring common-centroid matching) and **LVS/DRC** verification.

CSRL D Flip-Flop FBSR | *Digital Design, Xschem, Magic, LVS, netgen, SPICE* October 2025

- Designed a **CSRL D flip-flop** into a 4-bit shift register at **SkyWater 130 nm** to explore sequential CMOS logic design.
- Simulated functionality and propagation delay across **TT/FF/SS process corners** using **Ngspice**.
- Completed **layout**, **DRC**, and **LVS** verification, demonstrating manufacturable digital logic implementation.

32-Bit RISC-V RV32IM Processor | *SystemVerilog, GTKWave, Computer Architecture, FPGA Design* April 2025

- Built a **multi-cycle RV32IM** processor supporting integer and multiply/divide instructions in SystemVerilog.
- Integrated **memory module** using funct3 decoding for byte/halfword/word accesses and instruction fetch.
- Designed **ALU**, control FSM, register file, and program counter; verified on hardware and with **GTKWave** simulation.

Google Scholar: https://scholar.google.com/citations?user=DoJZKGEAAAAJ&hl=en&oi=ao Updated 2025