Miniproject 3
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The goal of this project was to design a digital circuit that generates a continuous sinusoidal voltage waveform using a 10-bit R-2R ladder DAC in the OSS Cad Suite FPGA Toolchain, while minimizing memory usage. Rather than storing all 512 samples for a full sine wave cycle, the design stores only the first 128 samples corresponding to the first quarter cycle (0 to $\pi/2$), then reconstructs the remaining three quarters using symmetry. To ensure accuracy, the values were pulled directly from the example GitHub repository, which included a verified 512-value sine wave. The first 128 entries were extracted and saved in quarter_waveform.txt, then loaded into a read-only memory structure at runtime using $readmemh. This approach preserved waveform accuracy while reducing storage by 75%.

The circuit's core logic is implemented in Miniproject3.sv. A 9-bit counter named sample_index drives waveform progression, incrementing from 0 to 511 to represent one complete cycle. The counter output feeds into a combinational logic block that determines which quadrant of the waveform the index belongs to, and how to retrieve or modify the base LUT values accordingly. Specifically, quadrant 1 (sample_index < 128) reads directly from the lookup table. Quadrant 2 mirrors the index, quadrant 3 inverts the amplitude, and quadrant 4 both mirrors and inverts. This quadrant-specific logic is implemented cleanly in an always_comb block, which outputs a 10-bit value to dac_output. The DAC output is then split into 10 individual bits, each connected to a pin on the FPGA that drives one input of the R-2R ladder DAC.

System-level operation was verified through simulation and hardware testing. The testbench in Miniproject3_tb.sv provides a basic clock signal and stimulus to the waveform generator, running for enough time to observe multiple waveform cycles. The output was simulated using OSS CAD Suite tools — specifically, iverilog for compilation and GTKWave for waveform visualization. Simulation confirmed smooth transitions across all quadrants and verified that the mirroring and inversion logic was functioning correctly. After simulation, the circuit was deployed to an iceBlinkPico board, and the resulting DAC output was visualized using an oscilloscope. The measured waveform matched the ideal sinusoid in both shape and timing, confirming that the symmetry logic and LUT structure worked correctly in hardware.

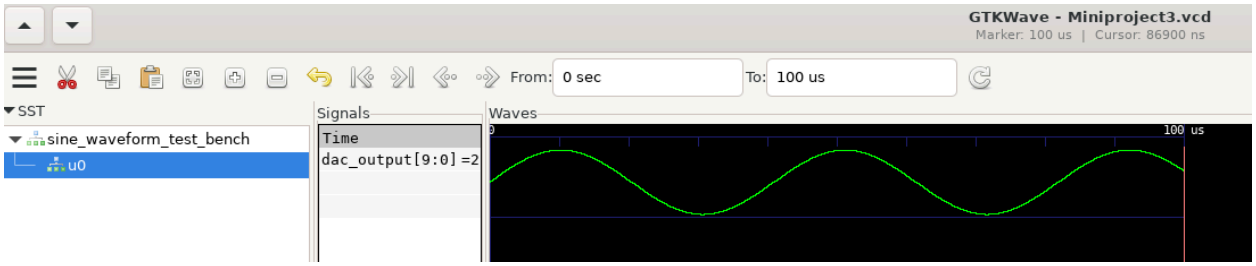

Figure 1. GTKWave simulation output showing more than one full cycle of the generated sine wave over time.

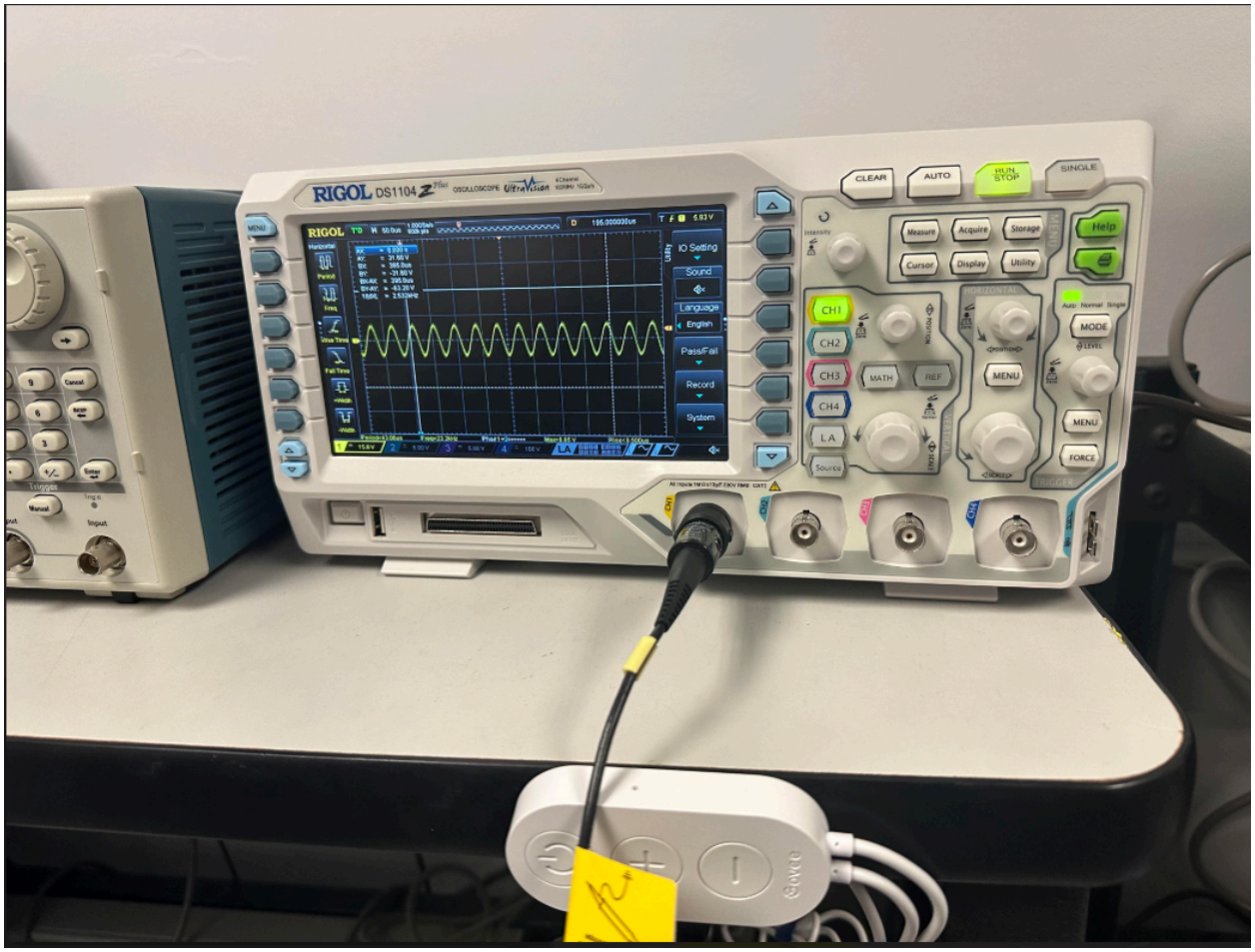

Figure 2. Oscilloscope capture of the analog sine wave output generated by the FPGA and 10-bit R-2R DAC circuit