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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

DIGITAL VLSI DESIGN

Experiential Learning Report

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In partial fulfillment of the requirements for the degree of

BACHELOR OF ENGINEERING
in

ELECTRONICS AND COMMUNICATION ENGINEERING
2023-2024

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1.Problem Statement

Problem Statement

Design a digital bank token number display system that generates sequential token numbers for a bank, starting from 00 and incrementing up to 99. The system should display the current token number on a seven-segment display in Binary Coded Decimal (BCD) format. The design should incorporate the following components:

2-input, 3-input, and 4-input NAND gates

2-input and 3-input NOR gates

4-input and 5-input OR gates

JK flip-flop with negative edge triggering

The system should consist of two cascaded 4-bit up counters, each capable of counting from 0 to 9. The output of the first counter should serve as the input to the second counter to create a modulo-100 counter. The final output of the counter should be decoded using a 7-segment decoder to display the token number on the seven-segment display.

2. Introduction

2. Introduction

Token issue systems have become indispensable infrastructural components, transforming the landscape of customer service and operational efficiency across a myriad of sectors encompassing banking, transportation hubs like airports, governmental offices, healthcare facilities such as hospitals and doctor's clinics, as well as the hospitality industry including restaurants and hotels. These systems, tailored to mitigate the perennial challenge of prolonged queues and wait times, epitomize a paradigm shift in the way patrons experience service delivery. By allocating numbered tokens on a fair and equitable basis, typically adhering to the first-come-first-serve principle, token issue systems revolutionize the waiting paradigm by affording individuals the luxury of waiting in comfort until their designated number is summoned, obviating the need for protracted periods of standing in serpentine queues. This customer-centric approach not only mitigates the vexations associated with protracted wait times but also engenders an environment conducive to enhanced staff productivity and resource optimization. Activation of a simple push switch by attendants signals the availability of a service counter, prompting the display to exhibit the corresponding token number, thus facilitating a seamless transition for patrons. This methodical modus operandi underscores the commitment to impartiality and efficiency in service delivery, curtailing the likelihood of discord and discontent among patrons. Moreover, the user-friendly nature and streamlined maintenance protocols associated with these systems render them accessible and adaptable to establishments of varying scales, with installation and upkeep requiring minimal technical acumen. In banking realms, the deployment of digital token issuance represents a linchpin in the orchestration of payment processes, ensuring a methodical and expeditious disbursement of services to clientele. In essence, token issue systems herald a new era in queue management technology, serving as an enabler of enhanced customer satisfaction and operational efficacy, poised to catalyze transformative change across multifarious industries.

In this project, we aim to design a digital bank token number display using digital circuits. The display will count from 00 to 99 using a cascaded 4-bit up counter. The design includes various logic gates, JK flip-flop, and a 7-segment decoder to display the count on a common cathode 7-segment display.

3. Design Process

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⇨ JK Flip-Flop Design:

We begin by constructing a JK flip-flop utilizing NAND gates, configuring it to operate on negative edge triggering. This JK flip-flop will serve as the fundamental memory element in our counter design, effectively storing and manipulating binary information.

⇨ 4-Bit Up Counter Design:

Next, we embark on the creation of a 4-bit up counter, utilizing a series of cascaded JK flip-flops. With each clock pulse, the counter increments by one, systematically progressing through its binary count. When the count reaches its maximum value of 9 (represented as 1001 in binary), it cyclically resets to 0 (0000), thus perpetuating the counting cycle seamlessly.

⇨ Mod 100 Counter (Cascaded Counters):

To extend our counting range from 00 to 99, we employ the principle of cascading by linking two 4-bit up counters together. The output of the first counter acts as the input to the second, ensuring that upon reaching its maximum count of 9 and resetting, it triggers the incrementation of the second counter. This synchronized operation allows us to achieve a comprehensive count range from 00 to 99, catering to a wide array of numerical requirements.

⇨ 7-Segment Decoder:

To translate the binary-coded decimal (BCD) output of our mod 100 counter into a format suitable for display, we integrate a 7-segment decoder into our design. This decoder functions as the intermediary between the digital counter output and the visual representation on the 7-segment display, converting the BCD input into signals capable of driving the individual segments of the display. Through this seamless integration, we ensure that the numerical information stored within our counter is conveyed accurately and comprehensibly to the end user, facilitating intuitive interpretation and interaction with the displayed data.

4. Component Used

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- ⇨ NAND Gates:

NAND gates are digital logic gates that perform the operation of the logical NAND function.

They have two or more inputs and one output.

The output is high (1) only when all inputs are low (0).

In this project, NAND gates are primarily used for constructing the JK flip-flop and other logic functions required for counting and control.

- ⇨ NOR Gates:

NOR gates are digital logic gates that perform the operation of the logical NOR function.

They have two or more inputs and one output.

The output is low (0) only when all inputs are high (1).

NOR gates might be used in various parts of the project for logical operations.

- ⇨ JK Flip-Flop:

A JK flip-flop is a sequential logic circuit with two inputs (J and K), a clock input (CLK), and two outputs (Q and Q').

It can store one bit of data and is commonly used in counters, shift registers, and memory storage applications.

JK flip-flops can be constructed using various logic gates, such as NAND gates in this project.

- ⇨ 4-Bit Up Counter:

A 4-bit up counter is a digital circuit that counts in binary from 0000 to 1111 (0 to 15 in decimal) and then resets.

It consists of four flip-flops, each representing one bit of the count.

The counter increments by one on each clock cycle.

In this project, four JK flip-flops are connected in cascade to form the 4-bit up counter.

- ⇨ Cascaded Counters:

Cascaded counters are multiple counters connected in series, where the output of one counter is connected to the input of the next counter.

In this project, two 4-bit up counters are cascaded to create a mod 100 counter, allowing counting from 00 to 99.

⇨ 7-Segment Display Decoder:

A 7-segment display decoder is a digital circuit that converts binary-coded decimal (BCD) input into signals that can drive a 7-segment display to represent decimal numbers (0-9).

It typically has four input lines (BCD inputs) and seven output lines (segments of the display).

Each output corresponds to one segment of the 7-segment display.

The decoder is essential for converting the binary count into a readable display format.

5. Implementation

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⇨ JK Flip-Flop Construction:

To construct a JK flip-flop using NAND gates, we first need to understand the functionality of a JK flip-flop. A JK flip-flop is a type of sequential logic circuit with two inputs (J and K), one clock input (CLK), and two outputs (Q and Q'). It has four possible input combinations: J=0, K=0 (no change), J=0, K=1 (reset), J=1, K=0 (set), and J=1, K=1 (toggle).

Here's how we can implement a JK flip-flop using NAND gates:

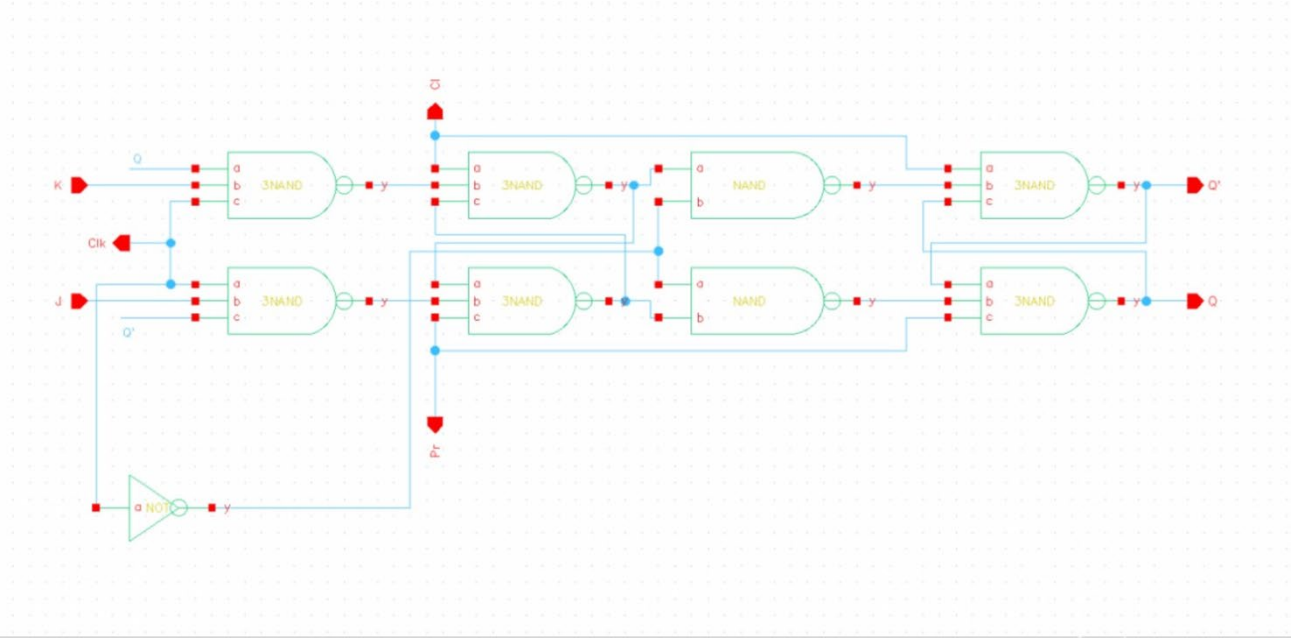

Fig: jk ff schematics using Nand

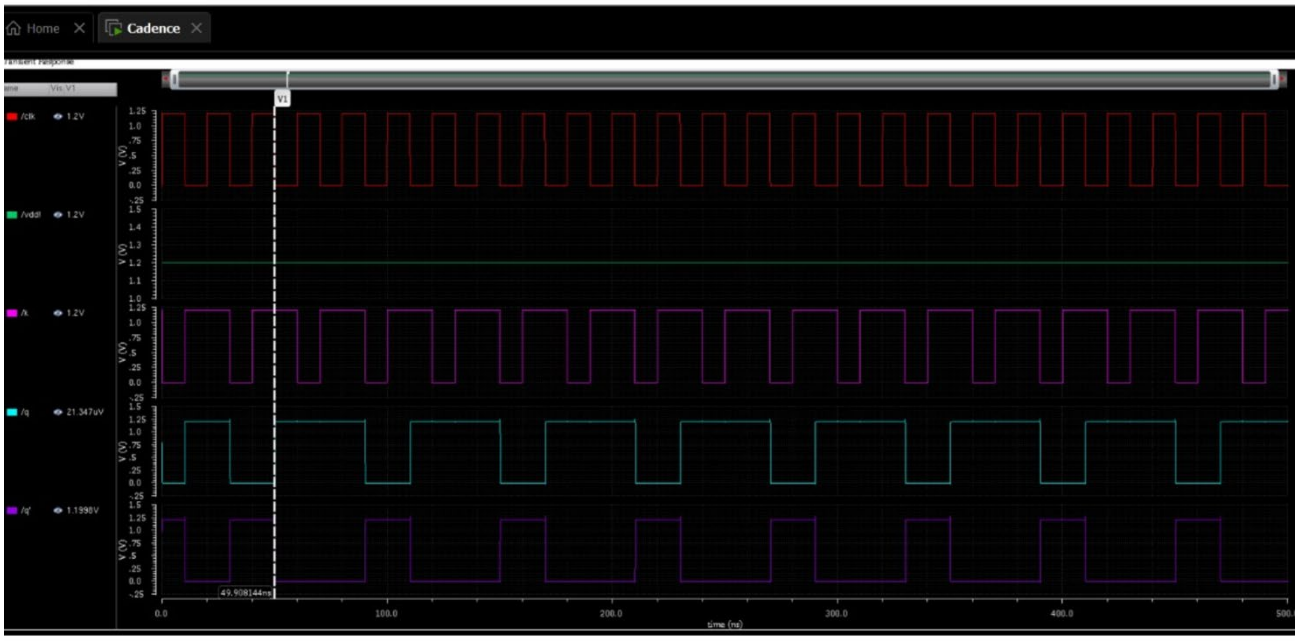

Fig: jk FF output

Latch Construction: We start by creating a latch using two NAND gates. Connect the output of each gate to one of the inputs of the other gate and tie one input of each gate to the opposite input. This creates a basic latch.

Feedback Loop: To make it a JK flip-flop, we introduce the clock input (CLK). We use a NAND gate with one input connected to CLK and the other input connected to one of the inputs (either J or K) of the latch. This creates a negative-edge triggered flip-flop.

Negative Edge Triggering: With the clock input connected to one input of the NAND gate, the other input of the NAND gate is connected to the complement of the clock signal. This ensures that the flip-flop toggles its state on the falling edge of the clock signal.

- ⇨ 4-Bit Up Counter Implementation:

Connection of Flip-Flops: Connect four JK flip-flops in cascade, also known as a ripple counter configuration. The output Q of each flip-flop serves as the input J of the next flip-flop, while the clock (CLK) signal is applied to the clock input of the first flip-flop.

Clock Signal: The clock signal is connected to the clock input (CLK) of the first flip-flop. Each flip-flop will toggle its state (count up) on the rising edge of the clock signal.

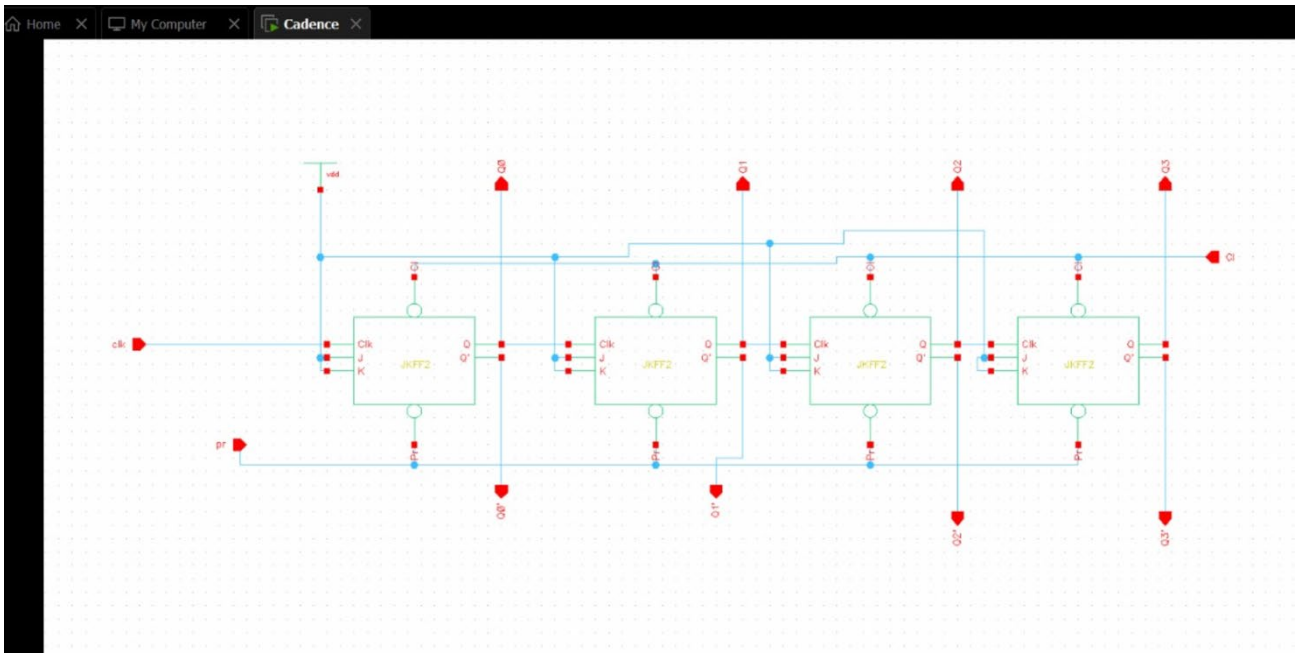

Fig: Circuit of 4-bit up counter

- ⇨ Cascaded Counters (Mod 100 Counter):

Connection of Counters: Connect the output Q3 (most significant bit) of the first 4-bit up counter to the input J of the first flip-flop of the second 4-bit up counter. This ensures that the second counter increments when the first counter overflows (reaches 9).

Synchronization: Ensure that there is proper synchronization between the two counters. This means that the clock signal must be stable and synchronized for both counters to prevent any timing issues.

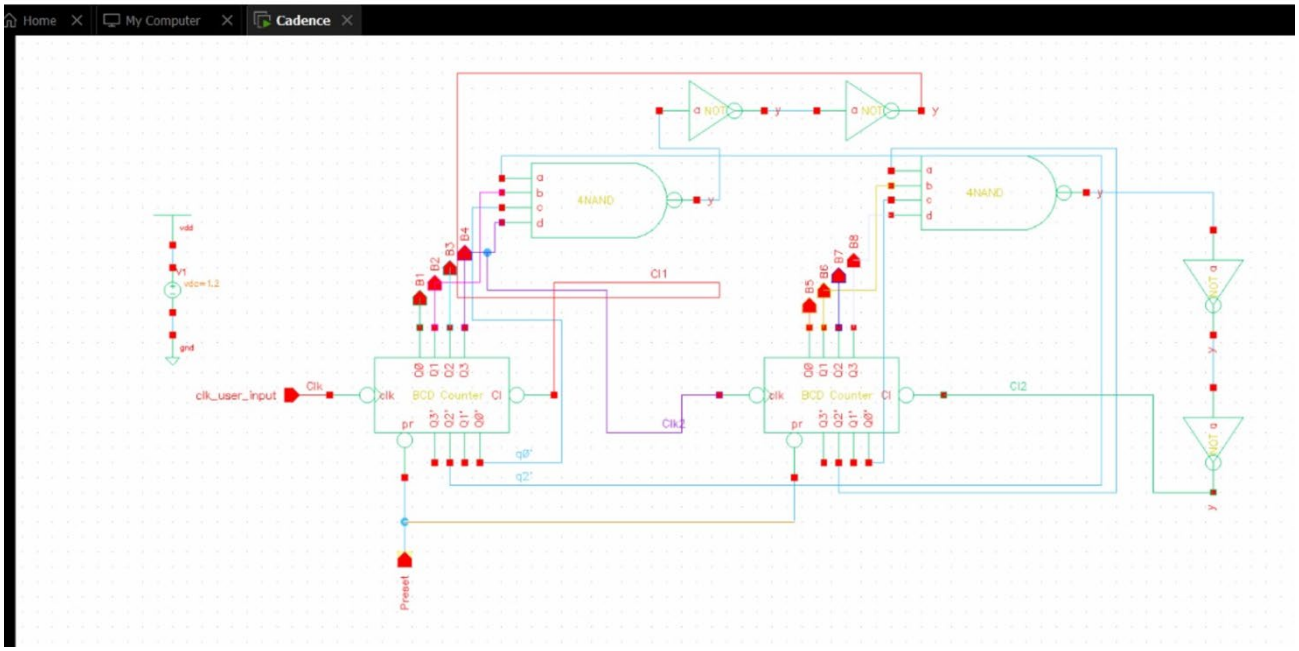

Fig: mod100 counter circuit

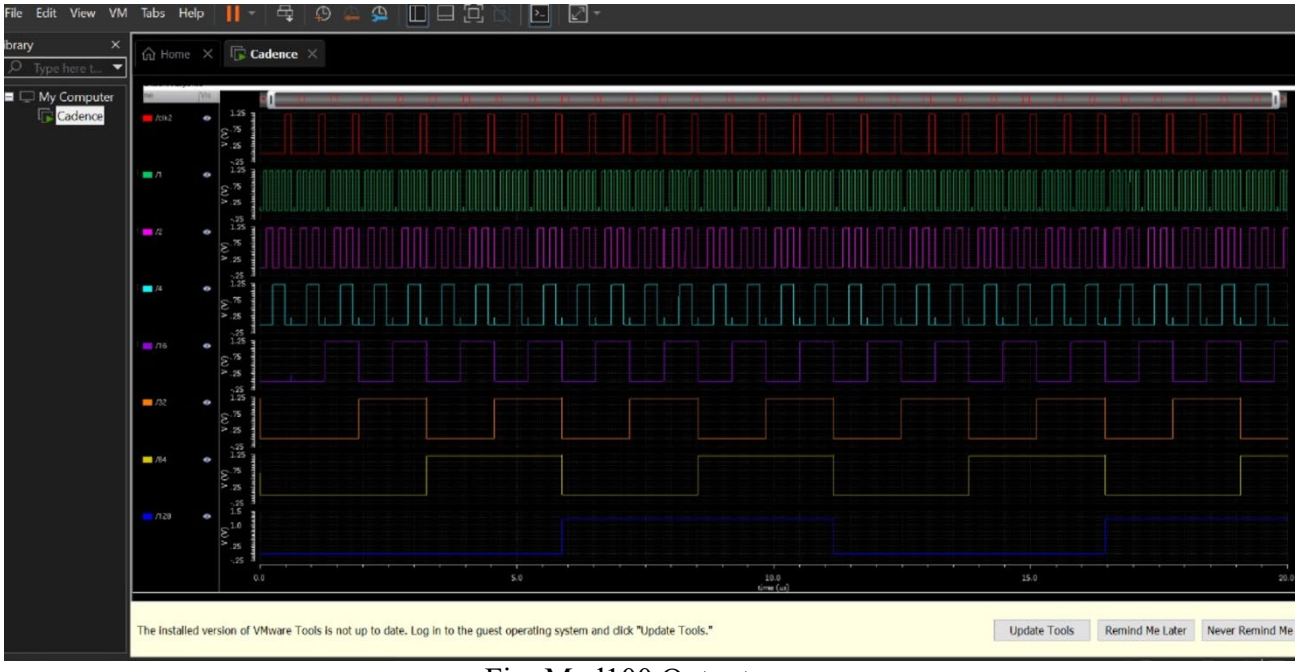

Fig: Mod100 Output

⇨ 7-Segment Display Connection:

Output of Mod 100 Counter: The output of the mod 100 counter, which represents the BCD value (0-99), is connected to the input of the 7-segment decoder.

7-Segment Decoder: The BCD input is decoded by the 7-segment decoder into signals that drive the segments of the 7-segment display. Each BCD digit corresponds to a specific combination of segments to display the corresponding number.

Segment Connection: Wire the outputs of the 7-segment decoder to the corresponding segments of the 7-segment display, ensuring that each segment is appropriately connected to display the desired numbers (0-9).

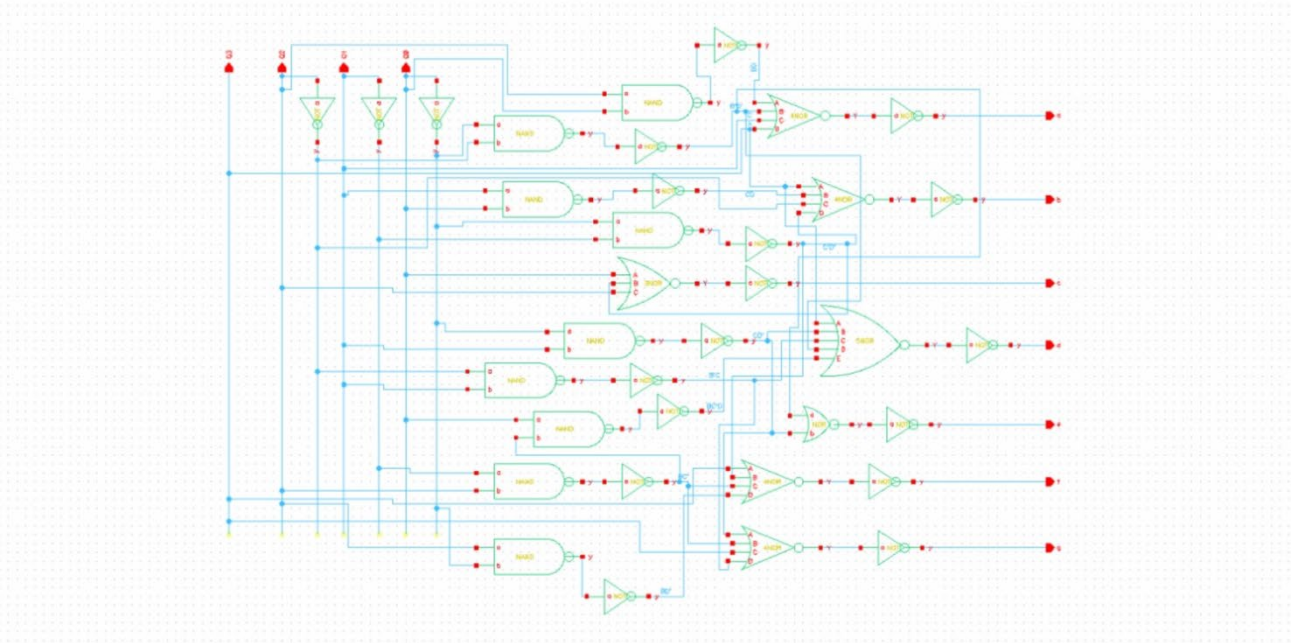

Fig: BCD to 7segment decoder

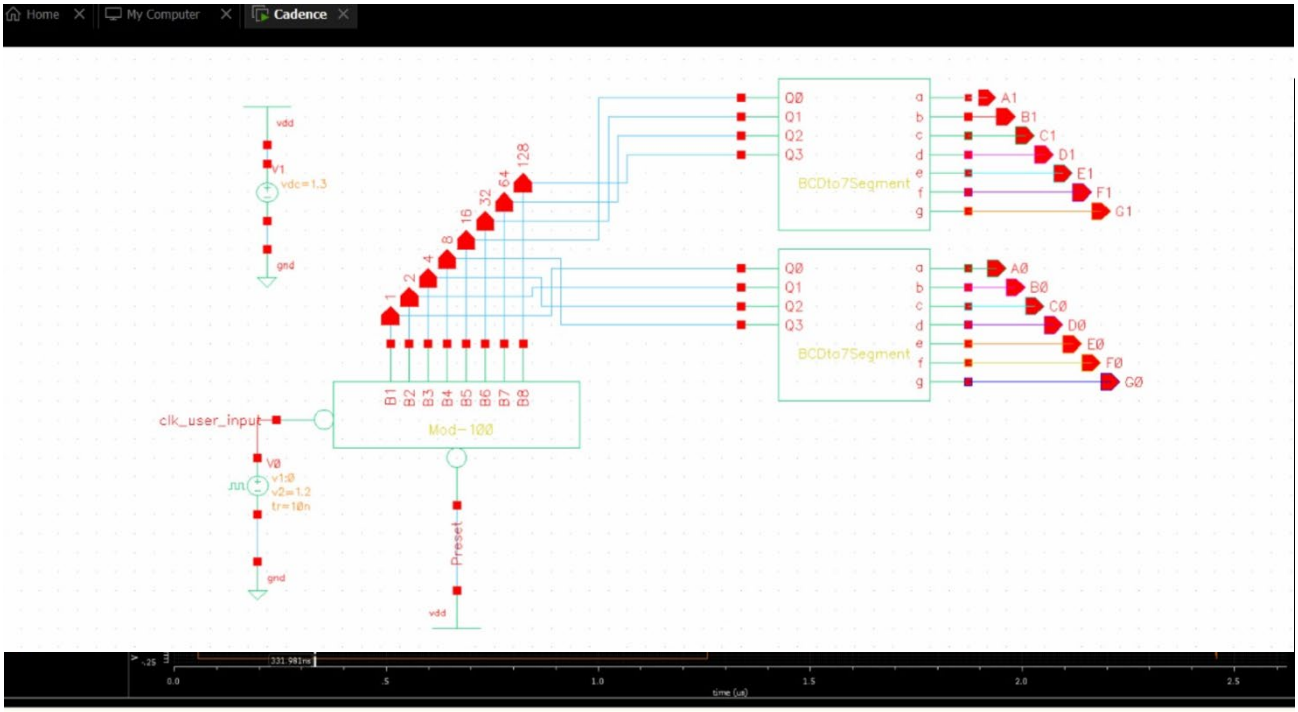

Fig: FINAL TEST BENCH FOR MOD100 TO 7 SEGMENT DISPLAY

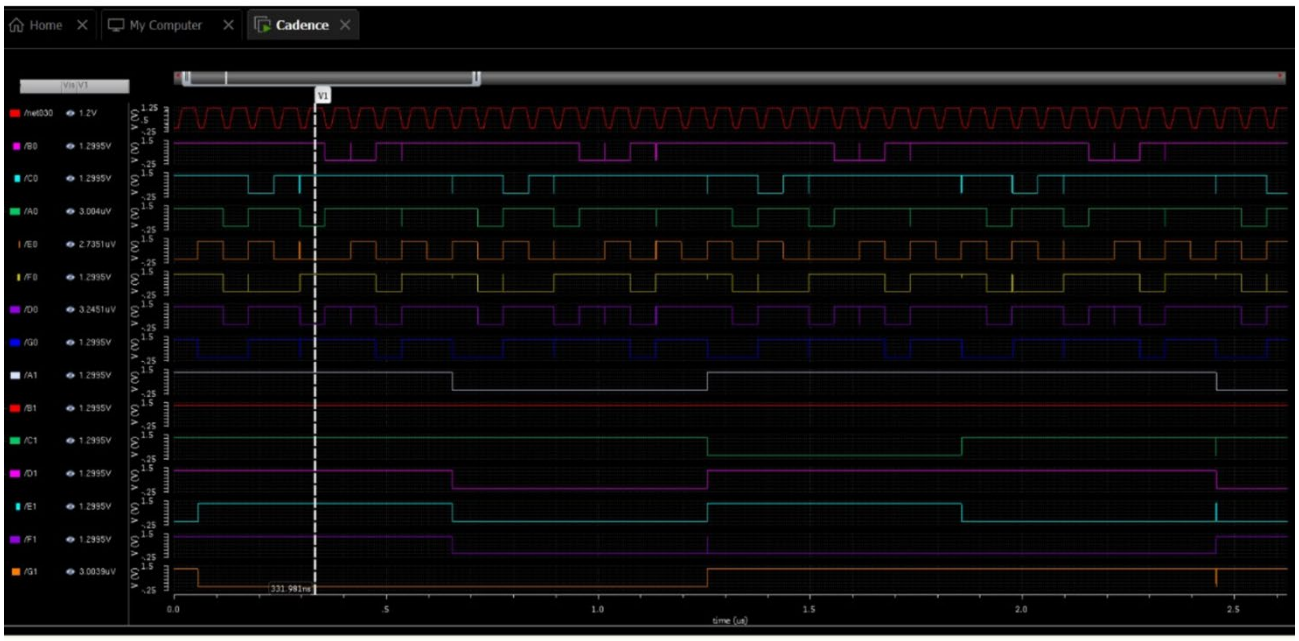

Fig: Final BCD to 7 segment display output

6. Conclusions

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The undertaken project presented formidable challenges, requiring a comprehensive approach to address. Our development of the "BANK TOKEN ISSUE SYSTEM" represents more than a mere replication of existing market models; it embodies a pioneering research endeavor poised to redefine industry standards. In light of the escalating demands of industrialization, the imperative for sophisticated interfacing systems has become increasingly apparent. The repercussions of inadequate time management and data oversight within industrial settings have been starkly evident.

The primary objective of this project is to facilitate seamless data management across diverse units within large-scale enterprises, particularly within multifaceted industrial plants. The automation of token issuance stands as a critical feature, particularly within the evolving landscape of banking services in India. The automatic allocation of tokens to customers is indispensable, serving as a cornerstone function in enhancing operational efficiency and customer satisfaction within banking institutions.

Furthermore, the versatility of token display systems extends beyond the banking sector, finding utility in various public-facing domains such as airports, governmental offices, healthcare facilities, and hospitality establishments. By leveraging these systems, organizations can optimize customer flow, eliminating the need for prolonged queuing and enhancing overall service delivery.

In essence, our project not only addresses immediate operational needs but also anticipates and aligns with the evolving demands of modern industries. By championing innovation and efficiency, we endeavor to set new benchmarks for excellence in data management and customer service across diverse sectors.