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STATIC TIMING ANALYSIS OF D FLIP FLOP USING OPENROAD

An Internship Report (21ECI57)

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Electronics and Communication Engineering 2023-24

RV College of Engineering®, Bengaluru

(*Autonomous institution affiliated to VTU, Belagavi*)

Department of Electronics and Communication Engineering

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Certified that the internship (21ECI57) work titled **STATIC TIMING ANALYSIS OF D FLIP FLOP USING OPENROAD** is carried out by **Ahan Tejaswi (1RV21EC010)** who is bonafide student of RV College of Engineering, Bengaluru, in partial fulfillment of the requirements for the degree of **Bachelor of Engineering in Electronics and Communication** Engineering of the Visvesvaraya Technological University, Belagavi during the year 2023-24. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the minor project report deposited in the departmental library. The internship project report has been approved as it satisfies the academic requirements in respect of internship project work prescribed by the institution for the said degree.

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DECLARATION

I, **Ahan Tejaswi** students of fifth semester B.E., Department of Electronics and Communication Engineering, RV College of Engineering, Bengaluru, hereby declare that the internship project titled '**STATIC TIMING ANALYSIS OF D FLIP FLOP USING OPENROAD**' has been carried out by me and submitted in partial fulfilment for the award of degree of **Bachelor of Engineering** in **Electronics and Communication Engineering** during the year 2023-24.

Further I declare that the content of the dissertation has not been submitted previously by anybody for the award of any degree or diploma to any other university.

I also declare that any Intellectual Property Rights generated out of this project carried out at RVCE will be the property of RV College of Engineering, Bengaluru and we will be one of the authors of the same.

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Lastly, I take this opportunity to thank my family members and friends who provided all the backup support throughout the project work.

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This is to certify that

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pursuing B.E in Electronics and Communication Engineering, RV College of Engineering, Bengaluru, has satisfactorily completed 4 weeks of internship at

Centre for Integrated Circuits and Systems

from 6th November to 2nd December 2023

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SYNOPSIS

In the realm of Very Large-Scale Integration (VLSI), precision and foresight are paramount to ensure the seamless functionality of integrated circuits (ICs). This report encapsulates the journey through an internship focused on Static Timing Analysis (STA), which delved into critical aspects of the VLSI design flow. The internship aimed to optimize parameters crucial for robust digital circuit operation, addressing challenges from project specification to manufacturing.

The internship commenced with an immersive exploration of the VLSI design flow, elucidating each stage from project specification to manufacturing. Understanding the intricacies of each phase laid the foundation for comprehensive comprehension of subsequent STA endeavors. A pivotal objective was mastering hold time and setup time analysis, essential for reliable data capture by flip-flops or latches. Through meticulous analysis and optimization using STA tools, interns honed skills to mitigate setup and hold time violations, fortifying the robustness of digital circuits. Additionally, the internship provided fertile ground for crosstalk analysis, shedding light on the detrimental effects of unwanted signal coupling between adjacent conductors. Through internship acquired theoretical knowledge on crosstalk's causes, effects, and mitigation strategies, paving the way for practical simulation-based experiences.

Furthermore, internship embarked on timing report interpretation, unraveling intricate insights within crucial outputs of STA tools. Critical path analysis unveiled the longest paths dictating circuit performance, while slack time assessment illuminated optimization margins and potential pitfalls. Clock domain analysis within timing reports enabled interns to grasp nuances of clock relationships and synchronization, crucial for circumventing timing-related anomalies. By identifying and rectifying setup and hold time violations flagged within timing reports, interns contributed to the overarching goal of enhancing circuit reliability and correctness. In essence, the internship served as a crucible for budding engineers, fostering a profound understanding of the VLSI design flow's intricacies and arming them with practical skills imperative for industrial settings. Through the exploration of STA, dissected critical parameters and harnessed optimization opportunities, ultimately augmenting the robustness and reliability of digital circuits.

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Chapter 1

Profile of Organization

CHAPTER 1

PROFILE OF THE ORGANIZATION

The internship work is carried out in the Centre of Excellence in the Centre for Integrated Circuits and Systems (CICS) in R.V College of Engineering. The Vision, Mission, Objectives, Outcomes and Benefits of the Organization are put forth in this chapter.

1.1 CoE in Integrated Circuits and Systems

The CoE consists of passionate students and faculty members willing to create an eco-system that inspires the VLSI/Electronics system designer, to nurture the skills and innovative ideas, and to promote sustainable and interdisciplinary research, with inclusive societal concerns. The CoE promotes a coherent training program that enhances the skill set of young designers in the specified areas with academia-industry collaboration in India and abroad. Figure 1.1 is CICS lab in R.V College of Engineering with logo shown in Figure 1.2.

It aims at engaging enthusiastic students in design/development activities through funded projects and consultancy works from various organizations thereby contributing to the growth of the nation.

1.2 Interdisciplinary Research & Innovation

Interdisciplinary research is a type of study or research that draws from two or more disciplines in order to gain a more well-developed perspective or discover something new. Interdisciplinary research is growing in popularity and is increasingly seen as essential. Multiple perspectives on research challenges will often lead to better outcomes.

In order to streamline and undertaking focused research, the institution has followed the following approach for execution of funded projects and industrial consultancy. Also to develop competency in students and faculty[1].

1. Identifying Thematic Areas of Research: Carrying out SWOC analysis of the institution and aligning goals in line with Thrust areas of Govt. & Industry is helping identifying need-based areas of research. Thrust areas are identified through road maps, govt. policy documents, Vision 2035, UN SDG 2030, funding agency requirements and such others.

Fig 1.1 COE-CICS

2.Aligning with existing infrastructure and identifying new infrastructure needed: The institution has separate PG / Research budget to cater to new equipment's and seed funding for students and faculty. Many companies and funding agencies have helped in establishing physical infrastructure and state of the art equipment and software are provided over a period of time

3.Assigning Team: Based on the specialization and competency of the faculty, various interdisciplinary teams are formed to undertake need based research, execute projects and consultancy assignments

4. Developing Modules and providing training: The newer areas of science and technologies need learning through training from experts. Based on the need of the faculty, training in thematic areas is provided through institutional funding and providing seed funding for initial experimentation & Simulation, wherever needed. Mentoring by Industry & Research Experts in the thematic areas are also taken up for better understanding of the need and execution[2].

Fig 1.2 Logo of CoE- CICS

5. Executing work as per standards: Funding agencies and industries expect deliver- able in terms of products, processes and systems, which are scalable. Efforts are made to execute the projects and consulting work based on the goals set and mea- sured through publishing in peer reviewed journals, developing prototypes and and obtaining Patents and copy rights.

6. Reporting periodically & Scale Up the CoE / CoC: Documentation of the work carried out and submitting to the agencies is a continuous assignment and also helps future work to be undertaken. The whole exercise of interdisciplinary research and innovation is also helping in developing incubation centre and Start-ups for commercialization of IPs, and alternate Revenue generation for sustainability.

1.3 Vision

Creating an ecosystem that inspires the VLSI/Electronics system designer, nurturing their skills and innovative ideas, promoting sustainable and interdisciplinary research, with inclusive societal concerns.

1.4 Mission

- To create an eco-system for ultra-low power analog, mixed signal, RF and power management services and realize their benefits to society in near future.
- To promote a coherent programme of training which will enhance the skill set of underprivileged people in the specified areas with academia - industry collaboration in India and abroad.
- To engage in design/development activities by carrying out funded projects and consultancy works for various organizations and thereby partake in the growth of the nation.

- To establish as a stand-alone center which can attract people from various domains and leverage substantial interdisciplinary research.

1.5 OUTCOMES

- Engage in fabless design of various IP blocks for Analog ICs / Mixed Signal ICs / RFICs / Memory / Digital ICs / SoCs/ASICs.

- Train students and faculty across India in the areas of Analog ICs / Mixed Signal ICs / RFICs / Memory / Digital ICs / SoCs/ASICs.

- Engage in R&D projects in the areas of Analog ICs / Mixed Signal ICs / RFICs /Memory / Digital ICs / SoCs/ASICs.

The activities under the proposed Centre can be categorized in 2 groups.

1. Provide industry-certified internships for UG/PG students throughout the year for all 3 modules in the areas of IC Design
    - Fundamental module (1st and 2nd sem UG students of all circuits branches)
    - Intermediate module (3rd and 4th sem UG students of all circuits branches, 1st sem PG students of VLSI/Communication Branch)
    - Advanced module (5th and 6th sem UG students of all circuits branches, 2nd and 3rd sem PG students of VLSI/Communication Branch)

2. Execute consultancy projects with the companies that we have tied up with. This will help PG/UG students to work on industry-related projects which will give them better exposure to the state of the artwork. Apart from regular workshops, the center can float specialized certificate programs in various areas of IC Design in the following years as it is in huge demand. The specialized certification programs can be run in online/offline mode with 3 Core courses and 2 Elective courses, with capstone projects. Apart from regular workshops, the center can float specialized certificate programs in various areas of IC Design in the following years as it is in huge demand. The specialized certification programs can be run in online/offline mode with 3 Core courses and 2 Elective courses, with capstone projects [3].

1.6 Value Addition to the Institution

The Center of Excellence brings value addition to the institution in the following ways. 1.By enhancing research, consultancy works in the proposed themes and domains.

2. By offering training programmes to students of all discipline from the various mod- ules offered by the centre and can carry out design projects in the centre.
3. Through funded projects from public and private sectors.
4. By promoting PG and full time PhD through research activities.
5. By offering value addition to the degrees offered by the institution through projects, training program, workshops, symposium.
6. Fabricated chips will be added to the chip gallery of the centre which can elevate the centre to a hub for Integrated Circuit Design.

1 .7 Benefits to the research community

The centre provides benefits to the research community in the following ways:

1. Students / Faculty, both internal and external, can take up the structured training programmes enhancing the research activities.
2. Research scholars can use the facility of the centre for their research.

This chapter explains the profile of the organization, the research facility provided to the students under the guidance of experienced faculty for the betterment of student's perspective on upcoming latest technologies with innovative and inspiring Talks in an Industry level.

The report is organized as follows:

- Chapter 2 discusses about the various activities performed under the Center of excellence in Integrated Circuits and Systems.
- Chapter 3 discusses about the tasks performed as a part of the internship.
- Chapter 5 discusses about the reflection, conclusions and the Future scope of the internship[4].

Chapter 2

Activities of the Organization

CHAPTER 2

ACTIVITIES OF THE ORGANIZATION

Various activities were planned under the centre, which involved the provision of industry certified internship through the completion of several modules in the areas of IC design and execution of consultancy projects with the companies that are tied up with the center. The following sections explain the activities planned and carried out by the center.

2.1 Various activities planned under the proposed center

The activities under the proposed Centre can be categorized in 2 groups.

1. Provide industry certified internship for Under-graduate and post-graduate students throughout the year for all 3 modules in the areas of IC Design.
Fundamental module (1st and 2nd semester under-graduate students of all circuits branches)
Intermediate module (3rd and 4th semester under-graduate students of all circuits branches, 1st semester PG students of VLSI/Communication Branch)
Advanced module (5th and 6th semester Under-graduate students of all cir- cuits branches, 2nd and 3rd semester PG students of VLSI/Communication Branch)

2. Execute consultancy projects with the companies that we have tied up with. This will help Under-graduate and post-graduate students to work on industry related projects which will give them better exposure to the state of the art work. This will help Under-graduate and post-graduate students to work on industry related projects which will give them better exposure to the state of the art work [5].
The center will focus on a handful of activities in future as shown in the Figure 2.1.

2.2 Various modules of training programmes

1. Module 1: Analog Design

(a) level 1: Introductory course on Analog IC Design with hands on simulations. (b)level 2: "Op-amps for everyone" with hands on simulations.

(b) level 2: "Op-amps for everyone" with hands on simulations.

Fig 2.1: Activities under the proposed center

(c) level 3: Design of low power analog modules with bias generation with hands simulations.

2. Module 2: Module 2: Mixed signal Design

(a) Level 1: Introductory course on Mixed signal IC Design with hands on simulations.

(b) Level 2: "Data converters for everyone" with hands on simulations.

(c) Level 3: Design of ADC/DAC Architectures from specifications with hands on simulations.

3.Module 3: Digital Design

(a) Level 1: Introductory course on Digital IC Design with hands simulations.

(b) Level 2: "FPGA For Everyone" with hands simulations.

(c)Level 3: Design of low power digital modules with hands on simulations.

2.3 Research Collaboration

The center is well equipped with trained faculty, computational infrastructure and necessary teaching learning software's both open source and commercial. Figure 2.2 shows the research activities by CICS.

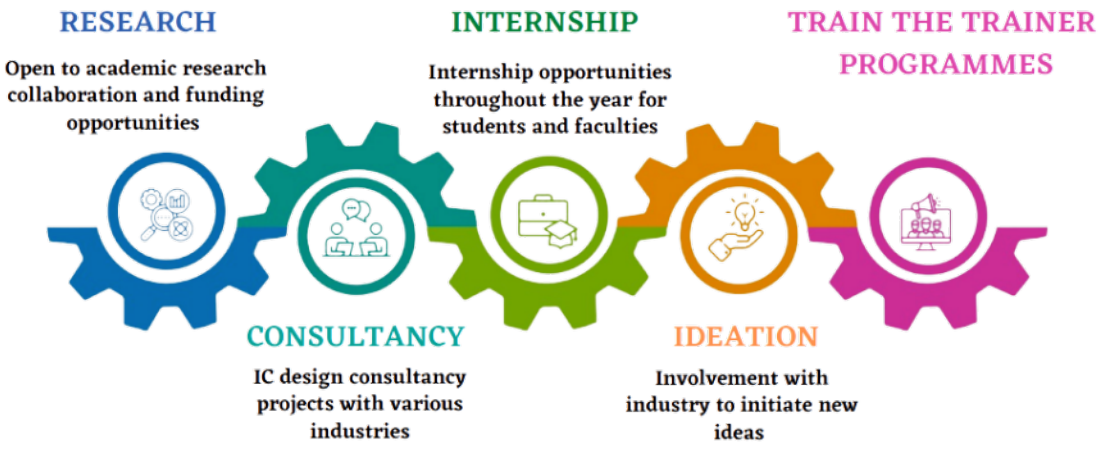

Fig. 2.2: Research Activities

Figure 2.3 shows the training program conducted for students by the department for research purposes with commercially licensed software and one of the Invited talks, delivered by Mr. Prakash Bettadapur on the topic "Product Engineering and Agility- An overview" for the students to catch up on the latest and advanced technologies at the industry level. A technical talk on 'Introduction to Micro/Nano Fabrication Technology with Device Examples' was delivered by Ms. Sabiha Sultana who is working at the Center for Nano Science and Engineering (CENSE), IISC Bangalore. There was also another technical talk delivered by Mr. Hariprasad Bhat, Lekha Wireless solutions which focused on 'Interfacing between ARM and FPGA in an SOC Chip' which was a new learning and was well received by the students [6].

2.4 Courses in Curriculum

The circuit branches of EC, EE, EI and ET have the foundation courses in the areas of IC Design in the curriculum so that any student from circuit branch can make use of the facility available in the centre. The curriculum of ECE has the specialized courses of the center as core and electives. This will bring in momentum to the activities in the centre. Members of CICS have their expertise in the following courses and this has been

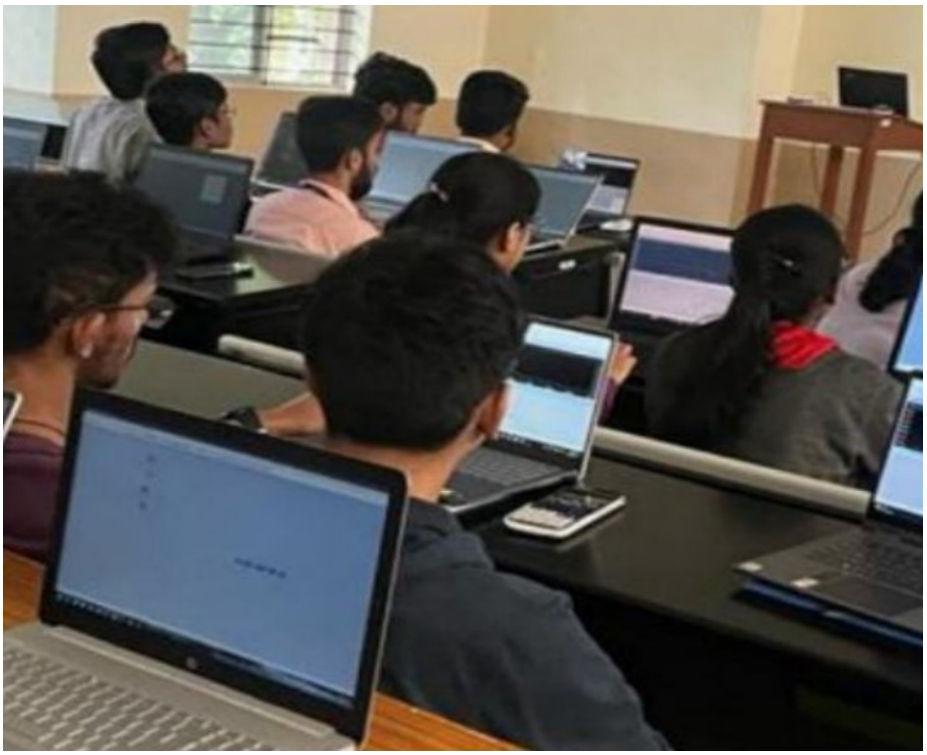

Fig. 2.3: Training Program for Students

shown in the Figure2.4

- Analog Microelctronic Circuits
- Analog Integrated Circuit Design
- Radio Frequency and Millimeter Wave IC Design
- Mixed Signal IC Design
- Digital VLSI Design
- VLSI for Testing and Testability

2.5 MOUs from COE

The centre has signed an MOUs with:

1. Entuple technologies to assist the centre with fabless design. This will be done bythe experts in the appropriate field from entuple technologies.

Fig 2.4: Modules by COE-CICS

2. Lekha Wireless solutions which will offer consultancy projects and internships tothe students from RVCE.
3. WPIF which will offer internships to students.
4. Semiconductor Laboratories technologies have offered 180nm Process Design Kit.

The chapter briefs about the possible outcomes from the internship with Industry level projects, benefits to the research community and value added to the institution with a possible publication and innovative projects carried out by the students for the welfare of community, adding a significant status to the Institution. The next chapter views on the tasks performed in the Internship which gives a brief introduction to analog to digitalconverters, their utility and the selection of algorithmic analog to digital converters for biomedical applications. It also explains about the various blocks in the algorithmic ADC and their design and simulation results in LTspice[7].

Chapter 3

Tasks Performed During the Internship

CHAPTER 3

TASKS PERFORMED DURING THE INTERNSHIP

Various activities or tasks were performed over the span of four weeks. Few of the major tasks being, identifying the objective of the worklet the team was going to work on during the internship. Mentors from CICS-COE were allotted to the team with the required domain knowledge for guidance throughout the internship. The worklet began with understanding of topic and objectives by doing necessary literature survey, followed by understanding of various concepts of digital vlsi design, including static timing analysis, cross talk and timing report. At a later stage various were identified to improve the overall efficiency of the model, observing a comparative study hence achieving the objectives or goals of the worklet [8].

3.1 Objectives of the Internship Worklet

The primary goal of my internship in Static Timing Analysis (STA) was to gain comprehensive insights into the VLSI (Very Large-Scale Integration) design flow, focusing on critical aspects such as hold time, setup time, slack time, crosstalk, and the interpretation of timing reports. The specific objectives included:

3.1.1 VLSI Design Flow Understanding:

Acquire a deep understanding of the overall VLSI design flow, encompassing various stages from specification and synthesis to place and route, and finally, static timing analysis. Figure 3.1 shows the VLSI design flow.

- **Specification**

  The design process begins with the identification of project requirements and specifications. This phase involves defining the functionality, performance, power consumption, and other critical parameters of the IC.

- **Design Entry**

  During this phase, engineers use Hardware Description Languages (HDLs) such as Verilog or VHDL to create a high-level representation of the circuit's functionality. This is known as RTL (Register Transfer Level) design [9].

- **Synthesis**

  Synthesis is the process of converting the RTL description into a netlist, which represents the logic gates and their interconnections. This netlist is a structural representation of the design.

- **Floor planning**

  In this stage, the physical layout of the IC is planned, including the placement of functional blocks and connections. Floor planning influences factors like area, power, and signal delays.

- **Placement**

  Placement involves assigning specific locations to the logic gates and other components within the chip's layout. Proper placement is critical for meeting performance and power targets [10].

- **Routing**

  Routing involves establishing the physical paths for interconnecting the components based on the netlist and placement information. Global and detailed routing are performed to ensure proper signal integrity.

- **Layout**

  The layout phase creates the physical representation of the IC, considering manufacturing constraints. Engineers need to adhere to design rules and guidelines to ensure successful fabrication.

- **Extraction**

  Once the layout is complete, parasitic elements such as resistors and capacitors are extracted. This information is crucial for accurate simulation and verification.

- **Simulation and Verification**

  Simulation is performed to ensure that the design meets the specified requirements. Various simulations include functional simulation, timing simulation, and power analysis. Verification ensures the correctness of the design at each stage [11].

- **Design for Test (DFT)**

DFT techniques are applied to facilitate efficient testing of the final product. This includes the insertion of test structures and logic for easy fault detection and diagnosis.

- **Tape-out**

  Tape-out marks the finalization of the design, and the data is sent to the semiconductor foundry for fabrication. It involves creating the final set of files needed for the manufacturing process.

- **Manufacturing**

  The semiconductor fabrication facility uses the provided data to manufacture the ICs. This involves multiple intricate processes, including photolithography, deposition, and etching [12].

VLSI design flow is a multifaceted process that demands careful consideration of various aspects, from initial specifications to the manufacturing phase. Successful execution of each stage is crucial for producing high-performance and reliable integrated circuits.

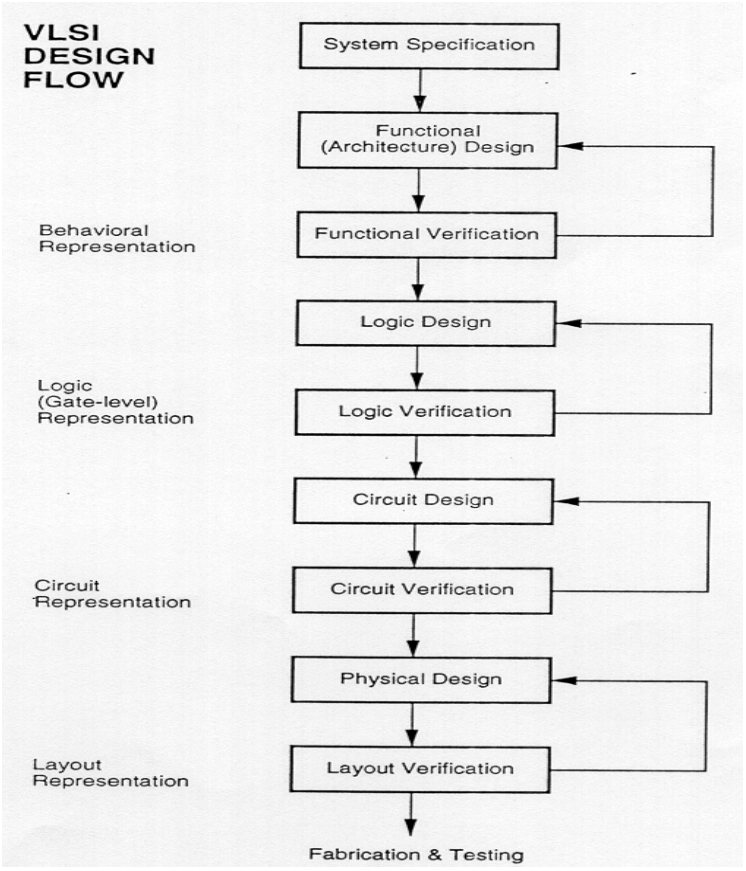

Fig 3.1 VLSI design flow

3.1.2 Hold Time and Setup Time Analysis:

Develop proficiency in analysing and optimizing hold time and setup time constraints, critical parameters in ensuring reliable and robust digital circuit functionality.

Setup Time

- **Definition:** Setup time refers to the minimum amount of time that data must be stable before the clock edge (transition) for proper capture by the receiving flip-flop or latch.
- **Importance:** Ensuring an adequate setup time is crucial to prevent data setup violations, which can lead to unpredictable behavior and errors in the digital circuit.
- **Analysis:** During the internship, the focus would have been on understanding how to analyze and optimize setup time constraints. This involves examining the timing paths in the circuit to ensure that the data signals meet the setup time requirements. Figure 3.2 shows the setup time waveform[13].

Hold Time

- **Definition:** Hold time represents the minimum duration that data must remain stable after the clock edge to ensure correct data capture by the receiving flip-flop or latch.
- **Importance:** Maintaining sufficient hold time is essential to prevent data hold violations, which can result in metastability issues and unreliable circuit behavior.
- **Analysis:** The internship would have involved analyzing hold time constraints within the design. This includes assessing the timing paths to guarantee that the data signals satisfy the hold time criteria. Figure 3.3 shows the hold time waveform[14].

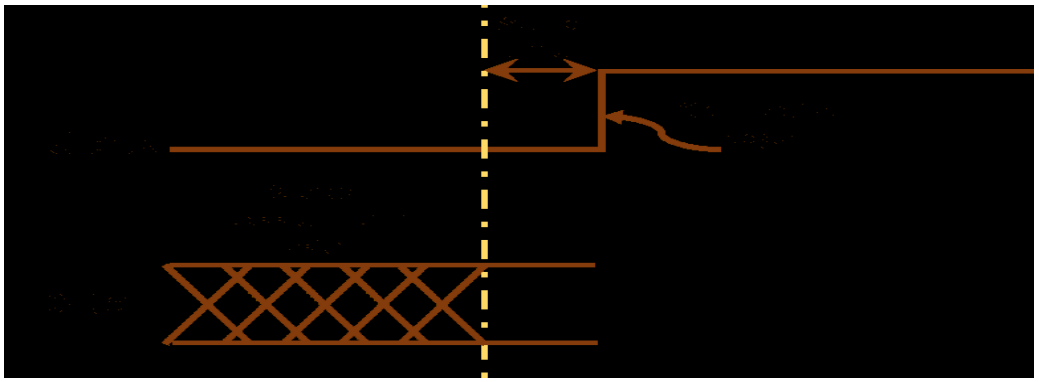

Fig 3.2: Setup time waveform

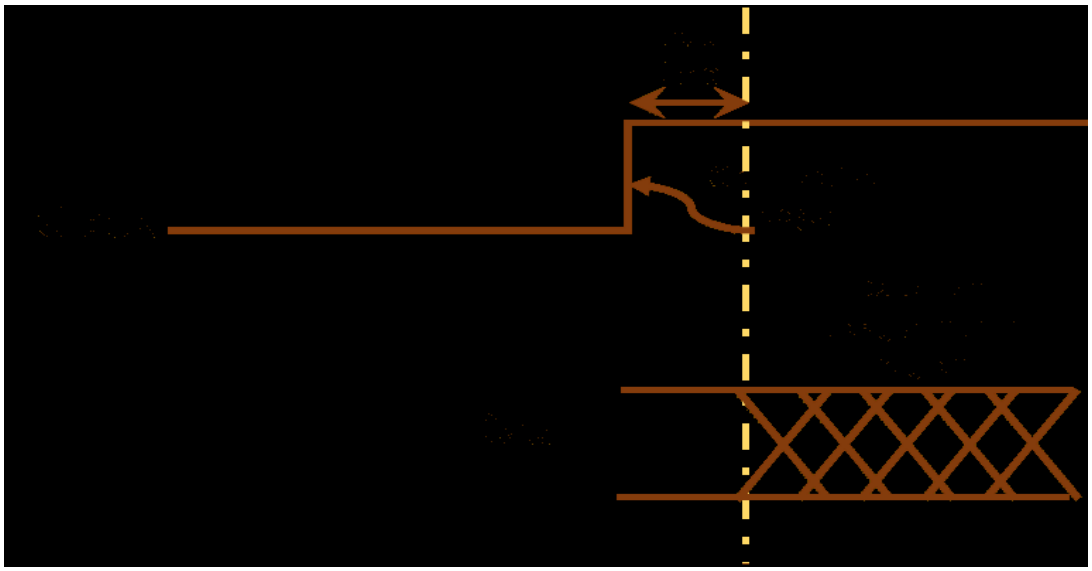

Fig 3.3: Hold time waveform

Optimization

- **Objective:** The internship aimed to develop proficiency in optimizing hold time and setup time constraints. Optimization involves adjusting various parameters in the design, such as clock skew, path delays, or logic structures, to meet the required timing specifications.
- **Tools and Techniques:** Utilizing STA tools, interns may have explored techniques to improve setup and hold times, such as adjusting clock relationships, optimizing logic paths, or redesigning critical sections of the circuit.

Circuit Robustness

Goal: The ultimate goal of hold time and setup time analysis and optimization is to enhance the robustness and reliability of the digital circuit.

- **Outcome:** By addressing setup and hold time constraints effectively, interns would have contributed to creating a more stable circuit that performs reliably under various conditions, reducing the risk of timing violations and associated issues.

3.1.3 Slack Time Assessment

During the internship in Static Timing Analysis (STA), focused on understanding and optimizing critical

parameters within the VLSI design flow, specifically hold time and setup time. Setup time denotes the minimum duration that data must be stable before the clock edge to ensure accurate capture by the receiving flip-flop or latch, while hold time represents the minimum duration data must remain stable after the clock edge. The internship aimed to cultivate proficiency in analyzing and optimizing these constraints, employing tools and techniques to adjust parameters such as clock skew, path delays, and logic structures. By delving into the intricacies of timing paths, I learned to identify and address potential setup and hold time violations, enhancing the robustness of digital circuits. The ultimate goal was to contribute to the creation of stable circuits that operate reliably under diverse conditions, mitigating the risk of timing-related issues. The experience not only broadened my understanding of VLSI design but also equipped me with practical skills applicable in industrial settings.

3.1.4 Crosstalk Analysis

Gain knowledge and hands-on experience in evaluating and mitigating crosstalk effects in digital circuits, ensuring signal integrity and minimizing potential issues.

- **Crosstalk Definition**

  Crosstalk refers to the unwanted coupling or interference between adjacent conductors in a circuit. It can lead to signal distortions, noise, and potential timing violations.

- **Importance of Crosstalk Analysis**

  Crosstalk can significantly impact signal integrity, potentially causing errors and malfunctions in digital circuits. Therefore, understanding and mitigating crosstalk effects are crucial for ensuring the reliability and performance of the overall design.

- **Knowledge Acquisition**

  During the internship, the focus would have been on gaining theoretical knowledge about crosstalk, including its causes, types, and effects on signal propagation.

- **Hands-on Experience**

  Practical experience in crosstalk analysis would involve using simulation tools to model and simulate the behavior of signals in the presence of crosstalk. This hands-on approach allows interns to observe and understand the impact of crosstalk on signal quality.

- **Evaluation Techniques**

  Interns would learn various techniques to evaluate crosstalk, including identifying vulnerable signal paths and analyzing the coupling capacitance between adjacent traces. These evaluations contribute to a comprehensive understanding of potential issues.

- **Mitigation Strategies**

  The internship would likely cover strategies for mitigating crosstalk effects. This may include adjusting the physical layout of the circuit, optimizing the spacing between conductors, or introducing shielding to minimize unwanted coupling.

- **Signal Integrity Assurance**

  The ultimate goal of crosstalk analysis is to ensure signal integrity by minimizing interference between signals. This involves implementing design practices and optimization techniques that reduce the impact of crosstalk on the overall performance of the digital circuit.

- **Collaboration with Other Design Aspects**

  Crosstalk analysis is often integrated into the broader VLSI design flow, intersecting with other aspects such as static timing analysis, power analysis, and physical design. Interns would likely collaborate with team members to address crosstalk issues in conjunction with these other considerations [15].

3.1.5 Timing Report Interpretation

Develop the ability to interpret timing reports generated during static timing analysis, extracting valuable insights into the performance metrics of the designed circuits.

- **Timing Reports in Static Timing Analysis**

  Timing reports are essential outputs generated by STA tools that provide a detailed analysis of the timing characteristics of a digital circuit. These reports contain information about critical paths, clock domains, and various timing metrics.

- **Objective of Interpretation**

  The primary goal of timing report interpretation is to extract valuable insights into how well the

designed circuit meets its timing requirements. This involves understanding the critical paths, identifying potential timing violations, and assessing the overall performance of the circuit.

- **Critical Path Analysis**

  Timing reports highlight critical paths, which are the longest paths in the circuit that determine the overall clock frequency and performance. Interns would learn to identify and analyze these critical paths to ensure they meet the specified timing constraints.

- **Slack Time Assessment**

  The timing report includes information about slack time, which represents the amount of time by which a signal can be delayed without violating timing constraints. Interns would be trained to interpret and analyze slack times to understand the margin available for optimization or potential issues.

- **Setup and Hold Time Violations**

  Timing reports flag any violations of setup and hold time constraints. Interns would gain expertise in identifying and resolving these violations, which are crucial for ensuring the reliability and correctness of the digital circuit.

- **Clock Domain Analysis**

  Many digital circuits involve multiple clock domains. Timing reports provide insights into the relationships between these domains, helping interns understand clock skew and synchronization issues that may impact the overall timing performance [16].

- **Optimization Opportunities**

  Timing reports serve as a roadmap for optimizing the circuit. Interns would learn to analyze the report to identify areas for improvement, whether it be optimizing critical paths, adjusting clock relationships, or refining the overall design to enhance performance.

Chapter 4

REFLECTIONS

Chapter 4

REFLECTIONS

In the dynamic realm of Very Large-Scale Integration (VLSI), the seamless functionality of integrated circuits (ICs) hinges on meticulous timing analysis. As the complexity of digital designs continues to evolve, the demand for precise Static Timing Analysis (STA) tools becomes increasingly vital.

4.1 Overview of the project

This project ventures into the domain of STA, focusing on the analysis of D flip-flops—a fundamental building block in digital circuits—using the OpenRoad tool. OpenRoad, an open-source, silicon-centric design methodology, offers a comprehensive suite of tools for VLSI design and optimization. By delving into the static timing analysis of D flip-flops, this project aims to elucidate critical timing parameters and optimize the performance and reliability of digital circuits.

The project embarks on a journey to explore the intricacies of static timing analysis within the context of D flip-flops. D flip-flops play a pivotal role in sequential logic design, facilitating storage and transfer of data in digital systems. Understanding the timing characteristics of D flip-flops is paramount for ensuring proper functionality and meeting timing constraints in VLSI designs. By leveraging the capabilities of the OpenRoad tool, this project seeks to unravel the timing intricacies inherent in D flip-flops, from setup and hold time constraints to critical path analysis and optimization.

Through this project, we endeavor to delve into the underlying principles of static timing analysis and its application to D flip-flops. Understanding the timing characteristics of D flip-flops is paramount for ensuring proper functionality and meeting timing constraints in VLSI designs. By leveraging the capabilities of the OpenRoad tool, this project seeks to unravel the timing intricacies inherent in D flip-flops, from setup and hold time constraints to critical path analysis and optimization. By utilizing the OpenRoad tool, we aim to gain insights into the timing behavior of D flip-flops under various design scenarios and constraints. Furthermore, this exploration will enable us to identify potential timing violations, optimize critical paths, and enhance the overall performance and reliability of digital circuits. Ultimately, the project aspires to contribute to the advancement of VLSI design methodologies by leveraging open-source tools for static timing analysis and fostering a deeper understanding of timing optimization techniques in digital circuit design.

4.2 working principal of D-flip flop

The D flip-flop, a fundamental component in digital logic design, serves as a crucial element for sequential logic operations. Its primary function revolves around the storage and transfer of data in digital circuits. At its core, a D flip-flop consists of two stable states, commonly referred to as "0" and "1", which represent binary values. The flip-flop comprises a data input (D), a clock input (CLK), and two outputs: the Q output, which reflects the current state of the flip-flop, and the complementary Q output (Q'), which represents the inverse of the Q output.

The operation of a D flip-flop is contingent upon the clock signal. When the clock signal transitions from a low to a high state (rising edge), the D input is sampled and stored within the flip-flop. This process effectively synchronizes the input data with the clock signal, ensuring that changes in the D input are only captured at the rising edge of the clock. As a result, the D flip-flop behaves as a data storage device, retaining the sampled data until the next clock transition.

Subsequent clock transitions do not affect the stored data unless a new value is presented at the D input during the rising edge of the clock. In this case, the new data is sampled and replaces the previous value stored within the flip-flop. Thus, the D flip-flop enables sequential logic operations by allowing data to be latched and transferred synchronously with the clock signal, facilitating the implementation of various digital functions such as registers, counters, and memory elements [17]. Fig. 4.1 depicts the symbol of d flip flop and its function table.

Overall, the D flip-flop's functioning embodies the fundamental principles of sequential logic, providing a reliable mechanism for data storage and transfer in digital circuits. It's simple yet versatile design makes it an indispensable building block in modern digital systems, serving as the backbone for numerous applications across diverse domains, from computer processors to communication networks.

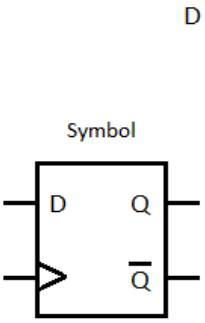

Table of truth:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

Fig. 4.1: Symbol and Function table of d flip flop

4.3 Code for D-flip flop

This Verilog module represents a simple D flip-flop. It has two inputs (d for data and clk for clock) and two outputs (q for the main output and q_bar for the complement of the main output). Inside the always block, the value of d is latched into q on the rising edge of the clock (clk). The complement of d is stored in q_bar. Fig. 4.2 is the given code for D flip flop.

In this Verilog testbench, we have defined inputs (**d_tb** and **clk_tb**) and outputs (**q_tb** and **q_bar_tb**) for the D flip-flop. We instantiate the D flip-flop module (**uut**) and connect its ports to the testbench signals. The testbench includes code to generate a clock signal (**clk_tb**) and apply stimulus to the D flip-flop by changing the input data (**d_tb**) at specific time intervals. The simulation ends after 25 time units using **$finish**.

This testbench provides a framework for simulating the behavior of the D flip-flop and verifying its functionality under different input conditions

.

```
Open
1  module dff(d,clk,q,qbar);
2       input d;
3       input clk;
4       output q,qbar;
5       reg q,qbar;
6
7       always@(posedge clk)
8       begin
9       case(d)
10           1'b0:
11                q = 0;
12           1'b1:
13                q=1;
14      endcase
15      qbar = ~q;
16      end
17 endmodule
18
19 module test;
20      reg d;
21      reg clk;
22      integer i;
23      wire q,qbar;
24
25      dff s(d,clk,q,qbar);
26      initial
27      begin
28      $display("sr flip flop");
29      $monitor("%b %b \t %b %b",d,clk, q,qbar);
30      $dumpfile("vcd/DFlipFlop.vcd");
31      $dumpvars(1,test);
32
33           d = 0;
34           #10
35           d = 1;
36           #10
37
38           d = 0;
39           #10
40           d = 1;
41           #10
42      $finish;
43      end
44
45      initial begin
46           clk = 0;
47           for(i=0;i<20;i=i+1)
48                #1 clk = ~clk;
49           end
50
51 endmodule
```

Fig. 4.2: Code for d flip-flop

4.4 Constraint file for D flip flop

In OpenRoad, a constraint file serves as a crucial component in the VLSI design flow, providing essential guidelines and specifications to guide the implementation process. Essentially, a constraint file encapsulates various design constraints and requirements, ranging from timing constraints to physical layout considerations. These constraints dictate parameters such as clock frequencies, input/output delays, placement constraints, and routing rules. By defining these constraints upfront in a structured and organized manner, the constraint file facilitates a systematic and efficient design process. Additionally, constraint files enable designers to communicate design requirements effectively across different stages of the design flow and ensure consistency throughout the entire implementation process. Overall, constraint files play a pivotal role in ensuring the successful realization of VLSI designs by guiding the optimization and synthesis processes to meet the desired performance, timing, and physical requirements [18]. Fig 4.3 shows the constraint file of the d flip flop and Fig 4.4 shows the config file od d flip flop.

Open ~/Work/vlsi/tools/O

```
1 current_design dff
2 set clk_period 1000
3 set clk_port_name clk
4
5 # No need to change below here
6 set clk_name clk
7 set clk_io_pct 0.2
8
9 set clk_port [get_ports $clk_port_name]
10
11 create_clock -name $clk_name -period $clk_period $clk_port
12
13 set non_clock_inputs [lsearch -inline -all -not -exact [all_inputs] $clk_port]
14
15 set_input_delay  [expr $clk_period * $clk_io_pct] -clock $clk_name $non_clock_inputs
16 set_output_delay [expr $clk_period * $clk_io_pct] -clock $clk_name [all_outputs]
```

Fig 4.3: Constraint file of D flip flop

4.5 Config file for D flip flop

In the context of OpenROAD, a config file, short for configuration file, serves as a vital component for managing various settings, options, and parameters associated with the design flow and tool configurations. This file, typically written in a structured format such as JSON or TCL, allows users to specify a wide range of options, including tool configurations, optimization strategies, design constraints, and file paths. The config file acts as a centralized repository for defining the environment and behavior of OpenROAD tools, enabling users to customize their design flow to suit specific project requirements. By providing a flexible and customizable framework, config files empower users to efficiently control and manage the entire design process, from synthesis and placement to routing and timing analysis, while facilitating repeatability and reproducibility across different design projects. Additionally, config files can be version-controlled and shared among team members, promoting collaboration and ensuring consistency in design practices within a project or organization. Overall, config files play a pivotal role in streamlining the design flow, optimizing tool usage, and enhancing productivity in OpenROAD-based VLSI design projects [19]. Fig 4.5 shows the schematics of d flip flop on openRoad.

Open

```
1 export DESIGN_NICKNAME = dff
2 export DESIGN_NAME=dff
3 export PLATFORM    = asap7
4
5 export VERILOG_FILES = ./designs/src/$(DESIGN_NICKNAME)/dff.v
6 export SDC_FILE      = ./designs/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc
7
8 export CORE_UTILIZATION = 20
9 export PLACE_DENSITY = 0.55
10 export CORE_ASPECT_RATIO = 1
11 export CORE_MARGIN = 1.0
```

Fig 4.4: Config file for d flip flop

4.6 RESULTS

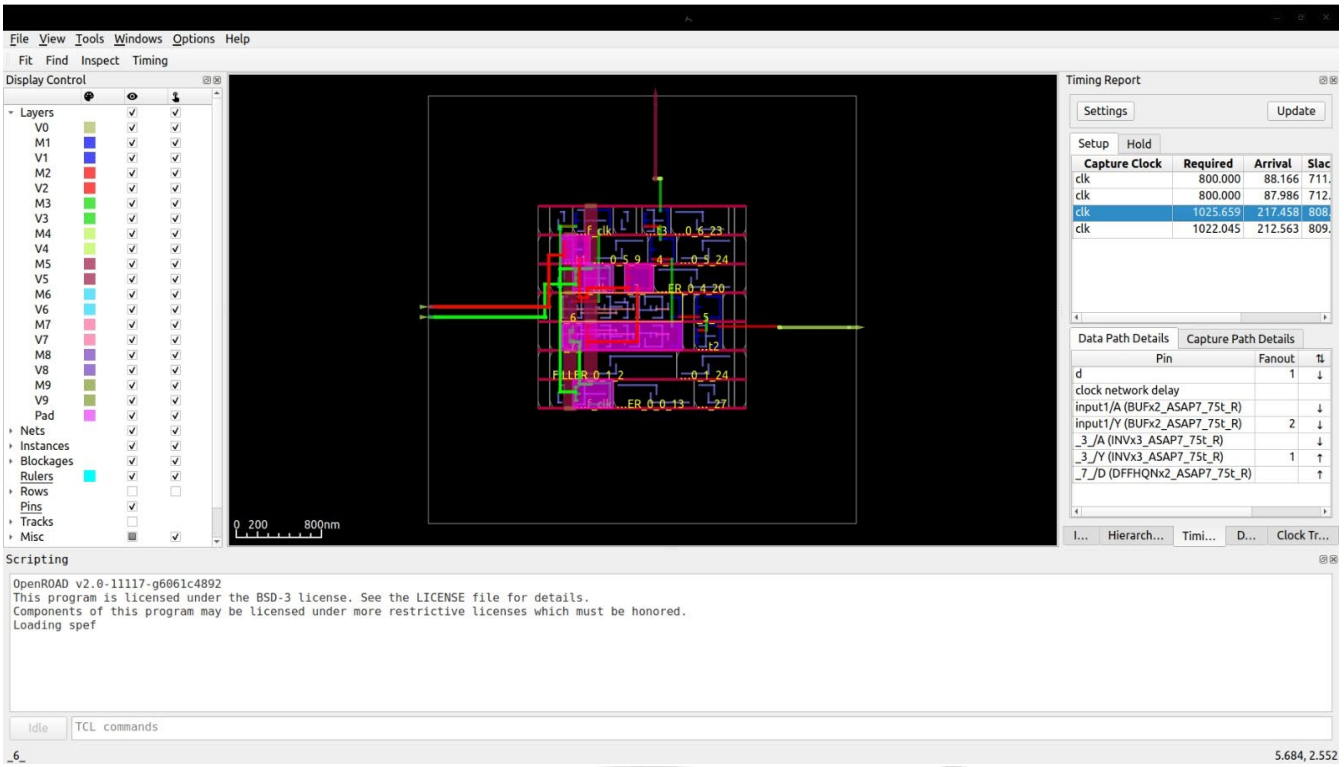

Fig 4.5: Schematic of D flip flop on OpenRoad

4.6.1 Setup time Analysis

Capture clock	Required	Arrival	Slack
Clk	800.00	88.166	711.834
Clk	1025.659	217.458	808.201
clk	1022.045	212.563	809.482

4.6.2 Hold time Analysis

Capture clock	Required	Hold	slack
Clk	629.12	202.34	426.78
Clk	895.36	356.84	538.52
clk	961.35	396.98	564.37

4.7 Learning Outcome of OpenRoad Project

The journey through the project conducted on OpenROAD, a silicon-centric design methodology, has been rich with invaluable learning experiences that have greatly enriched our understanding of Very Large-Scale Integration (VLSI) design processes and tools. As we reflect upon the project's outcomes, it becomes evident that our exploration of OpenROAD has provided us with a multifaceted set of skills and insights that transcend mere technical proficiency. Through this endeavor, we have not only deepened our understanding of the intricacies of VLSI design but also honed our problem-solving abilities, enhanced our collaboration skills, and gained a deeper appreciation for the complexities and nuances of modern semiconductor design.

At the technical level, the project has equipped us with a comprehensive understanding of the OpenROAD tool suite and its capabilities in facilitating various stages of the VLSI design flow. From synthesis and placement to routing and timing analysis, we have delved into the functionalities of each tool and learned how to leverage them effectively to optimize design performance and meet project objectives. Specifically, our proficiency in using OpenROAD for static timing analysis (STA) has been significantly enhanced, as evidenced by our ability to analyze critical timing parameters such as setup time, hold time, and slack time, and identify potential timing violations that could impact circuit reliability and performance.

Furthermore, the project has provided us with hands-on experience in designing and implementing a D flip-flop using Verilog and verifying its functionality through simulation. This practical aspect of the project has allowed us to apply theoretical concepts learned in the classroom to real-world design scenarios, thereby bridging the gap between academic knowledge and industrial practice. By working on a concrete design project, we have gained insights into the challenges and complexities inherent in VLSI design and developed the skills necessary to address them effectively.

In addition to technical skills, the project has also fostered the development of important soft skills such as teamwork, communication, and project management. Collaborating with team members to define project goals, allocate tasks, and coordinate efforts has provided us with valuable insights into the dynamics of teamwork in a professional setting. Moreover, the project has offered opportunities to communicate our ideas, findings, and solutions effectively through written reports, presentations, and discussions, thereby enhancing our ability to convey complex technical concepts to diverse audiences.

Beyond technical and soft skills, the project has also contributed to our personal and professional growth by fostering a spirit of curiosity, creativity, and lifelong learning. Engaging in the design process and

grappling with real-world design challenges has ignited our passion for VLSI design and motivated us to

pursue further exploration and innovation in this field. Moreover, the project has exposed us to the latest advancements and trends in semiconductor design, inspiring us to stay abreast of developments and continually expand our knowledge and skills [20].

In summary, the project conducted on OpenRoad has been a transformative learning experience that has enriched our understanding of VLSI design processes and tools, enhanced our technical and soft skills, and inspired our personal and professional growth. As we embark on the next phase of our journey, we carry with us the lessons learned and the experiences gained from this project, which will undoubtedly serve as a solid foundation for future endeavours in the dynamic and exciting field of semiconductor design.

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